# XIANGYU ZHANG

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## EDUCATION

**University of Massachusetts Amherst** *Expected: 12/2016*
M.S.in Electronic & Computer Engineering Overall GPA: 3.423

**Florida Institute of Technology** *05/2014*
B.S.in Electronic & Computer Engineering Overall GPA: 3.5

## TECHNICAL STRENGTHS

**Languages** Verilog, C++, Python.
**Tools** Quartus II, Linux, MINISAT, HSPICE, Cadence Virtuoso, Visual Studio, Git.
**Courses** Computer Architecture, VLSI, Testing in VLSI, Verification, Algorithm, Computer Network.

## RESEARCH AND TEACHING EXPERIENCE

**University of Massachusetts Amherst** Research Assistant
*Area: Formal Equivalence Checking, SAT, Circuit Security* *06/2015 - Present*

- Oracle-Guided Incremental SAT Solver Development
  - Participated in Oracle-Guided Incremental SAT Solver using **Python** and **C/C++**.
  - Developed Circuit Equivalence Checking tool based on **MINISAT** using **Python**.
- Camouflage Tools Development
  - Implemented Logic-level circuit obfuscation based on Anti-reverse Engineering using Transformable Interconnects in **Python**.
  - Implemented Logic Anti-propagation in **Python**.

**University of Massachusetts Amherst** Teaching Assistant
*Course: ENG Computer Systems Lab I* *09/2015 - 01/2016*

- Assisted in teaching design and analysis of digital systems using both hardware (Altera Complex Programmable Logic Device (CPLD) and **Verilog**) and software (Atmel **AVR** ATmega32 microcontroller, assembly language and **C**).

## ACADEMIC PROJECTS

- Parallel Pattern Single Fault Simulation (PPSFP) based Fault Simulator *(11/2015)*
  - Developed a parser and lexical analyzer based on **YACC & LEX** to read ISCAS benchmark circuits and convert to customized double undirected graph using **C**.
  - Implemented circuit levelization algorithm using **C/C++**.
  - Implemented Parallel Pattern Single Fault Simulation (**PPSFP**) algorithm using **C/C++**.
- MIPS Simulating Model *(10/2015)*
  - Simulated **MIPS** architecture in **C** and evaluated utilization of each gate.
- Universal Synchronous and Asynchronous Receiver Transmitter (**USART**) implementation on CPLD *(11/2015)*
  - Designed a USART for MIDI device that will read a MIDI signal to interpret its content and display the note number in binary on seven LEDs using **CPLD** and **Verilog**.
- General MIDI Explorer (GME) with Record/Playback implementation on AVR *(12/2015)*
  - Developed record and playback function using USART and store function using EEPROM on ATmega32 **AVR** in **C**.
  - Implemented Run-length encoding (RLE) to perform compression and uncompression in EEPROM.

## PUBLICATIONS

- Duo Liu, **Xiangyu Zhang**, Cunxi Yu, Daniel Holcomb, Oracle-Guided Incremental SAT Solving to Reverse Engineer Camouflaged Logic Circuits, Design Automation and Test in Europe, **DATE 2016** (accepted).