

# XIANGYU ZHANG

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## EDUCATION

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**University of Massachusetts Amherst**  
M.S.in Electronic & Computer Engineering

*Sep 2014 - Present*  
Overall GPA: 3.423

**Florida Institute of Technology**  
B.S.in Electronic & Computer Engineering

*Aug. 2012 - May. 2014*  
Overall GPA: 3.5

## TECHNICAL STRENGTHS

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**Languages** Verilog, C++, Python.

**Tools** Quartus II, Linux, MINISAT, HSPICE, Cadence Virtuoso, Visual Studio, Git.

**Courses** Computer Architecture, VLSI, Testing & Diagnosis VLSI System, Verification, Algorithm, Computer Network.

## RESEARCH AND TEACH EXPERIENCE

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**University of Massachusetts Amherst**  
*Area: Formal Equivalence Checking, SAT, Circuit Security*

Research Assistant  
*Jun 2015 - Present*

- Oracle-Guided Incremental SAT Solver Development
  - Participated in Oracle-Guided Incremental SAT Solver using **Python** and **C/C++**.
  - Developed Circuit Equivalence Checking tool based on **MINISAT** using **Python**.
- Camouflage Tools Development
  - Implemented Logic-level circuit obfuscation based on Anti-reverse Engineering using Transformable Interconnects in **Python**.
  - Implemented Logic Anti-propagation in **Python**.

**University of Massachusetts Amherst**  
*Course: ECE 353 - Computer Systems Lab I*

Teaching Assistant  
*Sep 2015 - Jan 2016*

- Assisted in teaching design and analysis of digital systems using both hardware (Altera Complex Programmable Logic Device (CPLD) and **Verilog**) and software (Atmel **AVR** ATmega32 microcontroller, assembly language and **C**).

## ACADEMIC PROJECTS

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- Parallel Pattern Single Fault Simulation (PPSFP) based Fault Simulator
  - Developed a parser and lexical analyzer based on **YACC & LEX** to read ISCAS benchmark circuits and convert to customized double undirected graph using **C**.
  - Implemented circuit levelization algorithm using **C/C++**.
  - Implemented Parallel Pattern Single Fault Simulation (**PPSFP**) algorithm using **C/C++**.
- MIPS Simulating Model
  - Simulated **MIPS** architecture in **C** and evaluated utilization of each gate.
- Universal Synchronous and Asynchronous Receiver Transmitter (**USART**) implementation on CPLD
  - Designed a USART for MIDI device that will read a MIDI signal to interpret its content and display the note number in binary on seven LEDs using **CPLD** and **Verilog**.
- General MIDI Explorer (GME) with Record/Playback implementation on AVR
  - Developed record and playback function using USART and store function using EEPROM on ATmega32 **AVR** in **C**.
  - Implemented Run-length encoding (RLE) to perform compression and uncompression in EEPROM.

## PUBLICATIONS

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- Oracle-Guided Incremental SAT Solving to Reverse Engineer Camouflaged Logic Circuits, Design Automation and Test in Europe, **DATE 2016**.