ECE 6913 Quiz 2 INET section Spring 2022

Computing Systems Architecture (New York University)

ECE 6913 INET, Quiz 2 Instructions

Quiz 2 Time: Thursday April 21st 2022, 8:30AM – 10:30AM.

Maximum time: 120 minutes : **8:30 AM - 10:30 AM** [+ 10 minutes to assemble PDF and upload]

Open Book, Open Notes,

Calculators allowed.

The Quiz will be visible to you as an assignment on NYU Brightspace at 8:30 AM on Thursday April 21st 2022

You Must show your work in steps – to get any credit

Instructor/CAs available online if you have questions on the Quiz, during the Quiz – Please enter question in Zoom chat box at any time during Quiz

You may not communicate with anyone by any means/media during the Quiz except with Course Staff

By University rules, students are required to open Zoom and turn on their video and audio. *Please check your laptops in advance to enable this during the Quiz*. If you do not have your camera and mic on, your Quiz cannot be graded.

This Quiz has 4 problems, each with multiple parts. Please attempt all of them. Please show **all work**. Please write **legibly**

1. Please be sure to have 10-15 sheets of white or ruled Paper, a Pen/Pencil & Eraser
2. Please write down your solutions on 8.5 x 11 sheets of white paper, single-sided with your name printed in top right corner of each sheet and with Page Number and Problem number identified clearly on each sheet
3. **Please stop working on your Quiz at 10:30 AM** – you have 10 minutes to scan/take pictures of each sheet and upload them as completed PDF assignment to NYU Classes **by 10:40 AM** – you may use any of several smartphone apps to integrate your scans/pictures of sheets into a PDF file.
4. Please take pictures of each sheet and **upload** the PDF of all sheets after checking you have all sheets in the right order **by 10:45 AM latest.**
5. You may use iPAD to write down your solutions directly rather than on paper
6. Portal **will close at 10:45 AM** not allowing upload of your quiz after **10:45 AM**

Problem 1. Your Company describes their latest Processor with the following features:
• 95% of all memory accesses are found in the cache.
• Each cache block is two words, and the whole block is read on any miss.
• The processor sends references to its cache at the rate of 10^9 words per second.
• 25% of those references are writes.
• Assume that the memory system can support 10^9 words per second, reads or writes.
• The bus reads or writes a single word at a time (the memory system cannot read or write two words at once).
• Assume at any one time, 30% of the blocks in the cache have been modified.
• The cache uses write allocate on a write miss.

You are considering adding a peripheral to the system, and *you want to know how much of the memory system bandwidth is already used*.

1.1 Calculate the percentage of memory system bandwidth used assuming the cache is Write Back.

1.2 Calculate the percentage of memory system bandwidth used assuming the cache is Write Through.

Please be sure to state your assumptions and show all work

Problem 2. One difference between a write-through cache and a write-back cache can be in the time it takes to write. During the first cycle, we detect whether a hit will occur, and during the second (assuming a hit) we actually write the data.

Let's assume that 50% of the blocks are dirty for a write-back cache. For this question, assume that the write buffer for the write through will never stall the CPU (no penalty). Assume a cache read hit takes 1 clock cycle, the cache miss penalty is 50 clock cycles, and a block write from the cache to main memory takes 50 clock cycles. Finally, assume the instruction cache miss rate is 0.5% and the data cache miss rate is 1%. Assume that on average 26% and 9% of instructions in the workload are loads and stores, respectively.

2.1 Estimate the performance of a write-through cache with a two-cycle write versus a write-back cache with a two-cycle write.

Problem 3.

Consider the following RISC V Instruction sequence executing in a 5-stage pipeline:

```
or   x13, x12, x11
ld   x10, 0(x13)
ld   x11, 8(x13)
add  x12, x10, x11
subi x13, x12, 16
```

3.1 Identify all of the data hazards and their resolution with NOPs assuming no forwarding or hazard detection hardware is being used

3.2 If there is forwarding, for the first seven cycles during the execution of this code, *specify which signals are asserted in each cycle by hazard detection and forwarding units* in Figure below.

Mux control	Source	Explanation
ForwardA = 00	ID/EX	The first ALU operand comes from the register file.
ForwardA = 10	EX/MEM	The first ALU operand is forwarded from the prior ALU result.
ForwardA = 01	MEM/WB	The first ALU operand is forwarded from data memory or an earlier ALU result.
ForwardB = 00	ID/EX	The second ALU operand comes from the register file.
ForwardB = 10	EX/MEM	The second ALU operand is forwarded from the prior ALU result.
ForwardB = 01	MEM/WB	The second ALU operand is forwarded from data memory or an earlier ALU result.

	Clock Cycle → Instruction ↓	1	2	3	4	5	6	7	8	9	10
1	or										
2	ld										
3	.										
.	.										
.	.										

Problem 4. Consider the following program and cache behaviors.

Data Reads per 1K instructions	Data Writes per 1K instructions	Instruction Cache Miss Rate	Data Cache Miss Rate	Block Size (Bytes)
300	150	0.5%	5%	128

Suppose a CPU with a write-through, write allocate cache achieves a CPI of 2.

4.1 What are the read and write bandwidths (measured by bytes per cycle) between RAM and the cache? (Assume each miss generates a request for one block.). *For a write-allocate policy, a write miss also makes a read request to RAM – please be sure to consider its impact on Read Bandwidth*