Xianwei ZHANG

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Summary Phd student working on hardware-software co-design to improve system performance and energy efficiency. Strong backgrounds on architecture and operating system fundamentals. Skilled at programming and scripting, and passionate about wide areas/topics, such as OS, compilation, and deep learning (see tech blog and notes).

Education

Ph.D. in Computer Science (GPA: 3.63/4.0) Aug 2011 - Jul 2017 (*exp.*)
University of Pittsburgh, Pittsburgh, USA
- `Thesis`: *"Exploration of DRAM Scaling via Hardware and Software Co-design"*

M.S. in Computer Science (GPA: 3.63/4.0) Aug 2011 - Dec 2016
University of Pittsburgh, Pittsburgh, USA
- `Project`: *"Improve Large-Scale System Reliability via Enhanced Memory Protection"*

B.E. in Software Engineering (GPA: 90/100.0) Sep 2007 - Jun 2011
Northwestern Polytechnical University (*NPU*), Xi'an, China
- `Thesis`: *"DNA Cryptography based on DNA Fragment Assembly"* (pub in `ICIDT'2012`)

Experiences

[Intern] **NVIDIA® Corporation** Austin, USA
`Research Intern`, Architecture Research Group May 2016 - Aug 2016
- `Mentor`: Niladrish Chatterjee `Manager`: Mike O'Connor

- Design memory system for next generation GPUs to achieve better latency tolerance

[GSR] **University of Pittsburgh** Pittsburgh, USA
`Graduate Student Researcher`, CS Department May 2013 – Apr 2016
- `Advisors`: Prof. *Youtao Zhang*, Prof. *Bruce Childers* and Prof. *Jun Yang* (ECE)

- Improve system performance and energy efficiency via hardware-software co-designs

[Intern] **Alipay® Technology Inc.**, Alibaba Hangzhou, China
`Java Developer Intern`, Group Products Division Aug 2010 – Dec 2010
- Implement a source management system based on SOFA/Spring framework

Comp Skills

Programming: C/C++, JAVA, Linux/Shell/AWK, Python, Android, SQL, R

Tools: Makefile, gcc/g++, GDB, Varius, Vim, Git/hg/P4, Intel Pin, LaTeX

Artifacts: *Framework of DRAM scaling study*, *Pin tool of assembly operation*
Real-time Twitter posts using Arduino and sensors
Python pub-quality plotting tool, *Motion-based Android App*, etc.

Projects (Selected research and course projects during Phd study)

[GPU] `Design Memory System for Future Generation GPUs` 2016 summer
Envision the memory system requirements on future generation GPUs after Pascal; characterize and understand latency tolerance of GPU applications, and adapt cache designs to mitigate performance degradation of relaxed memory access latency. [Internal Reports & Presentations]

[Approx] `Apply Approximate Computing to Improve Memory Performance` 2015.10-2016.08
Write Pintool to annotate variables in source codes and dynamically alter register and memory values to inject runtime errors; implement cache and virtual memory to collect memory access traces, and adapt memory simulator to report performance and energy results. [PACT'2017, MemSys'2016]

[Memory] `Improve performance and energy in DRAM and NVM` 2013.2-2015.9
Perform pioneering studies on DRAM further scaling issues via modeling and simulation [HPCA'2016, TODAES'2017, DATE'2015]; propose encodings to shorten PCM write latency, and re-organize *Domain Wall Memory* (DWM) to reduce cache access energy [ISLPED'2013, ICCD'2015].

< course projects >

[Compiler] `A Compiler for Mini-Java` cs2210: compiler design
Perform lexical analysis, syntax analysis, semantic analysis and code generation.

[Database] `Comparison of NoSQL Databases` cs3550: adv. topics in data management
Compare MongoDB and AsterixDB on YCSB under different query types and secondary indexing.

Research

Memory System, GPU, Computer Architecture and Systems, Software-Hardware Co-design

Publications

8 conference, 1 journal and 1 poster papers (full-list, Google Citation, DBLP)

[C8] `Xianwei Zhang`, Youtao Zhang, Bruce R. Childers and Jun Yang PACT'2017
- `DrMP: Mixed Precision-Guided DRAM Restore for High Performance Approximate and Precise Computing`. Parallel Architectures and Compilation Techniques (PACT), Portland, Oregon, USA, 2017.

[J1] `Xianwei Zhang`, Youtao Zhang, Bruce R. Childers and Jun Yang TODAES'2017
- `On the Restore Time Variations of Future DRAM Memory`. ACM Trans. on Design Automation of Electronic Systems, Vol. 22(2), 26:1-26:24.

[C7] `Xianwei Zhang`, Youtao Zhang, Bruce R. Childers and Jun Yang HPCA'2016
- `Restore Truncation for Performance Improvement in Future DRAM Systems`. The 22nd IEEE Symp. on High Performance Computer Architecture, Barcelona, Spain, 2016.

[C6] `Xianwei Zhang`, Lei Jiang, Youtao Zhang, Chuanjun Zhang and Jun Yang ISLPED'2013
- `WoM-SET: Lowering Write Power of Proactive-SET based PCM Write Strategy Using WoM Code`. The 19th Int'l Symp. on Low Power Electronics and Design, Beijing, China, 2013.
⋆⋆⋆ **Best Paper Award** ⋆⋆⋆

Honors & Awards

Andrew Mellon Predoctoral Fellowship *University of Pittsburgh*'2016
- *awarded to Phd students of exceptional achievement and promise*

Student Travel Awards *HPCA*'2016, *SPAA*'2015, *CS Dept.*'2016&2015

Best Paper Award *ISLPED*'2013
- *based on the rating of anonymous reviewers and a panel of judges*

Recipient of 2011 graduation design (Thesis) key support fund *NPU*'2011
- *small research grant for undergraduate thesis project, 2.5% funding rate*

Tencent® Technology Excellence Scholarship *Tencent Inc.*'2009
- *top grade, 3 winners NPU-wide*

Misc

Homepage: https://people.cs.pitt.edu/∼xianeizhang
Github: https://github.com/cinwell
Blog: http://iarchsys.com
Linkedin: https://www.linkedin.com/in/xianweizhang/