# 作业(3): Memory

截至时间: 2022.12.9/周五 23:59:59

提交方式:超算习堂 (https://easyhpc.net/course/157)

# **Q1-Sol**:

a. 92 + 7x4 = 120

b.  $1 + 10\% \times (10 + 20\% \times 120) = 1 + 0.1 \times (34) = 4.4$ 

c.  $1 + 10\% \times (10 + 20\% \times 92) = 1 + 0.1 \times (28.4) = 3.84$ 

d.  $1 \times 60\% + 2 \times 40\% + 10\% \times (10 + 20\% \times 120) = 1.4 + 3.4 = 4.8$ 

e. Yes, still useful. Way prediction results in faster cache access with hit time as direct mapped instead of associative. Thus, if the access time is longer (rather than the super-fast 1cycle), then way prediction can greatly help shorten the access time.

#### Q2-Sol:

Configuration	A	В	C	D
Cache size	32KB	64KB	16KB	8KB
Block size	16B	128B	32B	64B
Associativity	Direct-mapped	8-way associative	16-way associative	Fully associative
Address bits used for indexing	[14:4]	[12:7]	[9:5]	/
Address bits used for tagging	[63:15]	[63:13]	[63:10]	[63:6]
total # of bits in all tag arrays	51x2K	53x512	56x512	60x128
total # of bits in all data arrays	8x32K	8x64K	8x16K	8x8K

## **O3-Sol**:

- a.  $(64b/4 \times 2Gb) \times 4 \times 4 = 64GB$ ;  $(64b/8 \times 4Gb) \times 4 \times 4 = 64GB$ ;  $(64b/16 \times 8Gb) \times 4 \times 4 = 64GB$
- b.  $1200 \text{ MHz } \times 2 \times 64b \times 4 = 76.8 \text{ GB/s}$

c.

Row being accessed	Arrival time at memory controller	Open-page	Close-page
X	10ns	50ns	50ns
Y	75ns	135ns	115ns
X	150ns	210ns	190ns
X	210ns	230ns	250ns
X	250ns	270ns	290ns
Y	300ns	360ns	340ns

### **O4-Sol**:

- a. The second-level cache is 1 MB and has a 128B block size.
- b. The miss penalty of the second-level cache is approximately 105 ns.
- c. The second-level cache is 8-way set associative.
- d. The main memory is 512 MB.
- e. Walking through pages with a 16B stride takes 946 ns per reference. With 250 such references per page, this works out to approximately 240 ms per page.