Introduction to Digital Logic Design Lab

EECS 31L

LAB2

Date: 1/18/2020

1, Objective

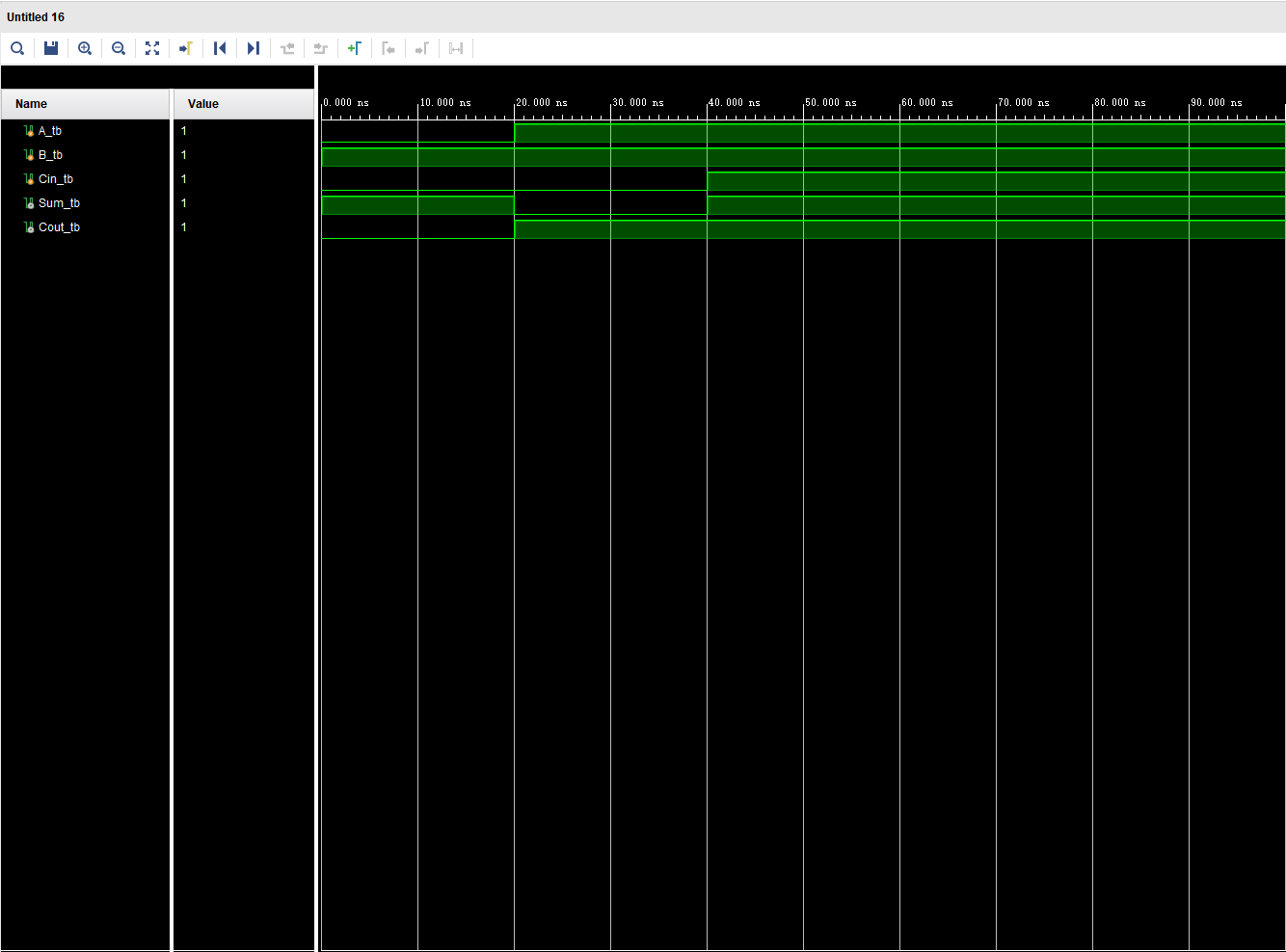
In this lab, I designed 4 Verilog programs to implement the circuit of one-bit full adder, 4 bits full adder, 2-1 multiplexer and 4-1 multiplexer. The relationship between inputs and outputs is obvious, which is outputs come out after inputs are plugged in. In the design of 4 bits full adder, I need to concatenate it with 4 one-bit full adder so there are 2 modules in the main program, which are connected with functions.

2, Procedure

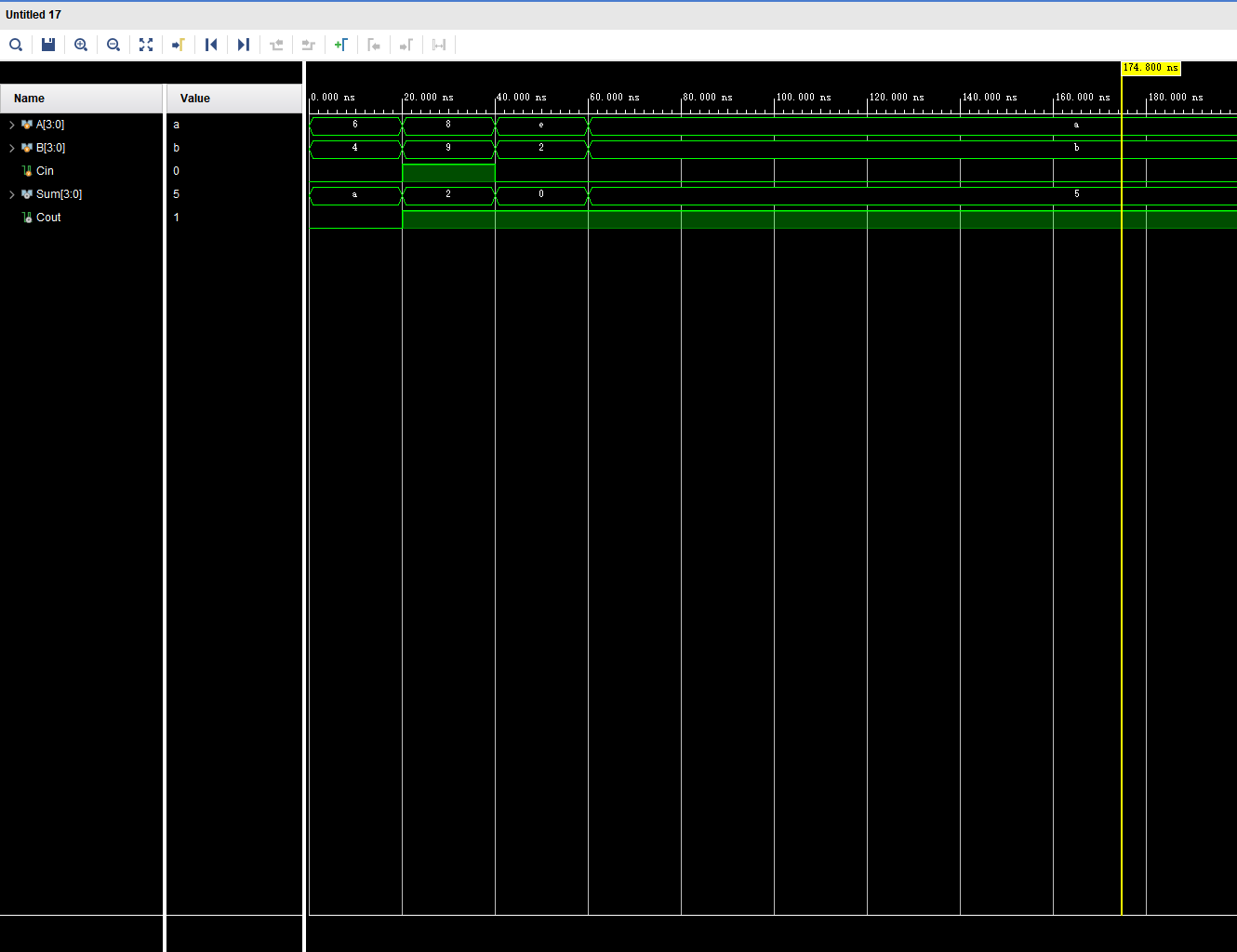
When I designed one-bit full adder, 2-1 multiplexer and 4-1 multiplexer, I used Boolean expression for each for the circuit, which is one of the most efficient ways to implement circuit. I used truth tables and k-maps to find the simplest Boolean expressions. For the design of 4-bit full adder, I literately connected it with 4 one-bit full adder so the only thing I did was I drew a graphic including 4 one-bit full adders.

3, Simulation Results

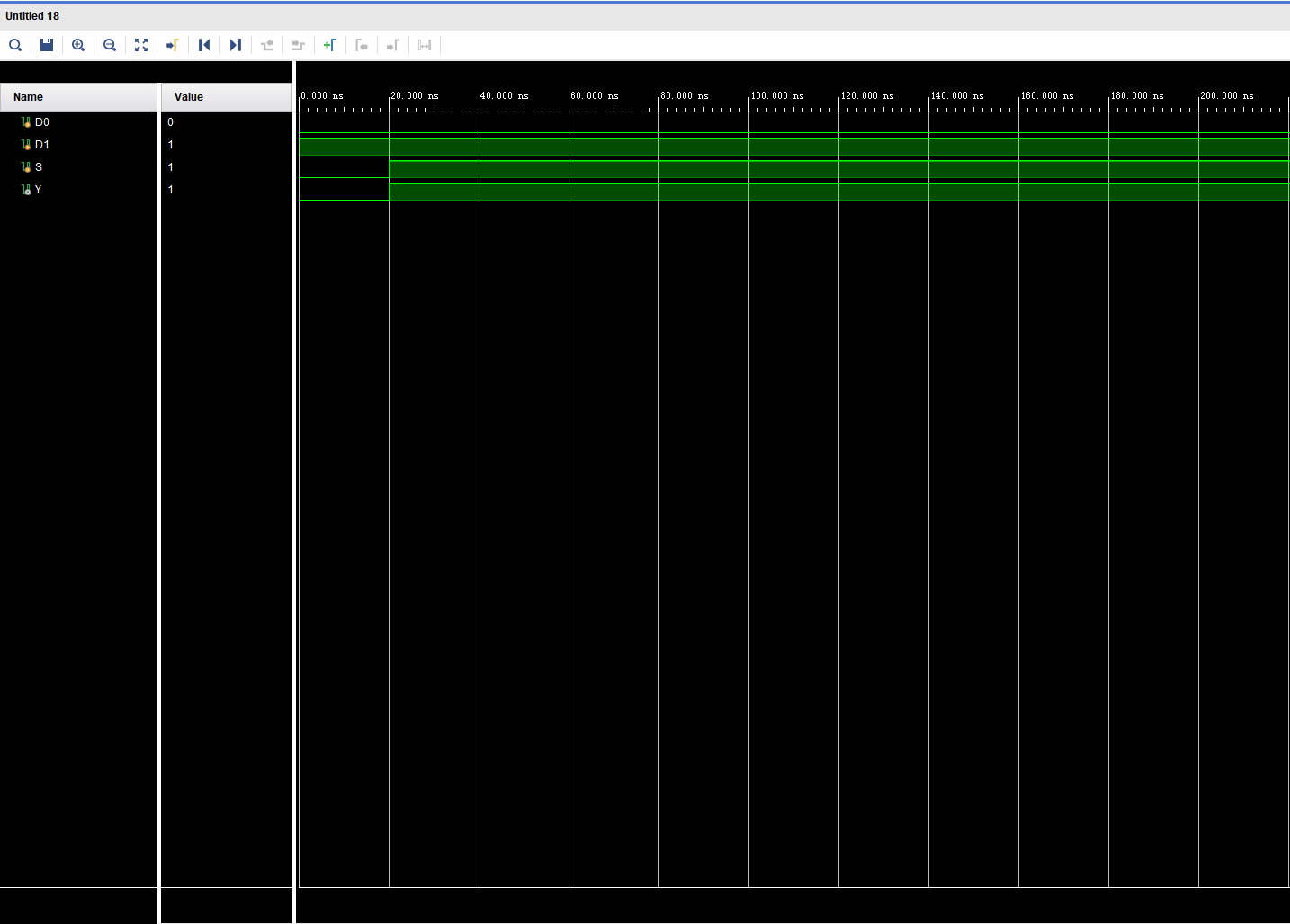
One-bit full adder



4 bits full adder



2-1 Mux



4-1 Mux

