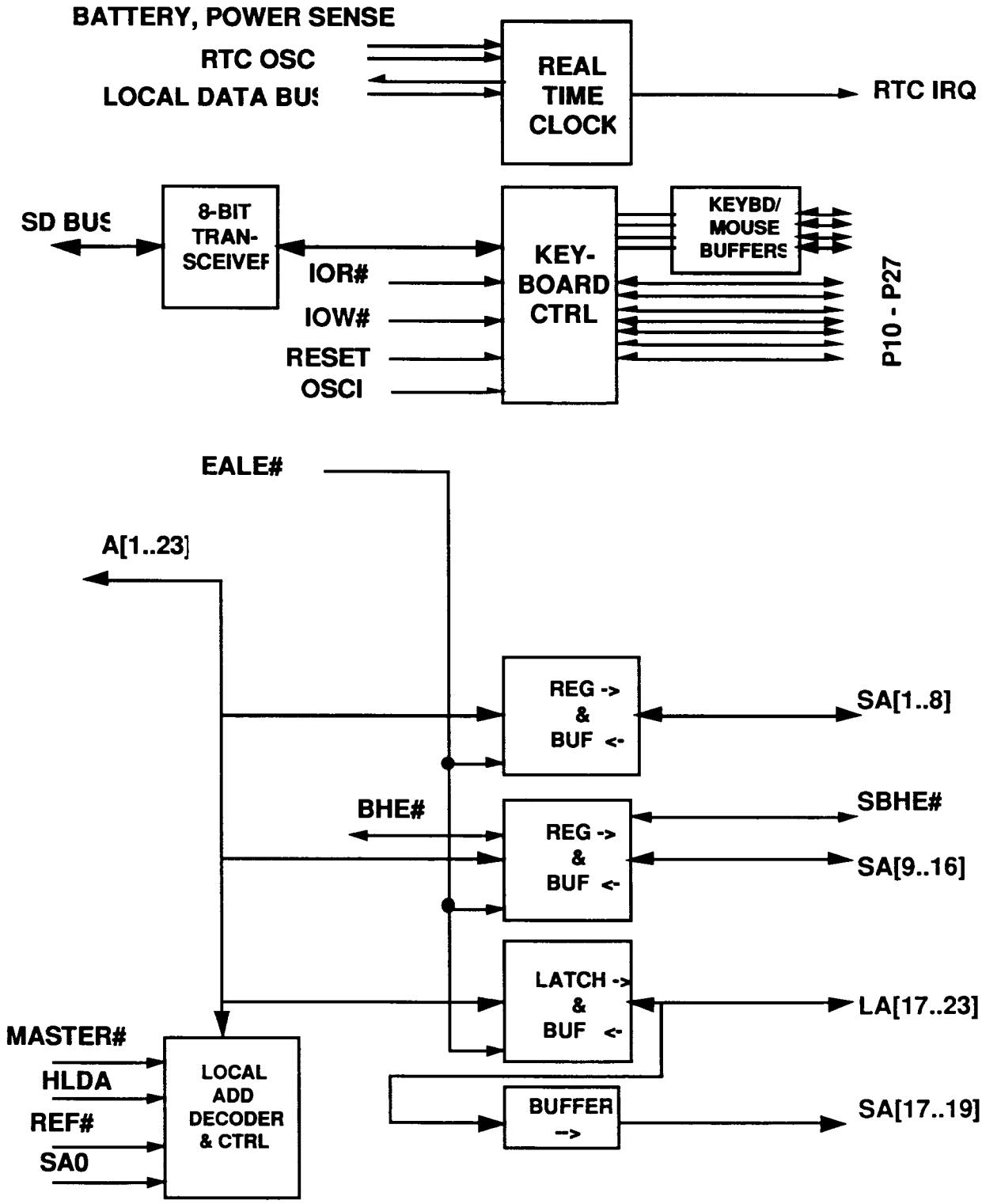
1.0 VL82C113 FEATURES

- Integrated Peripheral Controller for SCAMP VL82C310/311/311L Single Chip PC/AT Controllers
- 146818A Compatible Real Time Clock(RTC)
- 64 Bytes of Battery Backed CMOS RAM, part of RTC
- AT Compatible Keyboard Controller with Integrated PS/2 Mouse Support
- SCAMP Compatible Processor to ISA Bus Address Latches & Buffers
- 1.0µ CMOS in a 100-Pin PQFP
- Real Time Clock relocatable via SA15-SA0 address registers.

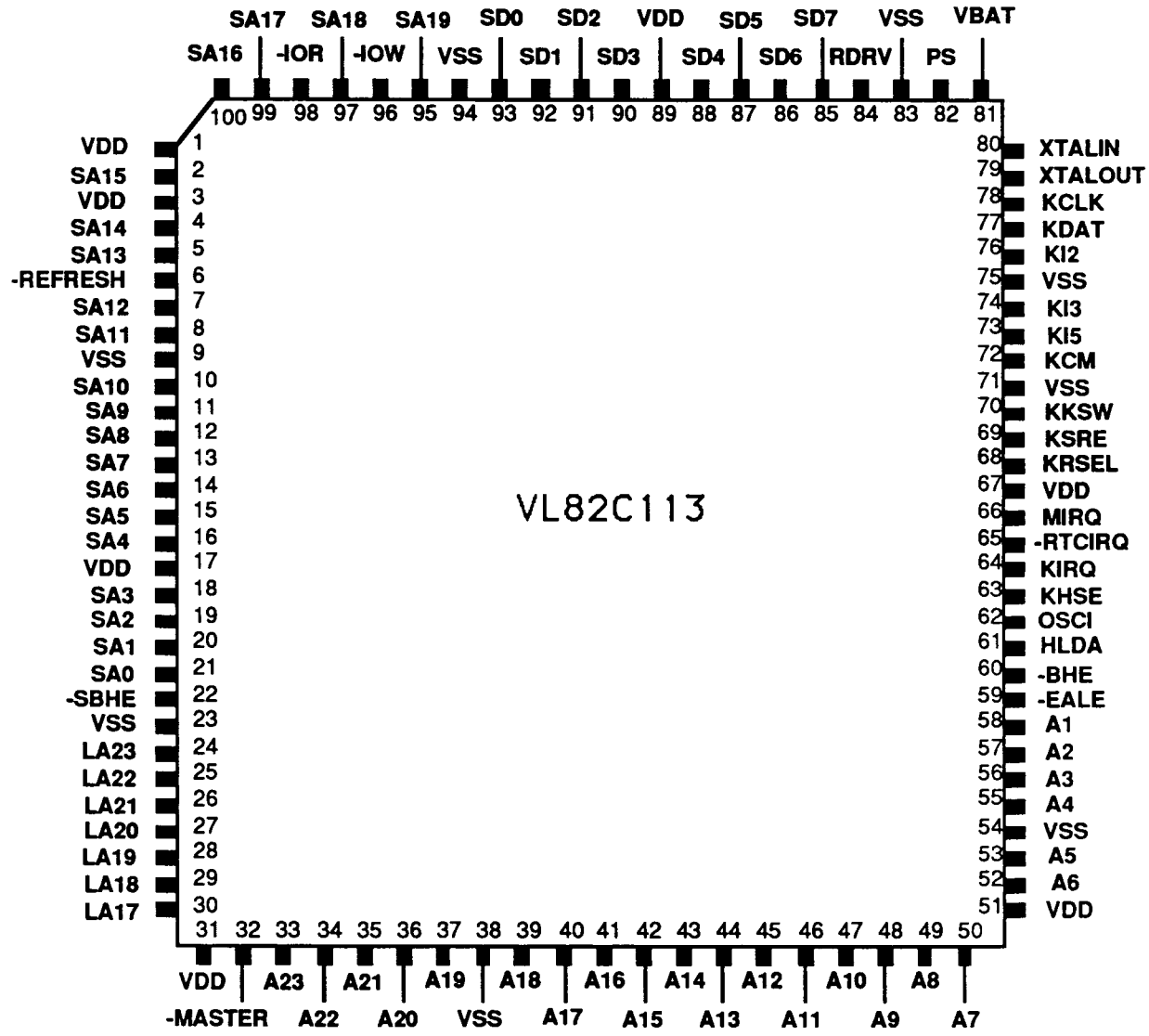
2.0 VL82C113 BLOCK DIAGRAMS



3.0 ORDER INFORMATION

Part Number	Item
VL82C113-FC	SCAMP Combination Chip

4.0 PIN DIAGRAM



5.0 SIGNAL DESCRIPTIONS

SECTION	NUMBER OF PINS
CPU Interface Signals	25
ISA Bus Signals	34
Keyboard Controller Signals	12
SD Data Bus Signals	8
Peripheral Interface Signals	5
Address Bus Control Signal	1
Power and Ground	15

5.1 CPU INTERFACE SIGNALS

Signal	Pin	Type	Description
HLDA	61	I-TTL	Hold Acknowledge. This is the Hold Acknowledge pin directly from the CPU. It is used to control direction on address and to enable the -DACK decoder.
A[1:23]	58,57,56 55,53,52 50,49,48 47,46,45 44,43,42 41,40,39 37,36,35 34,33	IO-TTL	Address bits are outputs when HLDA is high, -MASTER is low and -REFRESH is high. This bus is an input at all other times.
-BHE	60	IO-TTL	Byte High Enable. This pin is an output during MASTER mode non-Refresh cycles and it tracks the -SBHE input. It is an input at all other times.

5.2 ISA BUS SIGNALS

Signal	Pin	Type	Description
RSTDRV	84	I-TTL	This active high input is system reset generated from the POWERGOOD input.
-IOR	98	I-TTL	IO read command.
-IOW	96	I-TTL	IO write command.
-MASTER	32	I-TTL	Master input - active low. This input is used by an external device to disable the internal DMA controllers and get access to the system bus. When asserted it indicates that an external bus master has control of the bus.
-REFRESH	6	I-TTL	Refresh signal, active low. This input signal is pulled low whenever a refresh cycle is initiated.
LA[17:23]	24,25,26 27,28,29 30	IO-TTL	Latch-able Address bus. This bus is an input when HLDA is high, -REFRESH is high and -MASTER is low. It is an output bus driven by the values from the A bus when HLDA is low and -REFRESH is high. It is tri-stated when HLDA is high and -REFRESH is low. The LA bus is latched internally with the -EALE input.
SA[9:19]	95,97,99 100,2,4 5,7,8 10,11	IO-TTL	System Address bus Bits 19 through 9. This bus is an input when HLDA is high, -REFRESH is high and -MASTER is low. It is an output bus driven by the values from the A bus when HLDA is low and -REFRESH is high. It is tri-stated when HLDA is high and -REFRESH is low. The SA[9:19] bus is registered internally with the -EALE input rising edge.

Signal	Pin	Type	Description
SA[1:8]	12,13,14 15,16,18 19,20	IO-TTL	System Address bus Bits 8 through 1. This bus is an input when HLDA is high, -REFRESH is high and -MASTER is low. It is an output bus driven by the values from the A bus at all other times. The SA[1:8] bus is registered internally with the -EALE input rising edge.
SA[0]	21	I-TTL	System Address bus LSB. This is an input at all times and is used in the address decode of internal peripheral registers/ports.
-SBHE	22	IO-TTL	System Byte High Enable. This pin is controlled the same way as the SA bus. -SBHE is registered internally with the -EALE input rising edge.
OSCI	62	I-CMOS	This is the input for the 14.318 MHz oscillator.

5.3 KEYBOARD CONTROLLER SIGNALS

Signal	Pin	Type	Description: PC/AT Keybrd Controller Mode KBDCTRL[1] = 1		PS/2 KBDCTRL[1] = 0	
KCLK	78	IO-TTL	T0/-P26	Kbd Clock	T0/-P26	Kbd Clock
KDAT	77	IO-TTL	T1/P27	Kbd Data	P10/-P27	Kbd Data
KCM	72	I-TPU	P16	Color input	P16	input
KKSW	70	I-TPU	P17	Key Switch P17	input	
KHSE	63	IO-TODS	P22	High Speed	P11/-P22	Mouse Data
KSRE	69	IO-TODS	P23	Shadow RAM	T1/-P23	Mouse Clk
KIRQ	64	IO-TPU	P24	Kbd Int Req	P24	Kbd Int Req
			This pin is sampled on the high to low transition of RSTDRV. If IRQK is low at this time, the KBD function within the VL82C113 is disabled. If IRQK is high at this time, the KBD is enabled. This pin is internally pulled up to VCC.			
MIRQ	66	O	P25	general purpose output	P25	Mouse Int Req
KRSEL	68	I-TTL	P14	RAM Slct	P14	input
KI2/-TRI	76	I-TPU	P12	input	P12	Fuse Input
			This pin is sampled on the high to low transition of RSTDRV. If K12/-TRI is low at this time,all outputs will be tri-stated.. If K12/-TRI is high at this time, the chip will function normally. This pin is internally pulled up to VCC.			
KI3	74	IO-TPU	P13 MISC0	input output	P13 MISC0	input output
KI5	73	IO-TPU	P15 MISC1	input output	P15 MISC1	input output

5.4 SD DATA BUS

Signal	Pin	Type	Description
SD7-0	85,86,87 88,90,91 92,93	IO-TTL	System Data Bus - This bus connects directly to the slots. It is used to transfer data to/from the low byte of local and system devices.

5.5 PERIPHERAL INTERFACE SIGNALS

Signal	Pin	Type	Description
XTALIN	80	I-CMOS	Internal oscillator input for real time clock crystal. Requires a 32.768KHz external crystal or stand alone oscillator.
XTALOUT	79	O	Internal oscillator input for real time clock crystal. See XTALIN. This pin is a no connect when an external oscillator is used.
PS	82	I-TST	The Power Sense input (active-high) is used to reset the status of the Valid RAM and Time (VRT) bit. This bit is used to indicate that the power has failed, and that the contents of the RTC may not be valid. This pin is connected to an external RC network.
VBAT	81	I-TTL	Connected to the RTC hold up battery between 2.4 and 5 volts.

Signal	Pin	Type	Description
-RTCIRQ	65	IO-TODP	Real Time Clock Interrupt Request output(Active low). This pin is an input when RSTDRV is high. This pin is sampled on the high to low transition of RSTDRV. If -RTCIRQ is low at this time, the RTC function within the VL82C113 is disabled. If -RTCIRQ is high at this time, the RTC is enabled. Open drain output.

5.6 ADDRESS BUS CONTROL SIGNAL

Signal	Pin	Type	Description
-EALE	59	I-TTL	Early Address Latch Enable is an active low pulse which is generated at the beginning of any bus cycle initiated from the CPU which is not directed at on-board DRAM.

5.7 POWER AND GROUND PINS

Signal	Pin
GND	9,23,38,54,71,75,83,94
VDD	1,3,17,31,51,67,89

5.8 SIGNAL TYPE LEGEND

Signal Code	Signal Type
I-CMOS	CMOS Level input
I-TTL	TTL Level input
I-TPU	TTL Level input with 30K ohm pullup resistor
I-TST	TTL Level Schmitt trigger input
IO-TTL	TTL Level input/output
IO-TODP	TTL Level input/output open drain with 3K ohm pullup
IO-TODS	TTL Level with open drain output/Schmitt trigger input
IO-TPU	TTL Level input/output with 30K ohm pullup resistor
O	CMOS and TTL Level compatible output

6.0 GENERAL DESCRIPTION & PROGRAMMER'S MODEL

The VL82C113 Combination Chip combines a keyboard controller and Real Time Clock (RTC) with the address latches/buffers which are normally required in SCAMP based systems. While the VL82C113 has been optimized for use with the VL82C310/311/311L SCAMP controller, its uses are not restricted to this device combination.

The keyboard controller and Real Time Clock are enabled/disabled through a combination of hardware and software accessible mechanisms. Software accessible registers are programmed through a series of indexing registers. In this scheme, one register (INDEX Register) is loaded with an 8-bit value which represents the address of the control/data register located within the VL82C113 which is to be read or written. The second register (DATA Register) represents the data path to the register pointed to by the INDEX Register. One pair of indexed registers are used with the VL82C113 and are extensions of the registers used by the VL82C310/311/311L SCAMP controller. These index/data registers are located at the same location within the VL82C310/311/311L SCAMP system controller as they are in the VL82C113. The INDEX2 register is write only. Data2 can be read as well as written. Table 6.1 details the ISA I/O address for the index registers as well as the default addresses for the RTC and keyboard controllers.

Default values for these control registers have been selected so as to eliminate the need to change their values in typical system configurations when the VL82C113 is configured for Chip Select mode of operation.

TABLE 6.1
VL82C113 ISA
I/O Address Map

I/O Address	Register Name	Description
0060 Hex	KBDDAT	Keyboard Controller Input/Output Buffer
0064 Hex	KBDCTL	Keyboard Controller Status/Command Register
0070 Hex	RTCADD	Real Time Clock Address Register
0071 Hex	RTCDAT	Real Time Clock Data Registers
00EC Hex	INDEX2	Configuration INDEX 2 Register
00ED Hex	DATA 2	Configuration DATA 2 Registers

TABLE 6.2
VL82C113
(INDEX2 loc = 00ECh, DATA2 loc = 00EDh)

INDEX Address	Register Name	Description	READ/ WRITE
1B Hex	RTCLSB	RTC Register Address Register - Low Byte	R/W
1C Hex	RTCMSB	RTC Register Address Register - High Byte	R/W
1D Hex	KBDCTRL	Keyboard Controller Control Port	R/W
1F Hex	REVID	ID/Revision Register	Read only

TABLE 6.3
VL82C113
Control, Status, and Configuration Registers
Bit Definitions

Register	D7	D6	D5	D4	D3	D2	D1	D0
RTCLSB	A7	A6	A5	A4	A3	A2	A1	RENA
RTCMSB	A15	A14	A13	A12	A11	A10	A9	A8
KBDCTRL	-KISLP	HSLP	RAMEN	MISC1	MISC0	PRV	MODE	SLP
REVID	1	1	0	0	0	0	0	1

RTC Address Mapping Register - Low Address Byte (RTCLSB); Index Register : ECh, Index Address : 1Bh, Data Register : EDh, DEFAULT = 71h

Bit 0 (RENA), RTC Enable Bit : If set, when SA[15:1] match the 15 bit compare value in RTCLSB and RTCMSB, an access to the RTC is generated. If cleared, all accesses the RTC are disabled. Power on reset default = 1

Bits 1-7 , Lower 7 bits of RTC mapping address. Combined with RTCMSB, this determines the address at which the RTC is accessed.

RTC Address Mapping Register - High Address Byte (RTCMSB);Index Register : ECh, Index Address : 1Ch, Data Register : EDh, DEFAULT = 00h

Bits 0-7 , Upper byte of RTC mapping address : Combined with RTCLSB, this determines the address at which the RTC is accessed. Default is 00h.

Miscellaneous Control Register (KBDCTRL); Index Register : ECh, Index Address : 1Dh, Data Register : ED

Bit 0 Unused Bit. This bit can be written with no effect. Power on reset default = 1.

Bit 1 (MODE) , AT/PS2 Mode Select Bit : If set, Keyboard operates in the AT compatibility mode. If cleared, keyboard operates in the PS/2 keyboard and mouse mode. Power on reset default = 1.

Bit 2 (PRV), Private Controls Enable Bit : If set, this bit prevents the KHSE,KSRE, and IRQM pins from changing current state. If cleared, normal operation of these pins result Power on reset default = 0.

Bit 3 (MISC0), KI3 Output Bit : If the INOROUT bit is set then this bit controls the KI3 output pin directly. If the INOROUT bit is cleared, then this bit's state has no effect. This bit is typically used for Turbo Control.

Bit 4 (MISC1), KI5 Output Bit : If the INOROUT bit is set then this bit controls the KI5 output pin directly. If the INOROUT bit is cleared, then this bit's state has no effect.

Bit 5 (INOROUT), If this bit is set to 1 then KI3 and KI5 will be outputs, if set to 0 then KI3 and KI5 will be inputs, read via Port 1 of the keyboard controller. Power on reset default = 0.

Bit 6 Reserved Bit. This bit is reserved for possible future use. Do not use this bit. Power on reset default = 1.

Bit 7 Reserved Bit. This bit is reserved for possible future use. Do not use this bit.. Power on reset default = 1.

Revision/Chip ID Register (REVID); Index Register : ECh, Index Address : 0Fh, Data Register : EDh

Returns value based on version of 113. For the VL82C113, this value is C0h.

6.1 ADDRESS BUFFERING AND AUXILIARY LOGIC

Details to be supplied in future release of advance information data sheet.

6.2 KEYBOARD

The Keyboard Controller is accessed via internally decoded PORT 060H (read/write data) and PORT 064H (read status/ write command).

PC/AT or PS/2 compatibility is controlled via bit 1 in the KBDCTRL control register.

6.2.1 KEYBOARD CONTROLLER FUNCTIONAL DESCRIPTION

The VL82C113 Keyboard Controller's Micro Controller Unit (MCU) offers a subset of the instruction set of the 8042, with 8042-like instructions. Enhancements have been made to conditional jumps (jumps may be made between pages). The on-chip ROM is loaded with the code that is required to support the PC/AT and PS/2 command sets and 128 bytes of conversion code. A small amount of scratch-pad RAM is provided as an extension of the MCU register set for the purpose of keyboard to host interfacing.

Keyboard serial I/O is handled with hardware implementations of the receiver and transmitter. Both functions depend on an 8-bit timer for time-out detection. Enhanced status reporting is provided in hardware to simplify error handling in software. This logic is duplicated for the Mouse interface.

User RAM support is provided. The program writes the 5-bit address (32-byte range) to a register, and then reads or writes the data through accesses to another register, port 60 DBB.

Parallel ports 1 and 2 are provided, but are restricted to inputs only for P1 and outputs only to P2.

Support for port 60 DBB (reads and writes) and Status register (reads and writes) is provided in hardware for interface to the PC host.

Common PC/AT uses for the Parallel I/O bits are shown below.

- P16 - Color/Monochrome input
- P17 - Key Switch input
- P22 - Speed Select output

6.2.2 Keyboard Controller interface to PC/AT

The interface to the PC/AT consists of 1 register pair (60H/64H) for the keyboard and mouse. Access to the registers is determined by the state of A2 and the chip select. For host control signals involved, the command, status and data registers are accessed as follows. The signal -CS is an internal signal which is the decode of A0-A15 for the register pair 60H/64H:

-CS	-IOR	-IOW	A2	Register
0	0	1	0	Read - Data DBB Output Buffer
0	0	1	1	Read - Status
0	1	0	0	Write - Data DBB Input Buffer
0	1	0	1	Write - Command
1	x	x	x	Not valid

The port 60 DBB read operations output the contents of the Output Buffer to D0 - D7(host bi-directional, tri-statable data bus), and clears the status of the Output Buffer Full (OBF/Status Reg. bit 0) bit.

Status read operations output the contents of the Status register to D0 - D7. No status is changed as a result of the read operation.

The Port 60 DBB write operations cause the Input Buffer DBB to be changed. The state of the C/D bit is cleared (status Reg. bit 3, 0 indicates data) and the Input Buffer Full (IBF/Status Reg. bit 1) bit is set(1).

Command write operations are the same as DBB writes, except that the address is 64H. The C/D bit will be set(1) when a command has been written to address 64H.

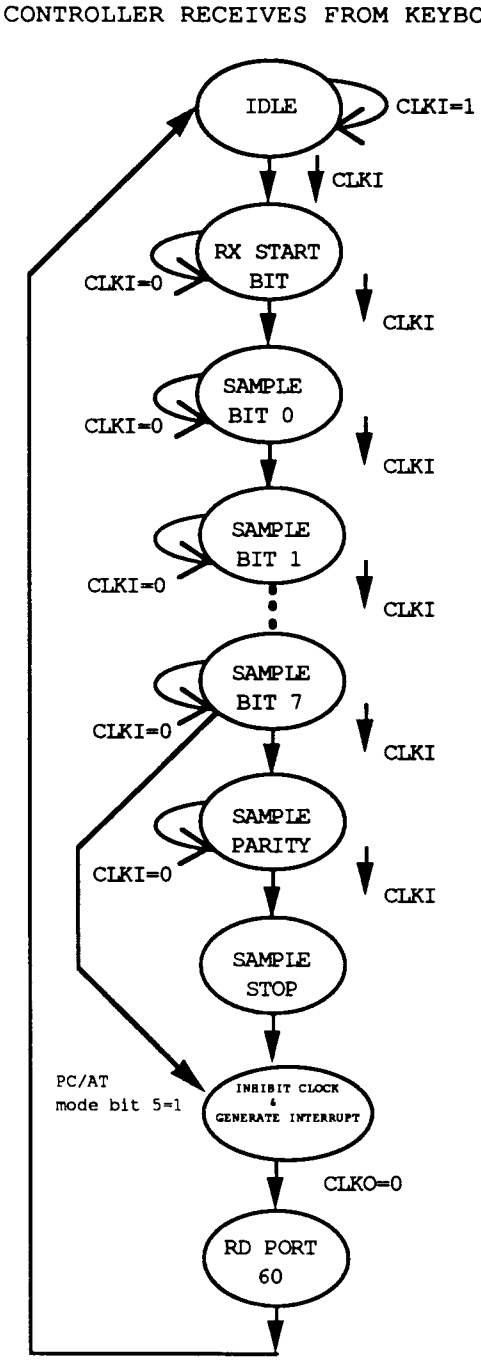
6.2.3 Keyboard Controller Interface Protocol

Data transmission between the controller and the keyboard or mouse consist of a synchronous bit stream over the data and clock lines. The bits are defined as follows:

Bit	Function
1	Start bit (always 0)
2	Data bit 0 (lsb)
3 - 8	Data bits 1 - 6
9	Data bit 7 (msb)
10	Parity bit (odd)
11	Stop bit (always 1)

6.2.3.1 Receive Operation

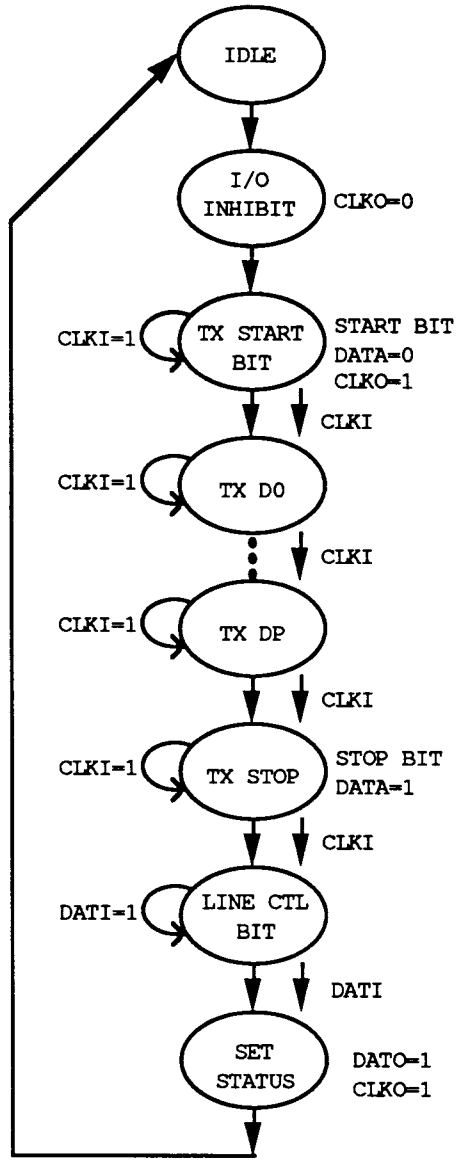
The states that are implemented for receive operations are as follows:



6.2.3.2 Transmit Operation

The states that are implemented for transmit operations are as follows:

CONTROLLER TRANSMITS TO KEYBOARD



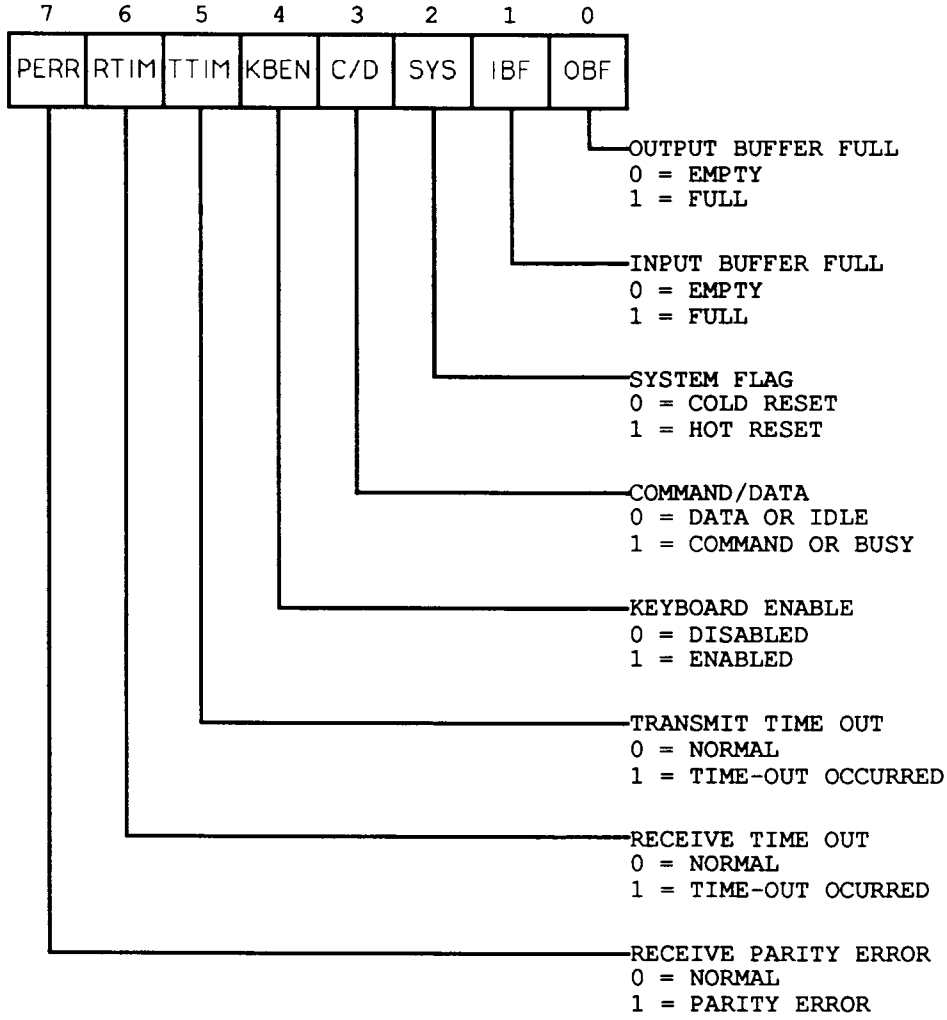
6.2.4 Programmer Interface

The programmer interface to the keyboard controller is quite simple, consisting of 4 registers:

Register	R/W	I/O (see 6.3.1)
Status	R	64H
Command	W	64H
Output Buffer	R	60H
Input Buffer	W	60H

The behavior of these registers differ according to the mode of operation (PC/AT or PS/2). There exists only one status register with different bit definitions for PC/AT mode and PS/2 mode. The bit definitions for the status register in each mode follow.

PC/AT Status Register (Read Only - Port 64H)



PC/AT STATUS REGISTER:

Bit 0 - Output Buffer Full (OBF). This flag is automatically set when the microcontroller loads DBBOUT. It is cleared on a read to port 60H.

Bit 1 - Input Buffer Full (IBF). This flag is set on a write to port 60H or 64H. It is cleared when the microcontroller reads the DBBin contents into the accumulator.

Bit 2 - System Flag (SYS), when set (1) indicates that the CPU has changed from virtual to real mode.

Bit 3 - Command/Data (CD), when set (1) indicates that a command has been placed into the Input Data Buffer of the controller. A (0) indicates data. The controller uses this bit to determine if the byte written is a command to be executed. This bit is updated when the next byte is written to the input Data Buffer.

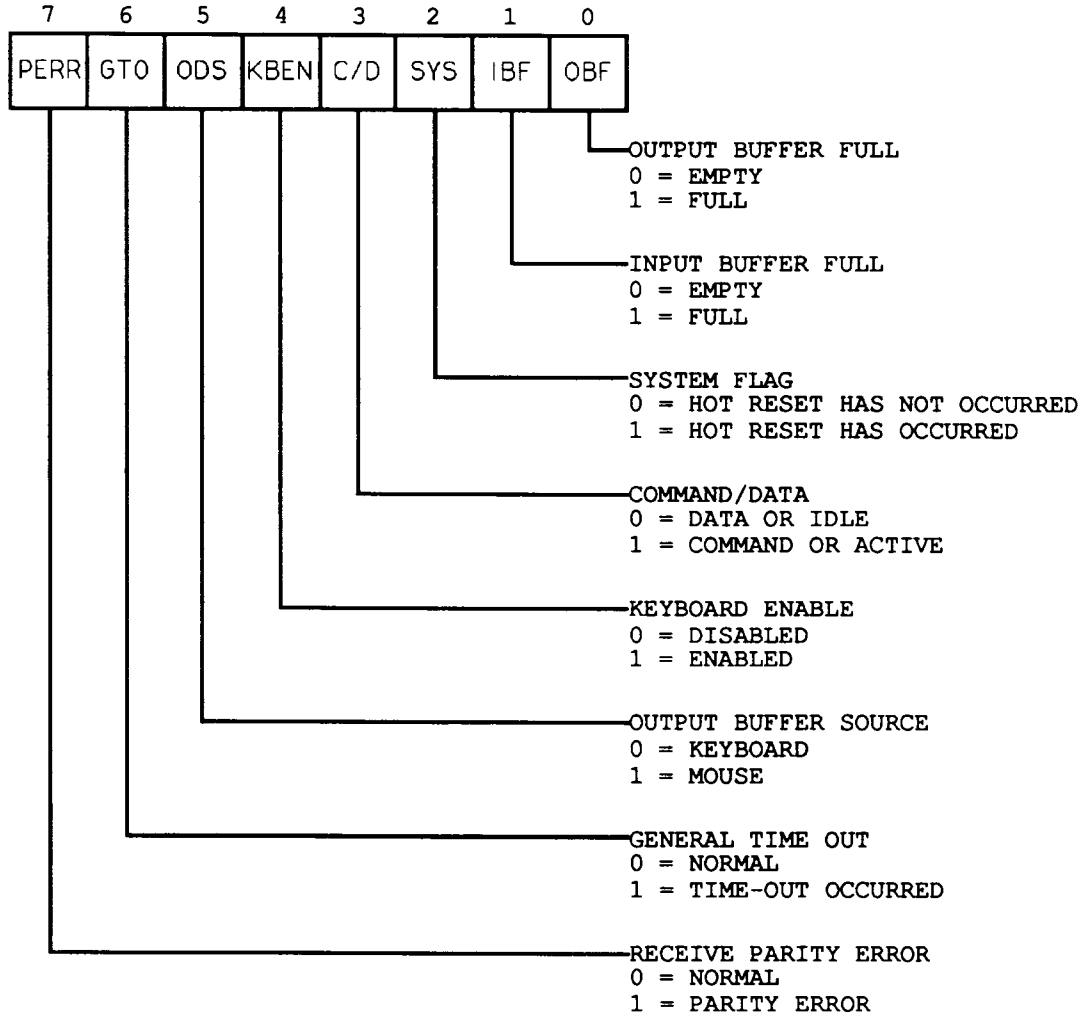
Bit 4 - Keyboard Enable (KBEN), when set (1) indicates that keyboard is currently enabled. When reset indicates that the Keyboard is inhibited.

Bit 5 - Transmit Time Out (TTIM), when set (1) indicates that a transmission to the keyboard was not completed before the controller's internal timer timed-out.

Bit 6 - Receive Time-Out (RTIM), when set (1) indicates that a transmission from the keyboard was not completed before the controller's internal timer timed-out.

Bit 7 - Parity Error (PERR),when set (1) indicates that a parity error (even parity = error) occurred during the last transmission (received scan code) from the keyboard. When a parity error is detected, the output buffer is loaded with FFH, the OBF Status bit is set and the IRQK pin is set (1 if the EKI bit/Mode Reg. bit 0 is set(1)).

PS/2 Status Register (Read Only - Port 64H)



Bit 0 - Output Buffer Full (OBF). This flag is automatically set when the microcontroller loads DBBOUT. It is cleared on a read to port 60H.

Bit 1 - Input Buffer Full (IBF). This flag is set on a write to port 60H or 64H. It is cleared when the microcontroller reads the DBBIN contents into the accumulator.

Bit 2 - System Flag (SYS), when set (1) indicates that the CPU has changed from virtual to real mode.

Bit 3 - Command/Data (CD), when set (1) indicates that a command has been placed into the Input Data Buffer of the controller. A (0) indicates data. The controller uses this bit to determine if the byte written is a command to be executed. This bit is updated when the next byte is written to the input Data Buffer.

Bit 4 - Keyboard Enable (KBEN), when set (1) indicates that keyboard is currently enabled. When reset indicates that the Keyboard is inhibited.

Bit 5 - Output Buffer Data Source (ODS), when set (1) indicates that the data in the output buffer is mouse data. When reset indicates the data is from the keyboard.

Bit 6 - Time-out Error (TERR), when set (1) indicates that a transmission was started and that it did not complete within the normal time taken (approximately 11 KCKIN cycles). If the transmission originated from the controller a FEH is placed in the output buffer. If the transmission originated from the keyboard a FFH is placed in the output buffer.

Bit 7 - Parity Error (PERR),when set (1) indicates that a parity error (even parity = error) occurred during the last transmission from the keyboard. When a parity error is detected, the output buffer is loaded with FFH, the OBF Status bit is set and the IRQK pin is set(1 if the EKI bit/Mode Reg. bit 0 is set(1)).

6.2.5 Keyboard Controller Command Set

The command set
supports 2 modes of operation, and a set of extensions to the AT command set for the PS/2. In both modes, the command is implemented by writing the command byte to 64H. Any subsequent data is read from 60H (see description of command 20) or written to 60H (see description of command 60H). The commands for each mode are shown in the table below:

PC/AT Mode

Command	Description	
20	Read Mode Register	
60	Write Mode Register	
21-3F	Read Keyboard Controller RAM	(Byte 1-31)
61-7F	Write Keyboard Controller RAM	(Byte 1-31)
AA	Self Test	
AB	KBD Interface Test	
AC	Diagnostic Dump	
AD	Disable Keyboard	
AE	Enable Keyboard	
C0	Read Input Port	(P10-P17)
D0	Read Output Port	(P20-P27)
D1	Write Output Port	(P20-P27)
E0	Read Test Inputs	(T0, T1)
F0-FF	Pulse Output Port	(P20-P27)

Added PS/2 Commands

Command	Description	
A4	Test Password	
A5	Load Password	
A6	Enable Password	
A7	Disable Mouse	
A8	Enable Mouse	
A9	Mouse Interface Test	
C1	Poll In Port Low	(P10-P13 -> S4-S7)
C2	Poll In Port High	(P14-P17 -> S4-S7)
D2	Write Kbd Out Buffer	
D3	Write Mouse Out Buffer	
D4	Write to Mouse	

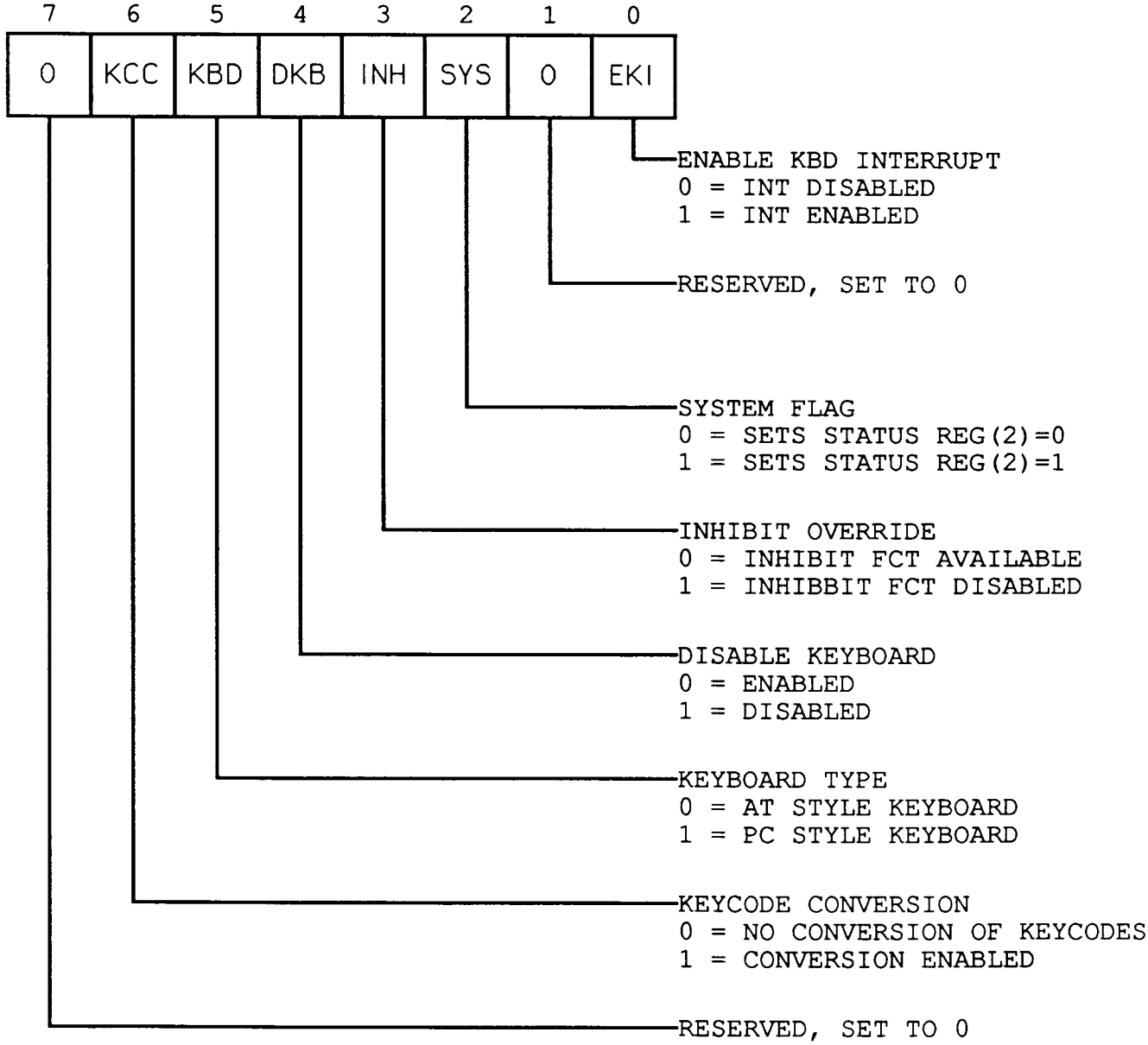
The Keyboard controller will support the following command set, which is described as the hex command code, followed by a description:

20 Read Keyboard controller's Mode Register (PC/AT and PS/2). The keyboard controller sends its current Mode byte to the output buffer (accessed by a Read of Port 60H).

60 Write keyboard controller's Mode Register (PC/AT and PS/2). The next byte of data written to the keyboard data port (60H) is placed in the controller's mode register.

The bit definitions of the mode register for each mode (PC/AT or PS/2) are as follows.

PC/AT Mode Register (R/W - Command 20H/60H to port 60H)



PC/AT MODE REGISTER:

Bit 0 - Enable Keyboard Interrupt (EKI), when set (1) allows the controller to generate a keyboard interrupt whenever data (keyboard or controller) is written into the output buffer.

Bit 1 - Reserved, should be written as 0.

Bit 2 - System Flag (SYS), when set (1) writes the System Flag bit of the Status Register to 1. This bit is used to indicate a switch from virtual to real mode when set.

Bit 3 - Inhibit Override (INH), when set (1) disables the keyboard inhibit function (P17 Switch).

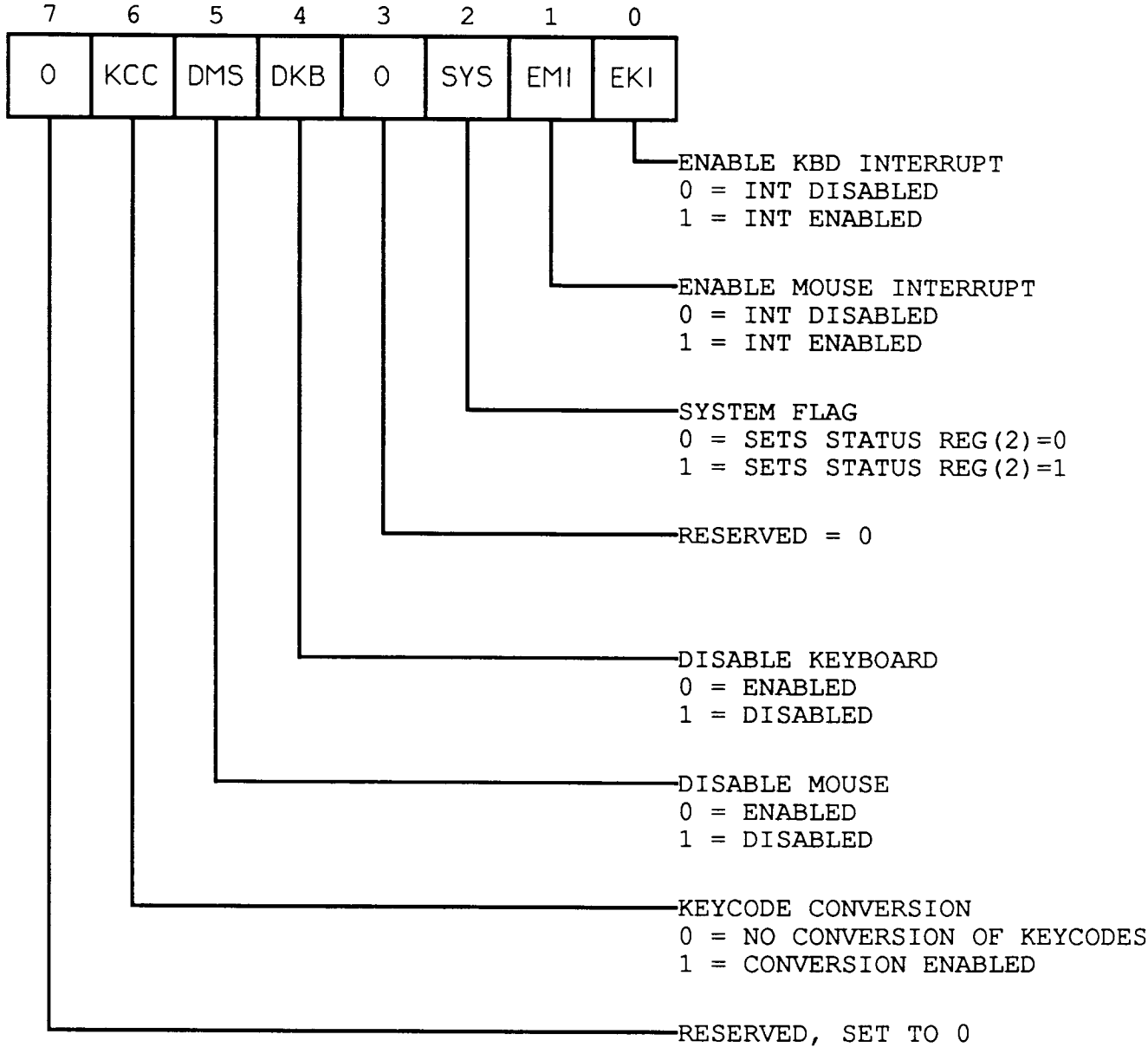
Bit 4 - Disable Keyboard (DKB), when set (1) disables the keyboard by holding the -KCKOUT line high.

Bit 5 - Keyboard Type (KBD), when set (1) allows for compatibility with PC-style keyboards. In this mode, parity is not checked and scan codes are not converted.

Bit 6 - Keycode Conversion (KCC), when set (1) causes the controller to convert the scan codes to PC format. When reset, the codes are passed along unconverted.

Bit 7 - Reserved, should be written as 0.

PS/2 Mode Register (R/W - Command 20H/60H to port 60H)



PS/2 MODE REGISTER:

Bit 0 - Enable Keyboard Interrupt (EKI), when set (1) allows the controller to generate a keyboard interrupt whenever data (keyboard or command) is written into the output buffer.

Bit 1 - Enable Mouse Interrupt (EMI), when set (1) allows the controller to generate a mouse interrupt when mouse data is available in the output buffer.

Bit 2 - System Flag (SYS), when set (1) writes the System Flag bit of the Status Register to 1. This bit is used to indicate a switch from virtual to real mode when set.

Bit 3 - Reserved, 0.

Bit 4 - Disable Keyboard (DKB), when set (1) disables the keyboard by holding the KCLK output high.

Bit 5 - Disable Mouse (DMS), when set (1) disables the mouse by holding the - KSRE output high in PS/2 mode.

Bit 6 - Keycode Conversion (KCC), when set (1) causes the controller to convert the scan codes to PC format. When reset, the codes are passed along unconverted.

Bit 7 - Reserved, 0.

21-3F Read Keyboard Controller RAM (PC/AT and PS/2). Bits D4 - D0 specify the address.

61-7F Write the Keyboard Controller RAM (PC/AT and PS/2). This command writes to the Keyboard Controller RAM with the address specified in bits D4 - D0.

A4 Test Password Installed (PS/2 only). This command checks if there is currently a password installed in the controller. The test result is placed in the output buffer (the OBF bit is set) and IRQK is asserted (if the EKI bit is set). Test result - FAH means that the password is installed, and F1H means that it is not.

A5 Load Password (PS/2 only). This command initiates the password load procedure. Following this command the controller will take data from the input buffer port (60H) until a 00H is detected or a full 8 byte password including a delimiter, 00h, is loaded into the password latches. Note: this means that during password validation the password can be a maximum of 7 bytes plus a delimiter 00h.

A6 Enable Password (PS/2 only). This command enables the security feature. The command is valid only when a password pattern is written into the controller (see A5 command). All keyboard or mouse characters will be discarded until the correct security sequence is completed. System commands are still accepted..

A7 Disable Mouse (PS/2 only). This command sets bit 5 of the mode register which disables the mouse by driving the MCLK line (pin 69) low.

A8 Enable Mouse (PS/2 only). This command resets bit 5 of the mode register, thus enabling the mouse again.

A9 Mouse Interface Test (PS/2 only). This command causes the controller to test the Mouse clock and data lines. The results are placed in the output buffer (the OBF bit is set) and the IRQK line is asserted (if the EKI bit is set). The results are as follows:

Data	Meaning
00	No error
01	Mouse clock line stuck low
02	Mouse clock line stuck high
03	Mouse data line stuck low
04	Mouse data line stuck high

AA Self Test command (PC/AT and PS/2). This commands the controller to perform internal diagnostic tests. A 55H is placed in the output buffer if no errors were detected. The OBF bit is set and IRQK is asserted (if the EKI bit is set).

AB Keyboard Interface Test (PC/AT and PS/ 2). This command causes the controller to test the keyboard clock and data lines. The test result is placed in the output buffer (the OBF bit is set) and the IRQK line is asserted (if the EKI bit is set). The results are as follows:

Data	Meaning
00	No error
01	Keyboard clock line stuck low
02	Keyboard clock line stuck high
03	Keyboard data line stuck low
04	Keyboard data line stuck high

AC Diagnostic Dump (PC/AT only, Reserved on PS/2) - Sends 16 bytes of the controller's RAM, the current state of the input port, and the current state of the output port to the system.

AD Keyboard Disable (PC/AT and PS/2) - This command sets bit 4 of the Mode Register to a 1. This disables the keyboard by driving the clock line (KCLK, pin 78) low. Data will not be received. The keyboard will be enabled after the system sends data to be transmitted to the keyboard.

AE Keyboard Enable (PC/AT and PS/2) - This command resets bit 4 of the mode byte to a 0. This enables the keyboard again by allowing the keyboard clock to free-run.

C0 Read P1 Input Port (PC/AT and PS/2) - This command reads the keyboard input port and places it in the output buffer. This command overwrites the data in the buffer.

C1 Poll Input Port low (PS/2 only) - P1 bits 0 - 3 are written into Status register bits 4 - 7. The bits are restored to their original status upon a write to port 64H.

C2 Poll Input Port high (PS/2 only) - P1 bits 4 - 7 are written into Status register bits 4 - 7. The bits are restored to their original status upon a write to port 64H.

D0 Read Output Port (PC/AT and PS/2) - This command causes the controller to read the P2 output port and place the data in its output buffer. The definitions of the bits are as follows:

Bit	Pin	PC/AT Mode	PS/2 Mode
0	P20		
1	P21		
2	P22	Speed Sel (ENMOD)	Mouse Data
3	P23	Shadow Enable	Mouse Clock
4	P24	Output Buffer Full	IRQK
5	P25		IRQM
6	P26	-KCKOUT	-KCKOUT
7	P27	KDOUT	-KDOUT

Note that P22 (bit 2) is the Speed Control pin used by Award BIOS, and this is different from what is used by Phoenix and AMI. However, the use of this bit is transparent to the Keyboard Controller.

D1 Write output port (PC/AT and PS/2) - The next byte of data written to the keyboard data port (60H) will be written to the controllers output port. The definitions of the bits are as defined above. In PC/AT mode P26 and P27 will not altered. For PS/2 mode, P22, P23, P26 and P27 cannot be altered.

D2 Write Keyboard Output Buffer (PS/2 only) - The next byte written to the data buffer (60H) is written the output buffer (60H) as if initiated by the keyboard (the OBF bit is set(1) and IRQK will be set if the EKI bit is set(1)).

D3 Write Mouse Output Buffer (PS/2 only) - The next byte written to the data buffer (60H) is written to the output buffer as if initiated by the mouse (the OBF bit is set(1) and IRQM will be set if the EMI bit is set(1)).

D4 Write to Mouse (PS/2 only) - The next byte written to the data buffer (60H) is transmitted to the Mouse.

Note: If data is written to the data buffer (60H) and the command preceding it did not expect data from port (60H) the data will be transmitted to the keyboard.

E0 Read Test inputs (PC/AT and PS/2) - This command causes the controller to read the T0 and T1 input bits. The data is placed in the output buffer with the following meanings:

Bit	PC/AT Mode	PS/2 Mode
0	Keyboard Clock	Keyboard Clock
1	Keyboard Data	Mouse Clock
3 - 7	Read as 0's	Read as 0's

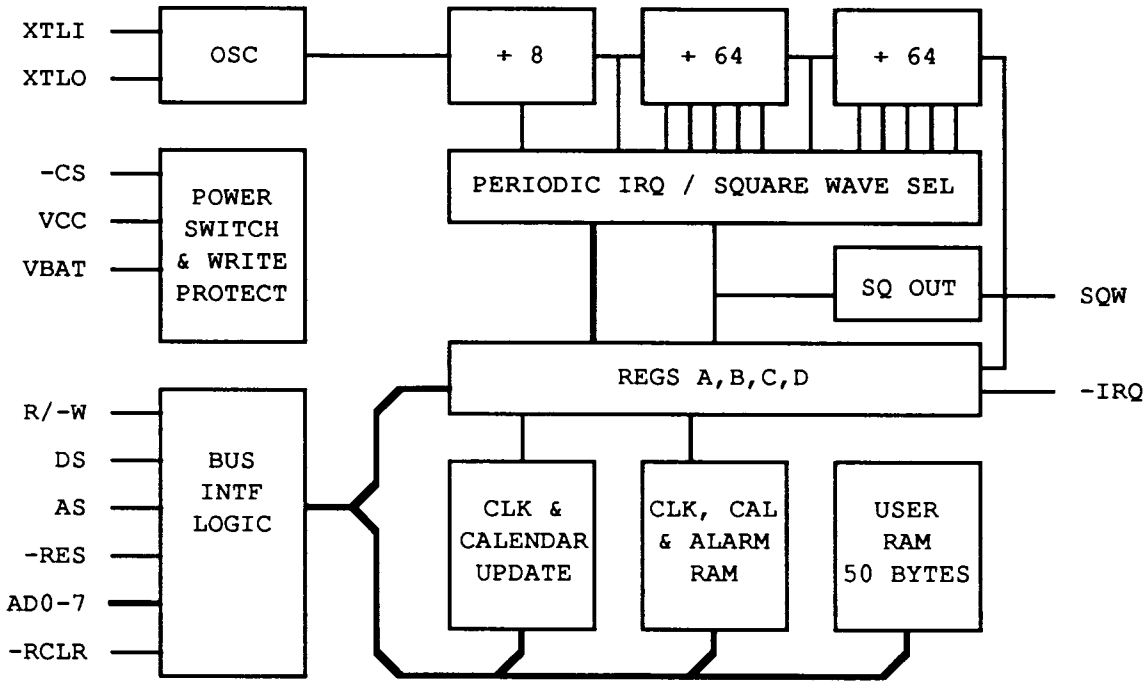
F0-FF Pulse Output Port (PC/AT and PS/2) - Bits 0 - 3 of the controller's output port may be pulsed low for approximately 6 μS. Bits 0 - 3 of the command specify which bit will be pulsed. A 0 indicates that the bit should be pulsed, a 1 indicates that the bit should not be modified. FF is treated as a special case (Pulse Null Port). (Note: In PS/2 mode, bits P22 and P23 will not be pulsed).

6.3 REAL TIME CLOCK DESCRIPTION

The Real Time Clock portion of the VL82C113 performs the following functions:

- Time of day clock
- Alarm function
- 100 year calendar function
- Programmable periodic interrupt output
- Programmable Square Wave output
- 50 Bytes of User RAM
- User RAM Preset feature

RTC BLOCK DIAGRAM:



The RTC memory consists of 10 RAM bytes which contain the time, calendar, and alarm data, four control and status bytes, and 50 general purpose RAM bytes. The address map of the real time clock is shown in the diagram below.

Address	Function	Range
0	Seconds (time)	0 - 59
1	Seconds (alarm)	0 - 59
2	Minutes (time)	0 - 59
3	Minutes (alarm)	0 - 59
4	Hours (time)	1 - 12 - 12 Hr mode
4	Hours (time)	0 - 23 - 24 Hr mode
5	Hours (alarm)	0 - 23
6	Day of week	1 - 7
7	Date of Month	1 - 31
8	Month	1 - 12
9	Year	0 - 99
10	RTC Register A	(R/W)
11	RTC Register B	(R/W)
12	RTC Register C	(R O)
13	RTC Register D	(R O)
14-127	User RAM (Standby)	

All 64 bytes are directly readable and write-able by the processor program except for the following:

1) Registers C and D are read only
2) Bit 7 of Register A is read only
3) Bit 7 of the seconds byte is read only.

The total address map is shown below:

Address	Function
0 - 13	Time portion of RTC
14 - 63	Scratchpad RAM portion of RTC
64 - 127	Additional Scratchpad RAM

The processor program obtains time and calendar information by reading the appropriate locations. The program may initialize the time, calendar, and alarm by writing to these RAM locations. The contents of the 10 time, calendar, and alarm bytes may be either binary or binary-coded decimal (BCD).

6.3.1 Time of Day Register Descriptions

The contents of the Time of Day registers can be either in Binary or BCD format. They are relatively straight-forward, but are detailed here for completeness. The address map of these registers is shown below:

Address	Function	Range
0	Seconds (time)	0 - 59
1	Seconds (alarm)	0 - 59
2	Minutes (time)	0 - 59
3	Minutes (alarm)	0 - 59
4	Hours (time)	1 - 12 (12 Hr mode)
4	Hours (time)	0 - 23 (24 Hr mode)
5	Hours (alarm)	0 - 23
6	Day of week	1 - 7
7	Date of Month	1 - 31
8	Month	1 - 12
9	Year	0 - 99

Address 0 - Seconds: The range of this register is 0 - 60 in BCD mode, and 0 - 3BH in Binary Mode.

Address 1 - Seconds Alarm: The range of this register is 0 - 60 in BCD mode, and 0 - 3BH in Binary Mode.

Address 2 - Minutes: The range of this register is 0 - 60 in BCD mode, and 0 - 3BH in Binary Mode.

Address 3 - Minutes Alarm: The range of this register is 0 - 60 in BCD mode, and 0 - 3BH in Binary Mode.

Address 4 - Hours: The range of this register is:

Range	Mode	Time
1 - 12	BCD	AM
81 - 92	BCD	PM
01H - 0CH	Binary	AM
81H - 8CH	Binary	PM

Address 5 - Hours Alarm: The range of this register is:

Range	Mode	Time
1 - 12	BCD	AM
81 - 92	BCD	PM
01H - 0CH	Binary	AM
81H - 8CH	Binary	PM

Address 6 - Day of Week: The range of this register is 1 - 7 in BCD mode, and 1 - 7H in Binary Mode.

Address 7 - Date: The range of this register is 1 - 31 in BCD mode, and 1 - 1FH in Binary Mode.

Address 8 - Month: The range of this register is 1 - 12 in BCD mode, and 1 - 0CH in Binary Mode.

Address 9 - Year: The range of this register is 0 - 99 in BCD mode, and 0 - 63H in Binary Mode.

6.3.2 RTC Control Register Descriptions

The 146818 has four registers which are accessible to the processor program. The four registers are also fully accessible during the update cycle.

Address	Function	Type
10	RTC Register A	(R/W)
11	RTC Register B	(R/W)
12	RTC Register C	(R O)
13	RTC Register D	(R O)
14-63	User RAM (Standby)	(R/W)

6.3.2.1 Register A Description

This register contains control bits for the selection of Periodic Interrupt, input divisor, and the Update In Progress Status bit. The bits in the register are defined as follows:

Bit	Description	Abbr
0	Rate Select bit 0	RS0
1	Rate Select bit 1	RS1
2	Rate Select bit 2	RS2
3	Rate Select bit 3	RS3
4	Divisor bit 0	DV0
5	Divisor bit 1	DV1
6	Divisor bit 2	DV2
7	Update In Progress	UIP

Bits 0 to 3 - The four rate selection bits (RS0 to RS3) select one of 15 taps on the 22-stage divider, or disable the divider output. The tap selected may be used to generate a periodic interrupt. These four bits are read/write bits which are not affected by RESET. The Periodic Interrupt Rate that results from the selection of various tap values is as follows:

RS Value	Periodic Interrupt Rate
0	None
1	3.90625 ms
2	7.8125 ms
3	122.070 µs
4	244.141 µs
5	488.281 µs
6	976.562 µs
7	1.953125 ms
8	3.90625 ms
9	7.8125 ms
0AH	15.625 ms
0BH	31.25 ms
0CH	62.5 ms
0DH	125 ms
0EH	250 ms
0FH	500 ms

Bits 4 to 6 - The three Divisor Selection bits (DV0 to DV2) are fixed to provide for only a 5-state divider chain, which would be used with a 32 kHz external crystal. Only bit 6 of this register can be changed allowing control of the reset for the divisor chain. When the divider reset is removed the first update cycle begins one-half second later. These bits are not affected by power-on reset (external pin).

DV Value	Condition
2	Operation mode, divider running
6	Reset mode, divider in reset state

Bit 7 - The update in progress (UIP) bit is a status flag that may be monitored by the program. When UIP is a 1 the update cycle is in progress or will soon begin. When UIP is a 0 the update cycle is not in progress and will not be for at least 244 µs. The time, calendar, and alarm information in RAM is fully available to the program when the UIP bit is 0. The UIP bit is a read-only bit, and is not affected by reset. Writing the SET bit in register B to a 1 will inhibit any update cycle and then clear the UIP status bit.

6.3.2.2 Register B Description

Register B contains command bits to control various modes of operations and interrupt enables for the RTC. The bits in this register are defined as follows:

Bit	Description	Abbr
0	Daylight Savings Enable	DSE
1	24/12 Mode	24/12
2	Data Mode (Binary or BCD)	DM
3	Not Used	
4	Update End Interrupt Enable	UIE
5	Alarm Interrupt Enable	AIE
6	Periodic Interrupt Enable	PIE
7	Set Command	SET

Bit 0 - The Daylight Savings Enable (DSE) bit is a read/write bit which allows the program to enable two special updates (when DSE is 1). On the last Sunday in April the time increments from 1:59:59 AM to 3:00:00 AM. On the last Sunday in October when the time first reaches 1:59:59 AM it changes to 1:00:00 AM. These special updates do not occur when the DSE bit is a 0. DSE is not changed by any internal operations or reset.

The elimination of this feature will be considered, since the start date of Daylight Savings time is currently being changed.

Bit 1 - The 24/12 control bit establishes the format of the hours bytes as either the 24-hour mode (1) or the 12-hour mode (0). This is a read/write bit, which is affected only by software.

Bit 2 - The data mode (DM) bit indicates whether time and calendar updates are to use binary or BCD formats. The DM bit is written by the processor program and may be read by the program, but is not modified by any internal functions or reset. A 1 in DM signified binary data, while a 0 in DM specifies binary-coded-decimal (BCD) data.

Bit 3 - This bit is unused in this version of the RTC, but is used for Square Wave Enable in the Motorola 146818.

Bit 4 - The UIE (Update-end Interrupt Enable) bit is a read/write bit which enables the update-end flag (UF) bit in register C to assert an -RTCIRQ. The reset pin being asserted or the SET bit going high clears the UIE bit.

Bit 5 - The Alarm Interrupt Enable (AIE) bit is a read/write bit which when set to a 1 permits the alarm flag (AF) bit in register C to assert an -RTCIRQ. An alarm interrupt occurs for each second that the three time bytes equal the three alarm bytes (including a "don't care" alarm code of 11XXXXXXb). When the AIE bit is a 0, the AF bit does not initiate an -RTCIRQ signal. The reset pin clears AIE to 0. The internal functions do not affect the AIE bit.

Bit 6 - The Periodic Interrupt Enable (PIE) bit is a read/write bit which allows the periodic-interrupt flag (PF) bit in Register C to cause the -RTCIRQ pin to be driven low. A program writes a 1 to the PIE bit in order to receive periodic interrupts at the rate specified by the RS3, RS2, RS1, and RS0 bits in Register A. A 0 in PIE blocks - RTCIRQ from being initiated by a periodic interrupt, but the periodic flag (PF) bit is still set at the periodic rate. PIE is not modified by any internal functions, but is cleared to 0 by a reset.

Bit 7 - When the SET bit is a 0, the update cycle functions normally by advancing the counts once-per-second. When the SET bit is written to a 1, any update cycle in progress is aborted and the program may initialize the time and calendar bytes without an update occurring in the midst of initializing. SET is a read/write bit which is not modified by reset or internal functions.

6.3.2.3 Register C Description

Register C contains status information about interrupts and internal operation of the Real Time Clock. The bits in this register are defined as follows:

Bit	Description	Abbr
0	Not used, read as 0	
1	Not used, read as 0	
2	Not used, read as 0	
3	Not used, read as 0	
4	Update Ended Flag	UF
5	Alarm Interrupt Flag	AF
6	Periodic Interrupt Flag	PF
7	-RTCIRQ Pending Flag	IRQF

Bits 0 to 3 - The unused bits of Status Register 1 are read as 0's, and cannot be written.

Bit 4 - The Update-ended Interrupt Flag (UF) bit is set after each update cycle. When the UIE bit is a 1, the 1 in UF causes the IRQF bit to be a 1, asserting -RTCIRQ. UF is cleared by a Register C read or a reset.

Bit 5 - A 1 in the AF (Alarm interrupt Flag) bit indicates that the current time has matched the alarm time. A 1 in the AF causes the -RTCIRQ pin to go low, and a 1 to appear in the IRQF bit, when the AIE bit also is a 1. A reset or a read of register C clears AF.

Bit 6 - The Periodic interrupt Flag (PF) is a read-only bit which is set to a 1 when a particular edge is detected on the selected tap of the divider chain. The RS3 to RS0 bits establish the periodic rate. PF is set to a 1 independent of the state of the PIE bit. PF being a 1 initiates an -RTCIRQ signal and sets the IRQF bit when PIE is also a 1. The PF bit is cleared by a reset or a software read of Register C.

Bit 7 - The Interrupt Request Flag (IRQF) is set to a 1 when one or more of the following are true:

PF = PIE = 1
AF = AIE = 1
UF = UIE = 1

The logic can be expressed in equation form as:

IRQF = PF • PIE + AF • AIE + UF • UIE

Any time the IRQF bit is a 1, the -RTCIRQ pin is asserted. All flag bits are cleared after Register C is read by the program or when the reset pin is asserted.

6.3.2.4 Register D Description

This register contains a bit that indicates the status of the on-chip stand-by RAM. The contents of the registers are described as the following:

Bit	Description	Abbr
0	Not used, read as 0	-
1	Not used, read as 0	-
2	Not used, read as 0	-
3	Not used, read as 0	-
4	Not used, read as 0	-
5	Not used, read as 0	-
6	Not used, read as 0	-
7	Valid RAM Data and Time	VRT

Bits 0 to 6 - The remaining bits of register D are unused. They cannot be written, but are always read as 0's.

Bit 7 - The Valid RAM and Time (VRT) bit indicates the condition of the contents of the RAM, provided the power sense (PS) pin is satisfactorily connected. A 0 appears in the VRT bit when the power-sense pin is low. The processor program can set the VRT bit when the time and calendar are initialized to indicate that the RAM and time are valid. The VRT is a read only bit which is not modified by the reset pin. The VRT bit can only be set by reading Register D.

6.3.3 RTC CMOS Stand-by RAM Description

In addition to the 50 general purpose RAM bytes that are not dedicated within the 146818, the VL82C113 provides an additional 64 bytes of battery- backed RAM for general purpose uses They can be used by the system BIOS or user program, and are available during the RTC update cycle.

6.3.4 General Operational Notes

Set Operation:

Before initializing the internal registers, the SET bit in Register B should be set to a 1 to prevent time/calendar updates from occurring. The program initialized the 10 locations in the selected format (binary or BCD), then indicates the format in the data mode (DM) bit of Register B. All 10 time, calendar, and alarm bytes must use the same data mode, either binary or BCD. The SET bit may now be cleared to allow updates. Once initialized the real-time clock makes all updates. Once initialized the real-time clock makes all updates in the selected data mode. The data mode cannot be changed without re-initializing the 10 data bytes.

BCD vs Binary Format:

The 24/12 bit in Register B establishes whether the hour locations represent 1-to-12 or 0-to-23. The 24/12 bit cannot be changed without re-initializing the hour locations. When the 12-hour format is selected the high-order bit of the hours byte represents PM when it is a 1.

Update Operation:

The time, calendar, and alarm bytes are not always accessible by the processor program. Once-per-second the 10 bytes are switched to the update logic to be advanced by one second and to check for an alarm condition. If any of the 10 bytes are read at this time, the data outputs are undefined. The update lockout time is 1948 µs for the 32.768 kHz time base. The Update Cycle section shows how to accommodate the update cycle in the processor program.

Alarm Operation:

The three alarm bytes may be used in two ways. First, when the program inserts an alarm time in the appropriate hours, minutes, and seconds alarm locations, the alarm interrupt is initiated at the specified time each day if the alarm enable bit is high. The second usage is to insert a "don't care" state in one or more of three alarm bytes. The "don't care" code is any byte from 0C0H to 0FFH. An alarm interrupt each hour is created with a "don't care" code in the hours alarm location. Similarly, an alarm is generated every minute with "don't care" codes in the hours and minutes alarm bytes. The "don't care" codes in all three alarm bytes create an interrupt every second.

Interrupts:

The RTC plus RAM includes three separate fully automatic sources of interrupts to the processor. The alarm interrupt may be programmed to occur at rates from one-per-second to one-a-day. The periodic interrupt may be selected for rates from half-a-second to 30.517 µs. The update-ended interrupt may be used to indicate to the program that an update cycle is completed.

The processor program selects which interrupts, if any, it wishes to receive. Three bits in register B enable the three interrupts. Writing a 1 to a interrupt-enable bit permits that interrupt to be initiated when the event occurs. A 0 in the interrupt-enable bit prohibits the -RTCIRQ pin from being asserted due to the interrupt cause.

If an interrupt flag is already set when the interrupt becomes enabled, the -RTCIRQ pin is immediately activated, though the interrupt initiating the event may have occurred much earlier. Thus, there are cases where the program should clear such earlier initiated interrupts before first enabling new interrupts.

When an interrupt event occurs a flag bit is set to a 1 in register C. Each of the three interrupt sources have separate flag bits in register C, which are set independent of the state of the corresponding enable bits in register B. The flag bit may be used with or without enabling the corresponding enable bits.

DIVIDER CONTROL

The divider-control bits are fixed for only 32.768 kHz operation. The divider chain may be held reset, which allows precision setting of the time. When the divider is changed from reset to an operating time base, the first update cycle is one-half second later. The divider-control bits are also used to facilitate testing the 146818.

SQUARE-WAVE OUTPUT SELECTION

This version of the 146818 does not support the Square-Wave output function.

PERIODIC INTERRUPT SELECTION

The periodic interrupt allows the -RTCIRQ pin to be triggered from once every 500 ms to once every 30.517 µs. The periodic interrupt is separate from the alarm interrupt which may be output from once-per-second to once-per-day.

UPDATE CYCLE

The 146818 executes an update cycle one-per-second, assuming one of the proper time bases is in place, the DV0-DV2 divider is not clear, and the SET bit in Register B is clear. The SET bit in the 1 state permits the program to initialize the time and calendar bytes by stopping an existing update and preventing a new one from occurring.

The primary function of the update cycle is to increment the seconds byte, check for overflow, increment the minutes byte when appropriate and so forth through to the year of the century byte . The update cycle also compares each alarm byte with the corresponding time byte and issues an alarm if a match or if a "don't care" code (11XXXXXX) is present in all three positions.

With a 32.768 kHz time base update cycle takes 1984 µs, during which, the time, calendar, and alarm bytes are not accessible by the processor program. The 146818 protects the program from reading transitional data. This protection is provided by switching the time, calendar, and alarm portion of the RAM off the microprocessor bus during the entire update cycle. If the processor reads these RAM locations before the update is complete the output will be undefined. The update is progress (UIP) status bit is set during the interval.

A program which randomly accesses the time and date information finds data unavailable statistically once every 4032 attempts. Three methods of accommodating non-availability during update are usable by the program. In discussing the three methods it is assumed that at random points user programs are able to call a subroutine to obtain the time of day.

The first method of avoiding the update cycle uses the update-ended interrupt. If enabled, an interrupt occurs after every update cycle which indicates that over 999 ms are available to read valid time and date information. Before leaving the interrupt service routine, the IRQF bit in register C should be cleared.

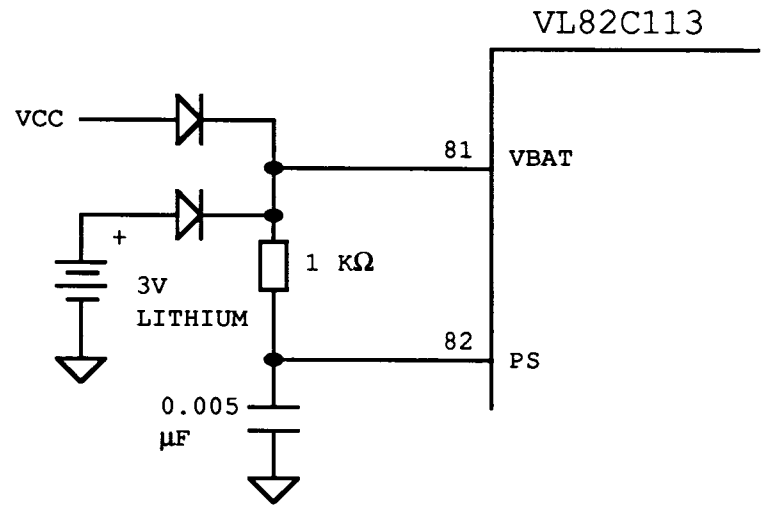
The second method uses the update-in-progress bit (UIP) in Register A to determine if the update cycle is in progress or not. The UIP bit will pulse once-per-second. Statistically, the UIP bit will indicate that time and date information is unavailable once every 2032 attempts. After the UIP bit goes high, the update cycle begins 244 µs later. Therefore, if a low is read on the UIP bit, the user has at least 244 µs before the time/calendar data will be changed. If a 1 is read in the UIP bit, the time/calendar data may not be valid. The user should avoid interrupt service routines that would cause the time needed to read valid time/calendar data to exceed 244 µs.

The third method uses a periodic interrupt to determine if an update cycle is in progress. The UIP bit in register A is set high between the setting of the PF bit in register C.

To properly setup the internal counters for daylight savings time operation, the user must set the time at least two seconds before the roll-over will occur. Likewise, the time must be set at least two seconds before the end of the 29th or 30th day of the month.

6.3.5 Power-Down Mode

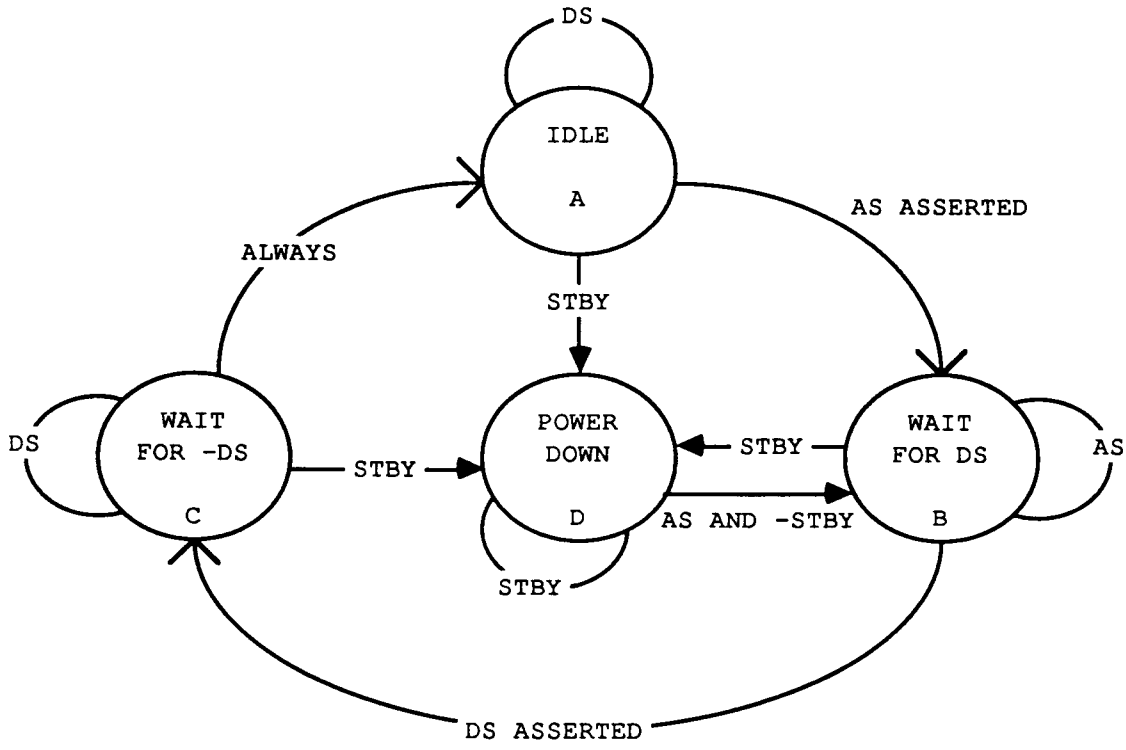
The passive components that are critical for low power operation are shown in the circuit below:



The above circuit is an example only. A NiCad battery can be used, also.

The Power Sense signal is used to reset the state of the Valid RAM and Time bit (VRT) and clear all internal RAM. This input must be asserted after power is applied to the RTC to set the state of the VRT bit properly.

The following is the bus-controller state-diagram that will be implemented in the RTC:



NOTES:

1. STBY IS DEFINED AS -STBY OR -RESET.

2. ONCE A WRITE OPERATION IS STARTED, IT WILL NOT BE INTERRUPTED UNTIL COMPLETED. READ OPERATIONS ARE IMMEDIATELY TERMINATED BY STAND-BY MODE.

The Power Sense signal is used to reset the state of the Valid RAM and Time (VRT) bit. This input must be asserted after power is applied to the RTC to set the state of the VRT bit properly.

With a power consumption target specification of 5 μA, and a Lithium battery with a capacity of 100 mA-Hr, time will be properly kept for approximately 2.25 years.

7.0 A.C. CHARACTERISTICS

TA = 0°C to 70°C, VDD = 5V +/- 5%, VSS = 0V

Symbol	Description	Min	Max	Unit	Conditions
I/O Read/Write Figures 1,2					
t5	Command Pulse Width	125		ns	
tSU6	Write Data Setup	60		ns	
tH7	Write Data Hold	20		ns	
tD8	Read Data Delay	0	130	ns	CL = 200pF
tH9	Read Data Hold	5	60	ns	CL = 50pF
WC	Write Cycle	280		ns	
RC	Read Cycle	280		ns	
tSU1	Address Valid to –EALE Rising	23		ns	
tSA	SA Valid from –EALE Rising		20	ns	
tLA	Address Valid to LA Valid		36	ns	
Master Mode Bus Timing Figure 3					
tAM	A Bus Valid from SA/LA Input (Master Mode)		15	ns	
Real Time Clock Timing Figure 4					
tPSPW	Power Sense Pulse Width	2		us	
tPSP	Power Sense Delay	2		us	
tVRTD	VRT Bit Delay		2	us	

7.1 AC TIMING DIAGRAMS, BUS TIMING

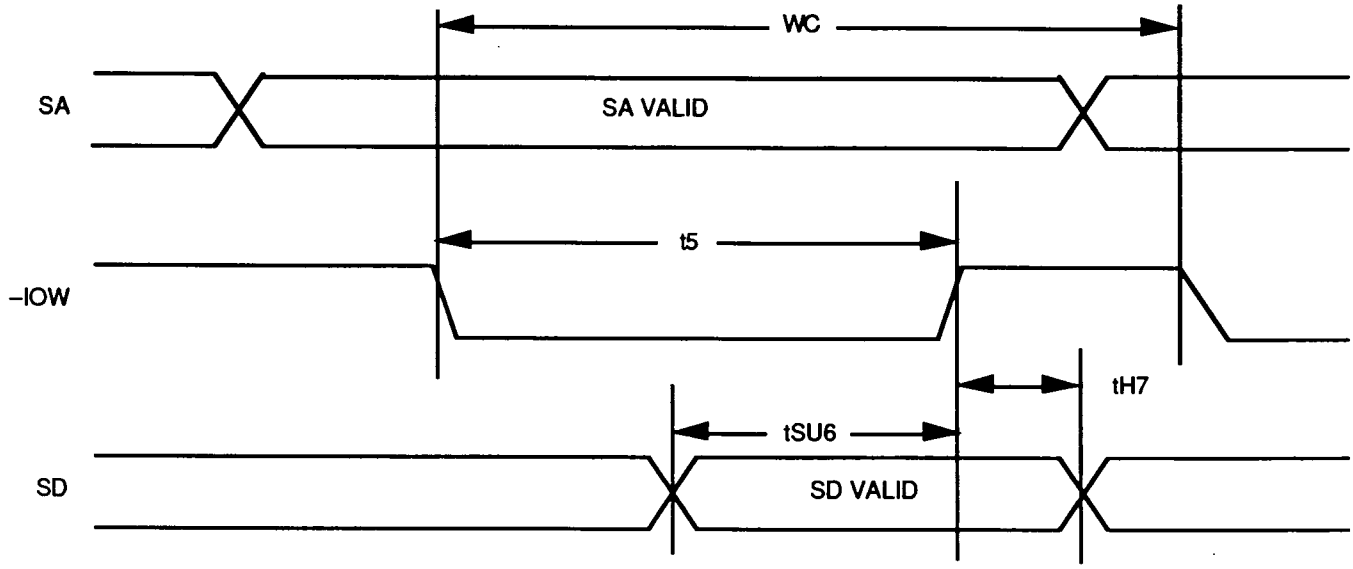


Figure 1a WRITE CYCLE

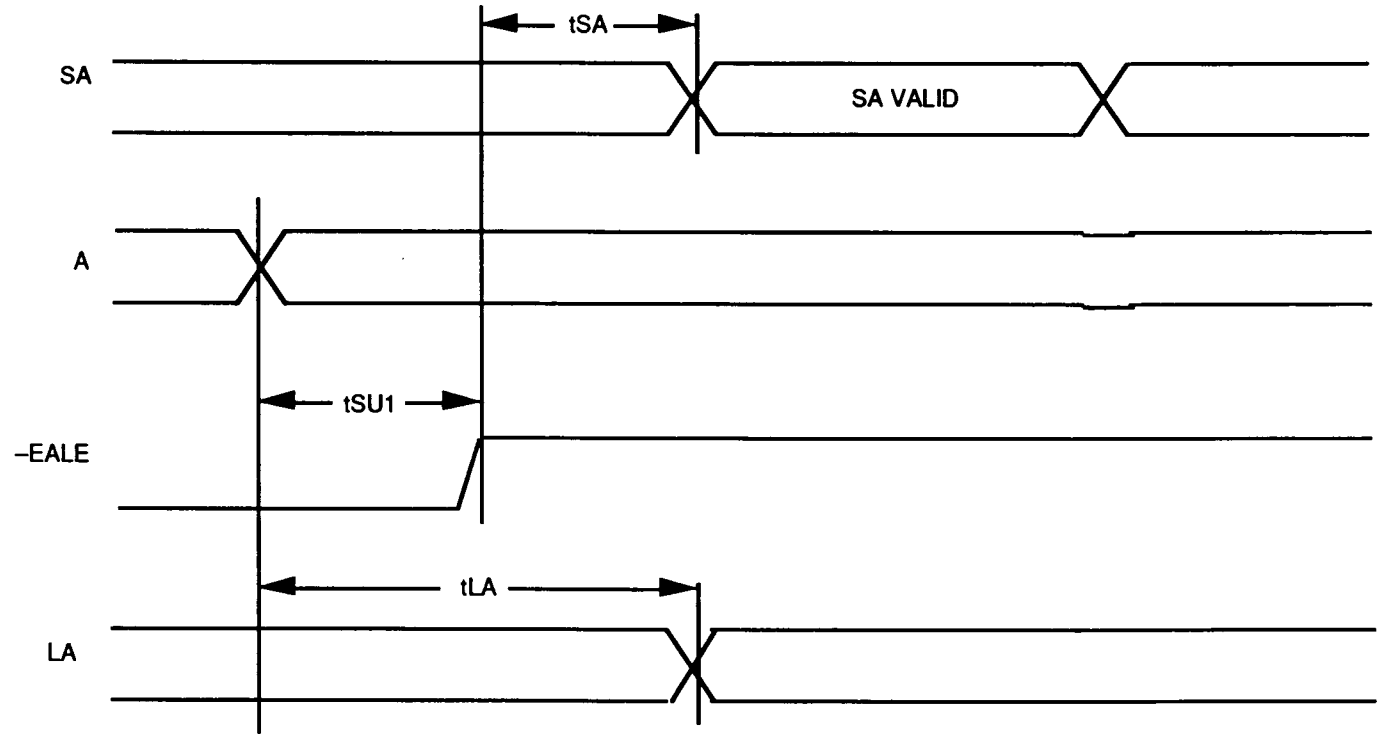


Figure 1b WRITE CYCLE

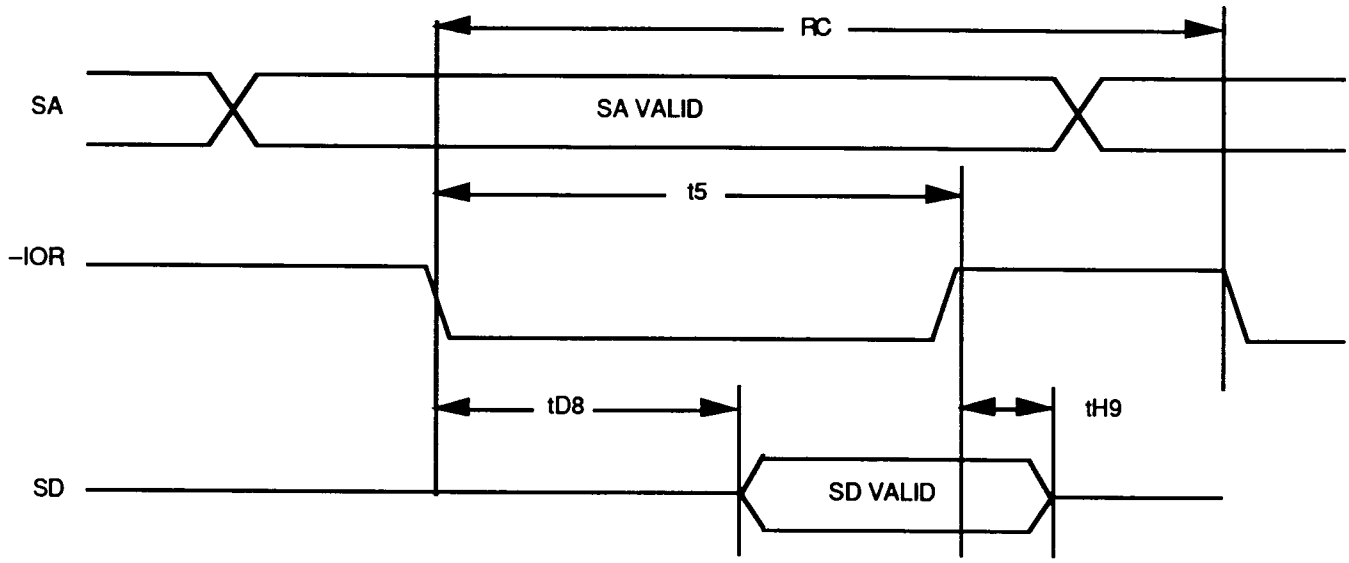


Figure 2 READ CYCLE

7.2 AC TIMING DIAGRAMS, MASTER MODE BUS TIMING

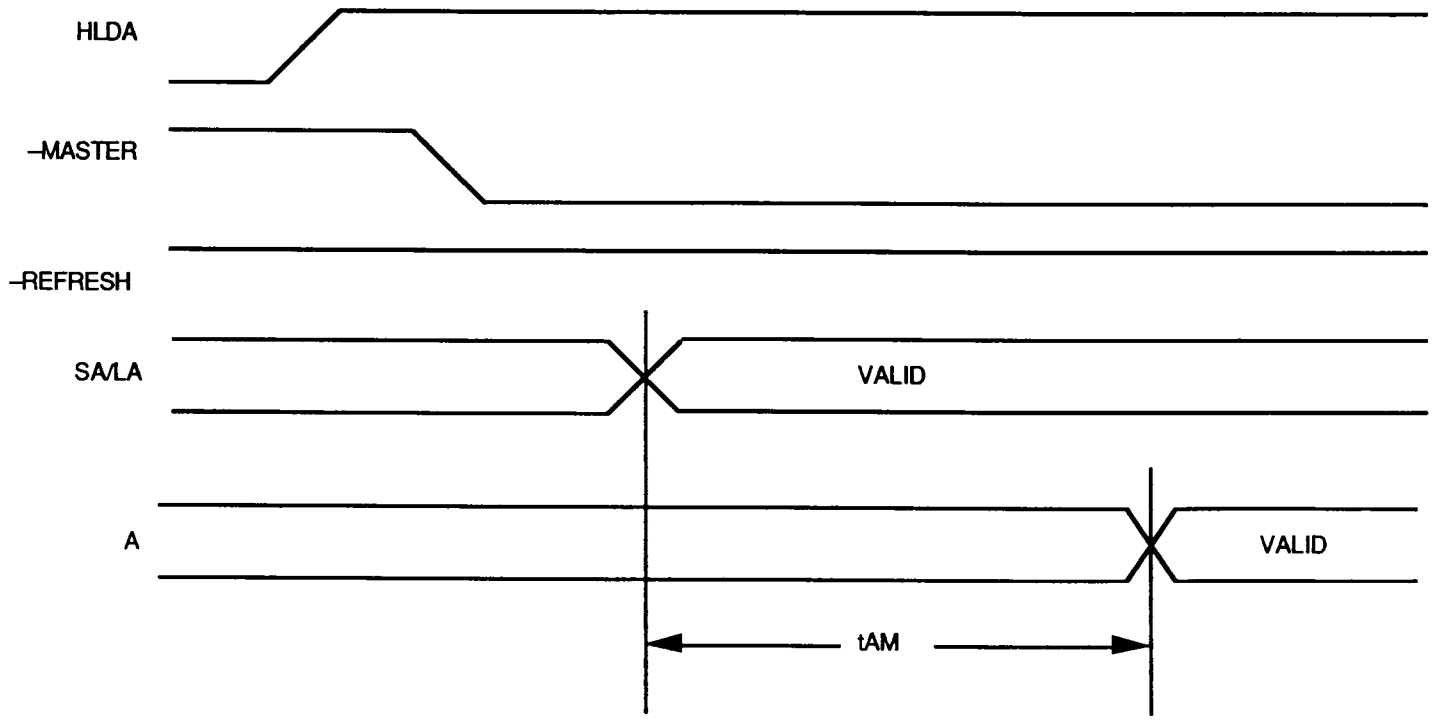


Figure 3 MASTER MODE

7.3 AC TIMING DIAGRAMS, REAL TIME CLOCK TIMING

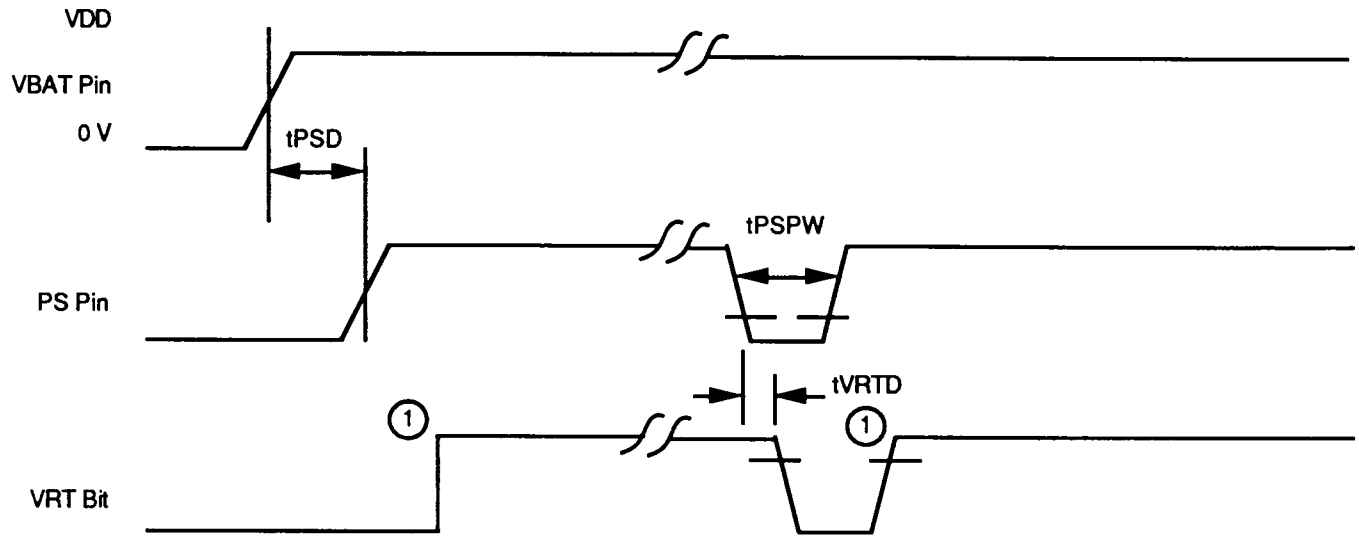


Figure 4 Real Time Clock Timing

7.4 CRYSTAL OSCILLATOR CONFIGURATION

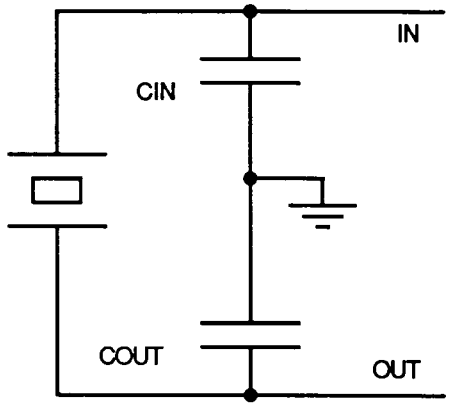


Figure 5 Crystall Oscillator Configuration

Frequency = 32.768KHz
CIN = COUT = 10 - 22 pF
CIN may be a trimmer for precision timekeeping applications.

Recommended Crystal Parameters

Rs (max) ≤ 40kΩ
Co (max) ≤ 1.7pF
Ci (max) ≤ 12.5pF
Parallel Resonance

8.0 D.C. CHARACTERISTICS

TA = 0 to +70°C, VDD = 5V ± 5%

Sym	Parameter	Min	Max	Units	Conditions
VILX	Clock Input Low	-0.5	0.8	Volts	
VIHX	Clock Input High	2.0	VDD	Volts	
VIL	Input Low Voltage	-0.5	0.8	Volts	
VIH	Input High Voltage	2.0	VDD	Volts	
VOL	Output Low Voltage	-	0.4	Volts	2 mA
		-	0.4	Volts	12 mA
VOH	Output High Voltage	2.4	-	Volts	2 mA
		2.4	-	Volts	12 mA
VILR	Reset VIL (Schmitt)	-	0.8	Volts	
VOLR	Reset VIH (Schmitt)	2.0	-	Volts	
IDD	Supply Current	-	20	mA	VDD= 5.25V
IDD	Dynamic Current	-	20	mA/MHz	Same as above
IIL	Input Leakage	-	±10	µA	VDD=5.25V, GND=0V
ICL	Clock Leakage	-	±10	µA	VDD=5.25V, GND=0V
IOZ	3-state leakage	-	±100	µA	VDD=5.25V, GND=0V

9.0 ABSOLUTE MAXIMUM RATINGS

Stresses above those listed below may cause permanent damage to the device. These are stress ratings only, functional operation of this device at these or any other conditions above those indicated in this data sheet is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Condition	Maximum
Ambient operating temperature	-10°C to +70°C
Storage temperature	-65°C to +150°C
Supply voltage to ground	-0.5 V to VDD=0.3 V
Applied output voltage	-0.5 V to VDD=0.3 V
Applied input voltage	-0.5 V to 7.0 V
Power dissipation	500 mW