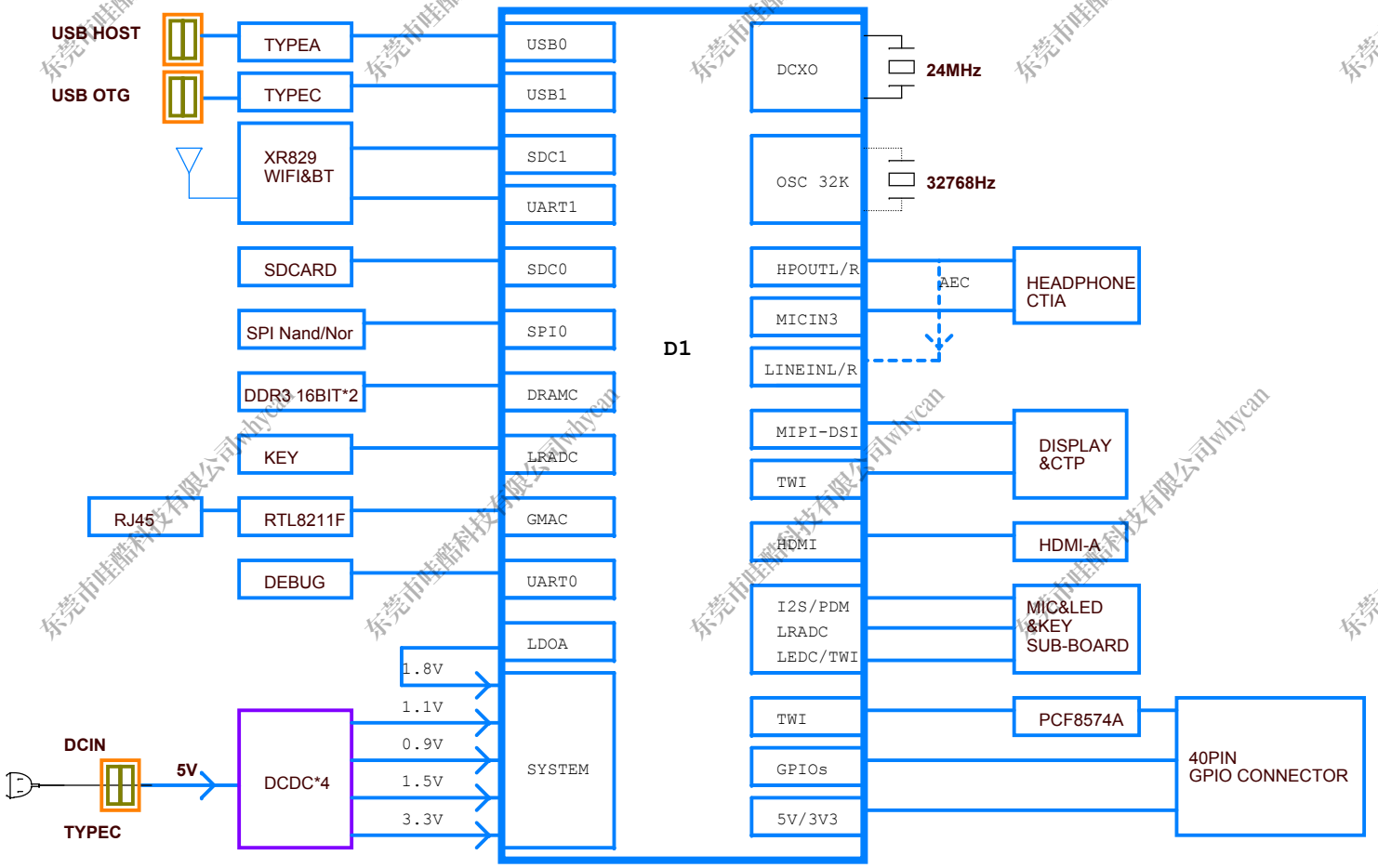
VERSION HISTORY

Index:

Revision	Description	Date	Drawn
Ver 1.0	Releas version	2021/05/10	AWOL010
Ver 1.1	update VDD-SYS 、 HDMI-I2C	2021/11/24	AWOL010
Ver 1.2	update HDMI-I2C 、HDMI-CEC	2021/11/26	AWOL010

BLOCK



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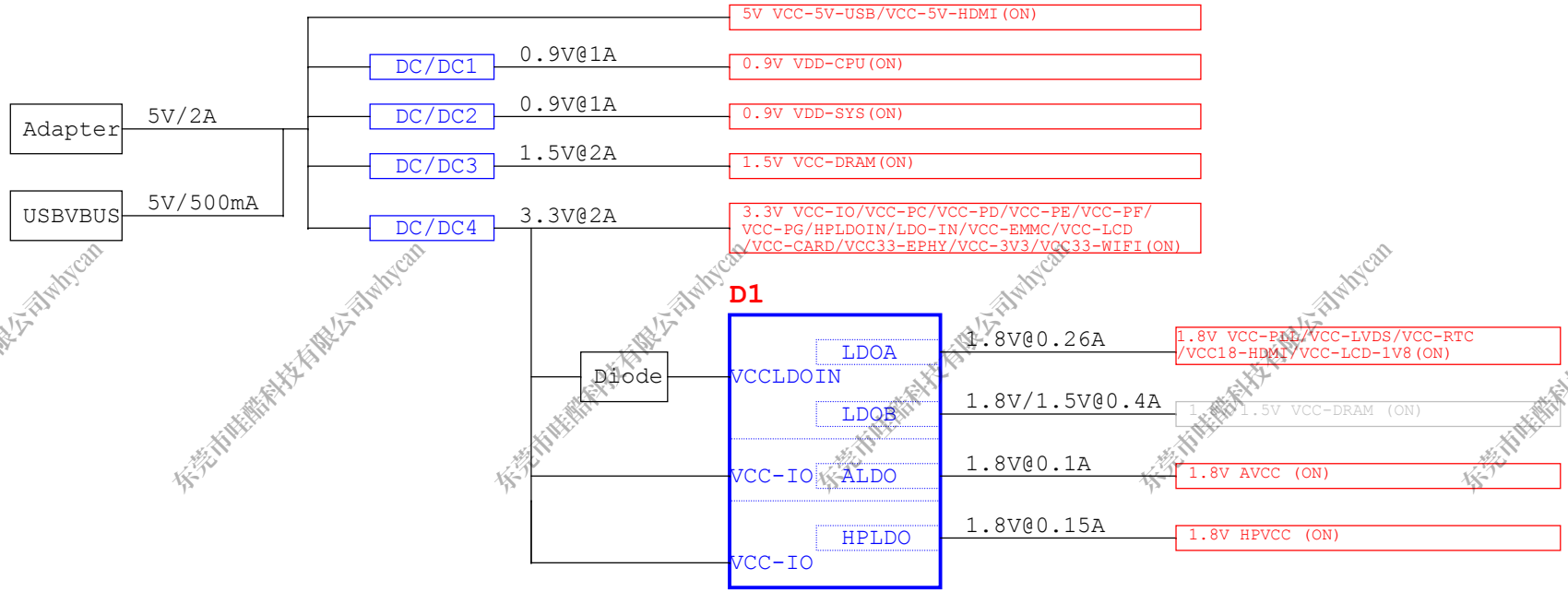
POWER TREE

DEFAULT POWER ON

DEFAULT NC



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GPIO ASSIGNMENT

40 PIN CONNECTOR

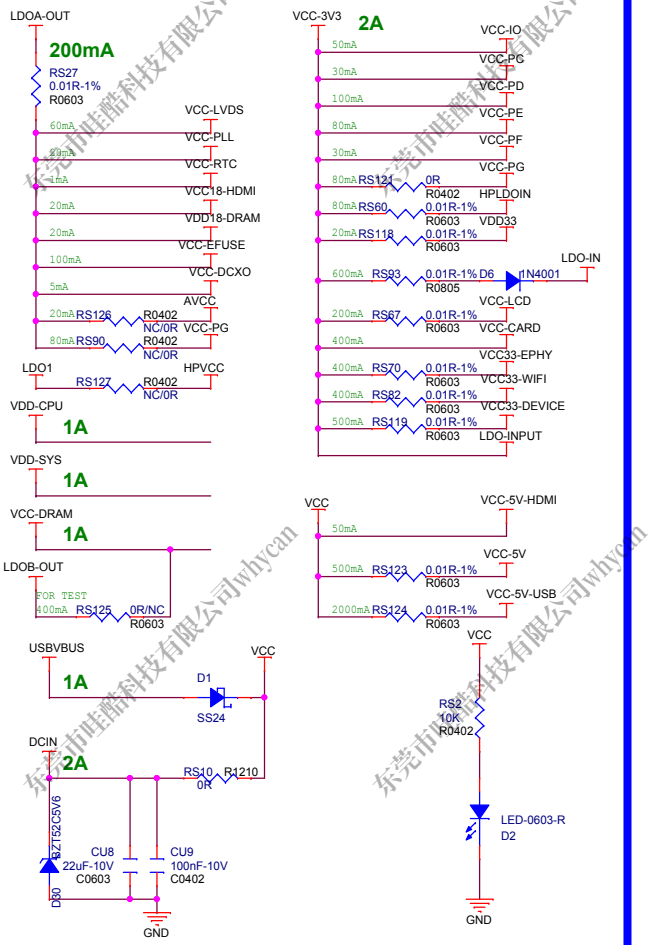
FUNCTION3	FUNCTION2	DEFAULT	SOC.No	PIN		PIN	SOC.No	DEFAULT	FUNCTION2	FUNCTION3
		3V3		1		2		5V		
	TWI2-SDA	GPIO1	PB1	3		4		5V		
	TWI2-SCK	GPIO2	PB0	5		6		GND		
IR-RX	PWM	GPIO3	PD22	7		8	PB8	GPIO4	UART0-TXD	
		GND		9		10	PB9	GPIO5	UART0-RXD	
		GPIO6	PP7	11		12	PB5	GPIO7	I2S2-BCLK	UART5-RX
		GPIO8	PP0	13		14		GND		
PWM	IR-RX	GPIO9	PB12	15		16	PP1	GPIO10		
		3V3		17		18	PP2	GPIO11		
	SPI1-MOSI	GPIO12	PD12	19		20		GND		
UART3-RTS	SPI1-MISO	GPIO13	PD13	21		22	PP4	GPIO14		
UART3-RX	SPI1-CLK	GPIO15	PD11	23		24	PD10	GPIO16	SPI1-CE0	UART3-TX
		GND		25		26	PP3	GPIO17		
UART3-CTS	SPI1-HOLD	GPIO18	PD14	27		28	PP5	GPIO19		
IR-RX	SPI1-WP	GPIO20	PD15	29		30		GND		
		GPIO21	PC1	31		32	PE17	NC	IR-TX	
		NC		33		34		GND		
PWM	I2S2-LRCK	GPIO22	PB6	35		36		NC		
		GPIO23	PP6	37		38	PB3	GPIO24	I2S2-DIN	
		GND		39		40	PB4	GPIO25	I2S2-DOUT	UART5-TX

备注：PP0~PP7为PCF8574A扩展GPIO

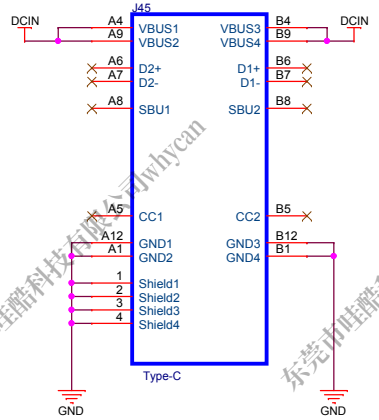
30 PIN CONNECTOR

PIN	SOC.No	DMIC	AMIC
1		GND	GND
2	PB10	DMIC-D1	TWI0-SCK
3	PB11	DMIC-D0	TWI0-SDA
4	PB7	NC	I2S2-MCLK
5	PB5	NC	I2S2-BCLK
6	PB6	NC	I2S2-LRCK
7	PB3	NC	I2S2-DIN0
8-10		NC	NC
11	LRADC	LRADC	LRADC
12	PB10	DMIC-D1	NC
13		GND	GND
14-20		NC	NC
21		GND	GND
22-25		5V	5V
26		3V3	3V3
27	PD17	DMIC-D2	NC
28	PE17	DMIC-CLK	NC
29	PD20	LEDC	LEDC
30		GND	GND

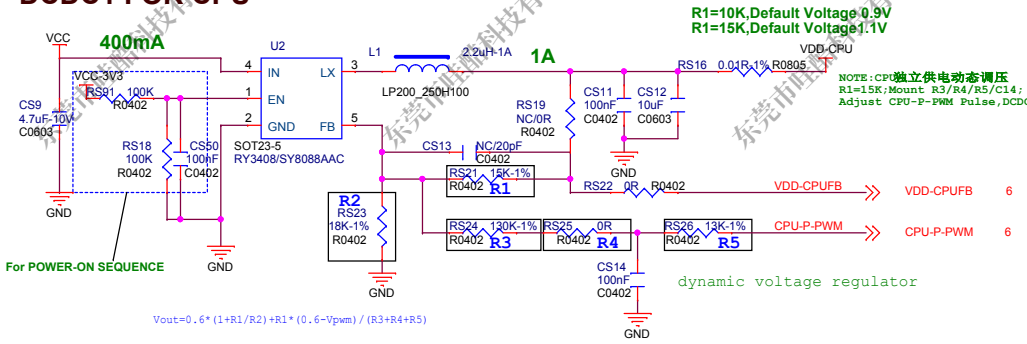
POWER



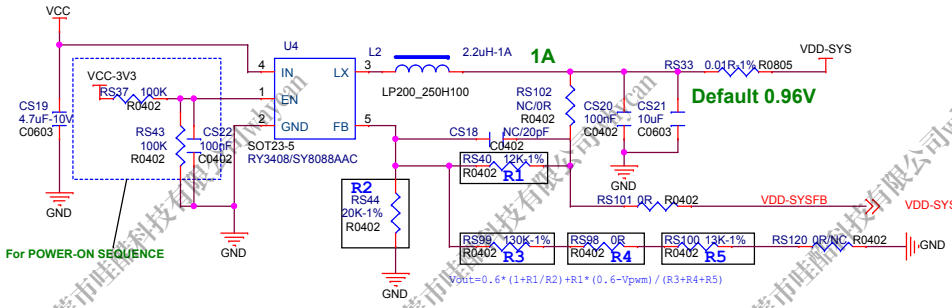
TYPEC-POWER



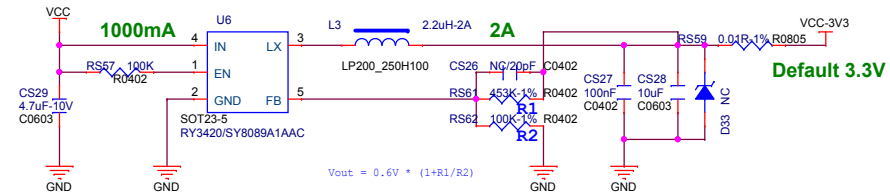
DCDC1 FOR CPU



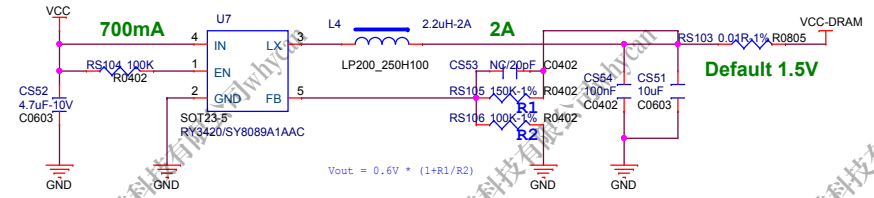
DCDC2 FOR SYS



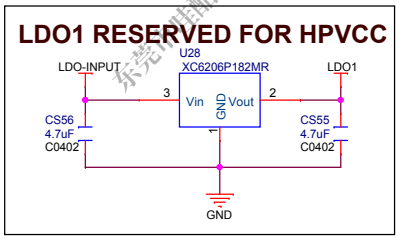
DCDC4 FOR 3V3

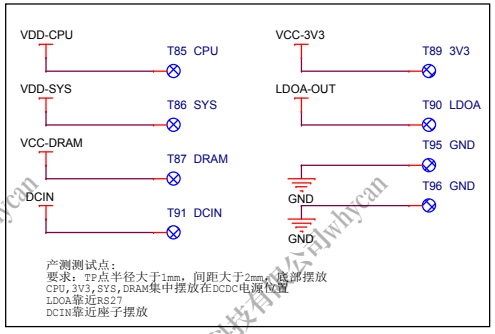


DCDC3 FOR DRAM



LDO1 RESERVED FOR HPVCC





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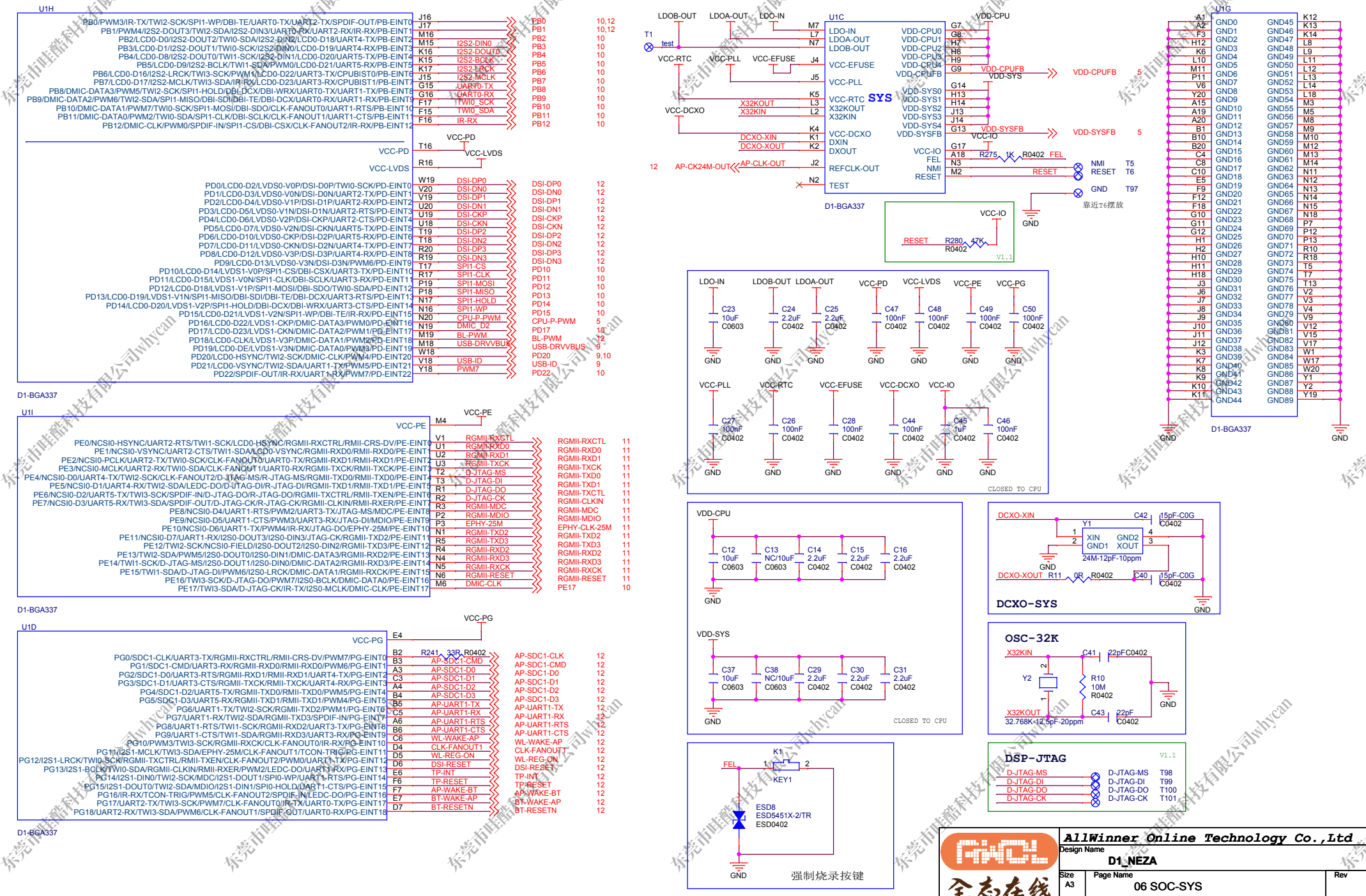
SOC SYS



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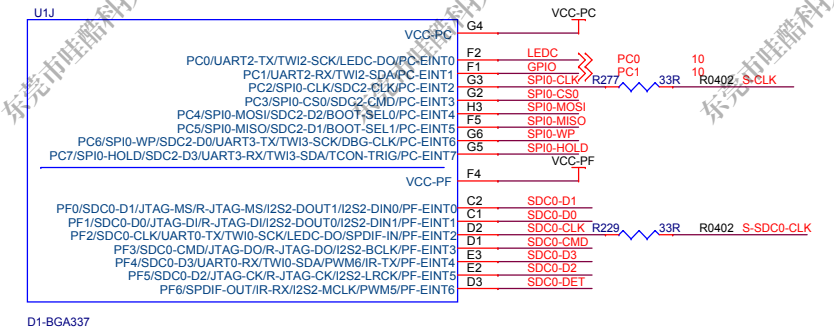
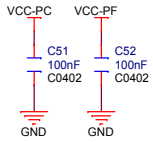
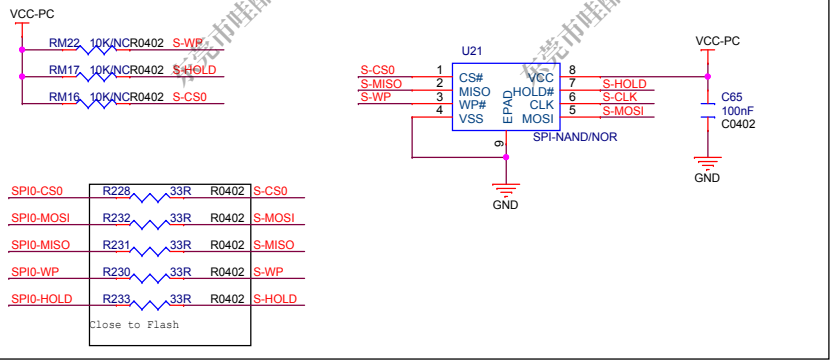
SOC-FLASH&CARD

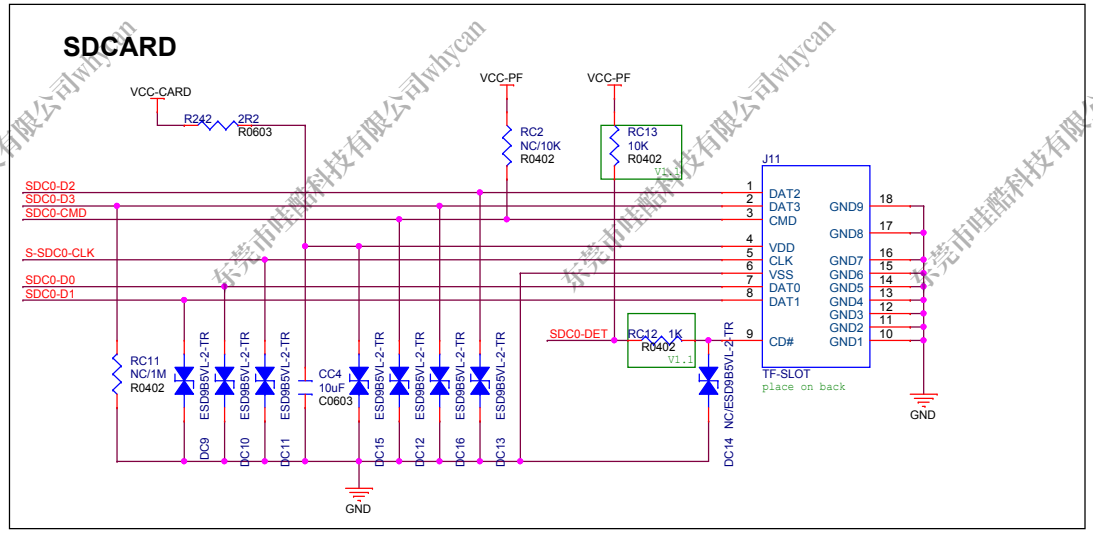




SPI-NAND/NOR



SDCARD



V1.1

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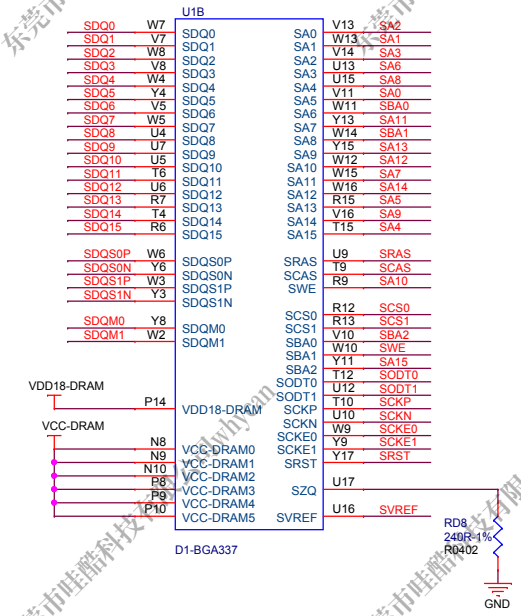
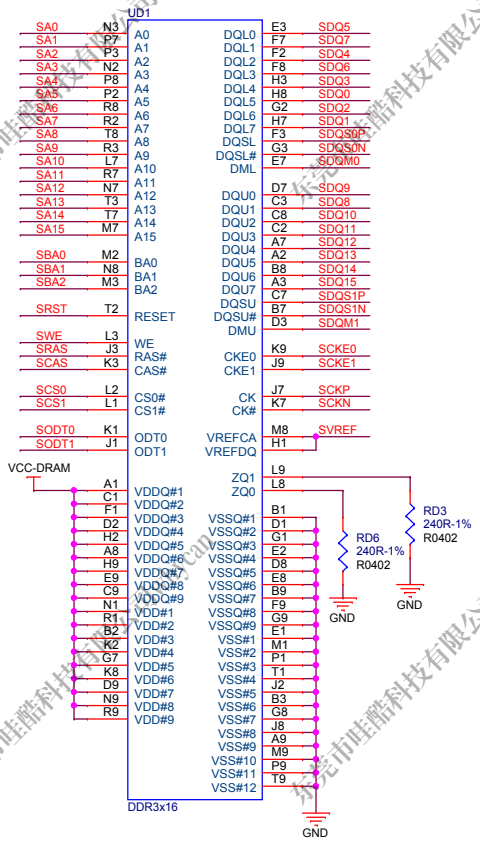
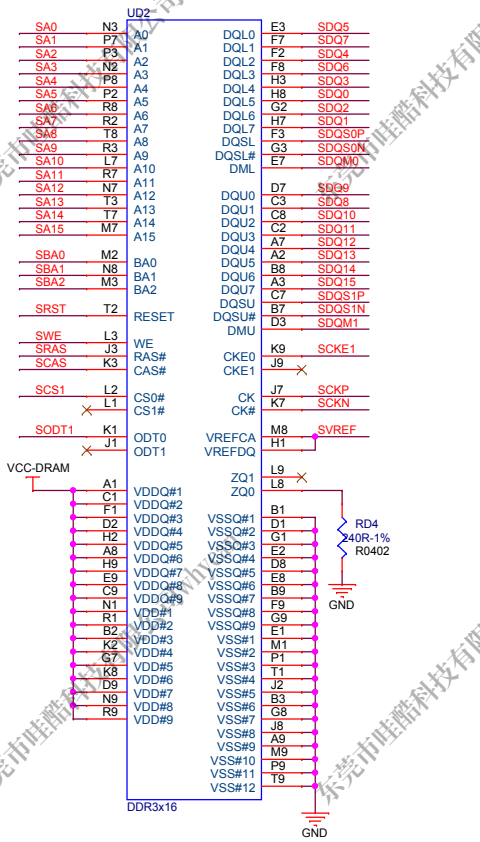
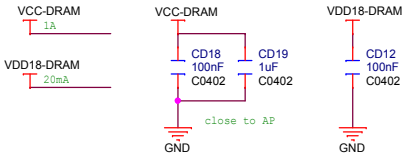
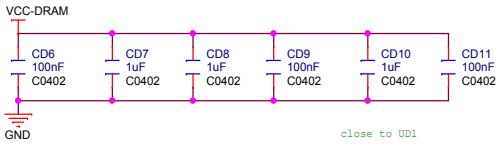
DDR3 16x2

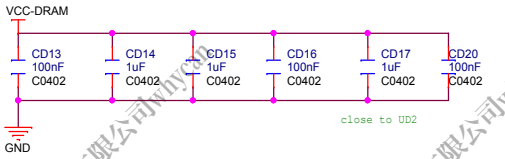


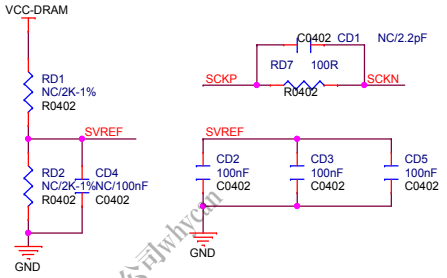












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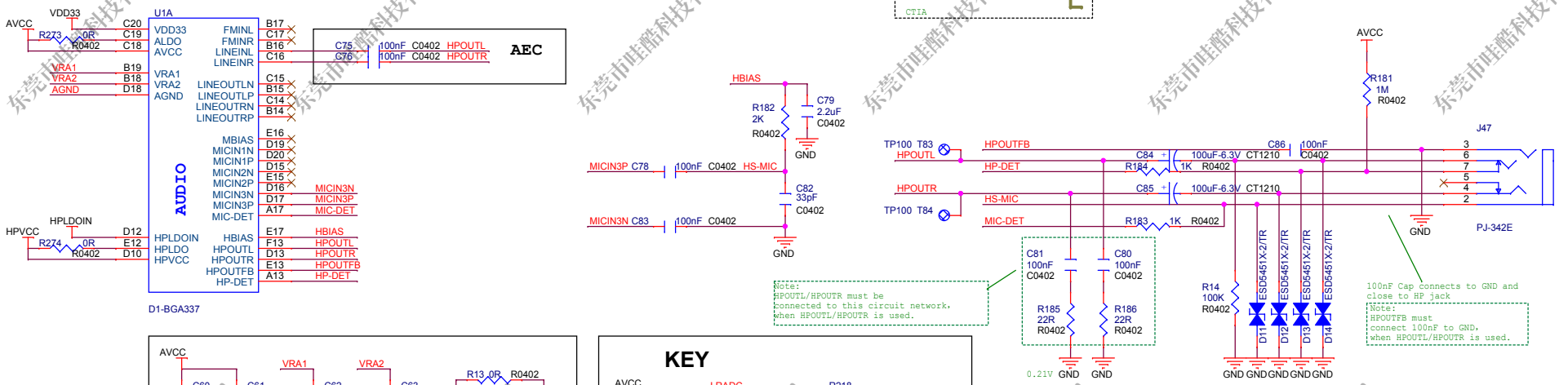
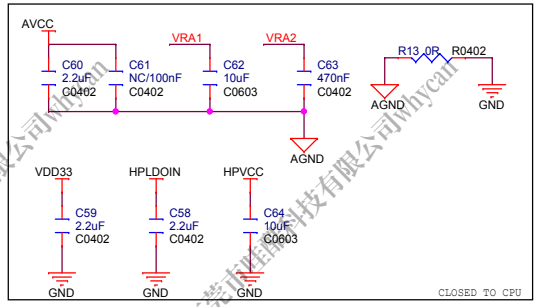
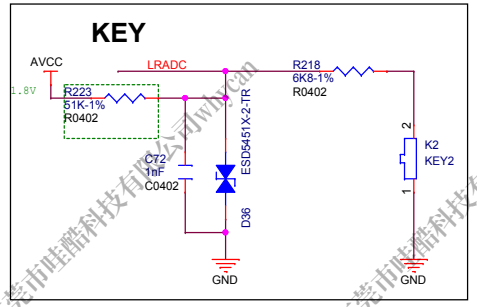
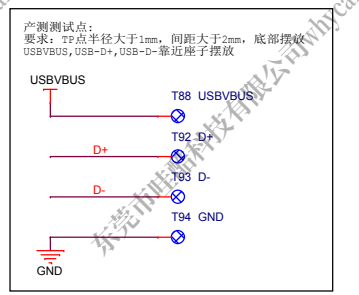
AUDIO&USB

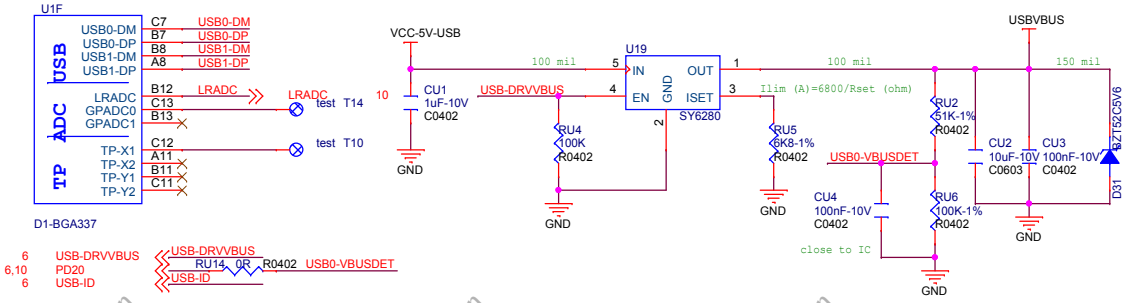


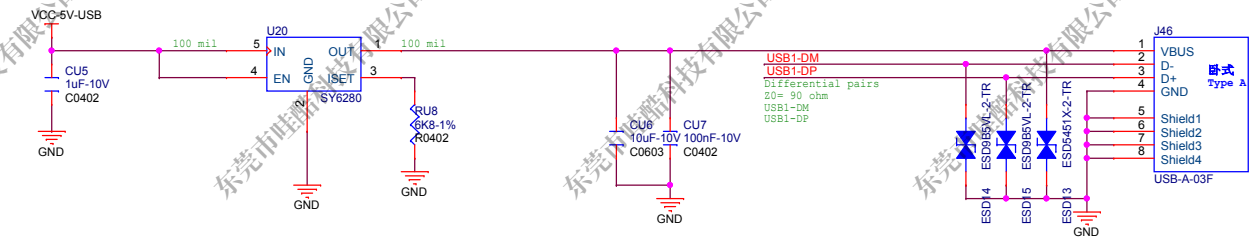




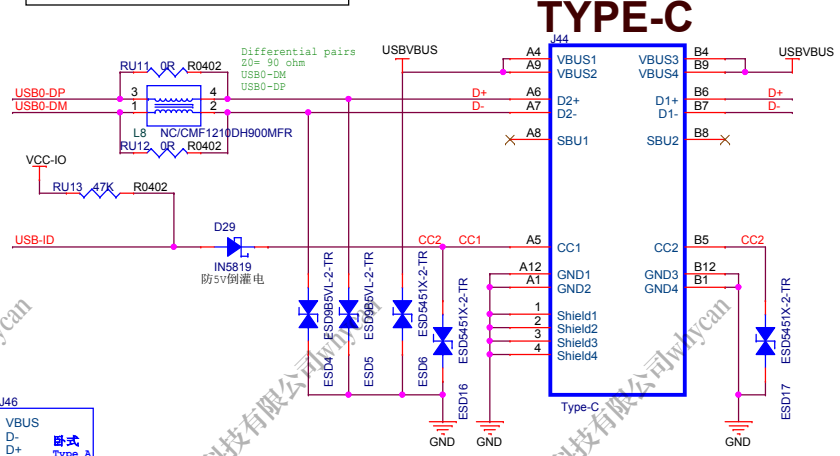


USB





TYPE-C



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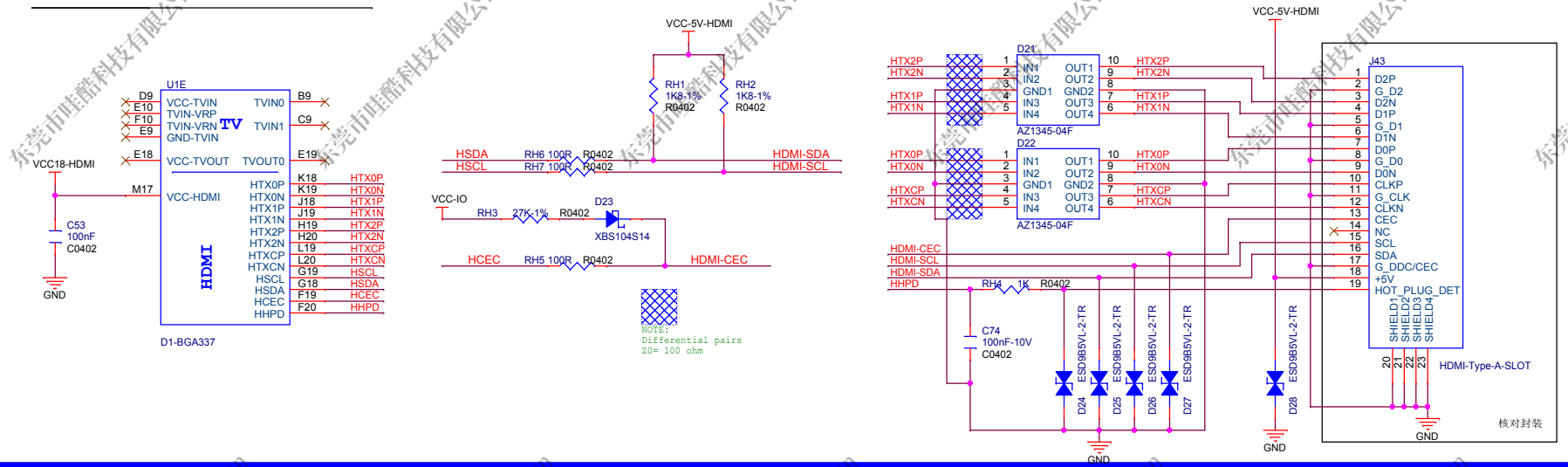
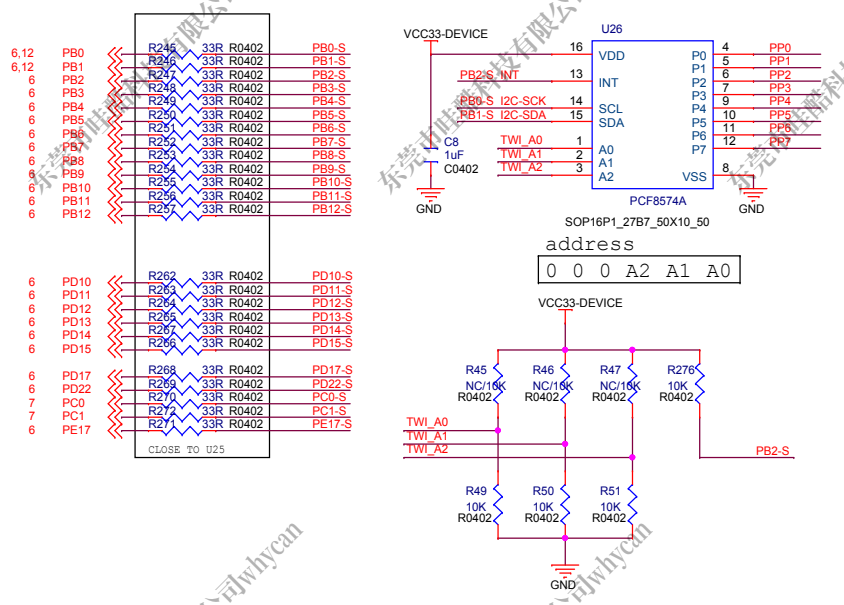
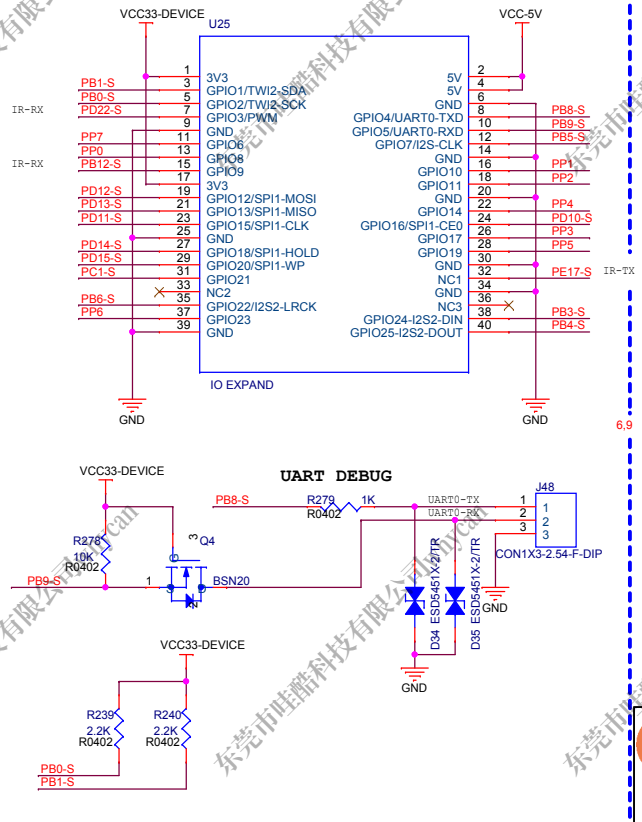
HDMI&IO EXPAND



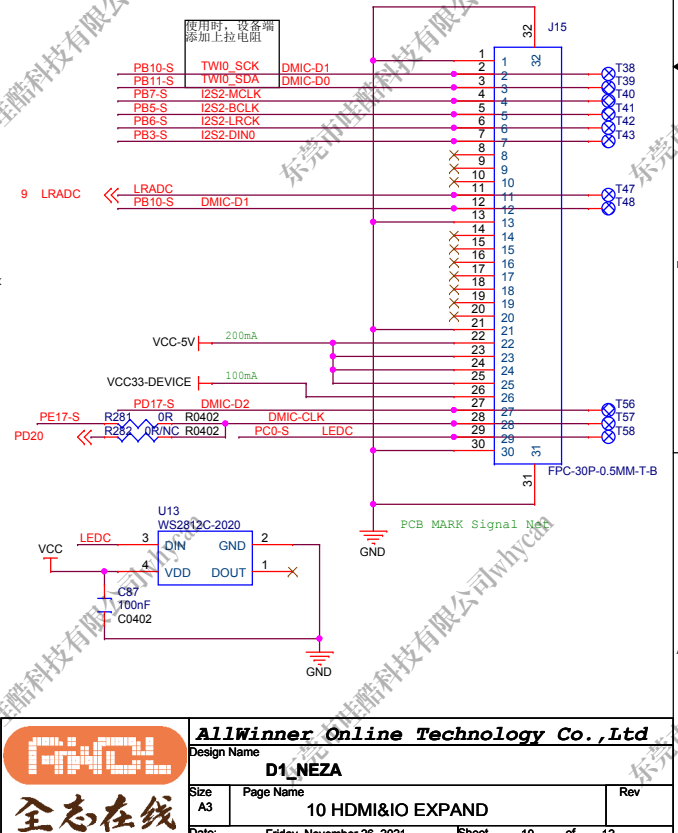
IO EXPAND



GPIO CONNECTOR



EXTERNAL AMIC/DMIC



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全志在线

EPHY

RGMII-RXD3
RGMII-RXD2
RGMII-RXD1
RGMII-RXD0
RGMII-RXCK
RGMII-RXCTL
RGMII-CLKIN-125M
RGMII-TXD3
RGMII-TXD2
RGMII-TXD1
RGMII-TXD0
RGMII-TXCK
RGMII-TXCTL
RGMII-MDC
RGMII-MDIO

RGMII-RESET → PHYRSTB
EPHY-CLK-25M

External Clock From SOC

VCC33-EPHY

VCC33-EPHY

RE1 0.01R-1% R0603 — CE1 100nF C0402 — CE2 100nF C0402 — AVDD33
Reserved for EMI (optional)
Close to PHY PIN11 and PIN40 for Analog Power
RE5 0.01R-1% R0603 — CE5 100nF C0402 — CE6 100nF C0402 — DVDD33
Close to PHY PIN29 for Digital Power & SWR

DVDD33 — RE10 0R — DVDDRG
CE13 100nF C0402
CE14 4.7uF C0402

Note 1: RE10 is not needed for ONLY 3.3V RGMII application, and DVDDRG can be connected directly to DVDD33.
Note 2: DVDDRG must be short (or RE10 be mounted) to DVDD33 if the external RGMII 3.3V is selected.
Note 3: RE10 must be removed if the internal or external 2.5V/1.8V/1.5V RGMII is selected.
Note 4: CAPs must be closed to pin28 for EMI consideration.

RGMII TX Filter Network

RE9 0R: RGMII-TXD3 → TXD3, RGMII-TXD2 → TXD2, RGMII-TXD1 → TXD1, RGMII-TXD0 → TXD0
RE14 0R: RGMII-MDC → MDC
RE15 0R: RGMII-MDIO → MDIO
RE16 0R: RGMII-TXCTL → TXCTL
RE18 0R: RGMII-TXCK → TXC
C0402-COG NC/22PF CE20 — GND
Close to SOC. Reserved for EMI.(optional)

RGMII RX Filter Network

RE20 0R: RGMII-RXCK → RXC/PHYAD1
CE21 NC/22PF C0402-COG — GND
RE21 0R: RGMII-RXD3 → RXD3/PHYAD0, RGMII-RXD2 → RXD2/PLLOFF, RGMII-RXD1 → RXD1/TXDLY, RGMII-RXD0 → RXD0/RXDLY
RE22 0R: RGMII-RXCTL → RXCTL/PHYAD2
Close to PHY. Reserved for EMI.(optional)

RGMII-CLKIN-125M — RE27 0R — CLKOUT-125M
CE23 NC/22PF C0402-COG — GND

8211FD For LDO mode / For SWR mode

20mil — A — RE3 NC/0R — 20mil
REGOUT — 20mil — L9 2.2uH-1A — 20mil
LP200_250H100
CE7 NC/100nF C0402
CE8 4.7uF C0603-X7R B
CE9 100nF C0402
RE2 0R — CE3 100nF C0402 — DVDD10
RE4 0R — CE10 100nF C0402 — CE11 100nF C0402 — CE12 100nF C0402 — GND AVDD10

Note 1: Bypass CAPs close to PHY DVDD10/AVDD10 power pins.
Note 2: Any inductance or bead except L9 is not allowed on the path from REGOUT to DVDD10/AVDD10.
Note 3: A is reserved to change the DVDD10/AVDD10 supply source to LDO mode (RTL8211FD).
Note 4: No design change of PCB model is needed if A is reserved. If only RTL8211FD used for particular PCB model, directly short REGOUT to DVDD10/AVDD10.
Note 5: If RTL8211FI is selected, the B should be replaced as 10uF X7R capacitor for industrial grade application. Please refer to the datasheet for other industrial grade information.

UE1 — RTL8211Fxx

V1.1

40	39	38	37	36	35	34	33	32	31	41	1	2	3	4	5	6	7	8	9	10	30	29	28	27	26	25	24	23	22	21
AVDD33	RSET	AVDD10	XTAL_OUT	XTAL_IN	CLKOUT_125M	LED2/CFG_LDO1	LED1/CFG_LDO0	LED0/CFG_EXT	INTB/PMEB	EGND	MDI0+	MDI0-	AVDD10 3	MDI1+	MDI1-	MDI2+	MDI2-	AVDD10 8	MDI3+	MDI3-	REG_OUT	DVDD33 29	DVDD_RG	RXC/PHYAD1	RXCTL/PHYAD2	RXD0/RXDLY	RXD1/TXDLY	RXD2/PLLOFF	RXD3/PHYAD0	DVDD10 21

AVDD33 40 RSET AVDD10 38 XTAL_OUT/EXT_CLK XTAL_IN CLKOUT LED2/CFG_LDO1 LED1/CFG_LDO0 LED0/CFG_EXT INTB/PMEB
MDI[0]+ MDI[0]- AVDD10 3 MDI[1]+ MDI[1]- MDI[2]+ MDI[2]- AVDD10 8 MDI[3]+ MDI[3]-
REG_OUT DVDD33 29 DVDD_RG RXC/PHYAD1 RXCTL/PHYAD2 RXD0/RXDLY RXD1/TXDLY RXD2/PLLOFF RXD3/PHYAD0 DVDD10 21
AVDD33 11 PHYRSTB MDC MDIO TXD3 TXD2 TXD1 TXD0 TXCTL TXC

RTL8211F-CG/RTL8211FD-CG

UE2 — RJ45-LED-TRANSFORMER-1000M

HR911130A

MDI3+ MDI3- MDI2+ MDI2- MDI1+ MDI1- MDI0+ MDI0- → TD3+ TD3- TD2+ TD2- TD1+ TD1- TD0+ TD0-

DVDD33 — LED2/CFG-LDO1 — RE59 0R
RE67 510R/NC
LED1/CFG-LDO0 — RE60 0R
LED0/CFG-EXT — RE63 0R/NC
RE68 510R
RE66 510R
GND

GREEN+ GREEN- YELLOW+ YELLOW- SHIELD SHIELD
CE29 100nF C0402 — GND

PHY RESET/INTB

DVDD33 — RE33 4.7K — INTB
RE34 4.7K — PHYRSTB
CE25 100nF C0402 — GND
DVDDRG — RE39 1.5K — MDIO
GND — RE40 2.49K-1% — RSET

Enable/Disable PLL @ ALDPS

RE45 4.7K RXD2/PLLOFF — RE46 NC/4.7K — DVDDRG
Pull-up to disable PLL @ ALDPS mode.

RGMII TXC/RXC Delay Config.

RE55 4.7K RXD1/TXDLY — RE56 NC/4.7K
RE57 NC/4.7K RXD0/RXDLY — RE58 4.7K — DVDDRG
Pull-up for additional 2ns delay to TXC/RXC for data latching.

External Clock Case

EPHY-CLK-25M — RE35 NC/0R — XTAL-OUT
XTAL-IN
The XTAL IN needs to be connected to GND if the external 25MHz clock used.

PHY Address Config.

DVDDRG
RE41 NC/4.7K RXD3/PHYAD0 — RE42 4.7K
RE47 4.7K RXC/PHYAD1 — RE48 NC/4.7K
RE51 4.7K RXCTL/PHYAD2 — RE52 NC/4.7K
GND

PHY Address	PHYAD[2:0]
0	3'b000
1 (default)	3'b001
2	3'b010
3	3'b011
4	3'b100
5	3'b101
6	3'b110
7	3'b111

RGMII Voltage Config.

DVDD33
RE43 NC/4.7K LED0/CFG-EXT — RE44 4.7K
RE49 4.7K LED1/CFG-LDO0 — RE50 NC/4.7K
RE53 4.7K LED2/CFG-LDO1 — RE54 NC/4.7K
GND

RGMII Power Source	CFG_EXT	CFG_LDO[1:0]
External 3.3V (default)	1'b1	2'b00
External 2.5V	1'b1	2'b01
External 1.8V	1'b1	2'b10
External 1.5V	1'b1	2'b11
Internal 2.5V	1'b0	2'b01
Internal 1.8V	1'b0	2'b10
Internal 1.5V	1'b0	2'b11

Crystal Case

XTAL-IN — CE80 22pF-C0G C0402 — YE1 (XIN GND2 GND1 XOUT) 25M-16pF-20ppm — CE79 22pF-C0G C0402 — XTAL-OUT
RE64 0R
GND

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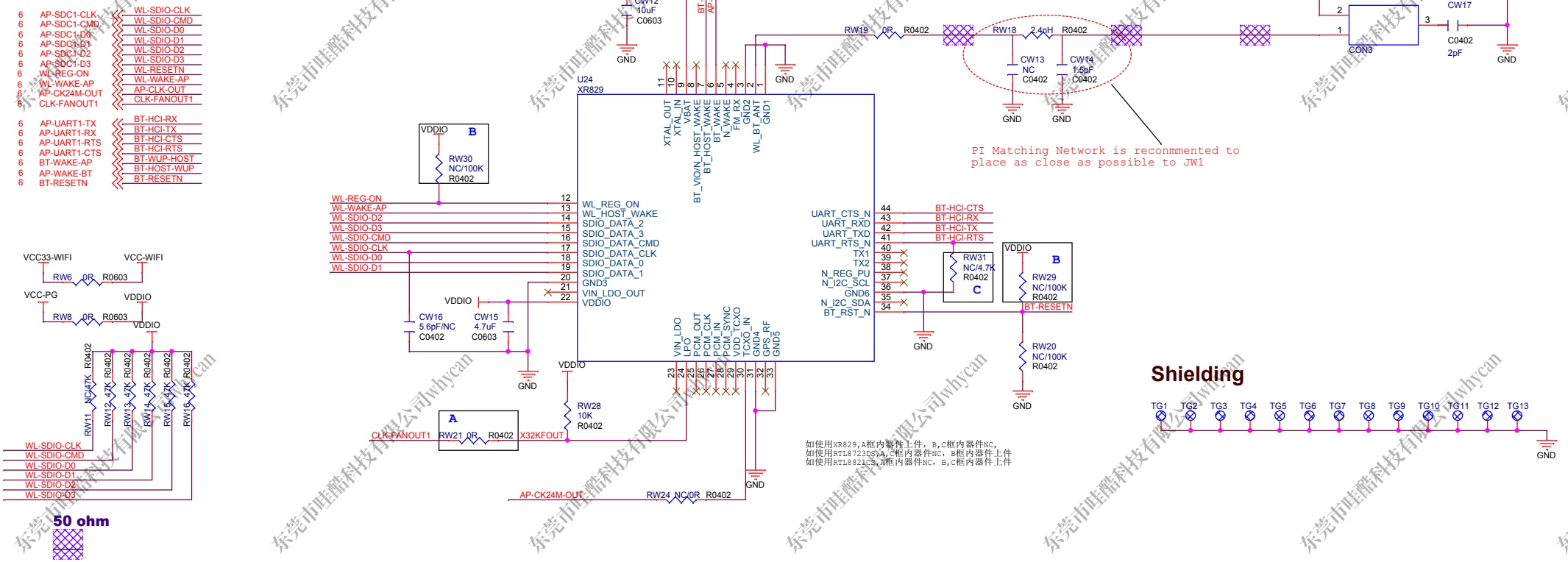
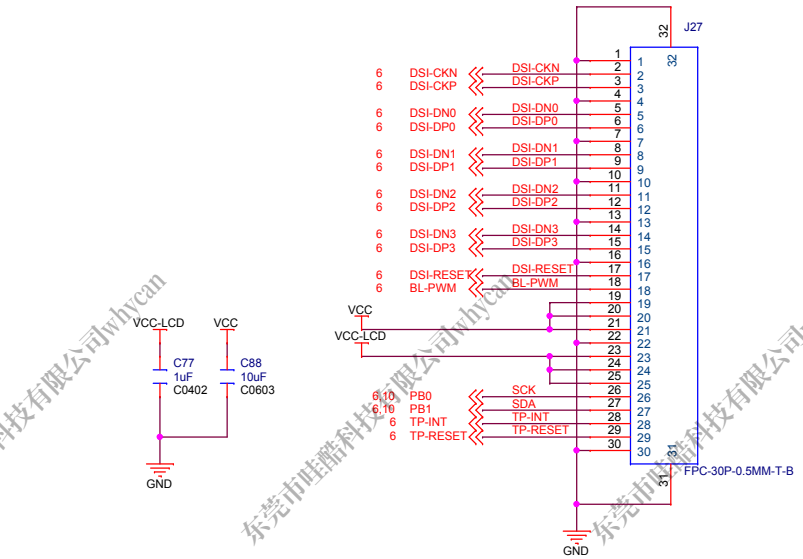
WIFI MODULE&MIPI DSI



MIPI-DSI



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