General Dual-Port SRAM
4096 WORDS X 16 BITS, MUX 8
SMIC 55nm LL Logic Process

Version 1.3.a

OVERVIEW

The General Dual-Port SRAM(BW) is designed for SMIC's 55nm CMOS Logic process. The memory is optimized for speed, power and area. It operates at a voltage range of 1.08V to 1.32V and a temperature range of -40°C to 125°C.

The write enable (WENA,WENB), bit-write enalbe (BWENA[n-1:0], BWENB[n-1:0]), chip enable(CENA,CENB), address(AA[i-1:0],AB[i-1:0]) and data in (DA[n-1:0],DB[n-1:0]) signals are latched on the rising-edge of the clock(CLKA,CLKB). When CENA(CENB) is low and WENA(WENB) is high the menory will be in read oprarion. When CENA(CENB) and WENA(WENB) are both low and BWENA[j](BWENB[j]) is high, the memory will be in read operation. By address AA[i-1:0](AB[i-1:0]) the data is read and output on the port QA[j](QB[j]). When CENA(CENB) and WENA(WENB) are both low and BWENA[j](BWENB[j]) is low, the memory will be in write operation. Data on DA[j](DB[j]) would be written through AA[i-1:0](AB[i-1:0]) and then be output on QA[j](QB[j]).When CENA(CENB) is high the memory is in standby mode. Meanwhile, the data stored in memory is retained but cannot be read or written.

CONFIGURATION:

PARAMETER	VALUE
Mux	8
Words	4096
Bits	16
Width	313.52um
Height	319.25um
Area	100091.260um^2

PIN DEFINITION:

PIN	DIRECTION	DEFINITION
AA[11:0]	Input	A Port Address Inputs
AB[11:0]	Input	B Port Address Inputs
DA[15:0]	Input	A Port Data Inputs
DB[15:0]	Input	B Port Data Inputs
BWENA[15:0]	Input	A Port Bit-Write Enable
BWENB[15:0]	Input	B Port Bit-Write Enable
CENA	Input	A Port Enable
CENB	Input	B Port Enable
CLKA	Input	A Port Clock Input
CLKB	Input	B Port Clock Input
QA[15:0]	Output	A Port Data Outputs
QB[15:0]	Output	B Port Data Outputs

TIMING:

PARAMETER	DESCRIPTION	FF CORNER 1.32V, -40°C		FF CORNER 1.32V, 0°C		FF CORNER 1.32V, 125°C		SS CORNER 1.08V, -40°C		SS CORNER 1.08V, 125°C		TT CORNER 1.2V, 25°C	
(ns)		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
Tcyc	Cycle Time	0.991		1.049		1.200		5.034		4.972		2.323	
Ta	Access Time[1]	0.751		0.795		0.909			3.814		3.767		1.760
Tah	Address Hold	0.121		0.126		0.129		0.149		0.157		0.131	
Tas	Address Setup	0.245		0.257		0.290		0.639		0.677		0.374	
Tbwh	Bwen Hold	0.162		0.160		0.154		0.216		0.210		0.174	
Tbws	Bwen Setup	0.166		0.178		0.192		0.331		0.390		0.210	
Tch	Cen Hold	0.067		0.065		0.058		0.235		0.182		0.084	
Tcs	Cen Setup	0.180		0.183		0.189		0.297		0.309		0.211	
Tdh	Data Hold	0.162		0.160		0.154		0.215		0.210		0.174	
Tds	Data Setup	0.169		0.181		0.196		0.348		0.406		0.226	
Twh	Wen Hold	0.084		0.084		0.073		0.091		0.075		0.079	
Tws	Wen Setup	0.170		0.187		0.222		0.413		0.470		0.265	
Tclkh	Clock High	0.020		0.020		0.020		0.040		0.040		0.020	
Tclkl	Clock Low	0.099		0.099		0.110		0.231		0.253		0.143	
Tclkr	Clock Rise Skew	0.500		0.500		0.500		1.000		1.000		0.600	
Tcc	Clock Collision	0.991		1.049		1.200		5.034		4.972		2.323	

Timing simulation conditions:

1. Access time = best case for fast corner and worst case for slow/typical corners

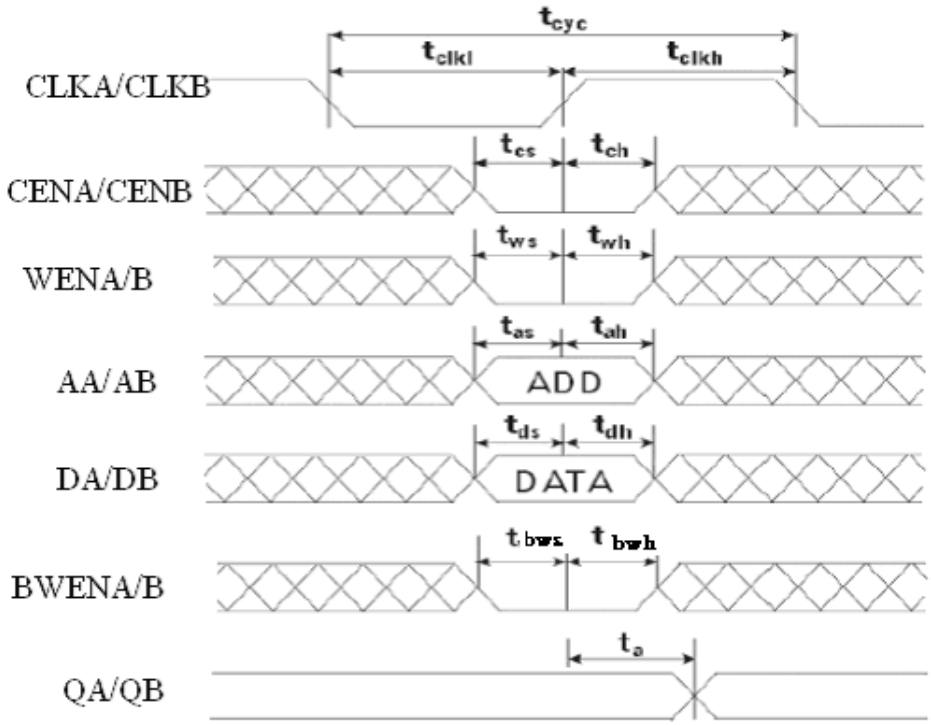
POWER:

PARAMETER	FF CORNER 1.32V, -40°C	FF CORNER 1.32V, 0°C	FF CORNER 1.32V, 125°C	SS CORNER 1.08V, -40°C	SS CORNER 1.08V, 125°C	TT CORNER 1.2V, 25°C
AC Current (uA/MHz)[2]	13.387	13.548	15.018	12.834	12.596	14.162
Read AC Current (uA/MHz)	11.508	11.653	13.047	11.450	11.087	12.439
Write AC Current (uA/MHz)	15.265	15.443	16.988	14.219	14.104	15.884
Standby Power (mW)	0.007105	0.032213	1.514120	0.000345	0.029510	0.005276
Deselect Power (uA/MHz)[3]	1.435	1.458	1.619	1.075	1.106	1.246

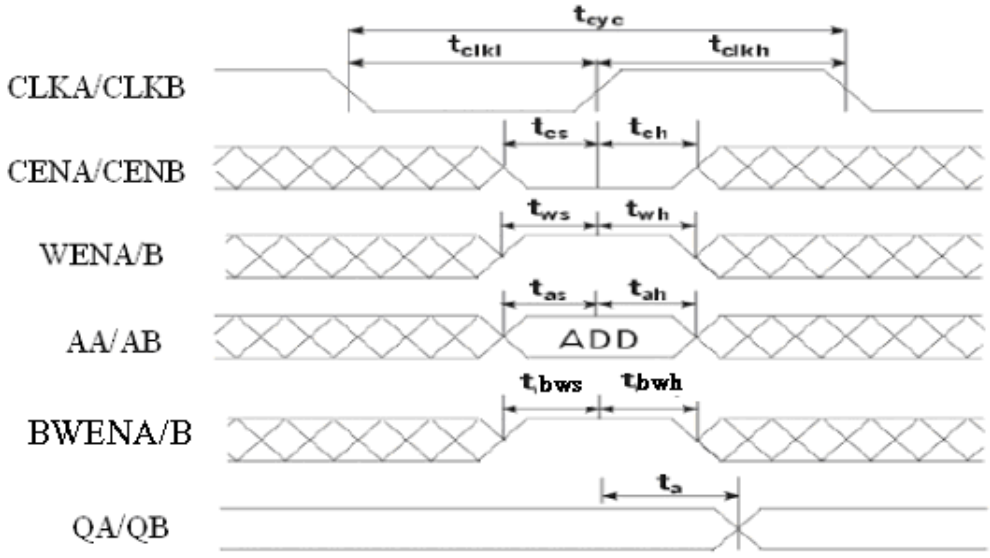
Power simulation conditions:

2. CEN is low, 50% read / 50% write operations, all addresses and 50% of input pins toggle at 1Mhz
3. CEN is high, 50% of input pins toggle at 1Mhz

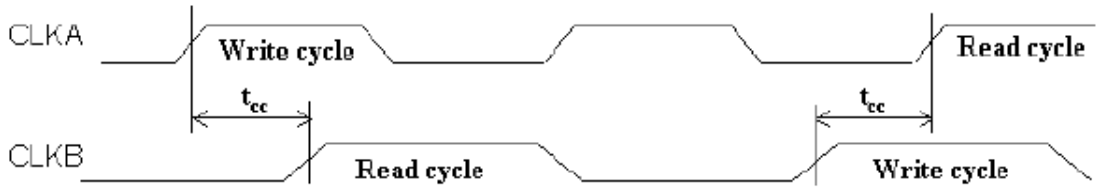
WRITE CYCLE TIMING:



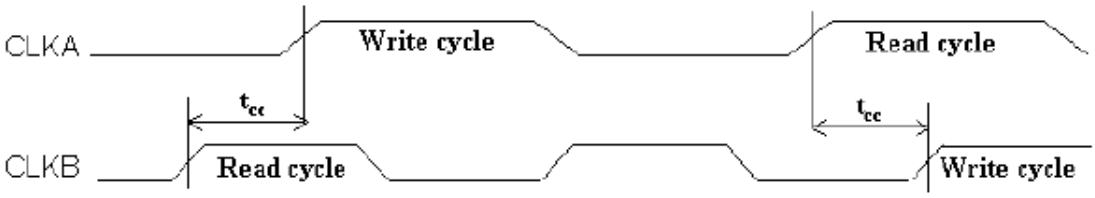
READ CYCLE TIMING:



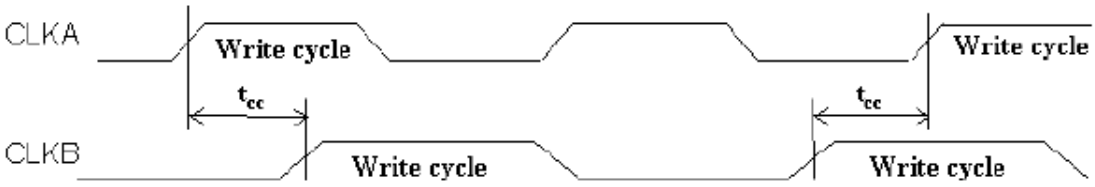
WRITE TO READ CYCLE TIMING:



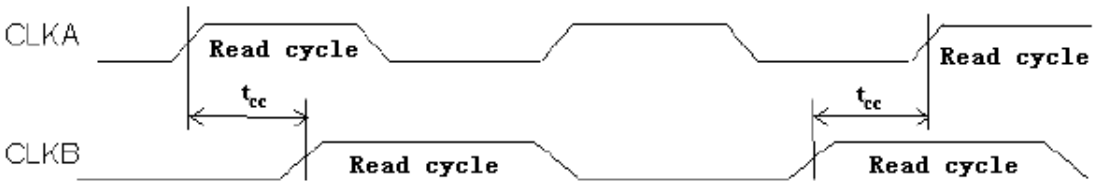
READ TO WRITE CYCLE TIMING:



WRITE TO WRITE CYCLE TIMING:



READ TO READ CYCLE TIMING:



Datasheet Revision History

Date	Version	Changes
	null	

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