XMC55_DPS
4096 WORDS X 16 BITS, MUX 8

MEMORY DESCRIPTION

The Dual-Port synchronous SRAM is designed for XMC 55nm EF Process. The memory is optimized for speed, power and area. It operates at a voltage range of 1.08V to 1.32V and a temperature range of -40 to 125^{o}C

The write enable (WENA, WENB), chip enable(CENA,CENB), address(AA,AB) and data in(DA,DB) signal are latched on the rising-edge of the clock(CLKA,CLKB). When CENA (CENB) is low and WENA (WENB) is high the memory will be in read operation. When CENA (CENB) and WENA (WENB) are both low the word on the data port will be written into the memory and the data will appear on the output port.When CENA (CENB) is high the memory is in standby mode. Meanwhile, the data stored in memory is retained but cannot be read or written.

CONFIGURATION

PARAMETER	VALUE
MUX	8
Word Depth	4096
Word Width	16
Bite Write	on
Test Mode	off
Array Pick-up Density	x1
Width (um)	294.36
Height (um)	326.068
Area (um2)	95981.376

PIN DEFINATION

PIN	DIRECTION	DEFINATION
AA<11:0>, AB<11:0>	Input	Address input
DA<15:0>, DB<15:0>	Input	Data input
CENA, CENB	Input	Chip enable
WENA, WENB	Input	Write enable
CLKA, CLKB	Input	Clock
QA<15:0>, QB<15:0>	Output	Data output
BWENA<15:0>, BWENB<15:0>	Input	Bit Write enable

SRAM LOGIC TABLE

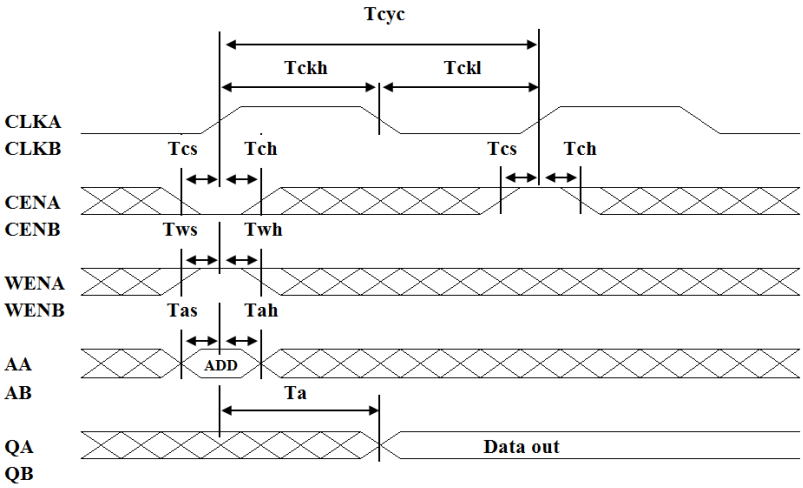
The following function description applies for both port-A and port-B.

CEN	WEN	BWEN	Data Out	Mode	Function
H	X	X	Last Data	Standby	Address inputs are disabled; data stored in the memory is retained, but the memory cannot be accessed for new reads or Writes. Data outputs remain stable.
L	L	L	Data In	Write	Data on the data input bus D is written to the memory location specified on the address bus.
L	L	H	SRAM Data	Masked Write	The specifed bit by BWEN on the data input bus D will NOT be written to the memory.
L	H	X	SRAM Data	Read	Data on the data bus Q is read from the memory location specified on the address bus.

1. X must be low or high state.

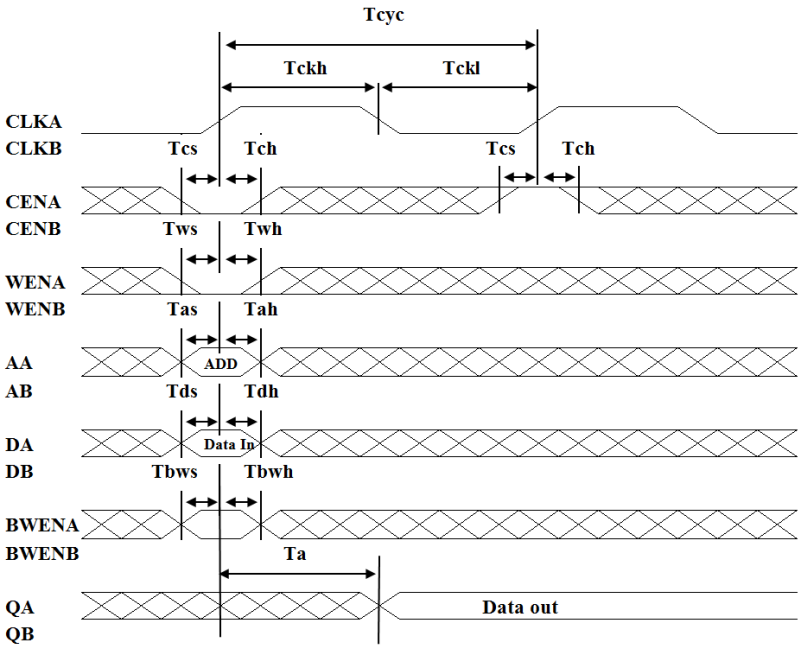
2. If bit write option is disabled, BWEN=L.

READ CYCLE TIMING



Read Operation

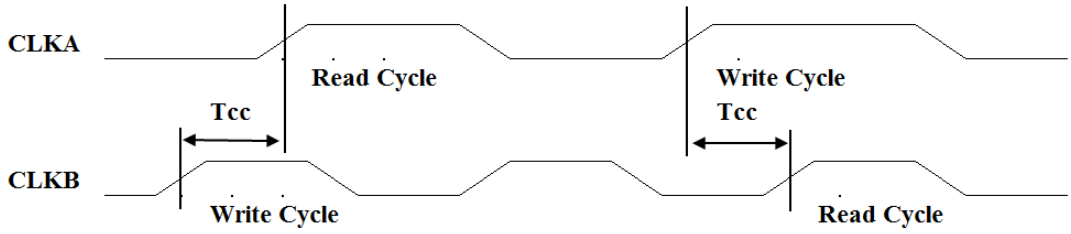
WRITE CYCLE TIMING



* Write through enabled

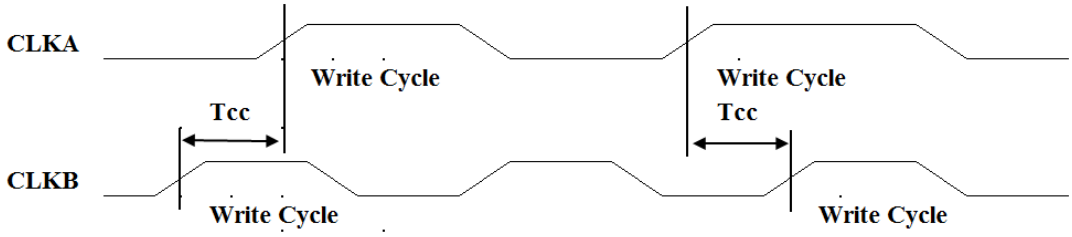
Write Operation

WRITE to READ TIMING



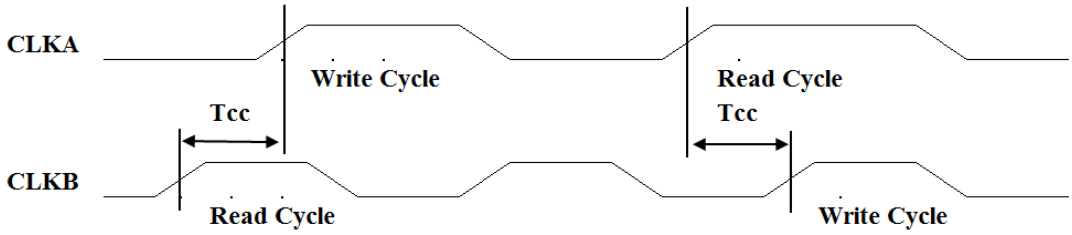
Write to Read Timing

WRITE to WRITE TIMING



Write to Write Timing

READ to WRITE TIMING



Read to Write Timing

The clock-collision parameter (Tcc) in the timing diagrams represent the minimum intervals between the rising-edge of the clock on one port and the rising-edge of the clock on the other port such that valid read and write operations can be performed at the same address during corresponding clock cycles. The collision behavior when Tcc is not met is described in this section.If AA equals AB:

1). Read on port A and port B, both reads pass.

2). Read on port A, write on port B: write passes, read fails.

3). Read on port B, write on port A: write passes, read fails.

4). Write on port A, write on port B: both writes fail, this is an illegal condition and causes higher power consumption

TIMING (ns)

PARAMETER	DESCRIPTION	TT		FF			SS	
Vol	Voltage (V)	1.2	1.2	1.32	1.32	1.32	1.08	1.08
Temp	Tempreture (^{o}C)	25	125	-40	0	125	125	-40
Tcyc	Cycle Time	2.636	2.864	1.572	1.696	2.01	5.052	5.049
Tckh	Clock High	1.151	1.188	0.664	0.696	0.784	2.395	2.661
Tckl	Clock Low	0.728	0.747	0.413	0.438	0.491	1.441	1.56
Ta	Access time[1,2]	2.311	2.416	1.379	1.454	1.632	4.405	4.73
Tas	Address Setup	0.585	0.602	0.411	0.418	0.438	1.013	1.004
Tah	Address Hold	0.749	0.764	0.527	0.539	0.563	1.255	1.272
Tds	Data Setup	0.41	0.432	0.304	0.314	0.337	0.626	0.563
Tdh	Data Hold	0.407	0.382	0.308	0.299	0.276	0.686	0.761
Tcs	Chip Enable Setup	0.4	0.4	0.3	0.3	0.3	0.65	0.65
Tch	Chip Enable Hold	0.4	0.4	0.3	0.3	0.3	0.65	0.65
Tws	Write Enable Setup	0.393	0.397	0.294	0.295	0.299	0.636	0.62
Twh	Write Enable Hold	0.415	0.412	0.311	0.311	0.308	0.677	0.693
Tbws	Bit write enable Setup	0.41	0.432	0.304	0.314	0.337	0.626	0.563
Tbwh	Bit write enable Hold	0.407	0.382	0.308	0.299	0.276	0.686	0.761

1. Parameters have a output load(cload) & input transition(tr) dependence.The condition used here is: cap=0.035pF, tr=0.08ns.

2. Access time is defined as the slowest possible output transition.

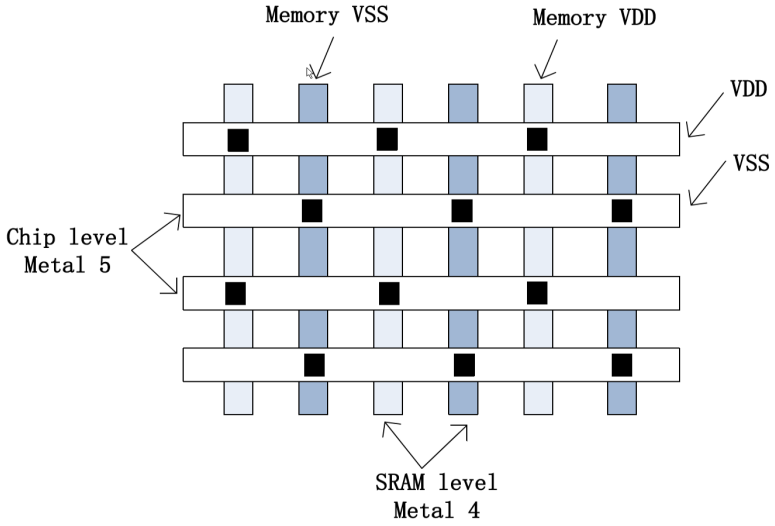
POWER

PARAMETER	DESCRIPTION	TT		FF			SS	
Vol	Voltage (V)	1.2	1.2	1.32	1.32	1.32	1.08	1.08
Temp	Tempreture (^{o}C)	25	125	-40	0	125	125	-40
Pac	AC Power (uW/MHz)	43.791	44.195	53.907	54.311	57.019	33.889	33.455
PacR	AC Read Power (uW/MHz)	35.99	36.388	44.05	44.455	47.042	28.542	28.128
PacW	AC Write Power (uW/MHz)	51.593	52.002	63.765	64.166	66.995	39.237	38.782
Psd	Standy Power (uW/MHz)	17.443	17.67	21.969	22.059	23.954	12.309	12.103
Pleak	Leakage Power (uW)	3.779	21.18	41.6813	42.634	225.4984	3.267	1.112

1.Power simulation condition: 50% read / 50% write, all addresses and 50% input pins toggle at 100Mhz.

P&R REQUIREMENT

1. Power: In order to get a good performance by top-down connection of power net, you must place chip-level VDD and VSS in horizontal (vertical) direction as power straps inside of SRAM is vertical (horizontal).



2. Latch-up guide: A single guard-ring is designed inside SRAM for area and flexibility consideration. To achieve better protection of latch-up, users can add guarding-ring(s) outside SRAM.
It is helpful to set 'Array Pick-up Density' option to higher value to reduce the array pick-up distance, which is about 64um by default.