

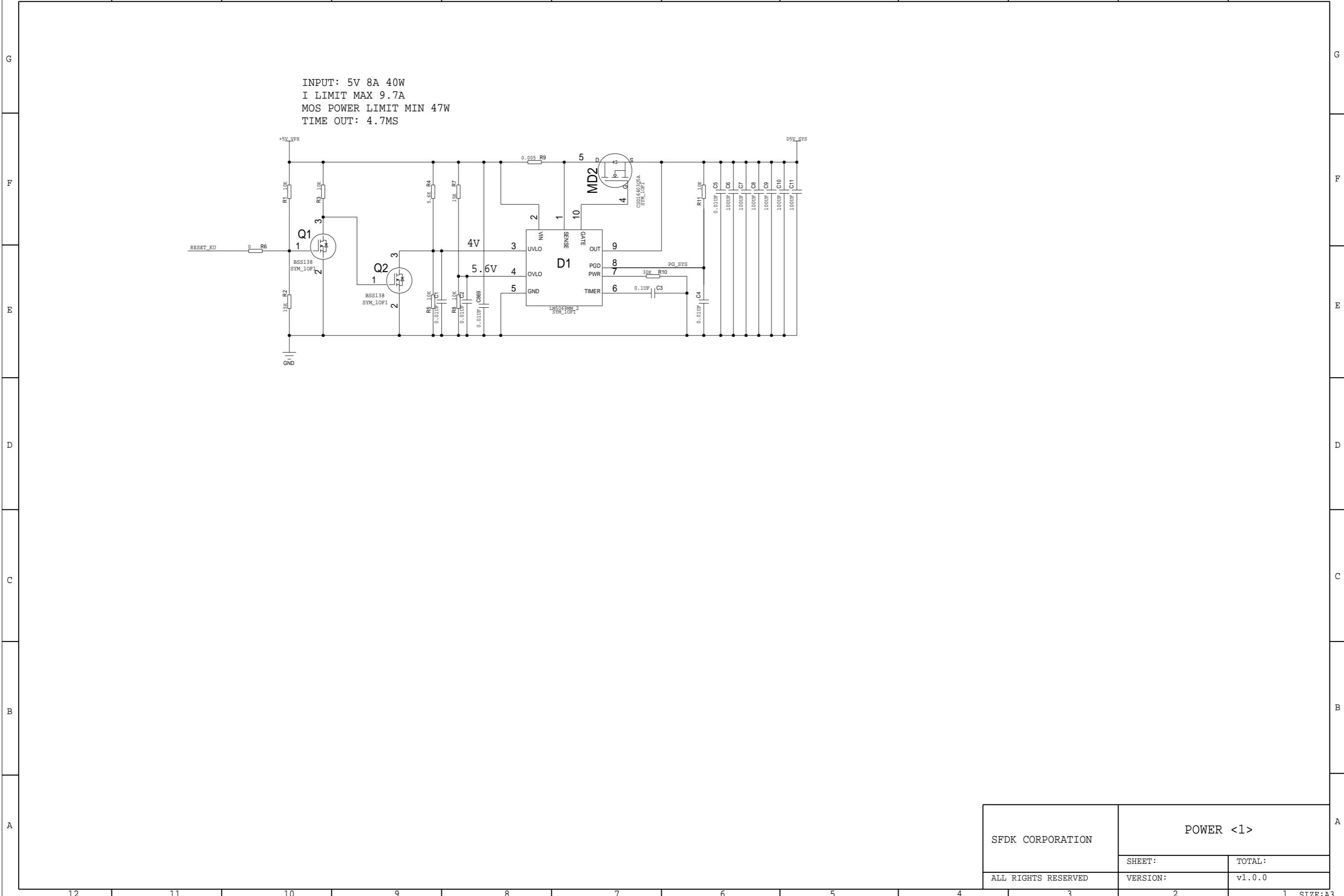
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										B	B
										A	A

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	DESIGNER:	NAME2	20XX-XX-XX	
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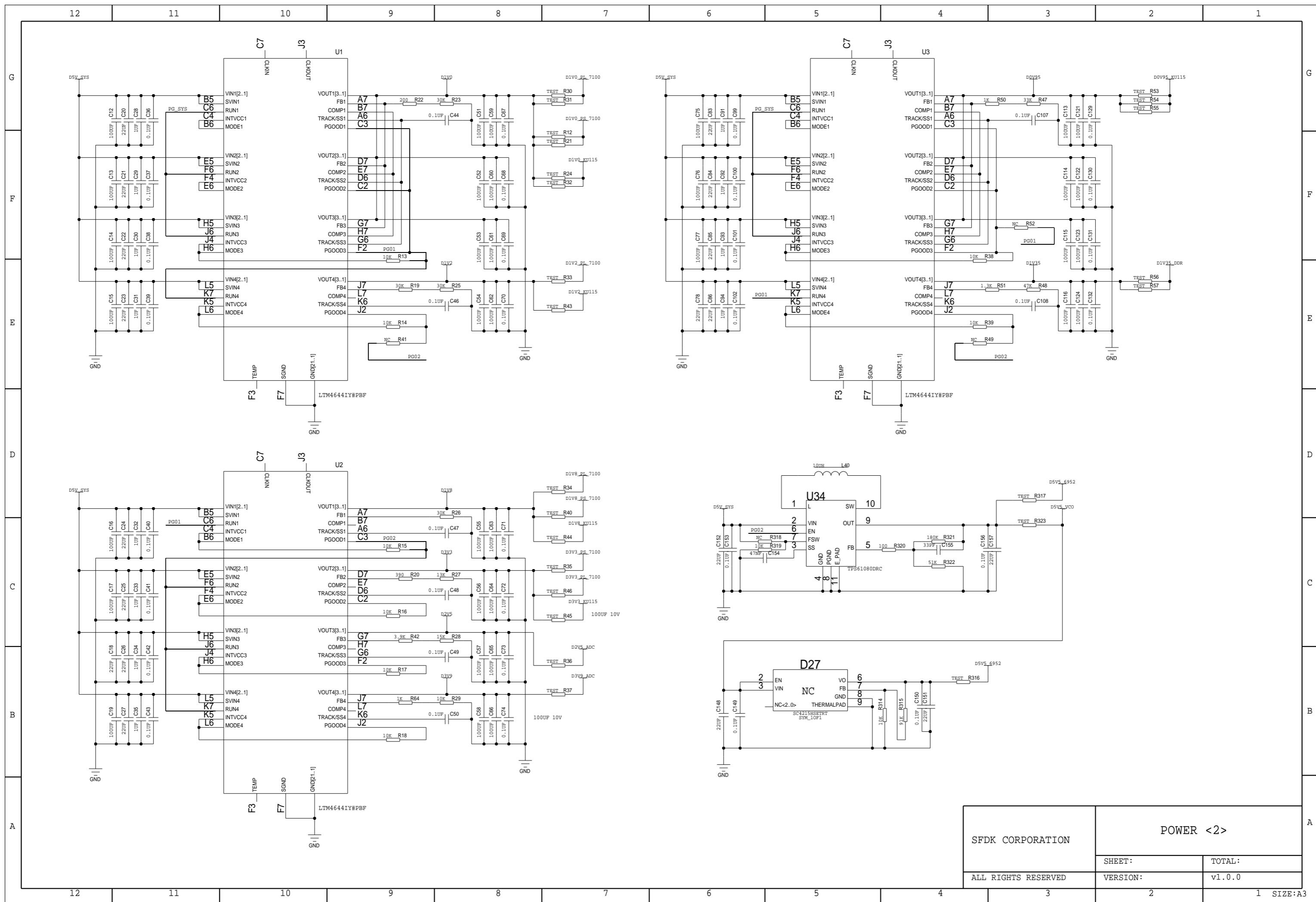
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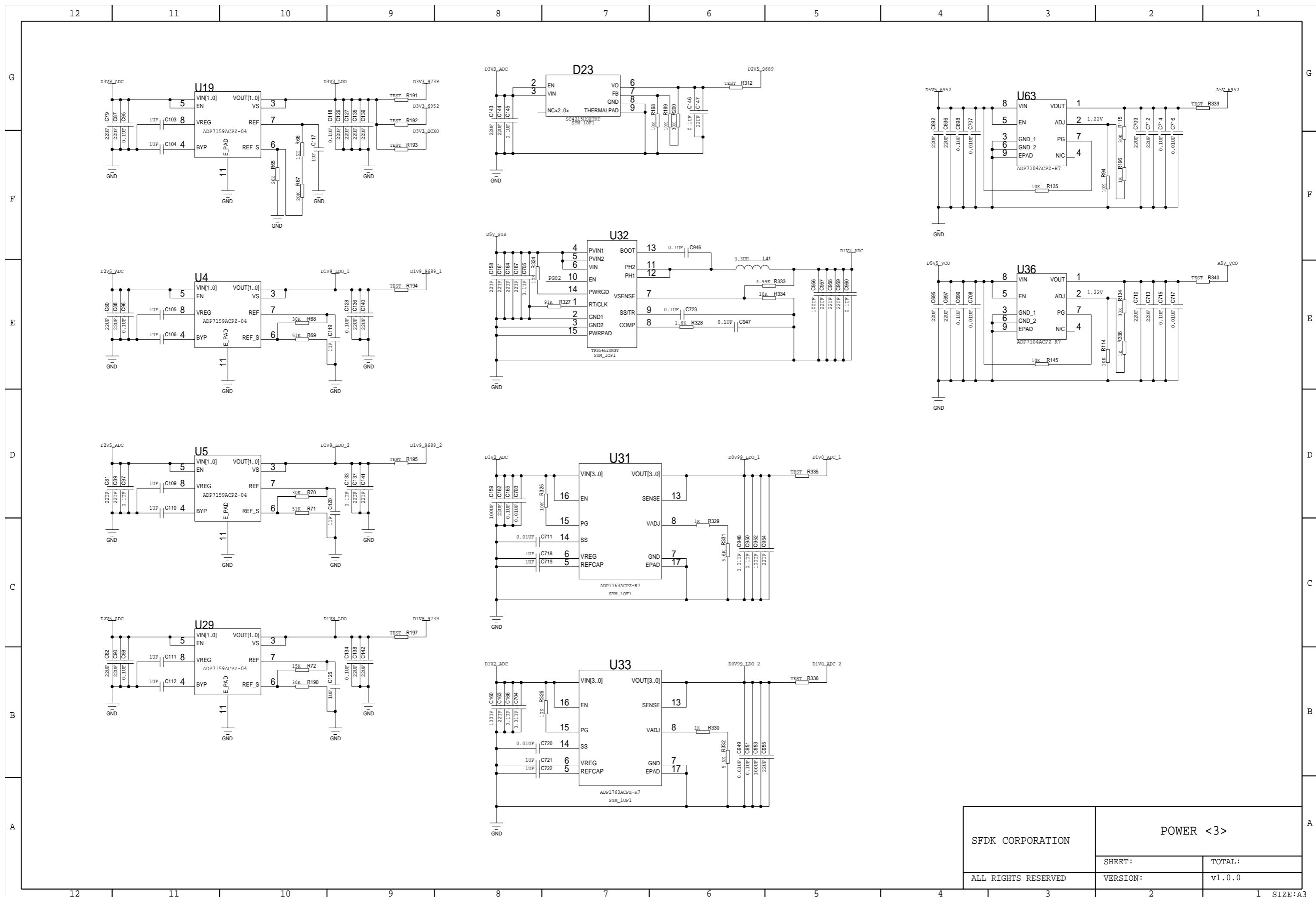
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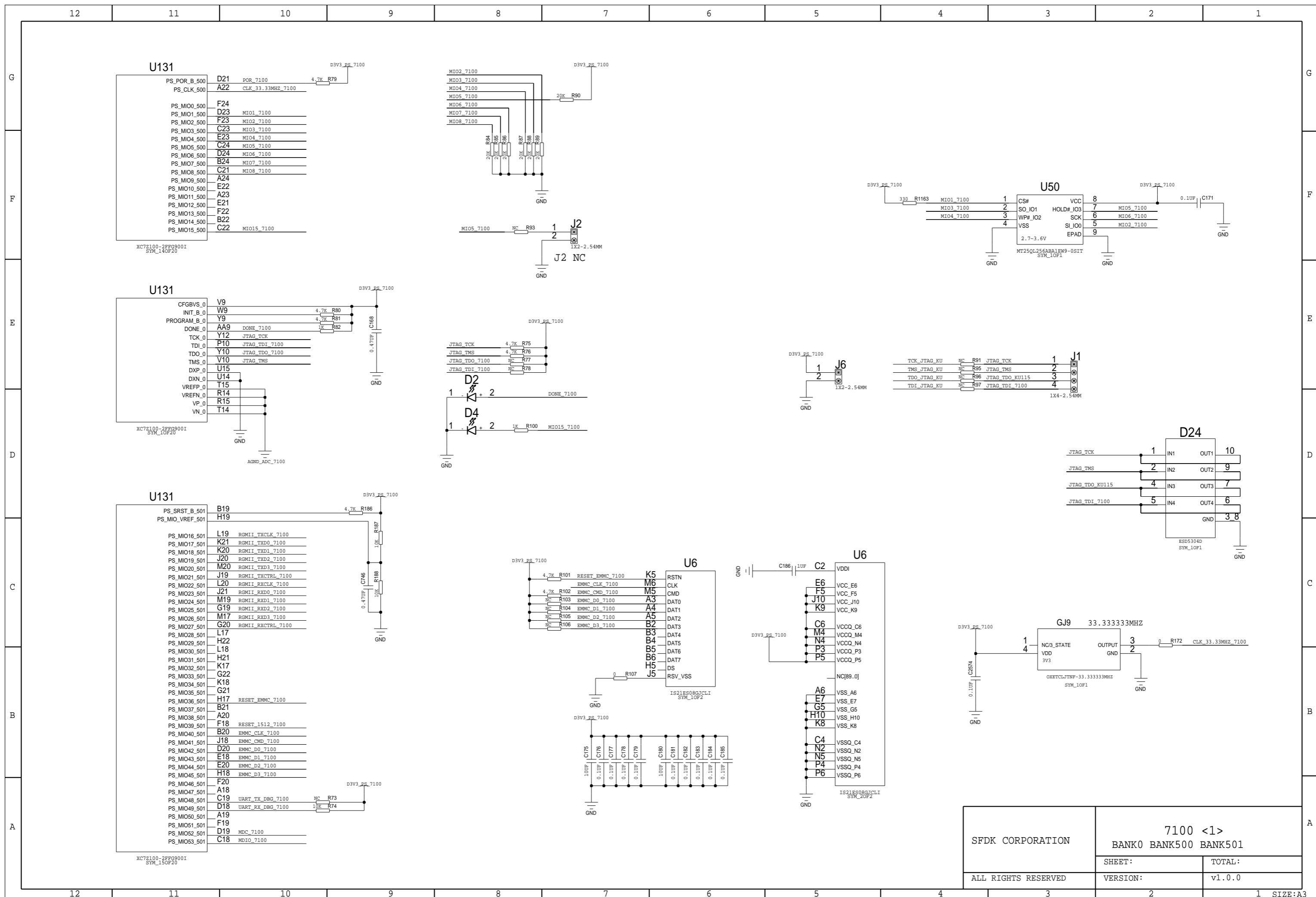


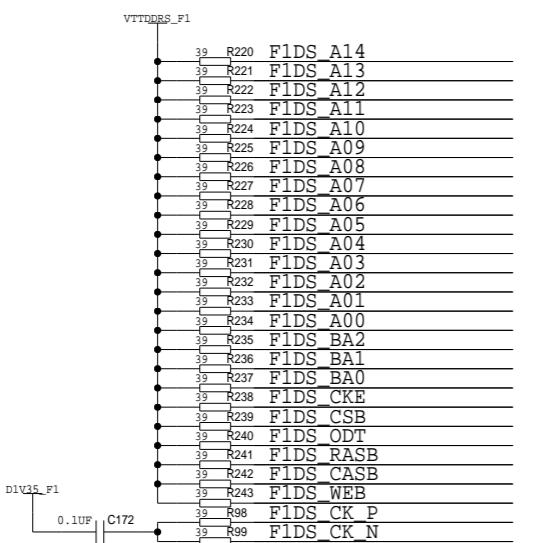
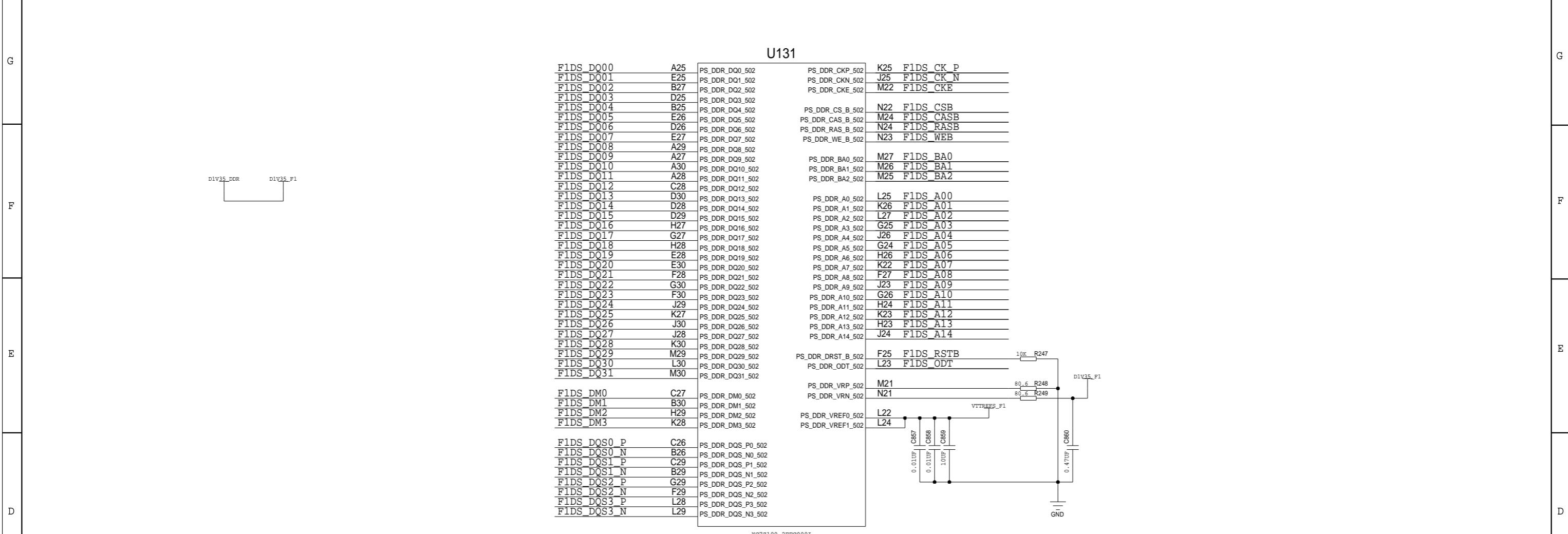
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ALL RIGHTS RESERVED	VERSION:	v1.0.0

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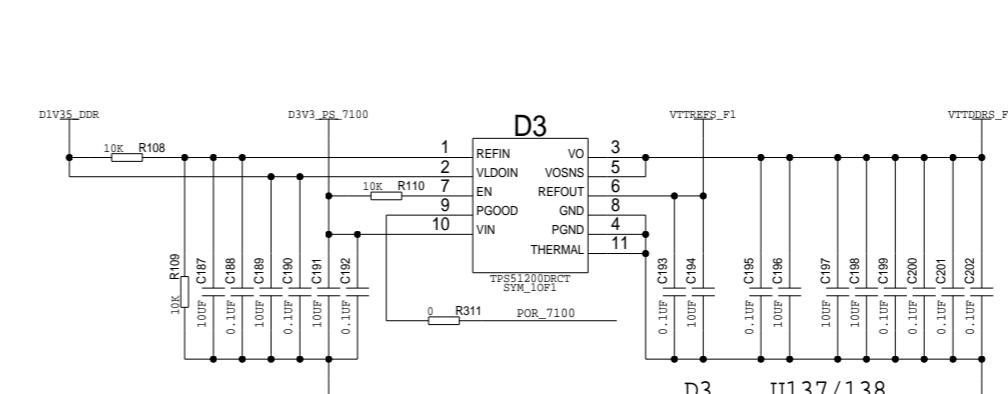








**FLYBY**



SFDK CORPORATION	7100 <2> PS DDR	
SHEET:	TOTAL:	
ALL RIGHTS RESERVED	VERSION:	v1.0.0

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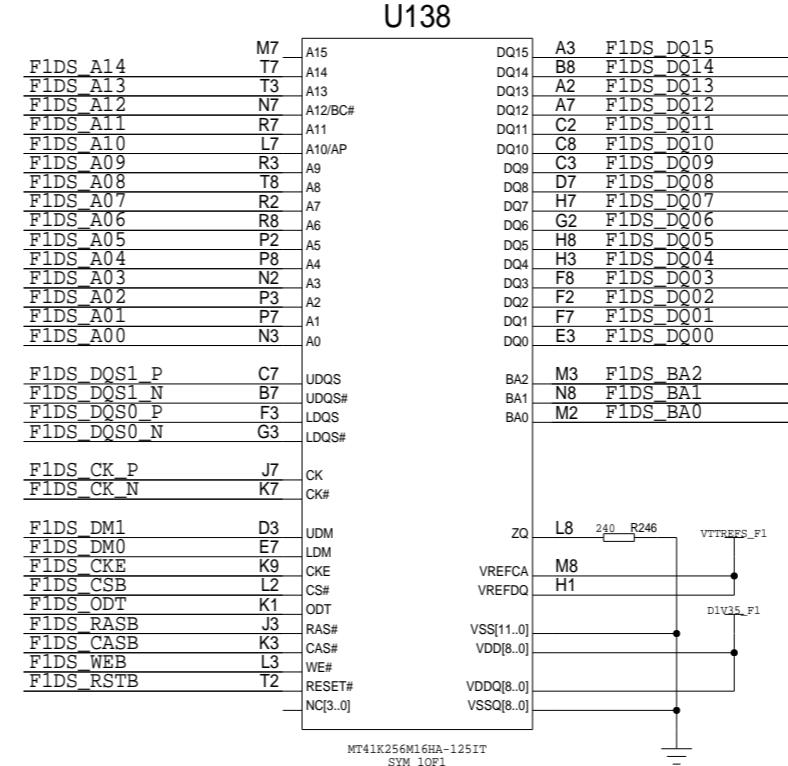
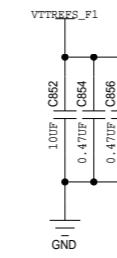
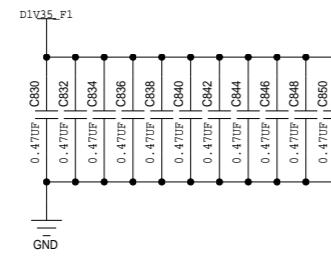
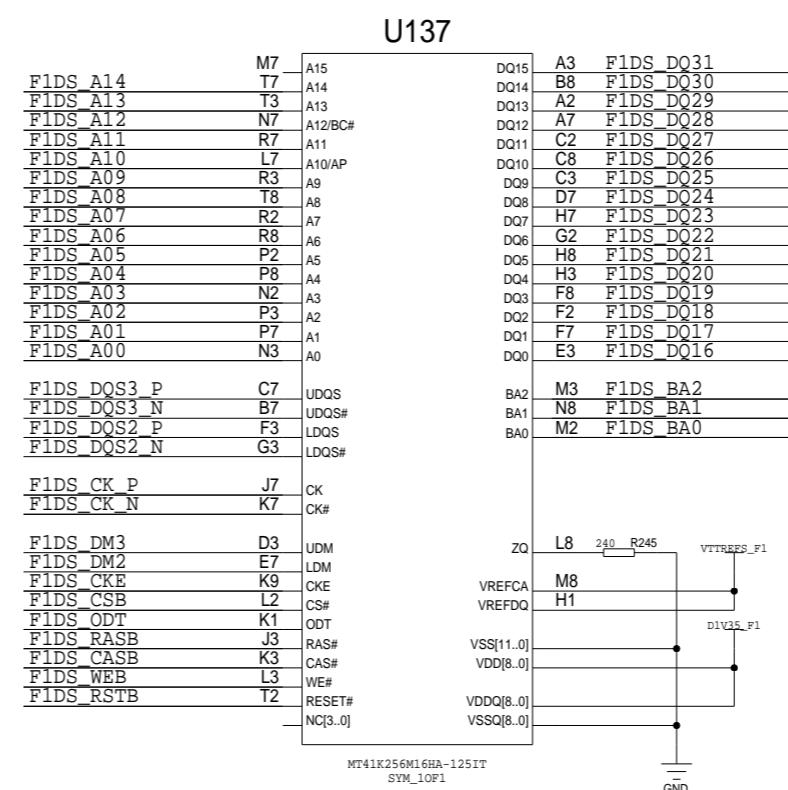
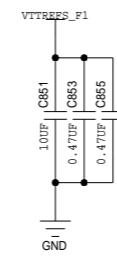
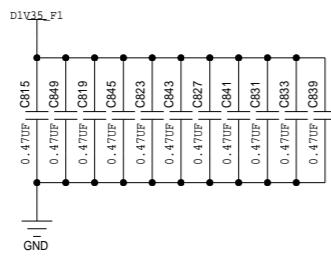
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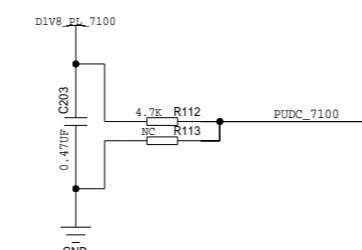
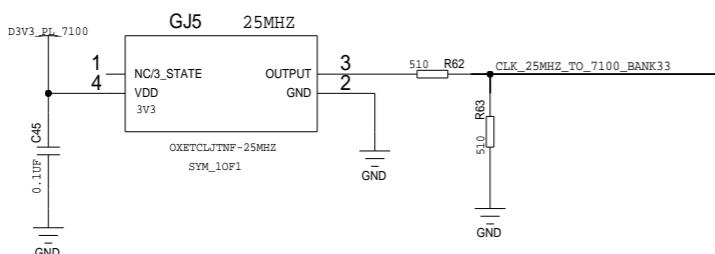
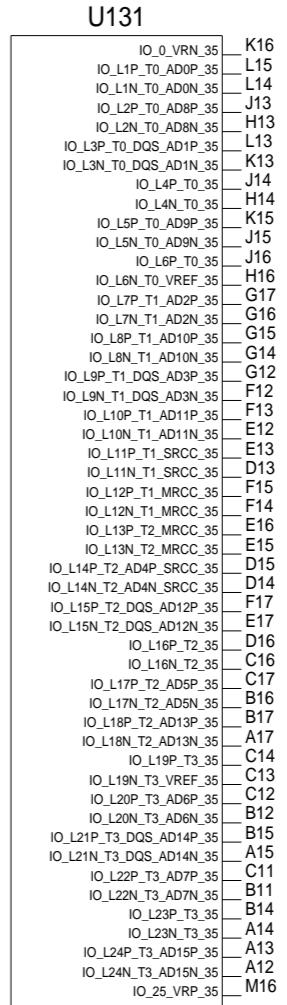
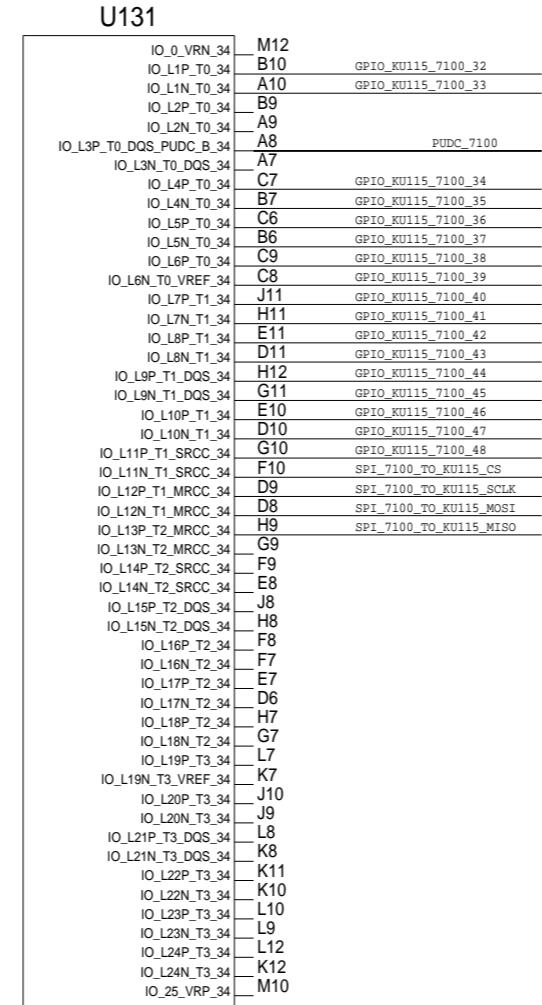
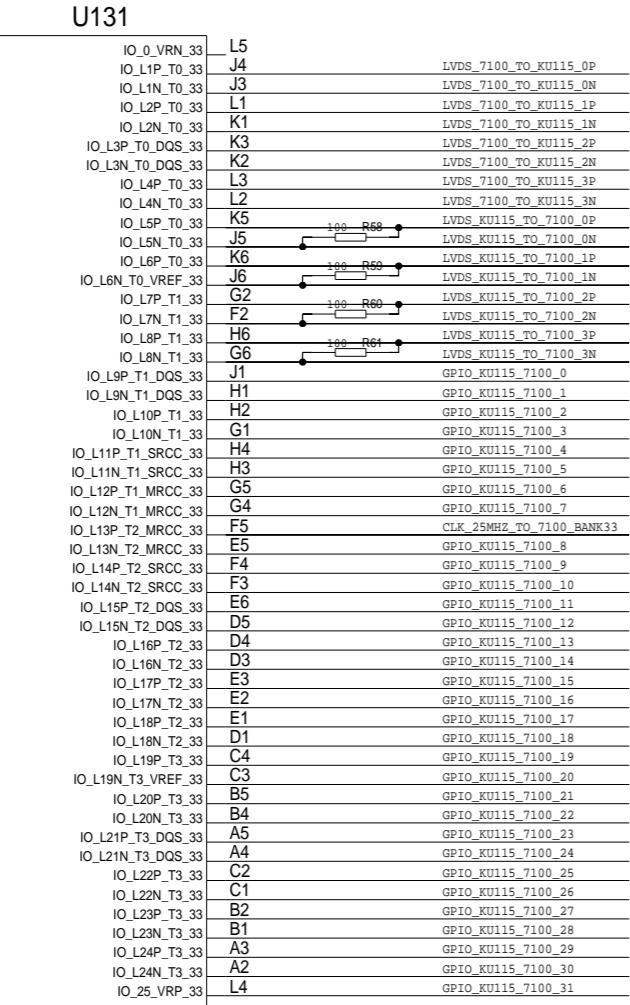


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SFDK CORPORATION	7100 <3> BANK 33 34 35
	SHEET: TOTAL
ALL RIGHTS RESERVED	VERSION: v1.0



G

G

U131

IO_0_10	AA13
IO_L1P_T0_10	AK13
IO_L1N_T0_10	AK12
IO_L2P_T0_10	AH18
IO_L2N_T0_10	AJ18
IO_L3P_T0_DQS_10	AJ14
IO_L3N_T0_DQS_10	AJ13
IO_L4P_T0_10	AJ16
IO_L4N_T0_10	AK16
IO_L5P_T0_10	AJ15
IO_L5N_T0_10	AK15
IO_L6P_T0_10	AH17
IO_L6N_T0_VREF_10	AH16
IO_L7P_T1_10	AE12
IO_L7N_T1_10	AF12
IO_L8P_T1_10	AH14
IO_L8N_T1_10	AH13
IO_L9P_T1_DQS_10	AD14
IO_L9N_T1_DQS_10	AD13
IO_L10P_T1_10	AG12
IO_L10N_T1_10	AH12
IO_L11P_T1_SRCC_10	AE13
IO_L11N_T1_SRCC_10	AF13
IO_L12P_T1_MRCC_10	AF14
IO_L12N_T1_MRCC_10	AG14
IO_L13P_T2_MRCC_10	AG17
IO_L13N_T2_MRCC_10	AG16
IO_L14P_T2_SRCC_10	AF15
IO_L14N_T2_SRCC_10	AG15
IO_L15P_T2_DQS_10	AF18
IO_L15N_T2_DQS_10	AF17
IO_L16P_T2_10	AE16
IO_L16N_T2_10	AE15
IO_L17P_T2_10	AE18
IO_L17N_T2_10	AE17
IO_L18P_T2_10	AD16
IO_L18N_T2_10	AD15
IO_L19P_T3_10	AC14
IO_L19N_T3_VREF_10	AC13
IO_L20P_T3_10	AA15
IO_L20N_T3_10	AA14
IO_L21P_T3_DQS_10	AB12
IO_L21N_T3_DQS_10	AC12
IO_L22P_T3_10	AB15
IO_L22N_T3_10	AB14
IO_L23P_T3_10	AC17
IO_L23N_T3_10	AC16
IO_L24P_T3_10	AB17
IO_L24N_T3_10	AB16
IO_25_10	AA17

XC7Z100-2FFG900I  
SYM\_30F20

U131

IO_0_11	W23
IO_L1P_T0_11	PWR TX0_RF_KU
IO_L1N_T0_11	PWR TX1_RF_KU
IO_L2P_T0_11	PWR TX2_RF_KU
IO_L2N_T0_11	PWR TX3_RF_KU
IO_L2N_T0_11	PWR TX4_RF_KU
IO_L3P_T0_DQS_11	AJ21
IO_L3N_T0_DQS_11	AK25
IO_L4P_T0_11	AK22
IO_L4N_T0_11	AK23
IO_L5P_T0_11	AK24
IO_L5N_T0_11	AH23
IO_L6P_T0_11	AG22
IO_L6N_T0_VREF_11	AH22
IO_L7P_T1_11	AC24
IO_L7N_T1_11	AD24
IO_L8P_T1_11	AG24
IO_L8N_T1_11	AG25
IO_L9P_T1_DQS_11	AF23
IO_L9N_T1_DQS_11	AF24
IO_L10P_T1_11	AD21
IO_L10N_T1_11	AE21
IO_L11P_T1_SRCC_11	AD23
IO_L11N_T1_SRCC_11	AE23
IO_L12P_T1_MRCC_11	AE22
IO_L12N_T1_MRCC_11	AF22
IO_L13P_T2_MRCC_11	DAC_CS#_2601
IO_L13N_T2_MRCC_11	DAC_SCK_2601
IO_L13N_T2_MRCC_11	AH21
IO_L14P_T2_SRCC_11	AF20
IO_L14N_T2_SRCC_11	AG20
IO_L15P_T2_DQS_11	AJ20
IO_L15N_T2_DQS_11	AK20
IO_L16P_T2_11	PWM1_FAN
IO_L16P_T2_11	AK17
IO_L16N_T2_11	AK18
IO_L17P_T2_11	KIND0+_KU
IO_L17N_T2_11	KIND0-_KU
IO_L18P_T2_11	KIND1+_KU
IO_L18P_T2_11	AG19
IO_L18N_T2_11	AB21
IO_L19P_T3_11	AB22
IO_L19N_T3_VREF_11	W21
IO_L20P_T3_11	Y21
IO_L20N_T3_11	Y22
IO_L21P_T3_DQS_11	Y23
IO_L21N_T3_DQS_11	AA24
IO_L22P_T3_11	AB24
IO_L22N_T3_11	AA22
IO_L23P_T3_11	AA23
IO_L23N_T3_11	AC22
IO_L24P_T3_11	AC22
IO_L24N_T3_11	AC23
IO_25_11	AC21

XC7Z100-2FFG900I  
SYM\_40F20

U131

IO_0_12	Y25
IO_L1P_T0_12	Y30
IO_L1N_T0_12	AA30
IO_L2P_T0_12	AB29
IO_L2N_T0_12	AB30
IO_L3P_T0_DQS_12	Y26
IO_L3N_T0_DQS_12	Y27
IO_L4P_T0_12	Y28
IO_L4N_T0_12	AA29
IO_L5P_T0_12	AA27
IO_L5N_T0_12	AA28
IO_L6P_T0_12	AB25
IO_L6N_T0_VREF_12	AB26
IO_L7P_T1_12	AC26
IO_L7N_T1_12	AD26
IO_L8P_T1_12	AD30
IO_L8N_T1_12	AE30
IO_L9P_T1_DQS_12	AC29
IO_L9N_T1_DQS_12	AD29
IO_L10P_T1_12	AD25
IO_L10N_T1_12	AE26
IO_L11P_T1_SRCC_12	AB27
IO_L11N_T1_SRCC_12	AC27
IO_L12P_T1_MRCC_12	AC28
IO_L12N_T1_MRCC_12	AD28
IO_L13P_T2_MRCC_12	AE28
IO_L13N_T2_MRCC_12	AF28
IO_L14P_T2_SRCC_12	AE27
IO_L14N_T2_SRCC_12	AF27
IO_L15P_T2_DQS_12	AF29
IO_L15N_T2_DQS_12	AG29
IO_L16P_T2_12	RES0_KU
IO_L16P_T2_12	AF30
IO_L16N_T2_12	AG30
IO_L17P_T2_12	AG26
IO_L17N_T2_12	AG27
IO_L18P_T2_12	AE25
IO_L18N_T2_12	AF25
IO_L19P_T3_12	AH28
IO_L19N_T3_VREF_12	AH29
IO_L20P_T3_12	AJ30
IO_L20N_T3_12	AK30
IO_L21P_T3_DQS_12	AJ28
IO_L21N_T3_DQS_12	AJ29
IO_L22P_T3_12	AK27
IO_L22N_T3_12	AK28
IO_L23P_T3_12	AH26
IO_L23N_T3_12	AH27
IO_L24P_T3_12	AJ26
IO_L24N_T3_12	AK26
IO_25_12	AA25

XC7Z100-2FFG900I  
SYM\_40F20

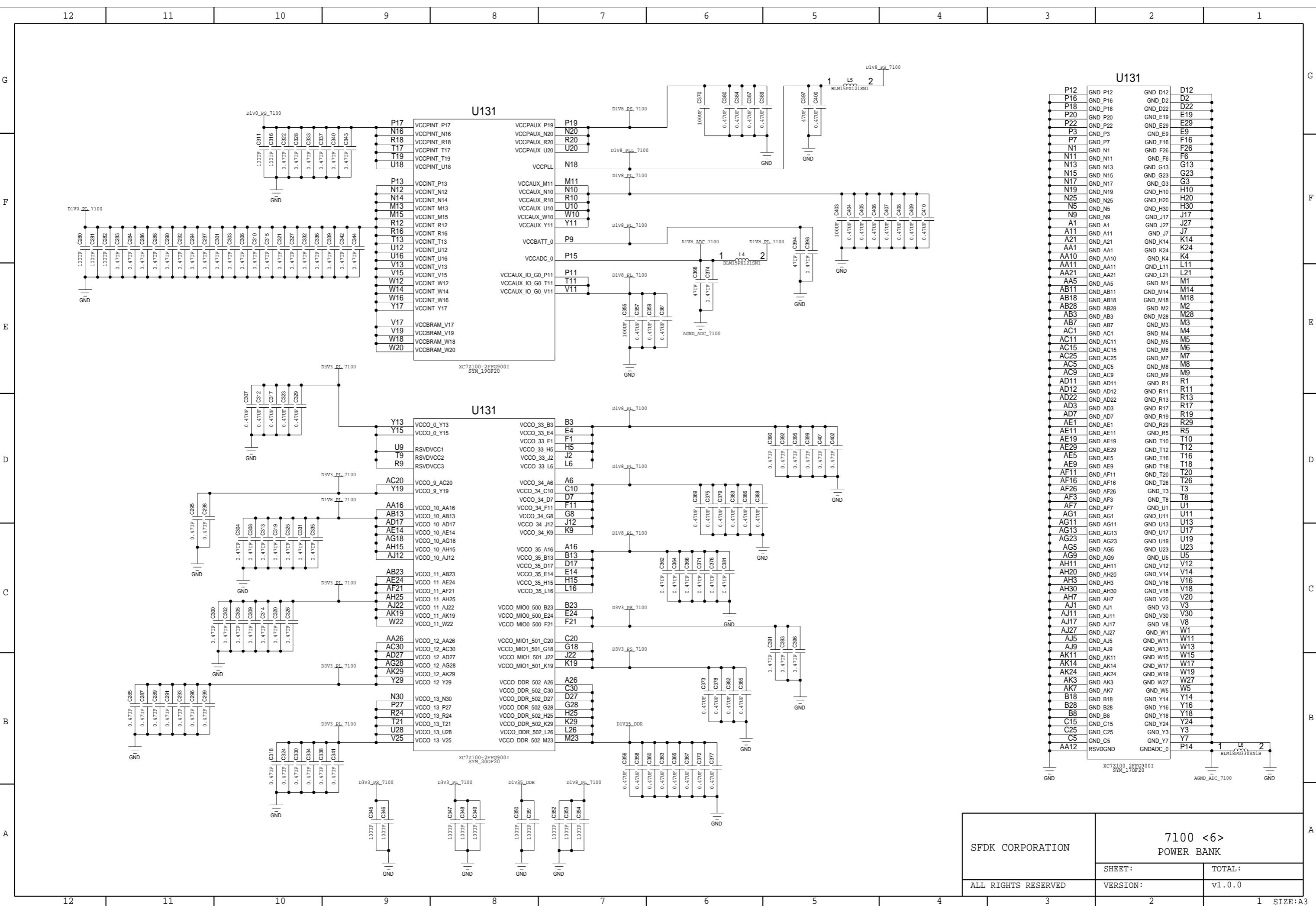
U131

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IO_L1P_T0_13	Y30
IO_L1N_T0_13	AA30
IO_L2P_T0_13	AB29
IO_L2N_T0_13	AB30
IO_L3P_T0_DQS_13	Y26
IO_L3N_T0_DQS_13	Y27
IO_L4P_T0_13	Y28
IO_L4N_T0_13	AA29
IO_L5P_T0_13	AA27
IO_L5N_T0_13	AA28
IO_L6P_T0_13	AB25
IO_L6N_T0_VREF_13	AB26
IO_L7P_T1_13	AC26
IO_L7N_T1_13	AD26
IO_L8P_T1_13	AD30
IO_L8N_T1_13	AE30
IO_L9P_T1_DQS_13	AC29
IO_L9N_T1_DQS_13	AD29
IO_L10P_T1_13	AD25
IO_L10N_T1_13	AE26
IO_L11P_T1_SRCC_13	AB27
IO_L11N_T1_SRCC_13	AC27
IO_L12P_T1_MRCC_13	AC28
IO_L12N_T1_MRCC_13	AD28
IO_L13P_T2_MRCC_13	AE28
IO_L13N_T2_MRCC_13	AF28
IO_L14P_T2_SRCC_13	AE27
IO_L14N_T2_SRCC_13	AF27
IO_L15P_T2_DQS_13	AF29
IO_L15N_T2_DQS_13	AG29
IO_L16P_T2_13	S15341_CS#
IO_L16N_T2_13	S15341_SCLK
IO_L17P_T2_13	S15341_MOSI
IO_L17N_T2_13	S15341_MISO
IO_L18P_T2_13	S15341_RST#
IO_L18N_T2_13	S15341_OUT_EN
IO_L19P_T3_13	P21
IO_L20P_T3_13	R21
IO_L20N_T3_13	T22
IO_L21P_T3_DQS_13	R23
IO_L22P_T3_13	U22
IO_L22N_T3_13	V22
IO_L23P_T3_13	U24
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IO_25_13	V21

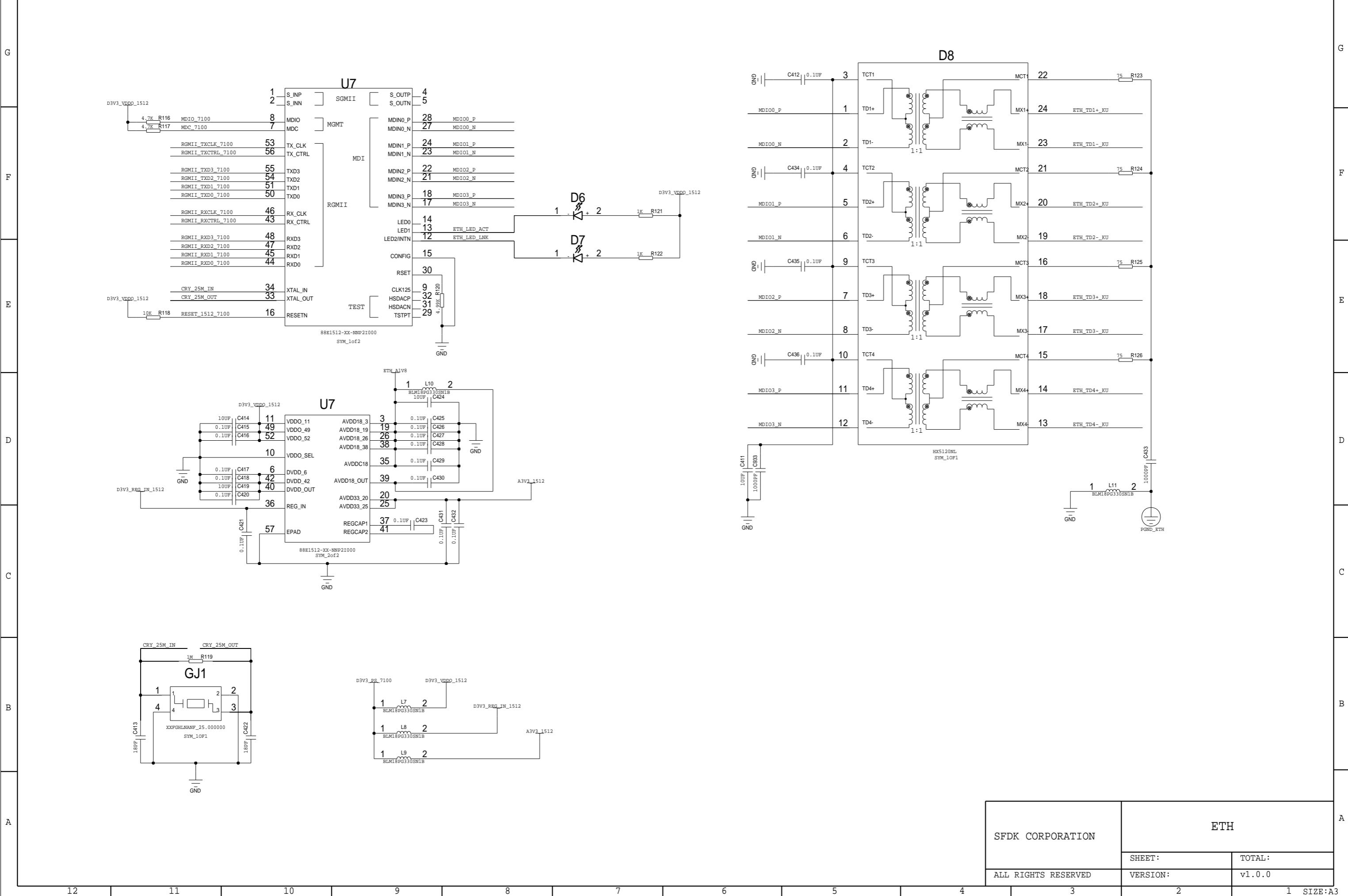
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U131

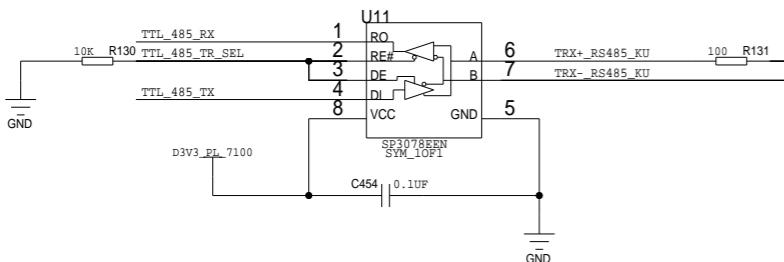
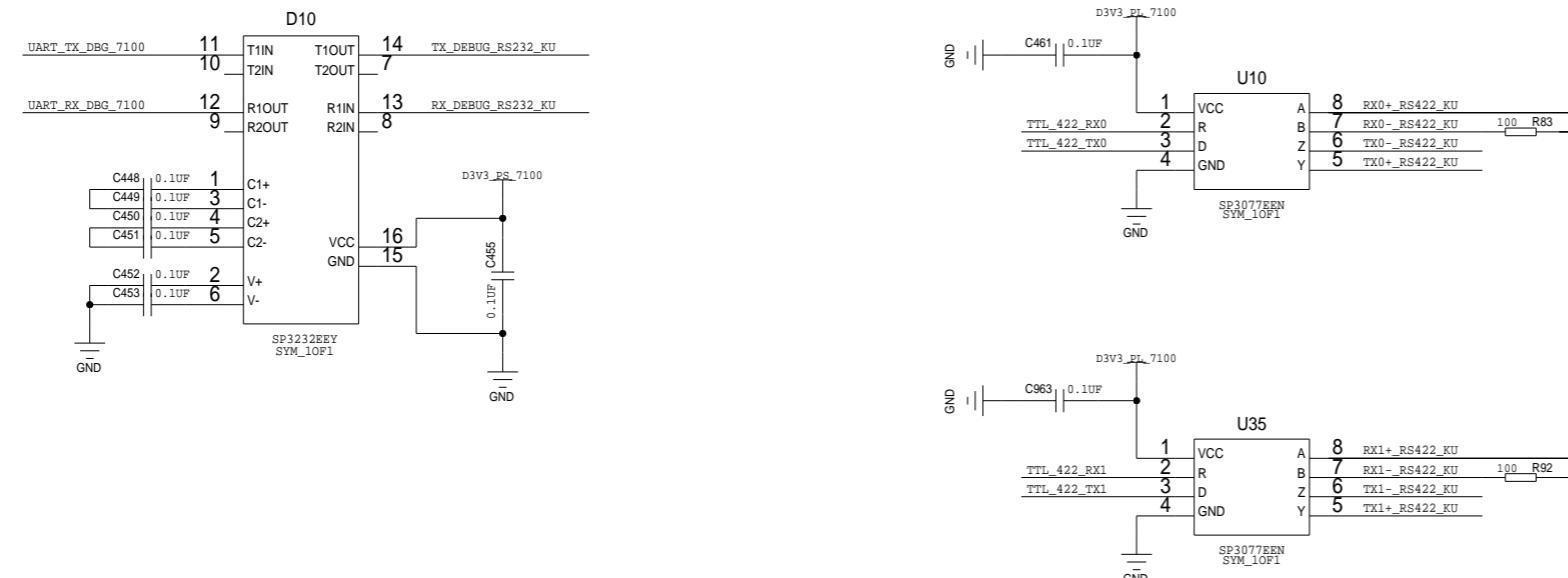
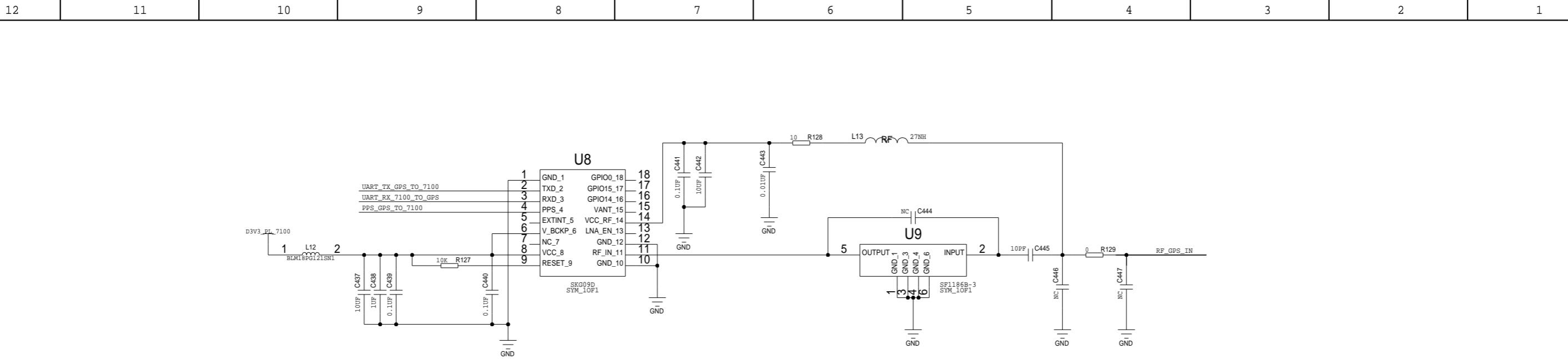
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IO_12P_T1_MRCC_9	AD18
IO_12N_T1_MRCC_9	AD19
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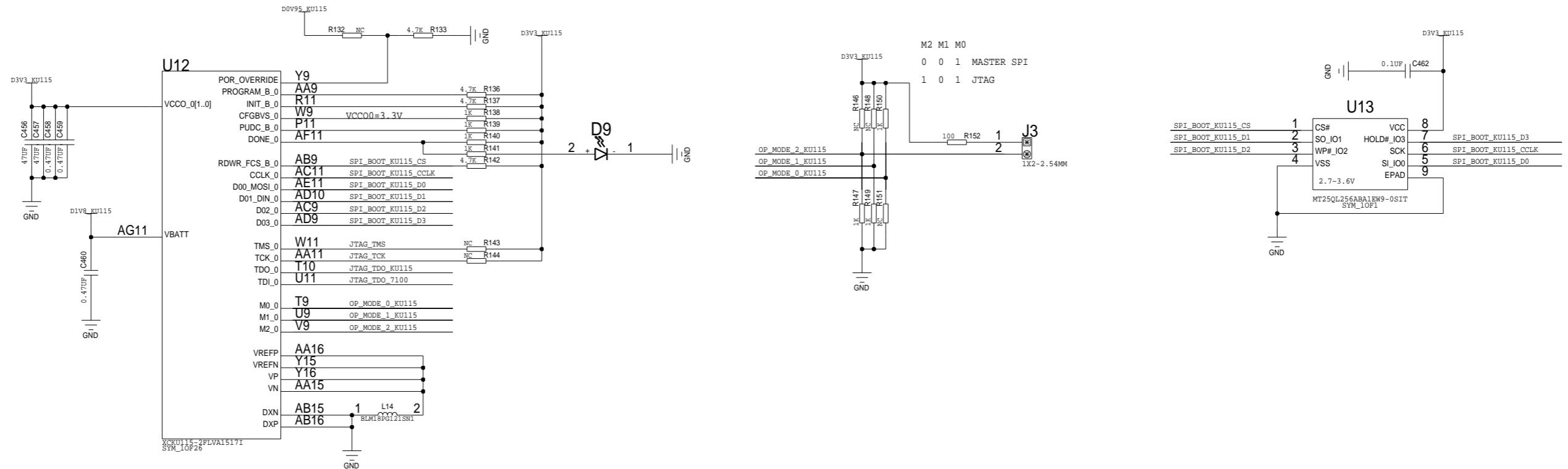
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SHEET:	TOTAL:	
ALL RIGHTS RESERVED	VERSION:	v1.0.0



SFDK CORPORATION

KU115 <1> BANK0

SHEET: TOTAL:

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VERSION: v1.0.0

ALL RIGHTS RESERVED

VERSION: v1.0.0

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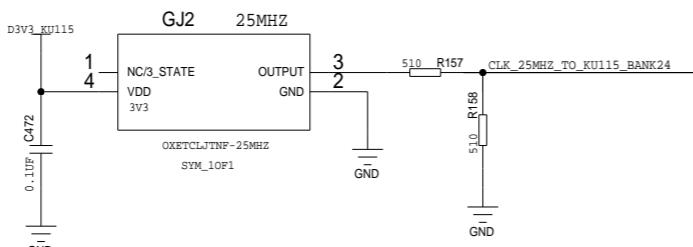
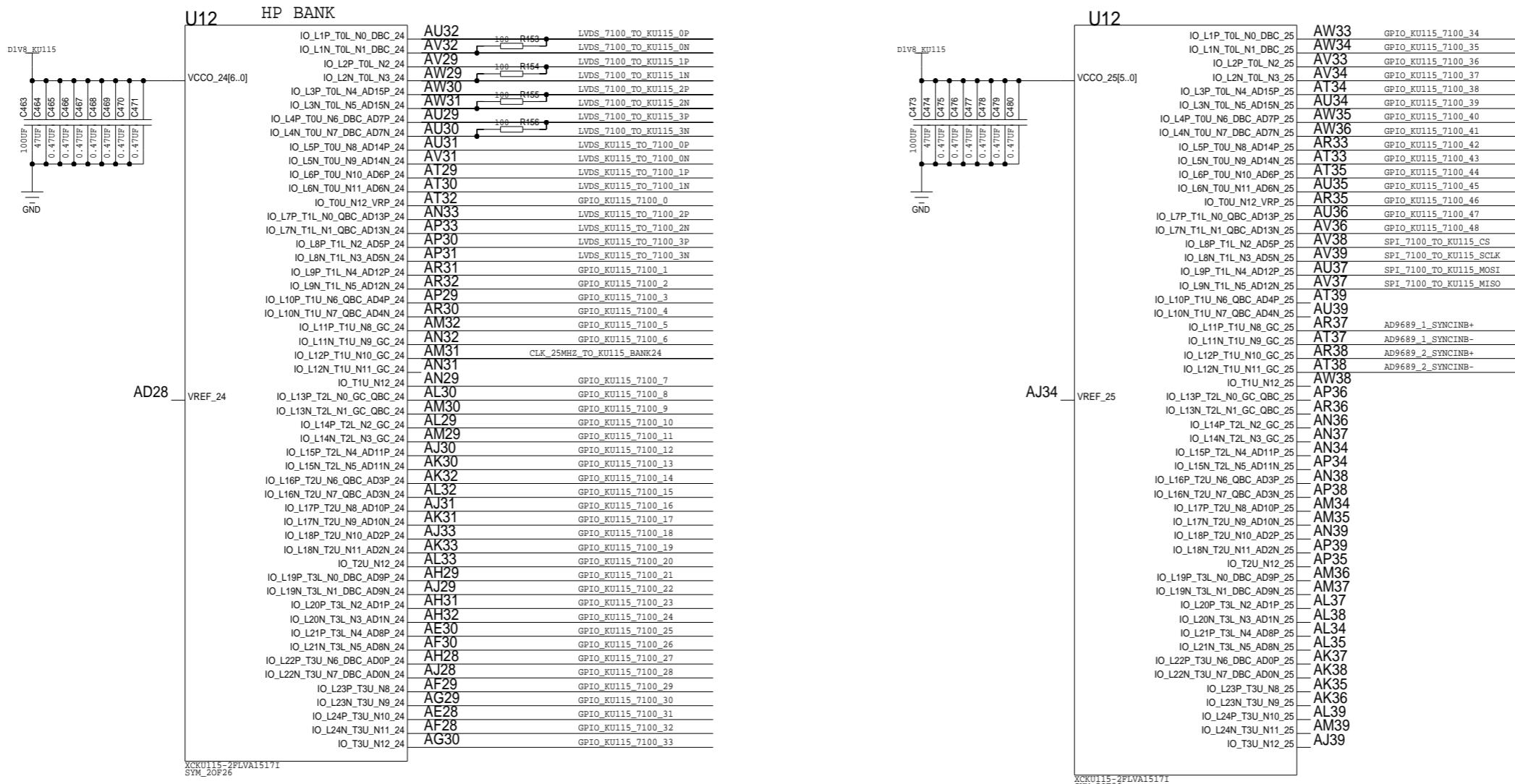
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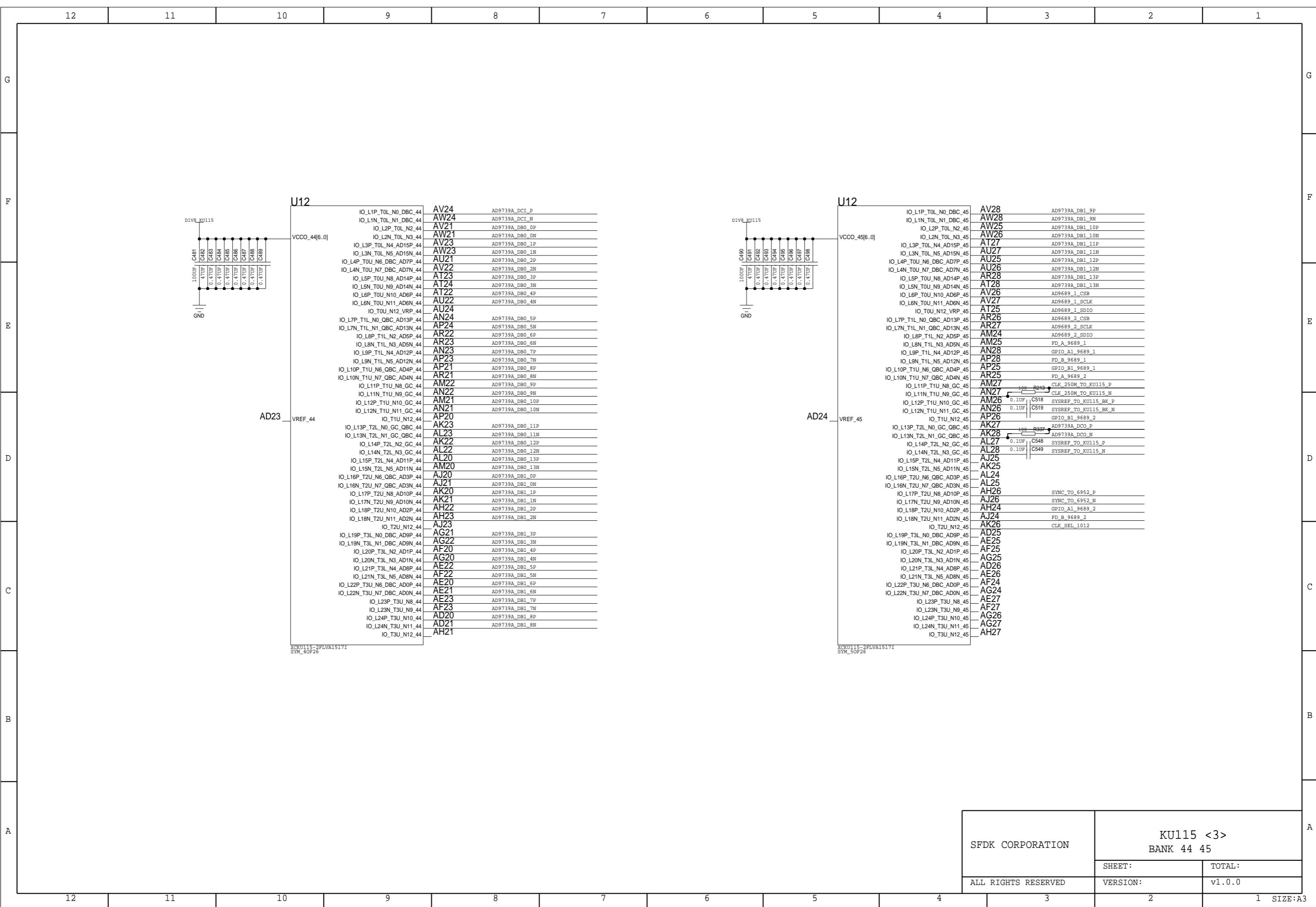
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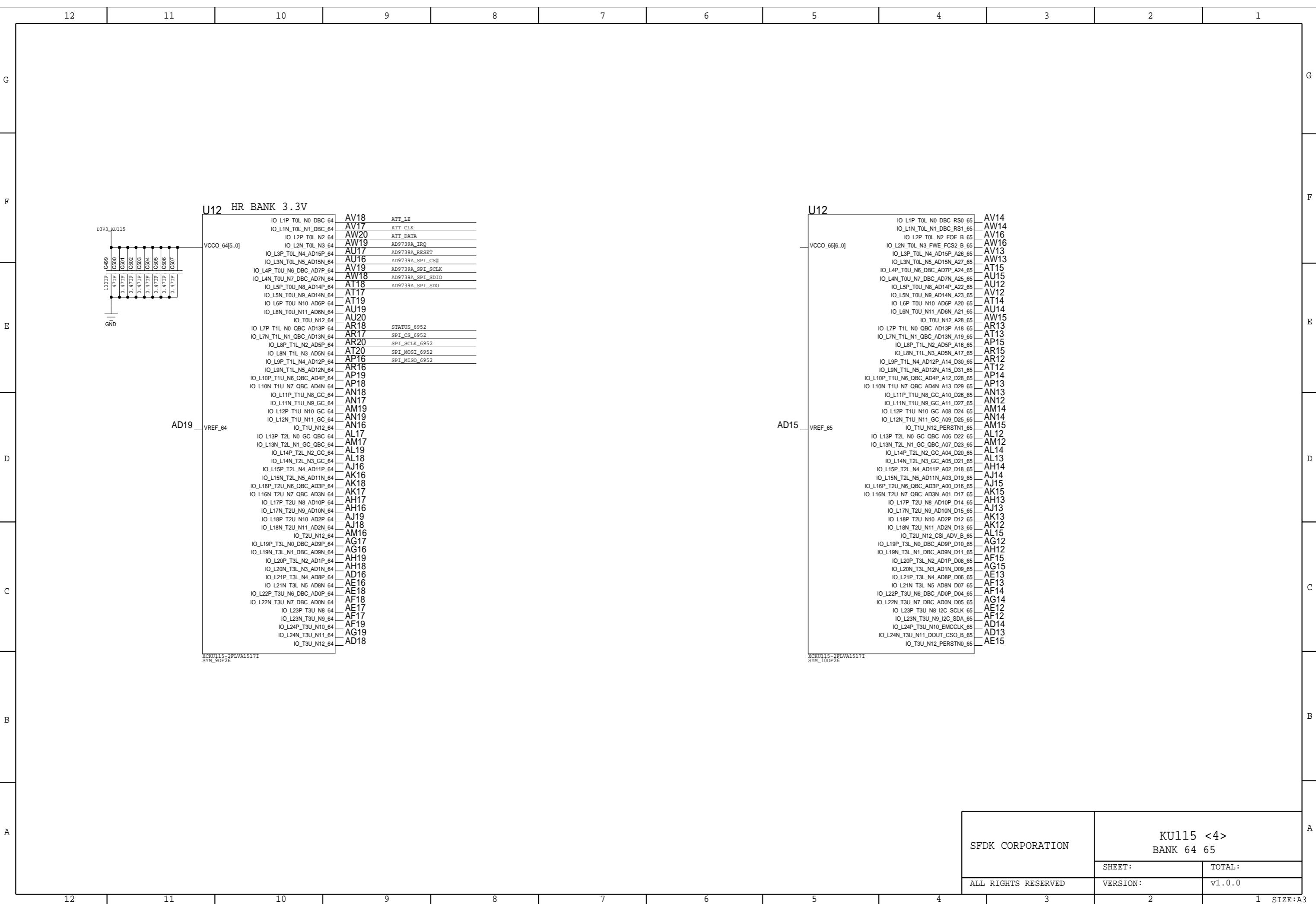
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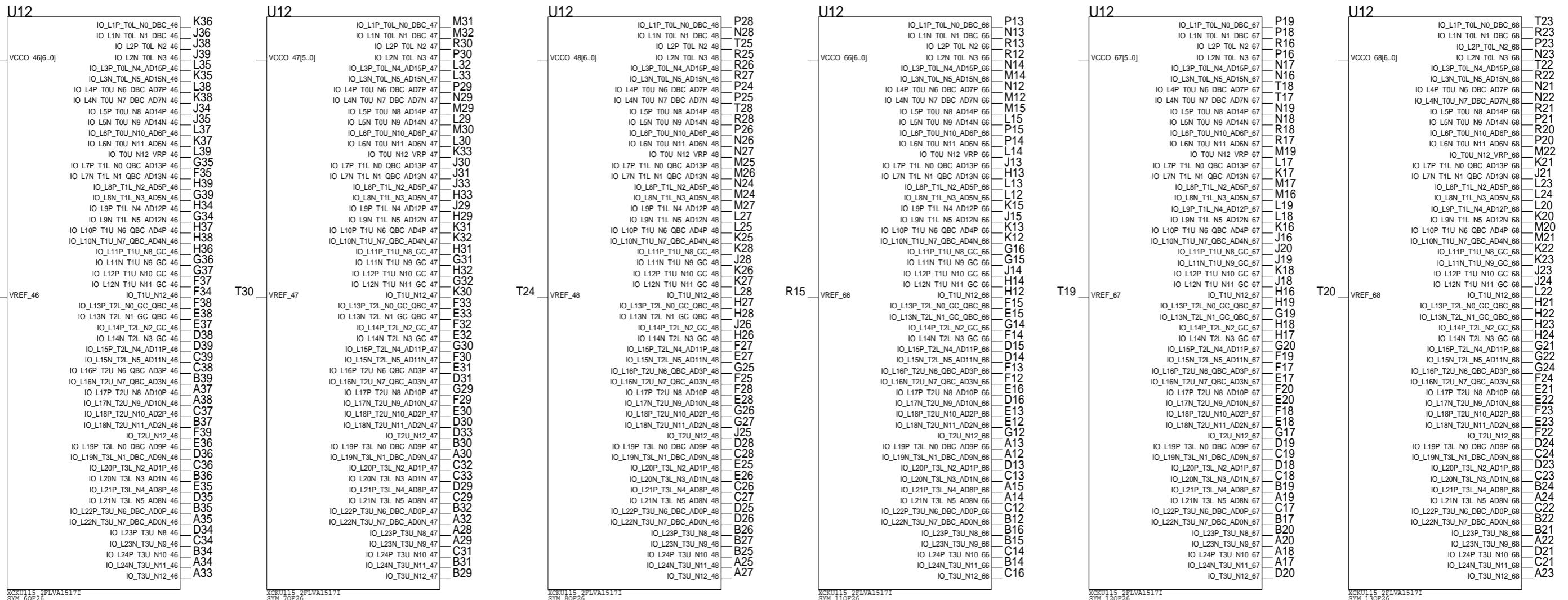
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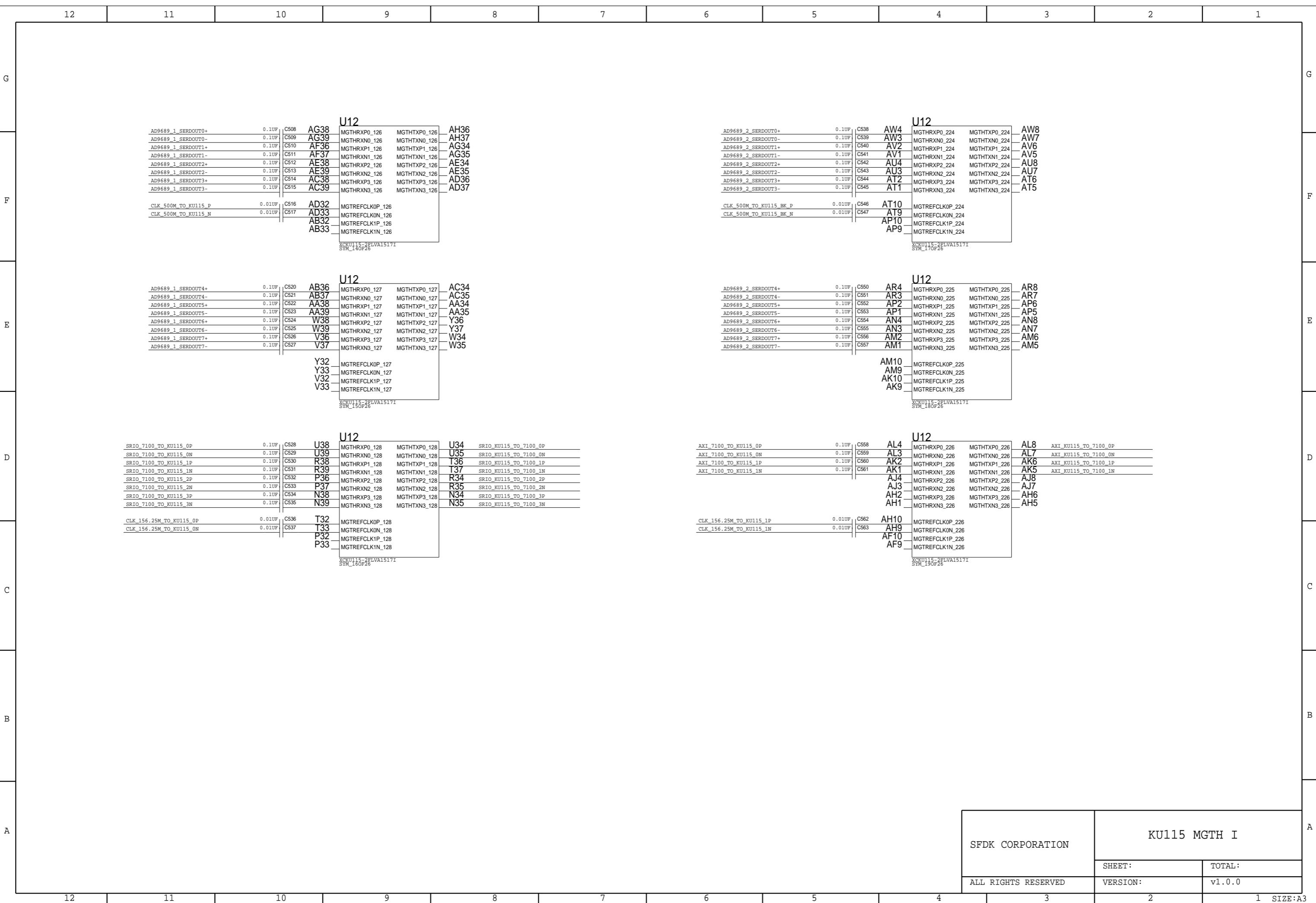




G

6





The diagram illustrates a complex digital circuit design, likely a Field-Programmable Gate Array (FPGA) layout. It features seven vertical columns (A through G) and seven horizontal rows (A through G) of components. The components are primarily U12 logic blocks, which are standard FPGA macrocells. Each U12 block has multiple pins labeled with letters (e.g., A, B, C, D, E, F, G, H, I, J, K, L, M, N, P, Q, R, S, T, U, V, W, X, Y, Z) and numbers (e.g., 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29). These pins are interconnected via a dense network of lines, many of which are labeled with values such as '0.1UF' or '0.01UF' indicating component values or connection characteristics. The overall layout is highly organized and follows a standard grid-based design typical for high-speed digital signal processing applications.

G

G

F

F

E

E

D

D

C

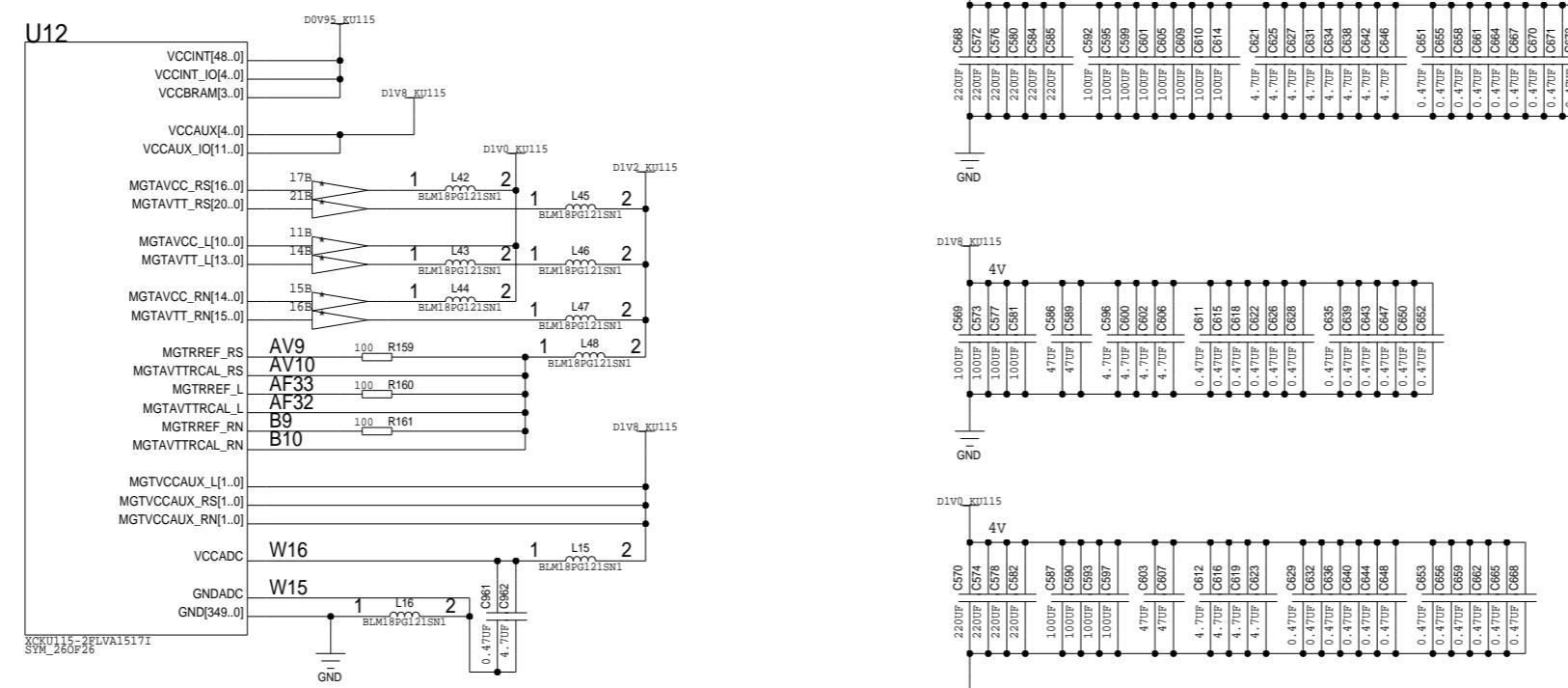
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B

B

A

A



SFDK CORPORATION

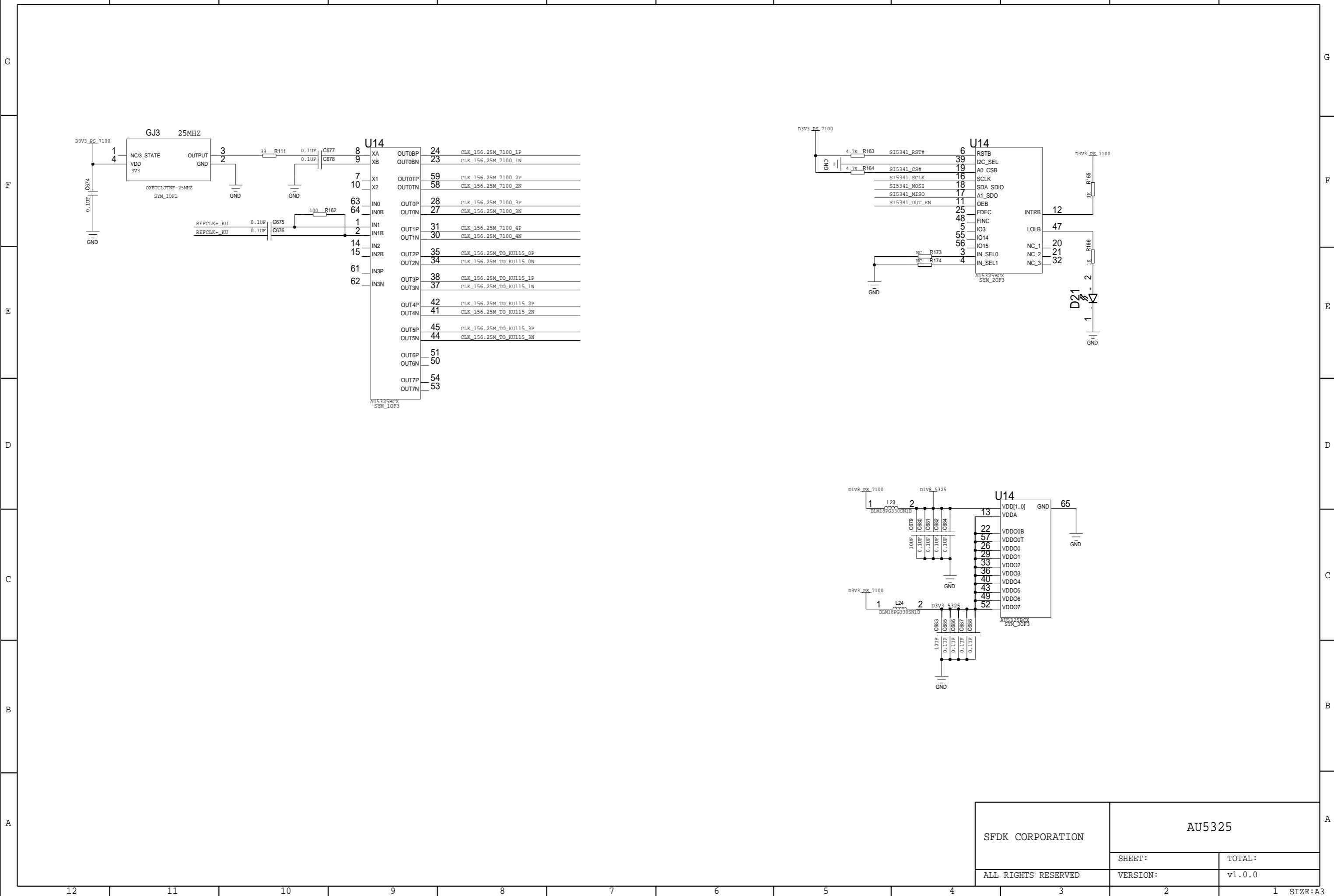
KU115 PWR BANK

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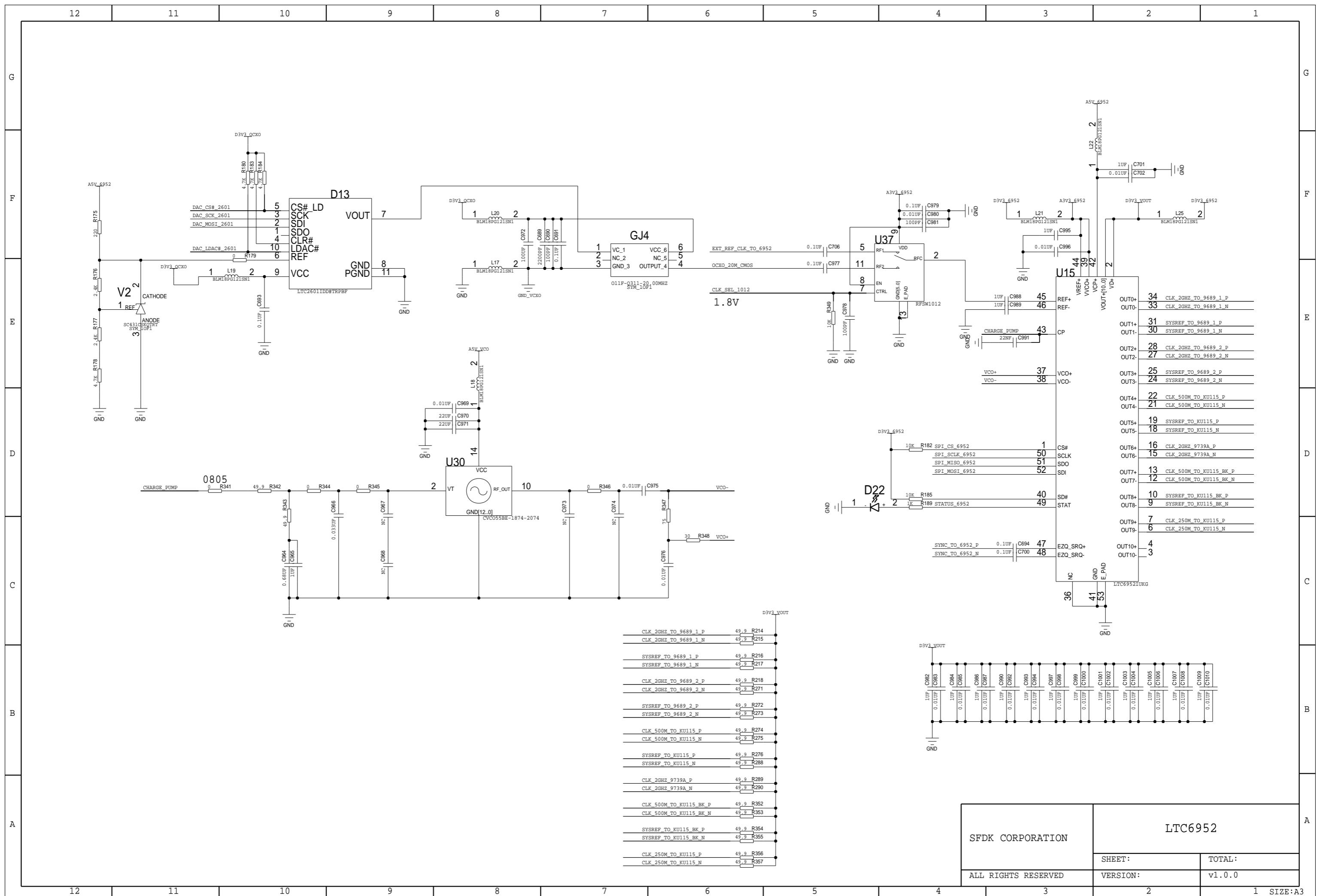
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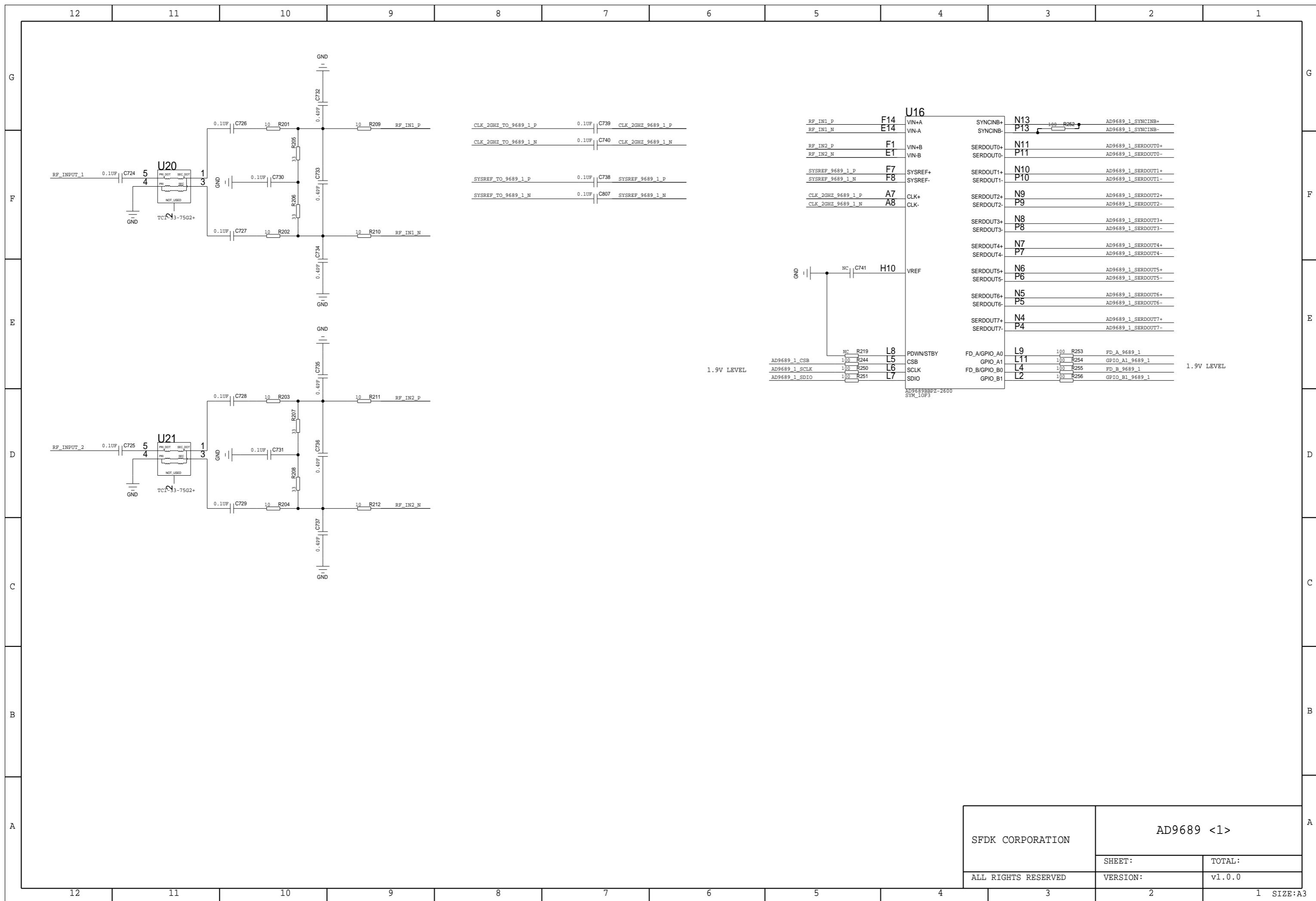
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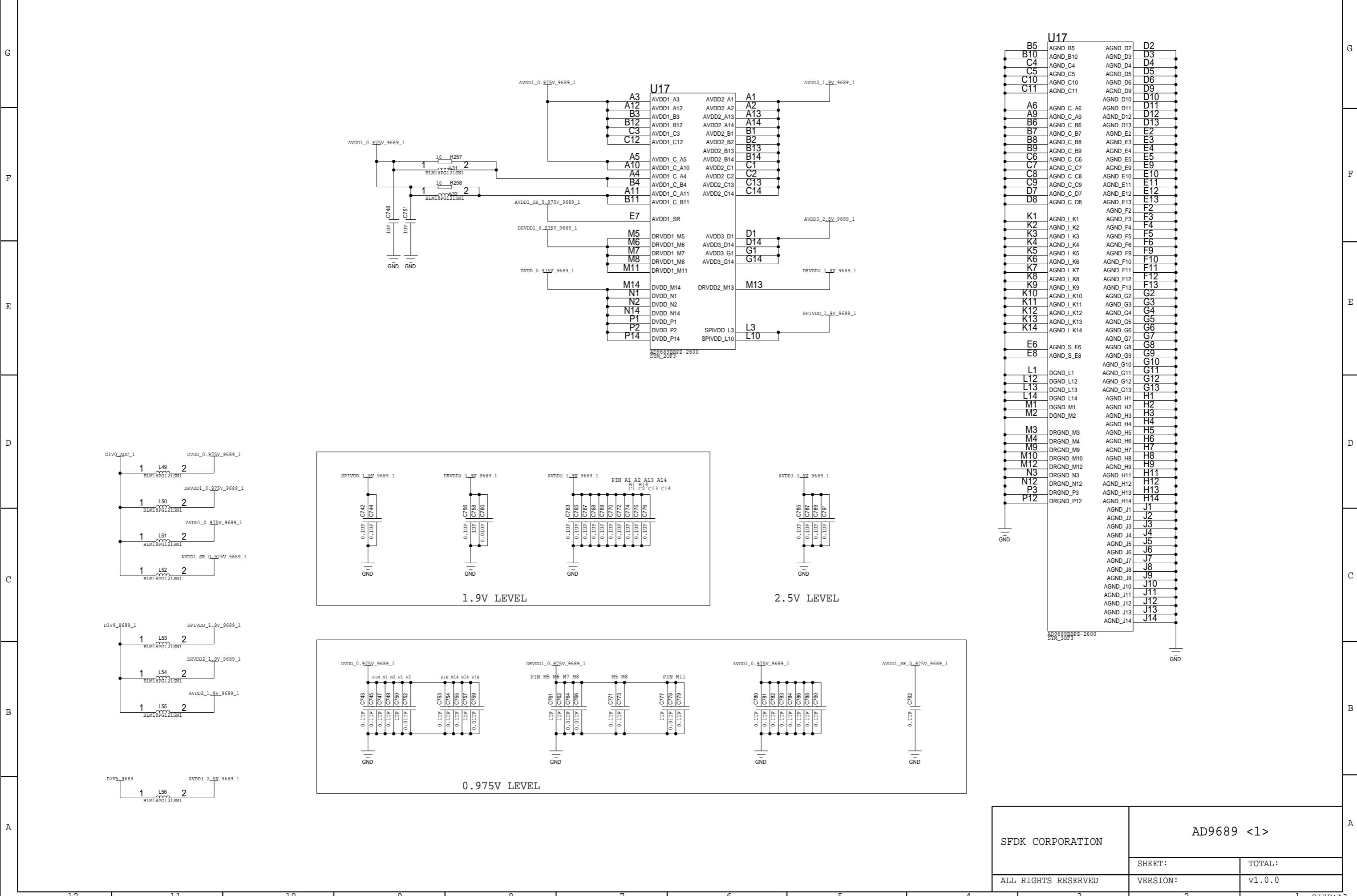


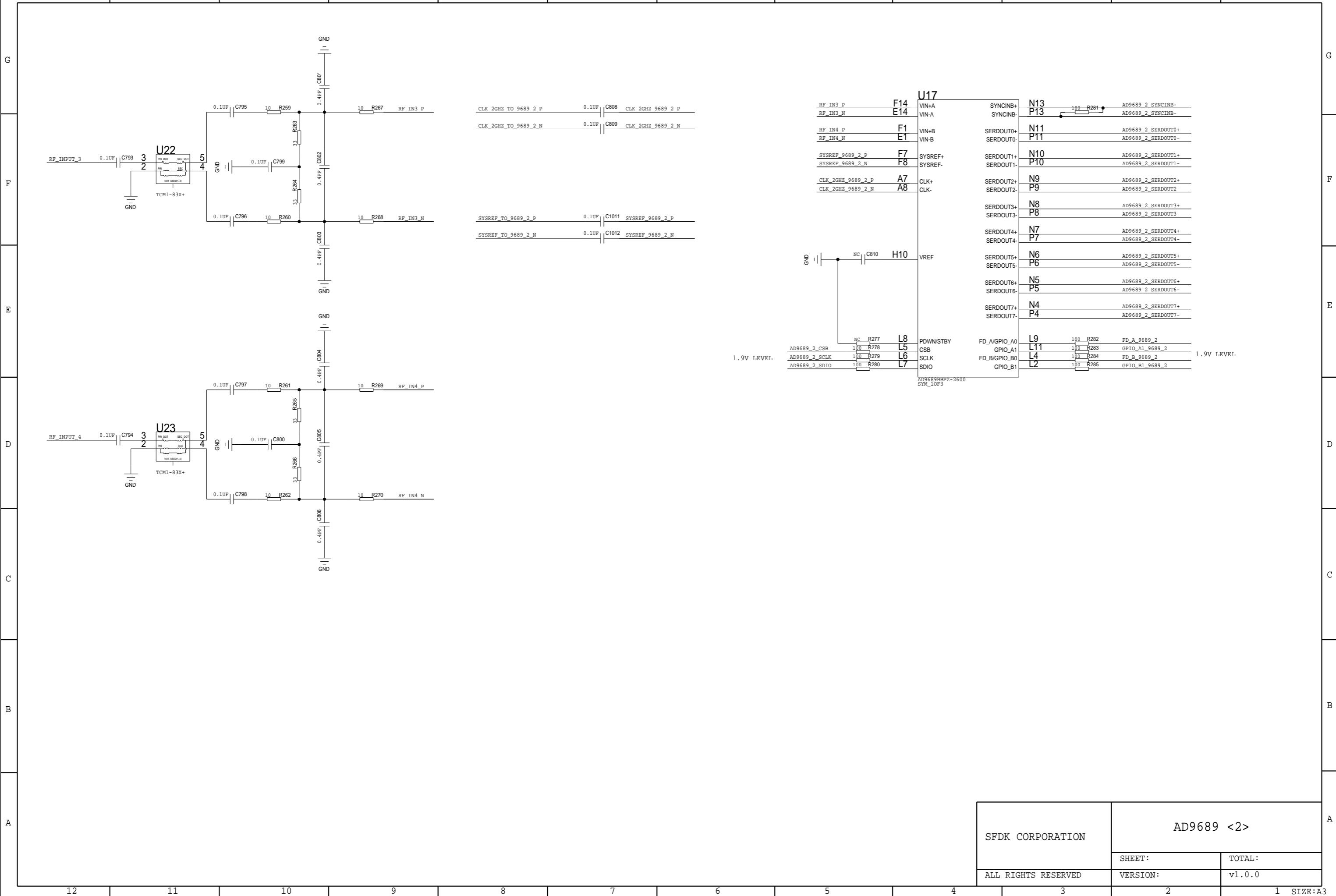
SFDK CORPORATION	AU5325	
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ALL RIGHTS RESERVED		VERSION: v1.0.0

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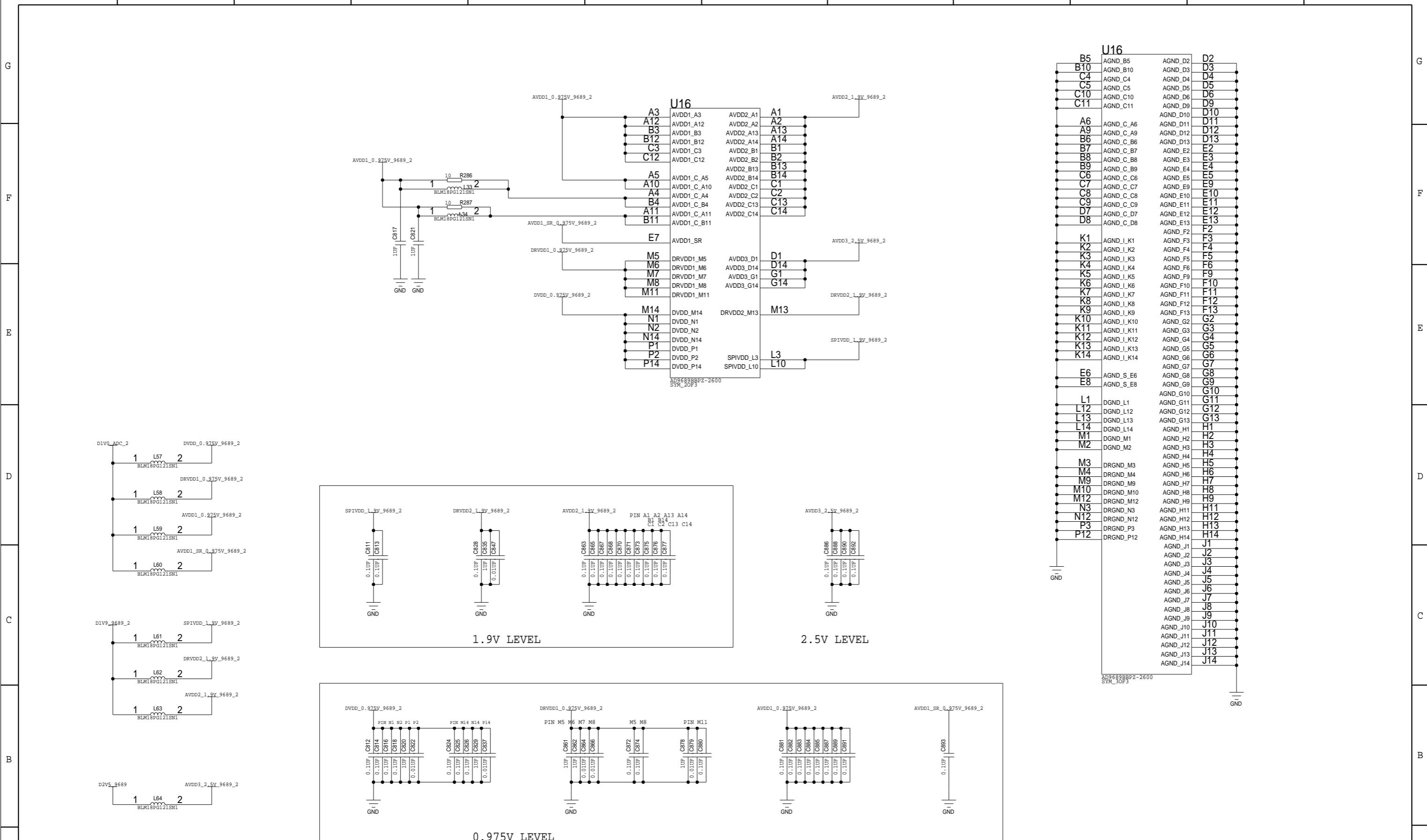




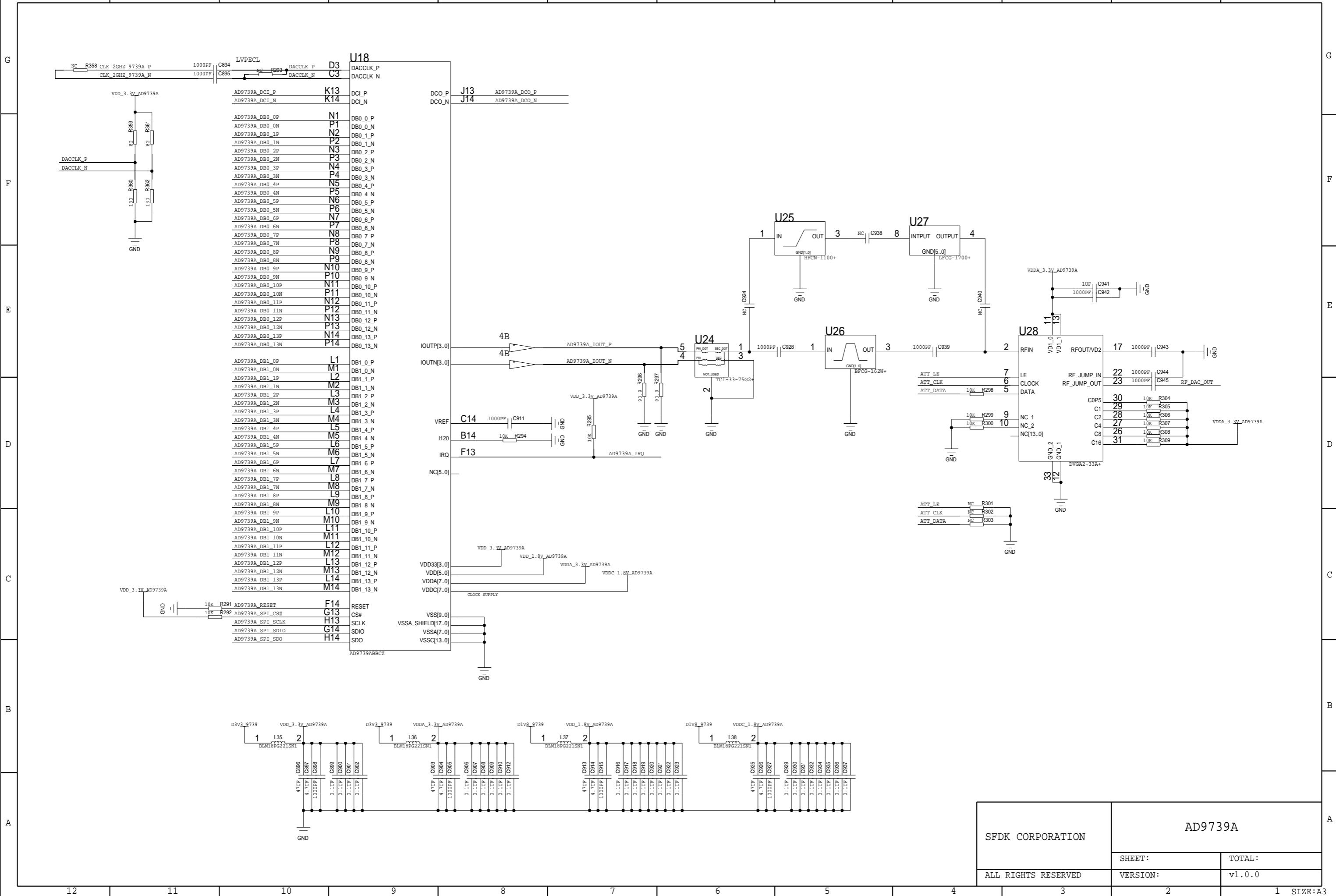




SFDK CORPORATION	AD9689 <2>	
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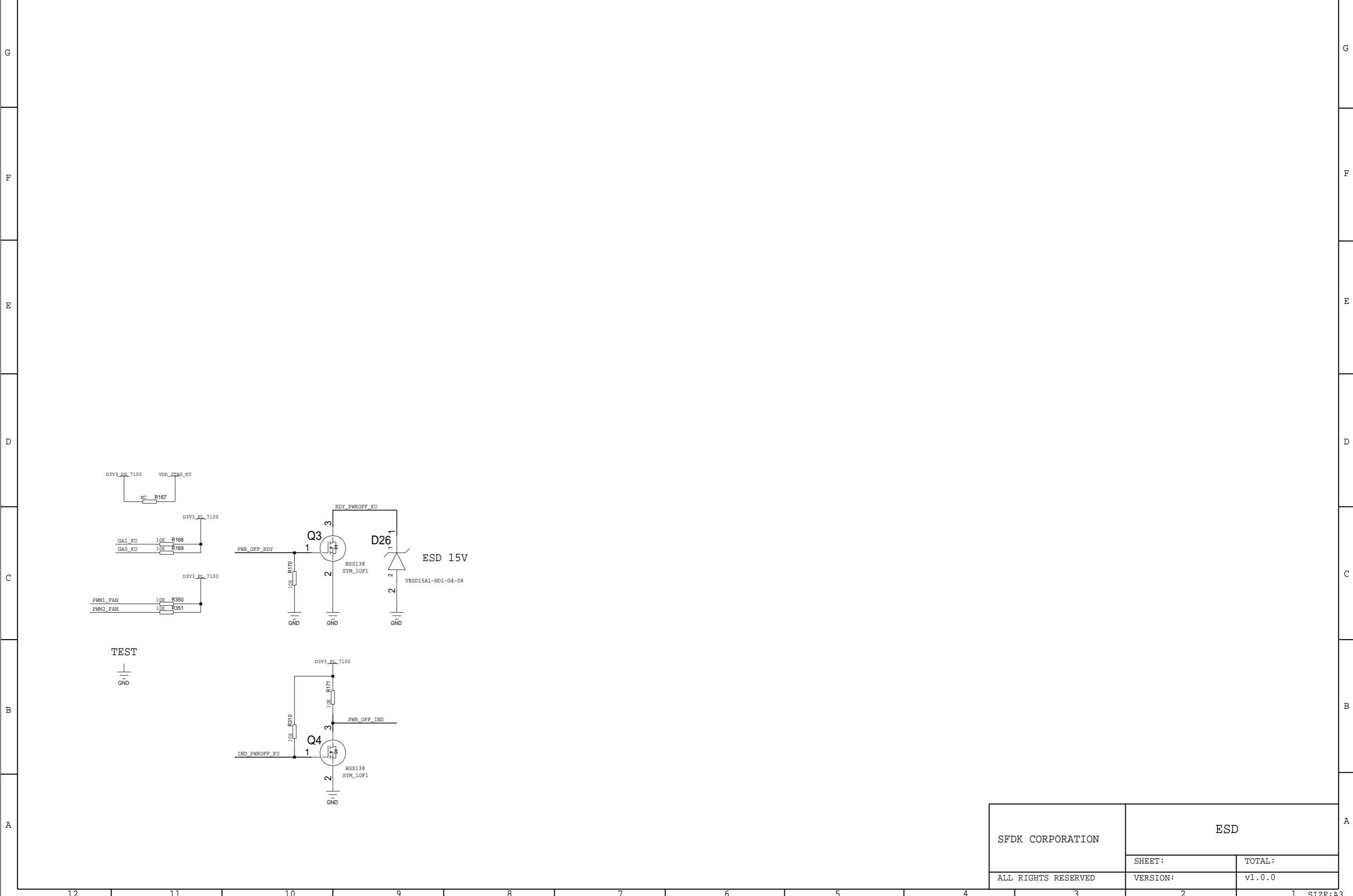


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12 11 10 9 8 7 6 5 4 3 2 1 SIZE:A3

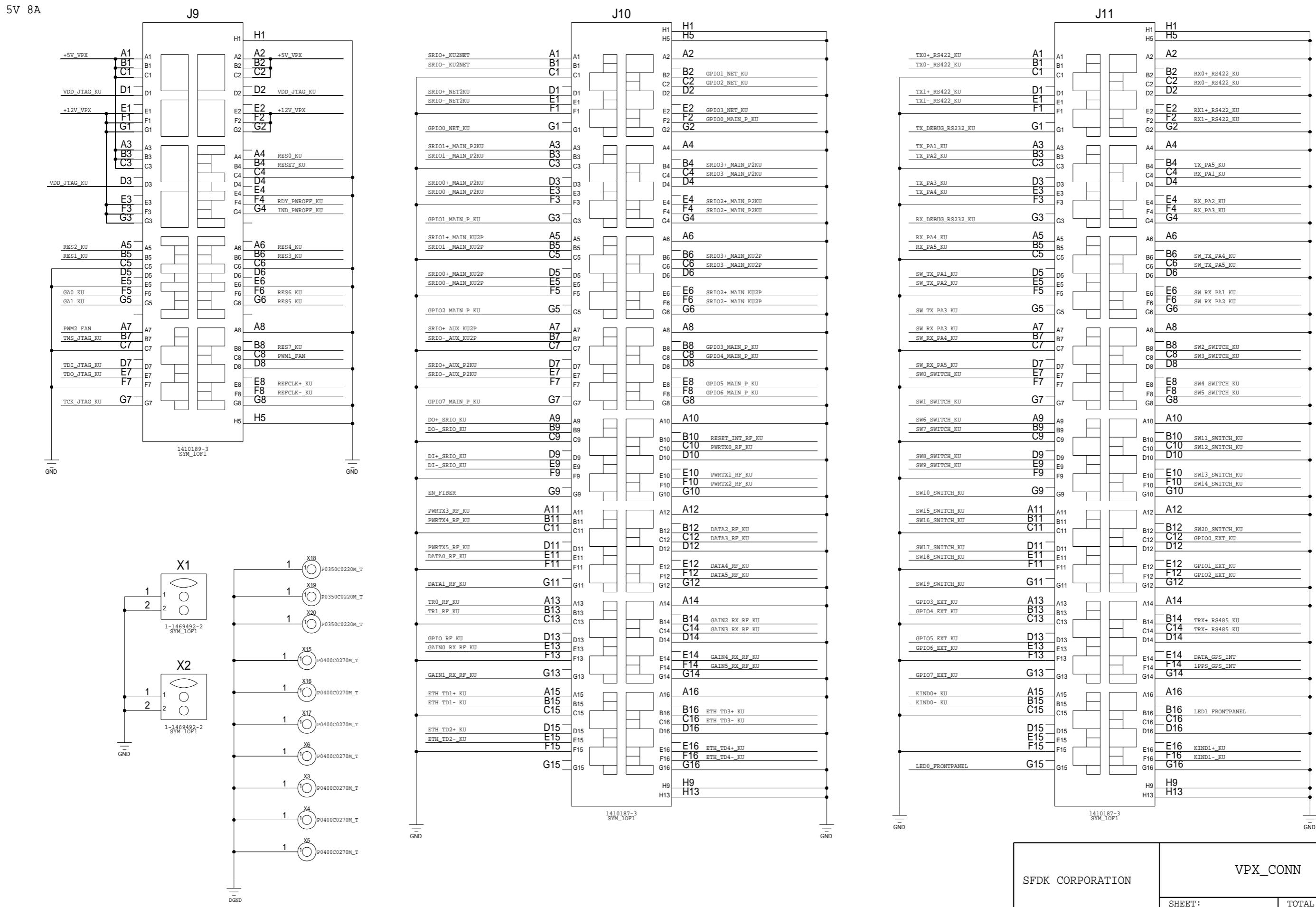
12	11	10	9	8	7	6	5	4	3	2	1
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SFDK CORPORATION	ESD	
SHEET:	TOTAL:	
ALL RIGHTS RESERVED	VERSION:	v1.0.0

12	11	10	9	8	7	6	5	4	3	2	1 SIZE:A3
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12 11 10 9 8 7 6 5 4 3 2 1



SFSDK CORPORATION

VPX\_CONN

SHEET: TOTAL:

ALL RIGHTS RESERVED VERSION: v1.0.0

12 11 10 9 8 7 6 5 4 3 2 1 SIZE:A3