

# A Graph and Number Theory Based Description Method and Equivalence Judgment of Power Electronics Topology

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**Abstract**—In the study of power electronics topology, the existing graph structure description methods cannot comprehensively manifest properties of topologies, leading to difficulties in their equivalence judgment. To address this issue, this article proposes a novel power electronics topology description method based on the fusion of graph and number theory. First, prime number weights are assigned to represent physical properties, such as components and connections. Then, the fundamental theorem of arithmetic and bijection functions are used to map the topology into a unique, concise, and reversible graph form with physical properties. Therefore, power electronics topology equivalence judgment can be conducted straightforwardly based on graph isomorphism. The proposed method effectively simplifies physical topology descriptions and related equivalence judgment. Case studies demonstrate the proposed method’s effectiveness.

**Index Terms**—Equivalence judgment, graph theory, number theory, topology description.

## I. INTRODUCTION

AS POWER electronics technology continues to advance, the utilization of power electronic topologies is steadily expanding across various industries [1]. To address the diverse demands of these industries, researchers have introduced numerous novel power electronic converter topologies [2]. Owing to factors like researchers’ preferences and established practices, a single power electronic topology may exhibit various configurations, potentially leading to misidentification as distinct topologies. Consequently, even though the analysis of topologies are important in research, the identification of equivalent power electronic converters has garnered substantial attention.

Meanwhile, the computer-aided derivation methods [3], [4], [5] and AI-based generation methods [6], [7], [8] mark the coming of a new era of power electronics topologies. Myriads of

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power electronic topologies can be generated by these methods rapidly. For example, hundreds of topologies may be generated in a few seconds by these programmable methods [3], [9], [10]. Obviously, more interests are on the novel topologies. Therefore, both in the computer-aided and AI based methods, filtering duplicate topologies plays an important role in the efficient study. Besides, during the every epoch in the process of the training of AI, more than hundreds of topologies may be generated [6], [8]. With the purpose of training the AI to generate topologies without repetition, a quick comparison of generated topologies is needed to give penalty to the redundant results. As a result, the swift comparison and analysis of these novel structures have become a central focus of research, creating a pressing need for a method capable of efficiently handling substantial volumes of data to ascertain the equivalence of power electronic topologies.

However, traditionally, the identification of power electronic converters has been predominantly a manual process [11], characterized by its inherent drawbacks of being time-consuming and error-prone. This significantly hampers the efficiency of power electronic converter identification [3]. Meanwhile, intrinsic physical properties embedded within certain power electronics topologies can render sole reliance on graph-theoretic depiction methods insufficient in capturing their true physical essence. Even the equivalent topologies may manifest in distinct mathematical forms rather than a uniform form, thereby impeding the comprehensive study of these topologies [3], [5]. For example, the order of the nodes of the topologies, the arrangement order of the components in the series circuit and many other connections may manifest in different forms even though they may be indeed the same or equivalent topologies. These discrepancies lead to the traditional mathematical representations, such as connection matrix, being different, which obviously impedes the efficient study of power electronics topologies.

Given the absence of a standardized topology depiction, designing specific algorithms for equivalence assessment has become a norm. Examples encompass the application of the depth-first search technique to detect loops within power electronics topologies for equivalence determination [12]. If the loops in two topologies are same, the two topologies are considered equivalent. While these approaches partially alleviate intricacies in specific topology investigations, the substantial investment required for designing new methodologies persists. Moreover,

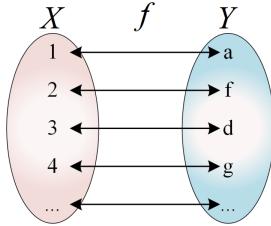


Fig. 1. Bijective function.

such techniques often lack broad applicability and, in certain instances, rigorous mathematical underpinnings.

To attain consistent depictions of equivalent power electronics topologies and address the aforementioned challenges, this article introduces a novel topology description approach, stemming from the fusion of graph theory [13], [14], [15] and number theory [16], [17], [18]. Through the integration of physical attributes into the mathematical portrayal, a standardized and more succinct topology depiction emerges, proficiently encapsulating the physical essence of topologies.

In this article, the study commences by delineating the parallels and distinctions between graph theory and the exploration of particular power electronics structures. Subsequently, the proposed power electronics topologies description method is introduced. Moreover, uniqueness, reversibility, and compatibility of the proposed method are validated. Instances of the utilization of graph isomorphism to judge topology equivalence are also presented. These illustrative case studies underscore that our approach not only facilitates a unified and more streamlined power electronics topology depiction, but also establishes a framework encompassing number theory, graph theory, and physical properties.

## II. PRELIMINARIES

### A. Basic Concepts About Number Theory

Number theory is a branch of mathematics that deals with the properties and relationships of numbers, particularly integers. In this article, the Fundamental Theorem of Arithmetic [16] and bijective functions [17], which are two essential parts in number theory are utilized.

The Fundamental Theorem of Arithmetic states that every positive integer greater than 1 can be uniquely expressed as a product of prime numbers, up to the order of the factors. In other words, the prime factorization of a number is unique. For example, the number 12 can be expressed as  $2^2 \times 3^1$  and this representation is unique. More related concepts will be illustrated in Section IV-A.

A bijective function, also known as a bijection, is a type of function between two sets where each element in the domain is paired with a unique element in the codomain, and every element in the codomain is the image of exactly one element in the domain. Bijective functions are fundamental in number theory for establishing one-to-one correspondences between sets of numbers. Fig. 1 shows a bijective function  $f$  mapping elements in set  $X$  to set  $Y$ .

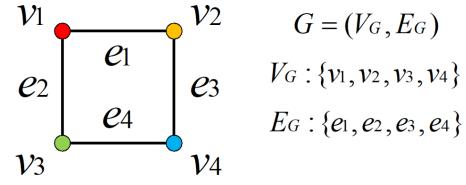


Fig. 2. Brief graph example.

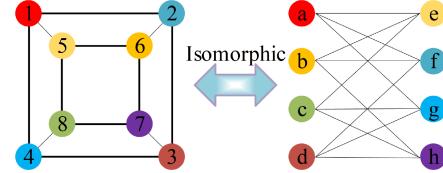


Fig. 3. Graph isomorphism.

### B. Basic Concepts About Graph Theory

Graph theory is a branch of mathematics that studies graphs. In graph theory, define graph  $G = (V_G, E_G)$ , where  $V_G$  represents the set of vertexes and  $E_G$  represents the set of edges [19], [14]. Such a structure is often used to represent a specific type of relationship between certain objects, with vertices representing the objects and edges representing the relationships between them. Fig. 2 shows a brief graph example  $G$ , which consists of four vertexes and edges.

Graph isomorphism is an important part of graph theory, which deals with the structural similarity between two graphs. If two graphs are isomorphic, their structures must be precisely identical. This entails a one-to-one correspondence between the vertices and edges of the two graphs, ensuring they are interconnected in an equivalent manner [20], [21]. Graph isomorphism is often used to judge whether two complex graphs match. Fig. 3 shows two graphs, where different types of vertexes are connected with edges. Colors are used to represent the types of the vertexes. For convenience, number "1,2,3..." and alphabet "a,b,c..." are assigned to represent each vertex in the two graphs, respectively. As shown in Fig. 3, it is difficult to manually identify that the two graphs have the same structure. But they are graph isomorphic since there is a bijective relationship between them, and the bijective transformation can be found:  $\mathcal{M} : \{\mathcal{M}(1) = a, \mathcal{M}(2) = f, \mathcal{M}(3) = d, \mathcal{M}(4) = g, \mathcal{M}(5) = e, \mathcal{M}(6) = b, \mathcal{M}(7) = h, \mathcal{M}(8) = c\}$ .

### C. Conflict Between Existing Graph Descriptions and Power Electronics Topology Representations

In existing graph descriptions of power electronics topologies, both assigning numbers to edges and marking edges with colors are usually utilized to distinguish the different components or connection relationships [22], [15]. When facing new components or connections, new numbers or colors will be assigned. However, some structures have their specific physical meanings, which means only assigning new numbers to represent them may be unable to express their whole inner properties. Even worse,

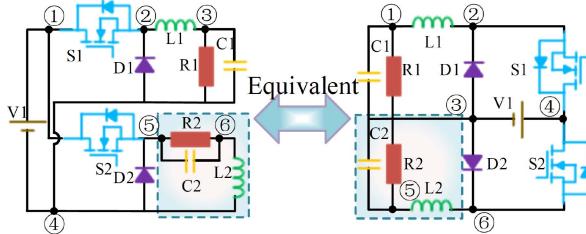


Fig. 4. Equivalent power electronics topologies.

in some situations, some physically equivalent topologies will be described in different forms by existing graph expression.

Fig. 4 illustrates two distinct representations of the single-inductor dual-output buck circuit. The absence of a standardized method for topology description results in the equivalent topologies being depicted in various forms, potentially leading to recognizing the two equivalent topologies as different ones. Meanwhile, it should be noted that the arrangement sequence of inductor  $L_2$ , capacitor  $C_2$ , and resistor  $R_2$  varies in each topology, as depicted in Fig. 4. Even though the different arrangements yield equivalent physical properties, the resulting graphs, or in other words, the mathematical presentations of the topologies, are not identical.

The distinct descriptions of the same or physically equivalent topology obscure further studies. To distinguish whether these two topologies are equivalent is to find out whether there is a certain correspondence that makes the two topologies match. In graph theory, the process of identifying graph isomorphism is very similar to the process of identifying whether two topologies are equivalent.

While there are resemblances in assessing topology equivalence and graph isomorphism, distinct variations also exist. Graph isomorphism underscores the stringent requirement for a strict one-to-one correspondence between all vertices, edges, and connection methods in both graphs. Nevertheless, due to the absence of uniform topology descriptions, the practical occurrence of equivalent topologies being expressed differently is common. Besides, the complete identity of topologies is only a necessary condition for establishing topological equivalence. In evaluating the equivalence of topological structures, the incorporation of supplementary factors, including scrutiny of physical properties, is paramount [12].

While graph theoretic methods, such as graph isomorphism, offer the potential for effectively tackling specific topological research challenges, the constraints inherent in the current topological description approach impede the direct application of these established and effective graph theoretic methods to specific topology investigations.

### III. GRAPH AND NUMBER THEORY BASED DESCRIPTION METHOD FOR POWER ELECTRONICS TOPOLOGIES

#### A. Fusion of Topology, Graph Theory, and Number Theory

To address the aforementioned challenges, this study presents an innovative approach that merges graph theory with number

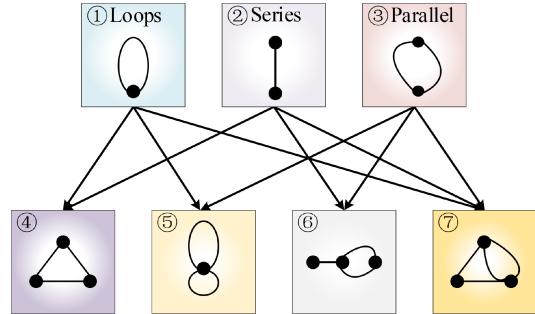


Fig. 5. Common connections in graphs.

theory to depict power electronics topologies. The fundamental concept behind this methodology involves assigning distinct prime values to represent the specific physical properties of structures. This enables the attainment of standardized and more concise depictions of power electronics topologies.

Before delving into the specifics of the proposed methods, it is essential to provide an overview of the fundamental connections within traditional graph structures. As shown in Fig. 5, there are three primary types of connections: loops, series, and parallel connections. Loop involves an edge that both originates and terminates at the same node, often referred to as a self-loop node. Series connections entail edges linked sequentially. In the case of multiple edges in series, the intermediate nodes between the edges must possess a degree of 2. Parallel connections denote the linkage of multiple edges between two nodes. Based on any combination of three basic connections, Fig. 5 illustrates some prevalent structures.

The purpose of our approach is to simplify and compress the information in the graphs, describing them as simple as possible while ensuring that the physical information is not corrupted. Clearly, it is anticipated that equivalent structures will possess identical and distinct representations. Hence, the uniqueness of prime values is harnessed. Through the assignment of prime values and the application of bijective functions, particular structures will acquire unique values for representation.

The method starts with the fundamental components and connections within topologies. First, the physical topology is delineated based on the original definitions of vertices and edges [3], [23]. Number theory is subsequently incorporated into the graph representations. Prime values are assigned to symbolize the components and fundamental connection relationships. The description then advances to simplify structures guided by their physical attributes, exemplified by certain structures in Fig. 5. Table I shows the symbols and their meanings used in establishing the rules.

In our investigation, we focus on power electronics topologies usually described with weighted directed graphs. Define a basic component or primary connection relationship  $|b_i| \in B$  and assign a prime weight  $|b_i| = p_i$  to it, where  $p_i \in P$  and  $2 < p_1 < p_2 < \dots < p_i < \dots < p_n$ . The products of prime numbers in the paper are written in the form of multiplication by prime factors. Meanwhile,  $[x', y'] = \mathcal{F}(x, y)$  is utilized to represent the bijective mappings.  $\mathcal{F}$  is used to map two-tuples  $(x, y)$  to

TABLE I  
SYMBOLS USED IN THIS ARTICLE AND THEIR MEANINGS

Symbols	Meaning
$b$	Basic components and connection relationships
$B$	Set of basic components and connection relationships $b$
$p$	Prime numbers
$P$	Set of prime numbers $p$
$  $	Encoded value (operator to assign a prime)
$S \rightarrow T$	Direction from endpoint $S$ to endpoint $T$
$CS_{S \rightarrow T}$	Coding value in the $S \rightarrow T$ direction of structures
$C_{S \rightarrow T}$	A collection of components connected in parallel in the direction $S \rightarrow T$
$D_{S \rightarrow T}$	A collection of components connected in series in the direction of branch $S \rightarrow T$
$\mathcal{F}$	The bijective function that maps to new prime values

new prime pair  $[x', y']$  and the mapping functions can be saved in computers similar to lookup table. Thus, the rules to describe the three kinds of connections are shown as follows:

- 1) *Rules for Parallel Connections*: For parallel connections, the combination of two prime values is given to represent them. The mapping function used to describe the parallel connections is as follows:

$$\begin{aligned} & [|CS|_{S \rightarrow T}, |CS|_{T \rightarrow S}] \\ &= \mathcal{F} \left( \prod_{b_i \in C_{S \rightarrow T}} |b_i|, \prod_{b_i \in C_{T \rightarrow S}} |b_i| \right) \end{aligned} \quad (1)$$

where  $|CS|_{S \rightarrow T}$  and  $|CS|_{T \rightarrow S}$  are the new prime weighted values of the parallel connection after mapping, from  $S \rightarrow T$  direction and  $T \rightarrow S$  direction, respectively. The combination of two prime values is essential for portraying information in opposite directions within a directed graph.

- 2) *Rules for Series Connections*: For series connections, number 2 is utilized to represent the series connection relationship, and the mapping is changed as

$$\begin{aligned} & [|CS|_{S \rightarrow T}, |CS|_{T \rightarrow S}] \\ &= \mathcal{F} \left( 2 * \prod_{b_i \in D_{S \rightarrow T}} |b_i|, 2 * \prod_{b_i \in D_{T \rightarrow S}} |b_i| \right). \end{aligned} \quad (2)$$

- 3) *Rules for Loop Connections*: Loop structures are a little different from parallel and series connections. Both parallel and series connections have two endpoints  $S$  and  $T$ . However, loops usually obtain only a single endpoint. Meanwhile, loop structures can be classified into two categories: parallel connected into loops and series connected into loops as shown in Fig. 5 ⑤ and ④, respectively. The former one can be described according to the rules for parallel connection while the other one is for series

### Algorithm 1: Graph and Number Theory Based Description Methods.

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Input: Traditional graphs of topologies  $G$  and prime numbers of basic components
Output: Simplest graphic descriptions of topologies
1: Initialize the graphs and the list of bijection mapping functions
2: Assign prime values weights to basic components in traditional graphs of topologies
3: for Structures can be simplified do
4:   Use Rules proposed in Chapter III-A to obtain new prime values
5:   Update the graphic representations and the list of mapping functions
6: end for

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connections. The only difference is the two endpoints  $S$  and  $T$  are the same endpoint in loops.

In the rules for the three connections, these structures are represented through the product of prime numbers by leveraging the fundamental theorem of arithmetic. Following by employing bijective functions, the resulting product values are mapped into new prime numbers. Consequently, the physical information of the original structures becomes compressed, represented by the newly obtained prime values weighted edges. These edges can be viewed as new components, further facilitating the simplification and compression of topological information of structures. The process continues until no additional physical structures can be combined or simplified based on the physical properties of the topology. Ultimately, the topologies are described in their simplified and unique graph representations, encapsulating their distinct physical properties.

By incorporating number theory into the conventional graph theory framework, the proposed method achieves a simple and unified representation of topological structures. This approach facilitates the seamless integration of graph theory, number theory, and specific topology. The overall concept and methodology of this approach are illustrated in Fig. 6. And the pseudocode of the proposed method is shown in Algorithm 1.

Obviously, except for structures that have been mentioned in Fig. 5, there exist other more complicated structures. These structures can be divided into irreducible structures or structures with unknown physical properties, the description rules of which need to be added accordingly to the specific physical properties.

For a better understanding of the proposed method, cases of power electronics circuits will be introduced in detail.

#### B. New Description Methods in Power Electronics Topologies

Power electronics topologies are usually described in directed graph forms. Beginning with the basic components and nodes, the circuit's basic components are depicted as edges with prime values, while the circuit nodes correspond to the graph nodes. The weighted values assigned to the resistor, inductor, capacitor, switch, diode, and voltage source are 3, 5, 7, 11, 13, and 17, respectively. Resistors, inductors, capacitors,

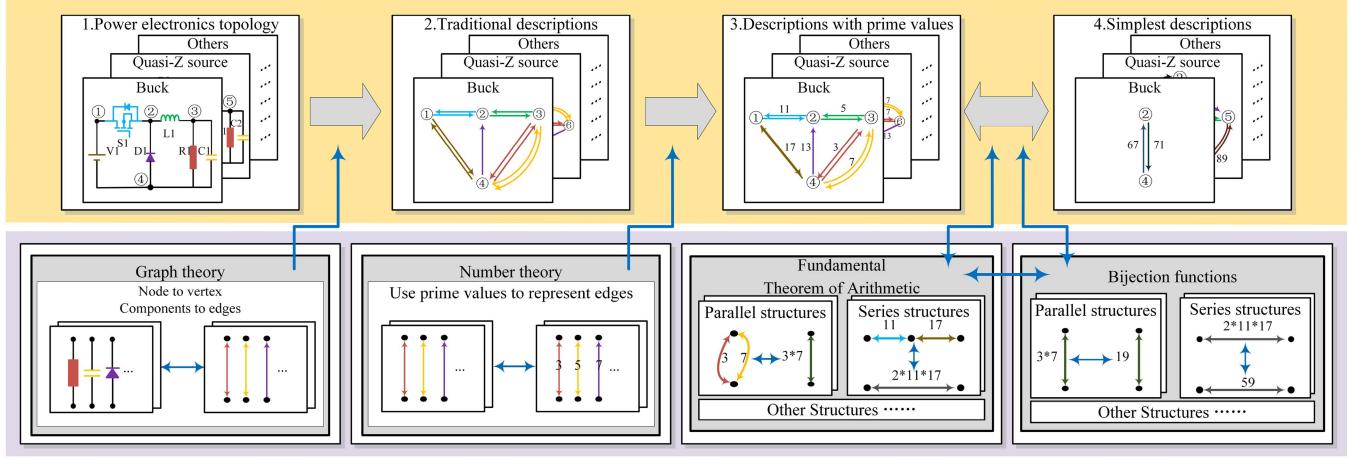


Fig. 6. Main structure of the proposed method.

TABLE II  
CODING OF BASIC COMPONENTS, PARALLEL CIRCUITS AND SERIES CIRCUITS

	Physical circuits	Encoding	Mapping Function	Mapping Result
(a)	R	3	N/A	
	L	5	N/A	
	C	7	N/A	
	S	11	N/A	
	D	13	N/A	
	V	17	N/A	
(b)	C    R	$3 * 7$	$[19, 19] = \mathcal{F}_{p1}(3 * 7, 3 * 7)$	
	D    R	$3 * 13$	$[23, 29] = \mathcal{F}_{p2}(3 * 13, 3)$	
	C    (S    D)	$7 * 11 * 13$	$[41, 43] = \mathcal{F}_{p3}(7 * 11, 7 * 11 * 13)$	
(c)	R    C    D	$2 * 3 * 7 * 13$	$[31, 37] = \mathcal{F}_{s1}(2 * 3 * 7 * 13, 2 * 3 * 7)$	
	V    S    L	$2 * 11 * 17$	$[59, 59] = \mathcal{F}_{s2}(2 * 11 * 17, 2 * 11 * 17)$	
	V    L    C	$2 * 5 * 17$	$[83, 83] = \mathcal{F}_{s3}(2 * 5 * 17, 2 * 5 * 17)$	

switches, and voltage sources are categorized as undirected components, represented by two edges with equal prime weights but opposing directions. Conversely, diodes are referred to as directed components and are depicted by unidirectional edges with prime-weighted values. Once the directions of the directed components and nodes are determined, the placement of the components can also be established. The depictions of the basic components are illustrated in Table II(a). Fig. 7 shows the

expression of a buck circuit described with weighted directed graph form, where the voltage source, switch, inductor, capacitor, and diode are denoted as  $V, S, L, C$ , and  $D$ , respectively.

After assigning prime values to represent basic components, the graph expressions are processed to simplify. It should be noted that the different orders of the simplification actually may yield discrepant simplified results. Therefore, to ensure standardized expressions, the order in which the structures are

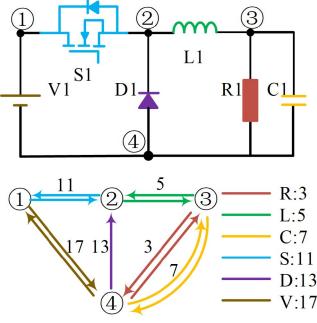


Fig. 7. Buck circuit topology and its directed graph expression with prime values weighted edges.

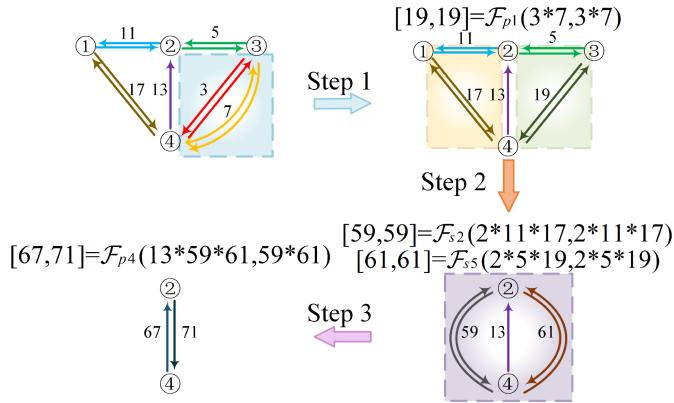
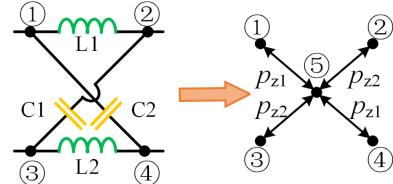


Fig. 8. Implementation process of encoding and simplification of Buck circuits.

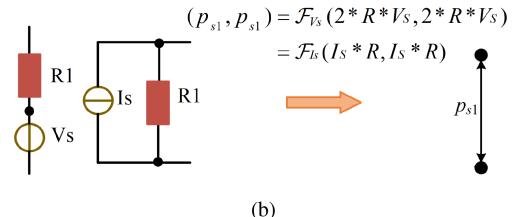
simplified needs to be harmonized. In each step of the simplification, parallel structures are first simplified, then the series structures are dealt with. Prior to proceeding with additional simplification, it is essential to verify whether the simplification of series structures has given rise to any parallel structures. In the event of such occurrences, the simplification process should revert to its initial step to deal with parallel structures. Only after addressing both parallel and series structures should the simplification extend to loop structures. It is important to note that the specified order is tailored for this article; however, in practical applications, alternative orders are permissible, provided that consistency in the simplification order is maintained.

Based on the proposed rules, some parallel and series circuits can be expressed and simplified as shown in Table II(b) and (c), respectively. As to the design and implementation of bijective functions, unique prime values and bijective functions are assigned according to the properties of edges. For a pair of edges that have the same weights, only one prime value is needed, such as  $\mathcal{F}_{p1}$  in Table II(b) and  $\mathcal{F}_{s2}$  in Table II(c). When the weights of the pair of edges are different, two prime values are assigned, such as  $\mathcal{F}_{p2}$  in Table II(b) and  $\mathcal{F}_{s1}$  in Table II(c). In general, prime values are utilized from small to large.

The corresponding encoding process of the Buck circuit is shown in Fig. 8. First,  $R_1$  and  $C_1$  in the parallel circuit are replaced by coded values 3 and 7, respectively, and the mapping



(a)



(b)

Fig. 9. Other simplification examples of power electronics topologies. (a) A part of a Z-source circuit; (b) Voltage source and current source.

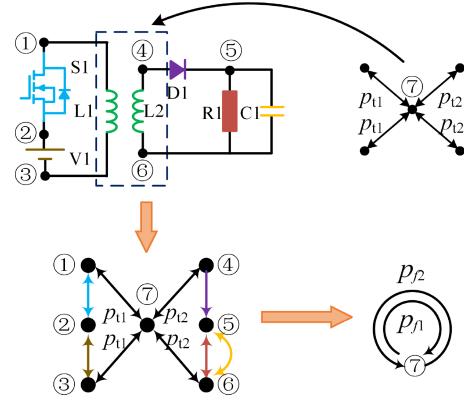


Fig. 10. Flyback circuit.

function  $\mathcal{F}_{p1}$  is established. Next, the series circuits are considered as a whole and the mapping  $\mathcal{F}_{s2}$  and  $\mathcal{F}_{s5}$  are established. After completing Step 2, parallel structures emerge as a result of the simplification of series circuits. Consequently, in accordance with the simplification order outlined in this article, the newly generated parallel structures must undergo further simplification. Establish the mapping function  $\mathcal{F}_{p4}$ , which describes that the diode \$D\_1\$ with code value 13 is connected in parallel with structures represented by prime values 59 and 61. After this step, the simplest representation of buck circuit is obtained. Fig. 8 shows the final simplified form of the buck circuit. Compared with the original form consisting of 4 nodes and 11 edges, the final simplified form only uses 2 nodes and 2 edges to represent the buck circuit and meanwhile, the whole properties of the circuit are represented by the pair of prime values. Some simplification processes of other basic dc–dc circuits are shown in Fig. 11.

Since the topological information has been compressed in the process, the physically equivalent structures, such as the different placement of components in series connections, will be described uniformly, resulting in the standardized expressions.

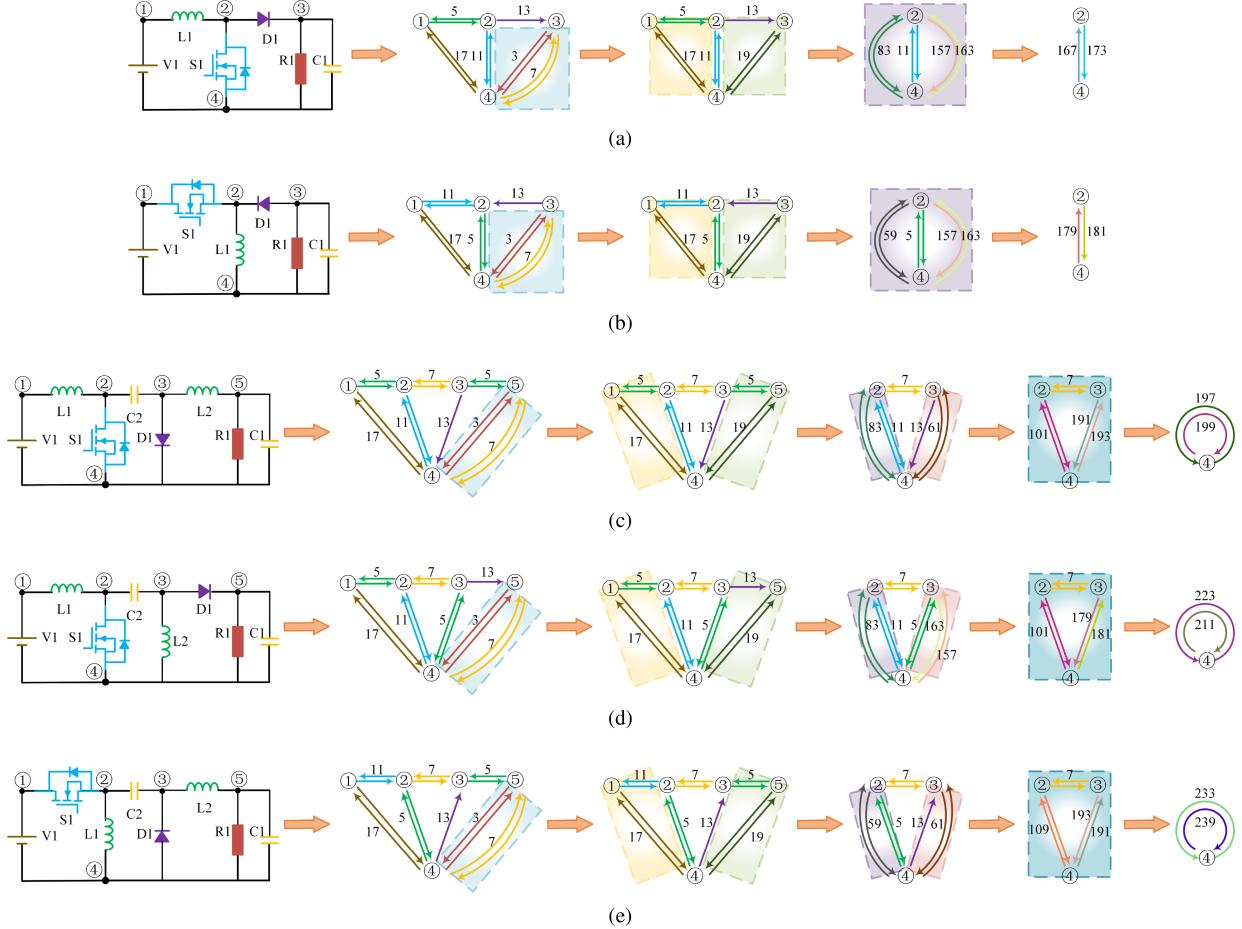


Fig. 11. Some simplification examples of power electronics topologies. (a) Boost; (b) Buck-boost; (c) Cuk; (d) Sepic; (e) Zeta.

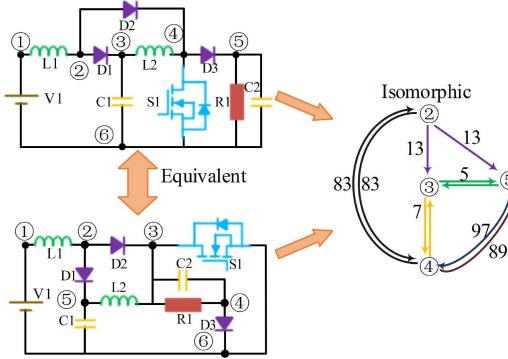


Fig. 12. Two single-tube quasi-Z source boost converters and their simplest forms.

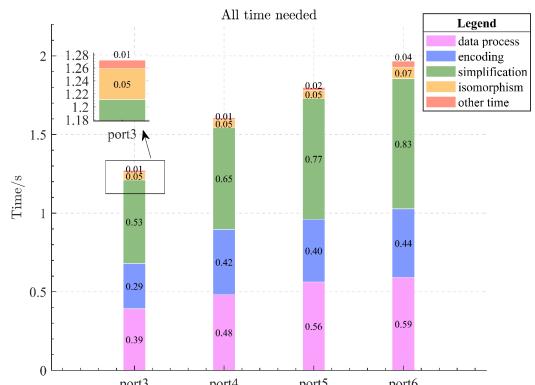


Fig. 13. Time needed for judgment for sets with same number of ports.

When no structures in the circuit can be further combined and simplified by rules and the physical properties of circuits, the simplest and uniform diagram form of the circuit is obtained.

*Remark 1:* Obviously, parallel and series circuits are the most common structures in power electronics topologies. Except for parallel and series circuits, there are still irreducible structures and structures with unknown physical properties. The former ones can be considered as irreducible parts in practical

researches while the latter usually imply physical properties that are not determined only by physical connections. Still, take the circuit as an example. A part of the Z-source circuit [24], [25] as shown in Fig. 9(a), is considered an irreducible part of the research. And some unknown physical properties include that current sources and voltage sources are equivalent in some cases [11] shown in Fig. 11(b). Our description method can still

describe these irreducible and unknown structures by incorporating new expression rules. For irreducible structures, these structures are usually unable to be decomposed and obtain multiple latent connection edges. A method similar to the  $\Delta$ -Y conversion can be applied to handle irreducible structures. Transform these irreducible structures into a node connected with multiple prime-weighted edges and the number of prime-weighted edges is equal to the original latent connection edges. Fig. 11(a) shows the transformation of the Z-source circuit. Due to the symmetry of the structure, only two prime numbers are needed to represent the four edges.

As to the structures with unknown physical properties, such as current and voltage sources, a new mapping function can be designed that maps the prime weights used to represent the two structures into equal results as shown in Fig. 11(b).

*Remark 2:* Even though the majority of examples in this article are nonisolated topologies, the proposed method is also capable of handling with isolated power electronic topologies. A flyback circuit is depicted in Fig. 10. The transformer can be considered as an irreducible part. Therefore, the method dealt with irreducible structures can be utilized again, as shown in Fig. 10.  $p_{t1}$  and  $p_{t2}$  are assigned to represent the primary side and the secondary side, respectively. After the simplification, eventually, the flyback circuit can be represented with one self-loop node and two edges weighed  $p_{f1}$  and  $p_{f2}$ , respectively.

Significantly, beyond the instances highlighted in *Remark 1* and *Remark 2*, several other distinct structures exist within power electronic topologies, and the descriptions of these structures are intricately tied to their physical properties. Consequently, a part of these structures and their simplifications are provided here. The precise description rules can be added based on specific requirements.

#### IV. PROPERTIES OF THE PROPOSED DESCRIPTION METHOD

Our description method has three important properties, uniqueness, reversibility, and compatibility.

##### A. Uniqueness

Before proving uniqueness, the fundamental theorem of arithmetic is first introduced.

*Theorem 1* Any natural number  $N$  greater than 1, if  $N$  is not prime, then  $N$  can be uniquely decomposed into the product of a finite number of primes

$$N = p_1^{a_1} p_2^{a_2} p_3^{a_3} \cdots p_n^{a_n} \quad (3)$$

where  $p_1 < p_2 < p_3 < \cdots < p_n$ , and they are all prime numbers, and  $a_i$  is a positive integer. The proof of this theorem is omitted. See reference [16] for details.

Before using bijective functions to map, the codes of structures can be decomposed into a unique product of weights that represent components and connection relationships. Meanwhile, due to the properties of bijection functions, there will be a unique mapping result for an input. Bidirectional edges are used to express the directional components or structures. The encoding method based on the fundamental theorem of arithmetic and

bijection functions ensures the uniqueness of the encoded structures, where each encoding value represents a unique physical meaning and corresponds to a unique structure. Building upon Theorem 1, we propose the self-evident Lemma 1.

*Lemma 1:* If two physical topology structures have the same encoding weight values obtained by the methodology proposed in this article, then these two structures can be considered equivalent and have the same physical meanings.

##### B. Reversibility

Another property of our proposed method is that the method is reversible. The simplified result can be deduced back to its original structure composed solely of elementary components and basic connectivity patterns. Since bijection functions are designed to obtain new prime values, the new prime values can also be converted to the original products by the inverse functions of the bijection functions, which means that the simplified results can be converted to original forms. The reversibility of bijection functions has been proved and utilized in [17], [18], [26]. The reversibility of the proposed method indicates that it can fully encapsulate the physical information of the original topology using fewer nodes and edges. In other words, it effectively achieves lossless compression of the physical information pertaining to the topology. This holds significant implications for the storage and judgement of power electronics topologies.

##### C. Compatibility

As has been mentioned in Section IV-B, the description method achieves lossless expression of the power electronics topologies. This means, even though the description has been changed, the description indeed represents a power electronics topology, which means the existing equivalence judgment methods or algorithms, such as [12] and [11], can still be applied to the novel description for topology equivalence judgement. Meanwhile, since the numbers of edges and nodes needed to represent the topology have been reduced, even by the existing equivalence judgment methods, the efficiency of equivalence judgment can be improved.

#### V. EQUIVALENCE JUDGMENT ALGORITHM BASED ON GRAPH ISOMORPHISM FOR POWER ELECTRONICS TOPOLOGIES

##### A. Basic Concept of the Equivalent Judgment Algorithm

After realizing the simplest and standardized graph representations of physical topology, the fusion of number theory, graph theory, and physical topology is achieved. Some graphical methods that could not be used directly in power electronics topology studies can now be utilized without restriction. Take the problem of equivalence judgment of the topology mentioned above as an example. With the help of our proposed expression method, the problem can be changed into a graph isomorphism problem and easily solved.

To compare whether the structure is equivalent, the power electronics topologies are first simplified by our method, and then use the existing graph isomorphism algorithm to judge. If

TABLE III  
EXAMPLES OF SOME EQUIVALENT AND NONEQUIVALENT POWER ELECTRONICS TOPOLOGIES

No.	I	II	III	IV	V
Original topologies					
Simplified results					
No.	VI	VII	VIII	IX	X
Original topologies					
Simplified results					
No.	XI	XII	XIII	XIV	XV
Original topologies					
Simplified results					

the simplest forms are isomorphic, the two topologies are considered equivalent. To fully understand the process of our proposed topological recognition method, examples of comparison of two power electronics topologies are illustrated in Fig. 12, which shows the topological structure diagram of two single-tube quasi-Z source boost converters illustrated in different forms. After transforming them into their simplest forms, the graph isomorphism algorithm is utilized to judge whether they are equivalent.

### B. Computing Efficiency Test

In order to demonstrate the actual running speed of the proposed method, the judgment examples, which are running using a laptop AMD Ryzen 7 5800H cpu in a MATLAB environment, are designed. Fig. 13 shows the time needed for equivalence judgment in four sets of power electronics topologies, respectively. The four sets of topologies, which are derived from the topology templates in [27], are designed depending on the number of ports. The topologies in the same set share the equal number of components and kinds of components, which means they can be more likely to be mistaken as same topologies manually. Each dataset contains 100 pairs power electronic topologies to be compared, 50 of them are equivalent and 50 are

unequal. In Fig. 13, data process means the time used for loading the original graph forms of topologies, encoding means the time used for obtaining prime values and mapping, simplification represents time for simplification process and isomorphism is the time for using isomorphic algorithm to determine equivalence. All the time is round to 2 decimal places. The major part of time is spent on the simplification process and the time for isomorphism is rather less, which proves the efficiency of utilizing graph isomorphism for power electronics topology equivalence judgement. Meanwhile, the simplification process is not only for equivalence judgement, but also for storage and other uses.

### C. Classification Performance Under Big Volumes of Data

With the widespread use of neural networks in power electronics, the use of AI to generate topologies is becoming a mature technique [6], [7]. It has also become a necessary need to quickly screen out equivalent topologies from Big Data. The method proposed in this article can not only quickly compare whether a pair of topologies is equivalent or not, but also quickly classify equivalent topologies in a large amount of data.

*Case1:* Table III shows some examples of equivalent and nonequivalent physical topologies, which are illustrated in different ways [3], [27]. Conventional methods are only capable of

determining equivalence for a pair of power electronics topologies, or require the information other than the topology itself. However, our method can handle large data volume of power electronics topology equivalence judgments by categorizing topologies according to their simplest forms. By simplifying the topologies to simplest forms, our method allows for rapid identification of the circuits. In some cases, even the naked eye can discern whether the circuit topologies are the equivalent, such as topology II, X, and XIII in Table III. As for other topologies with slightly more complex forms, it is also possible to quickly determine whether the topologies are equivalent by determining whether the simplest forms are isomorphic. In this manner, our proposed method offers an effective approach to efficiently handle equivalence judgement among vast quantities of circuit topologies.

*Case2:* As to the other classification problems, such as in [28], where 40 topologies are classified into 6 cases, our proposed method is also capable of solving the problem more efficiently. By utilizing our method to simplify the 40 topologies, 6 kinds of simplest results are obtained, which are consistent with the 6 cases classified in [28] manually.

#### D. Comparisons and Analysis of the Proposed Method

Compared with traditional topology equivalence recognition methods that rely on manual identification [11] or computer based recognition methods [12], the proposed equivalence recognition method only requires changing the description method of power electronics topologies and can use existing graph isomorphism algorithms for topological equivalence recognition, which helps to reduce workload and improve the efficiency of the recognition. Our description method is not only more general and better mathematically supported, but also compatible with other methods used for determining the equivalence of physical topologies. The number of vertices and edges used to describe topologies is also reduced by the proposed description method. For weighted directed graphs with self-loops that originally have  $n$  non-self-loops nodes and  $k$  self-loops nodes, the number of edges in the simplified graphs should be less than or equal to  $2(C_{n'+k'}^2 + k')$ , where  $n'$  and  $k'$  are the numbers of non-self-loop nodes and self-loop nodes after simplification respectively, and  $n' \leq n$ ,  $k' \leq k$ . Since the proposed equivalence judgment method is based on graph isomorphism, the time and space complexity are also same with the graph isomorphism algorithm. Considering the algorithmic complexity of the graph isomorphism algorithm [13] [usually  $O((n+k)^2)$ ], the reduction of vertices and edges undoubtedly saves the time required to determine equivalence.

## VI. CONCLUSION

This article presents an innovative method for expressing power electronics topologies by combining prime numbers and graph theory. Prime values are assigned to represent physical properties, and the fundamental theorem of arithmetic and bijection functions are employed to compress and simplify the physical information of topologies, resulting in streamlined and standardized expressions. Case studies are employed to illustrate

the simplification processes for power electronics topologies described with directed graphs. Properties including uniqueness, reversibility, and compatibility are also illustrated and proved. Furthermore, a case study employing graph isomorphism to address power electronics topology equivalence showcases how the proposed method effectively facilitate a comprehensive study of power electronics topology.

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