

Topology Derivation Method of DC/DC Converter with Wide Third-order Voltage Conversion Ratio

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Abstract—This paper introduces a method for deducing the topology of a DC/DC converter with wide third-order voltage conversion ratio. Initially, two sets of parameters are proposed to describe the topology based on the volt-second balance equations, and the coefficients of the voltage conversion ratio in terms of these parameters are derived. Subsequently, parameter constraints, such as avoiding input or output disconnection, are proposed to ensure the validity of the converter topology. Finally, a fitness function related to voltage conversion ratio coefficients and parameter constraints is developed. Genetic Algorithm is applied to obtain a solution with optimal parameters, resulting in the optimal converter topology. The methodology is demonstrated by using examples of the third-order boost converter (TOBCT) and the third-order buck converter (TOBCKT). The effectiveness of the proposed method is validated through circuit simulations and experiments, confirming that the designed converter meets the specified voltage conversion ratio requirements.

Index Terms—Third-order DC/DC converter, Topology derivation, Genetic Algorithm

I. INTRODUCTION

WITH the increasing diversity of application scenarios, DC/DC converters with wide gain are widely used in various fields, especially in emerging renewable energy and hybrid applications [1], such as electronic chip power supply technology [2], power management system [3], semiconductor power device circuit [4], natural and circulating gas power sources [5] and automotive fuel cell [6].

Among many design requirements, high-order voltage conversion ratio/voltage gain ($G = V_{out}/V_{in}$) is the most basic requirement to achieve wide gain DC/DC converter [7] [8], and it is also the basic characteristics of DC/DC converter [9]. Therefore, it is particularly necessary to develop a DC/DC converter topology with high voltage conversion ratio.

In [10]–[14], many wide-gain converter topologies have been proposed for 48V/1V direct conversion. However, there is no universal topological derivation method. At present, many studies are devoted to proposing topology derivation methods for high-order DC/DC converters, including cascade method [15], switching unit method [16] [17], and three-level method [18]. In addition, in [19], a three-terminal unit with a coupled inductor is designed to derive a DC/DC converter with high gain. In [20], a new topology is obtained by using a chart to invert the three-terminal converter unit through inversion, input or output flipping operations. However, these

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methods rely on prior knowledge for manual analysis and design, placing high demands on developers.

In order to realize topology derivation systematically and automatically, many new methods have been proposed, such as topology derivation method based on reinforcement learning [21], [22] and topology derivation method based on graph theory [23]. Nevertheless, these methods do not derive the topology based on a specific voltage conversion ratio, and cannot directly obtain a wide-gain converter.

In [24], the voltage conversion ratio is combined with the topology, and a topology synthesis method for reverse derivation based on volt-second balance equations is proposed. The scholar also proposed parameter constraints on the volt-second balance equations and associated de-redundancy methods [25]. However, this method is still limited to second-order converters, and cannot completely solve the topology derivation problem of wide-gain high-order converters. Moreover, this method uses the exhaustive method for analysis and synthesis, and the process is cumbersome and time-consuming. In [26], based on the volt-second balance equations, the four-step method is used to synthesize the circuit topology such as multiplication, addition, and nesting, and to eliminate the input and output pulsating currents. However, this method uses the existing circuit as the topology unit, and cannot essentially obtain an optimal new converter.

In order to solve the aforementioned problems, a converter topology derivation method of third-order voltage conversion ratio based on Genetic Algorithm is proposed in this paper. The main contributions are as follows :

- 1) The volt-second balance equations are represented by two sets of parameters, illustrating the relationships among the connections within the converter topology.
- 2) A relationship is derived between the parameters of the volt-second balance equations and the coefficients of the voltage conversion ratio for the third-order converter.
- 3) Parameter constraints are introduced to ensure the validity of the derived topologies and prevent the creation of invalid configurations.
- 4) Genetic Algorithm is employed to improve the parameter solving process, efficiently achieving the optimal converter topology with fast speed.

The rest of this paper is organized as follows. In Section II, the basic assumptions of this paper and the parameter combination expression based on the volt-second balance equations are proposed. In Section III, a parameter solving method based on Genetic Algorithm is proposed. In Section IV, the third-order boost converter and the third-order buck

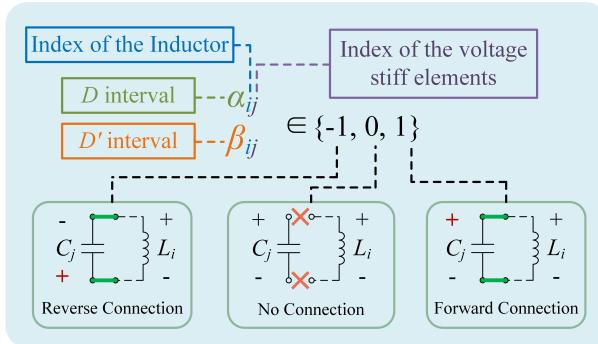


Fig. 1. Topology related parameters α_{ij} and β_{ij} .

converter are derived by the proposed method. In section V, the proposed converter is simulated and verified by experiments. Finally, Section VI concludes this paper.

II. BASIC ASSUMPTIONS AND PARAMETER SOLUTION

A. Basic assumptions

The following basic assumptions are made throughout the entire text:

- 1) All circuit elements are considered ideal. The parasitic resistance of the elements and the forward voltage drop of the diodes are not considered.
- 2) There is only one input voltage (V_{in}) and one control variable (D).
- 3) The order of a converter is defined as the number of LC pairs in the topology [24].
- 4) The switching frequency (F_s) is much higher than the LC resonant frequency.
- 5) The switching period ($T_s = 1/F_s$) is divided into two interval DT_s and $(1-D)T_s$. It means that the topology has only 2-state operation.

B. Volt-second balance equations and the general form of voltage conversion ratio

According to the third basic assumption, for a third-order converter, there are three pairs of LC in the topology, defined as L_1, L_2, L_3 and C_1, C_2, C_3 , respectively.

The principle of inductor volt-second balance serves as a vital tool for the steady-state analysis of DC/DC converters. During the time intervals D and D' (where $D = 1 - D'$), the voltage across the inductor can be expressed as a linear combination of the input voltage (V_{in}) and the capacitor voltages ($V_{C_1}, V_{C_2}, V_{C_3}$).

In this paper, we propose two sets of parameters (α_{ij}, β_{ij}) that can characterize the component connectivity relationship of the converter topology to generalize the volt-second balance equations as shown in Fig. 1. The properties of these parameters (α_{ij}, β_{ij}) are summarized as follows. The parameters α and β correspond to the D and D' intervals, respectively. The subscript parameters i and j pertain to the inductor and the voltage regulator, respectively. Specifically, $i = 1, 2, 3$ represent L_1, L_2 , and L_3 , while $j = 0, 1, 2, 3$ represent V_{in}, V_{C_1}, V_{C_2} and V_{C_3} , respectively. The values of

the parameters (α_{ij}, β_{ij}) are selected from the set $\{-1, 0, 1\}$ based on the circuit conditions. For instance, $\alpha_{10} = 1$ denotes the connection between V_{in} and L_1 during the D interval, with the polarity matching the assumed reference voltage polarity. On the other hand, $\beta_{22} = 0$ indicates that V_{C_2} does not appear on the inductor L_2 during the D' interval. Moreover, $\alpha_{33} = -1$ denotes the connection between V_{C_3} and L_3 during the D interval, with the polarity being opposite to the assumed reference voltage polarity.

For a third-order converter, the general form of the volt-second balance equations for the inductors can be expressed as follows:

$$\langle V_{L_1} \rangle_{T_s} = (\alpha_{10}V_{in} + \alpha_{11}V_{C_1} + \alpha_{12}V_{C_2} + \alpha_{13}V_{C_3})D + (\beta_{10}V_{in} + \beta_{11}V_{C_1} + \beta_{12}V_{C_2} + \beta_{13}V_{C_3})D' = 0 \quad (1)$$

$$\langle V_{L_2} \rangle_{T_s} = (\alpha_{20}V_{in} + \alpha_{21}V_{C_1} + \alpha_{22}V_{C_2} + \alpha_{23}V_{C_3})D + (\beta_{20}V_{in} + \beta_{21}V_{C_1} + \beta_{22}V_{C_2} + \beta_{23}V_{C_3})D' = 0 \quad (2)$$

$$\langle V_{L_3} \rangle_{T_s} = (\alpha_{30}V_{in} + \alpha_{31}V_{C_1} + \alpha_{32}V_{C_2} + \alpha_{33}V_{C_3})D + (\beta_{30}V_{in} + \beta_{31}V_{C_1} + \beta_{32}V_{C_2} + \beta_{33}V_{C_3})D' = 0 \quad (3)$$

In equation (1) - (3), capacitors C_1, C_2 and C_3 are equivalent and can all be considered as converter outputs. For ease of description, the voltage across capacitor C_3 is chosen as the converter output in this paper. Thus, the voltage conversion ratio (G) is defined as the ratio of V_{C_3} to V_{in} . The voltage conversion ratio (G) can be expressed as the ratio of two third-order polynomials of the duty cycle (D), represented as follows:

$$G = \frac{V_{C_3}}{V_{in}} = \frac{N_3D^3 + N_2D^2 + N_1D + N_0}{M_3D^3 + M_2D^2 + M_1D + M_0} \quad (4)$$

where $M_0 \sim M_3$ denote the order coefficients of the denominator and $N_0 \sim N_3$ denote the order coefficients of the numerator. By choosing different values of the coefficients, wide third-order voltage conversion ratio can be obtained.

C. Parameter expression solution

To simplify the parameter expression, define the determinants with three rows and three columns as shown in Fig. 2.

By solving the equation (1), (2), (3) and $D = 1 - D'$, the expressions of $M_0 \sim M_3$ and $N_0 \sim N_3$ with respect to the parameters (α_{ij}, β_{ij}) can be obtained as shown in equation (5). There are a couple of interesting patterns in equations (5). First, the expressions for $M_0 \sim M_3$ and $N_0 \sim N_3$ are very similar. Second, $(A_2, A_3, A_4), (A_5, A_6, A_7), (B_2, B_3, B_4)$, and (B_5, B_6, B_7) don't appear individually, but together in the expressions. Finally, accumulating the expressions of $M_0 \sim M_3$ and $N_0 \sim N_3$ reveals the law of equation (6), which guides the selection of the voltage conversion ratio coefficients.

Through the exhaustion of the parameters (α_{ij}, β_{ij}), the value range that the voltage conversion ratio coefficients should satisfy is shown in equation (7).

If the topology of the third-order DC/DC converter is known, the values of all (α_{ij}, β_{ij}) parameters can be determined based on the operating mode of the circuit topology.

$A_1 = \begin{vmatrix} \beta_{11} & \beta_{12} & \beta_{13} \\ \beta_{21} & \beta_{22} & \beta_{23} \\ \beta_{31} & \beta_{32} & \beta_{33} \end{vmatrix}$	$A_2 = \begin{vmatrix} \alpha_{11} & \alpha_{12} & \alpha_{13} \\ \beta_{21} & \beta_{22} & \beta_{23} \\ \beta_{31} & \beta_{32} & \beta_{33} \end{vmatrix}$	$A_3 = \begin{vmatrix} \beta_{11} & \beta_{12} & \beta_{13} \\ \alpha_{21} & \alpha_{22} & \alpha_{23} \\ \beta_{31} & \beta_{32} & \beta_{33} \end{vmatrix}$	$A_4 = \begin{vmatrix} \beta_{11} & \beta_{12} & \beta_{13} \\ \beta_{21} & \beta_{22} & \beta_{23} \\ \alpha_{31} & \alpha_{32} & \alpha_{33} \end{vmatrix}$
$A_5 = \begin{vmatrix} \alpha_{11} & \alpha_{12} & \alpha_{13} \\ \alpha_{21} & \alpha_{22} & \alpha_{23} \\ \beta_{31} & \beta_{32} & \beta_{33} \end{vmatrix}$	$A_6 = \begin{vmatrix} \alpha_{11} & \alpha_{12} & \alpha_{13} \\ \beta_{21} & \beta_{22} & \beta_{23} \\ \alpha_{31} & \alpha_{32} & \alpha_{33} \end{vmatrix}$	$A_7 = \begin{vmatrix} \beta_{11} & \beta_{12} & \beta_{13} \\ \alpha_{21} & \alpha_{22} & \alpha_{23} \\ \alpha_{31} & \alpha_{32} & \alpha_{33} \end{vmatrix}$	$A_8 = \begin{vmatrix} \alpha_{11} & \alpha_{12} & \alpha_{13} \\ \alpha_{21} & \alpha_{22} & \alpha_{23} \\ \alpha_{31} & \alpha_{32} & \alpha_{33} \end{vmatrix}$
$B_1 = \begin{vmatrix} \beta_{10} & \beta_{11} & \beta_{12} \\ \beta_{20} & \beta_{21} & \beta_{22} \\ \beta_{30} & \beta_{31} & \beta_{32} \end{vmatrix}$	$B_2 = \begin{vmatrix} \alpha_{10} & \alpha_{11} & \alpha_{12} \\ \beta_{20} & \beta_{21} & \beta_{22} \\ \beta_{30} & \beta_{31} & \beta_{32} \end{vmatrix}$	$B_3 = \begin{vmatrix} \beta_{10} & \beta_{11} & \beta_{12} \\ \alpha_{20} & \alpha_{21} & \alpha_{22} \\ \beta_{30} & \beta_{31} & \beta_{32} \end{vmatrix}$	$B_4 = \begin{vmatrix} \beta_{10} & \beta_{11} & \beta_{12} \\ \beta_{20} & \beta_{21} & \beta_{22} \\ \alpha_{30} & \alpha_{31} & \alpha_{32} \end{vmatrix}$
$B_5 = \begin{vmatrix} \alpha_{10} & \alpha_{11} & \alpha_{12} \\ \alpha_{20} & \alpha_{21} & \alpha_{22} \\ \beta_{30} & \beta_{31} & \beta_{32} \end{vmatrix}$	$B_6 = \begin{vmatrix} \alpha_{10} & \alpha_{11} & \alpha_{12} \\ \beta_{20} & \beta_{21} & \beta_{22} \\ \alpha_{30} & \alpha_{31} & \alpha_{32} \end{vmatrix}$	$B_7 = \begin{vmatrix} \beta_{10} & \beta_{11} & \beta_{12} \\ \alpha_{20} & \alpha_{21} & \alpha_{22} \\ \alpha_{30} & \alpha_{31} & \alpha_{32} \end{vmatrix}$	$B_8 = \begin{vmatrix} \alpha_{10} & \alpha_{11} & \alpha_{12} \\ \alpha_{20} & \alpha_{21} & \alpha_{22} \\ \alpha_{30} & \alpha_{31} & \alpha_{32} \end{vmatrix}$

Fig. 2. Parameter determinant of the equation (5).

Subsequently, $M_0 \sim M_3$ and $N_0 \sim N_3$ can be calculated using the equation (5). By substituting the values of $M_0 \sim M_3$ and $N_0 \sim N_3$ into formula (4), the expression for the voltage conversion ratio can be obtained.

$$\left\{ \begin{array}{l} M_0 = A_1 \\ M_1 = A_2 + A_3 + A_4 - 3A_1 \\ M_2 = A_5 + A_6 + A_7 \\ \quad - 2(A_2 + A_3 + A_4) + 3A_1 \\ M_3 = A_8 - (A_5 + A_6 + A_7) \\ \quad + (A_2 + A_3 + A_4) - A_1 \\ N_0 = -B_1 \\ N_1 = -(B_2 + B_3 + B_4) + 3B_1 \\ N_2 = -(B_5 + B_6 + B_7) \\ \quad + 2(B_2 + B_3 + B_4) - 3B_1 \\ N_3 = -B_8 + (B_5 + B_6 + B_7) \\ \quad - (B_2 + B_3 + B_4) + B_1 \end{array} \right. \quad (5)$$

$$\left\{ \begin{array}{l} M_0 + M_1 + M_2 + M_3 = A_8 \\ N_0 + N_1 + N_2 + N_3 = -B_8 \end{array} \right. \quad (6)$$

$$\left\{ \begin{array}{l} M_0 \in \{-2, -1, 0, 1, 2\} \\ M_1 \in \{i \mid i \in \mathbb{Z}, -13 \leq i \leq 13\} \\ M_2 \in \{i \mid i \in \mathbb{Z}, -26 \leq i \leq 26, i \neq \pm 25\} \\ M_3 \in \{i \mid i \in \mathbb{Z}, -16 \leq i \leq 16, i \neq \pm 15\} \\ N_0 \in \{-2, -1, 0, 1, 2\} \\ N_1 \in \{i \mid i \in \mathbb{Z}, -13 \leq i \leq 13\} \\ N_2 \in \{i \mid i \in \mathbb{Z}, -26 \leq i \leq 26, i \neq \pm 25\} \\ N_3 \in \{i \mid i \in \mathbb{Z}, -16 \leq i \leq 16, i \neq \pm 15\} \end{array} \right. \quad (7)$$

III. TOPOLOGY DERIVATION METHOD AND PARAMETER CONSTRAINTS

A. Overview of the methodology

The focus of this paper is to obtain the optimal converter topology for a given voltage conversion ratio. The object of this paper is the third order converter by solving the 24 unknowns α_{ij} and β_{ij} in the volt-second balance equations of the form equation (5), given the voltage conversion ratio of the form formula (4). The proposed methodology is divided into three steps as shown in Fig. 3.

- In Step1, the corresponding $M_0 \sim M_3$ and $N_0 \sim N_3$ are obtained from the given voltage conversion ratio, and the α_{ij} and β_{ij} values are solved by Genetic Algorithm.
- In Step2, based on the obtained α_{ij} and β_{ij} values, the corresponding volt-second equilibrium equations are written and two linear circuits are designed based on the α_{ij} values in D interval and β_{ij} values in D' interval, respectively.
- In Step3, the two linear circuits are combined into a converter topology that satisfies the given voltage conversion ratio using ideal switches.

B. Parameter constraint

To achieve a feasible and optimal converter topology, the parameters (α_{ij}, β_{ij}) of these equations must satisfy the following constraints:

- Input or output disconnection

To avoid input or output disconnection, specific conditions must be satisfied. When $\alpha_{10} = \alpha_{20} = \alpha_{30} = \beta_{10} = \beta_{20} = \beta_{30} = 0$, the input voltage source V_{in} is completely isolated, as depicted in Fig. 4(a). Similarly, when $\alpha_{13} = \alpha_{23} = \alpha_{33} = \beta_{13} = \beta_{23} = \beta_{33} = 0$, the output voltage V_{C3} is completely isolated, as shown in Fig. 4(b). This configuration clearly does not represent the desired converter topology and should be avoided.

- Order degradation

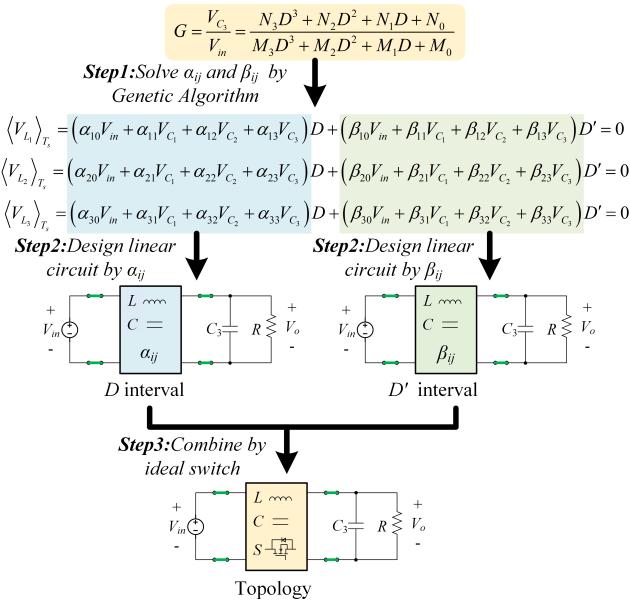


Fig. 3. Process of topology derivation.

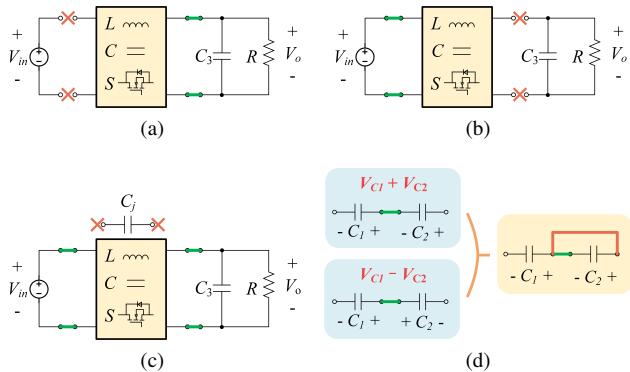


Fig. 4. Parameter constraint. (a) Input disconnection. (b) Output disconnection. (c) Order degradation. (d) Voltage conflict.

To prevent order degradation, certain conditions need to be met. When $\alpha_{11} = \alpha_{21} = \alpha_{31} = \beta_{11} = \beta_{21} = \beta_{31} = 0$, the regulated capacitor voltage V_{C_1} does not impact the circuit operation. Similarly, when $\alpha_{12} = \alpha_{22} = \alpha_{32} = \beta_{12} = \beta_{22} = \beta_{32} = 0$, the regulated capacitor voltage V_{C_2} does not affect the circuit operation. Both of these cases can result in circuit order degradation, as illustrated in Fig. 4(c), and should be avoided.

3) Voltage conflict

Voltage conflict arises from the contradiction between the voltage combinations required by the different inductor at same time intervals. Since all essential components are two-terminal devices, their voltage addition or subtraction can occur at a specific time interval but not simultaneously, as depicted in Fig. 4(d). To determine whether a parameter combination results in voltage conflict, a function $f(u, v)$ is defined with the one-dimensional arrays u and v as independent variables, as shown in

formula (8).

$$f(u, v) = \bigwedge_{a,b \in \{0,1,2,3\}} [(u_a \neq 0) \wedge (v_a \neq 0) \wedge (u_b \neq 0) \wedge (v_b \neq 0) \wedge (u_a \cdot v_a + u_b \cdot v_b = 0)] \quad (8)$$

In formula(8), the symbol \wedge denotes the intersection of sets, representing the set containing elements that are common to two or more sets. This function is utilized to ascertain if the four non-zero elements u_a, v_a, u_b , and v_b of the one-dimensional arrays u and v with a length of 4 satisfy the condition $u_a \cdot v_a + u_b \cdot v_b = 0$ at any two subscript positions a and b . Fig. 5 illustrates the flowchart for determining whether a parameter combination exhibits voltage conflict.

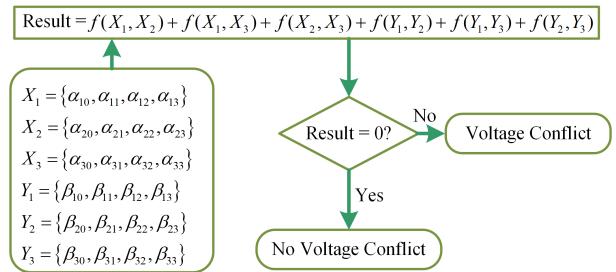


Fig. 5. Detection of Voltage Conflict.

4) Minimization of the number of switches

If there is a higher level of similarity between the voltage expressions for the same inductor between DT_s and $D'T_s$, fewer changes are required in the circuit, leading to a reduction in the number of switches. The similarity is determined by examining the number of different parameter values (α_{ij}, β_{ij}) for the same subscripts i and j . Fig. 6 provides an example of calculating the similarity of parameter combinations.

$$[\alpha_{10}, \alpha_{11}, \alpha_{12}, \alpha_{13}, \beta_{10}, \beta_{11}, \beta_{12}, \beta_{13}, \alpha_{20}, \alpha_{21}, \alpha_{22}, \alpha_{23}, \beta_{20}, \beta_{21}, \beta_{22}, \beta_{23}, \alpha_{30}, \alpha_{31}, \alpha_{32}, \alpha_{33}, \beta_{30}, \beta_{31}, \beta_{32}, \beta_{33}]$$

$$[1, 0, 0, -1, 0, 0, 1, 0, 1, 0, -1, -1, 0, 1, -1, 0, 1, -1, 0, -1, 0, -1, 0]$$

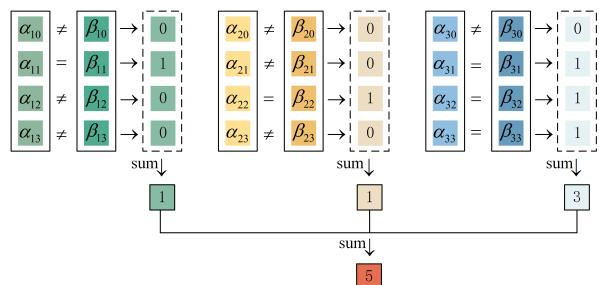


Fig. 6. Calculation of parameter combination similarity.

C. Fitness function

Based on the aforementioned constraints and equation requirements, this paper proposes a fitness evaluation criterion. When the parameter combination satisfies equation (5), a high reward R_L is assigned. When there is no input or output disconnection, order degradation, or voltage conflict in the

parameter combination, a moderate reward R_M is given. Finally, a lower reward R_S is assigned based on the similarity criterion. By incorporating these criteria, the fitness function for the parameter combination can be formulated as shown in formula (9):

$$\text{fitness} = mR_L + (x + y + z)R_M + qR_S \quad (9)$$

where m denotes the number of items satisfying equation (5), $0 \leq m \leq 8$; $x = 0$ means that there is input or output disconnection; $x = 1$ means that there is no input or output disconnection; $y = 0$ indicates that there is order degradation, and $y = 1$ indicates that there is no order degradation; $z = 0$ denotes that there is a voltage conflict, and $z = 1$ denotes that there is no voltage conflict; q represents the similarity of parameter combination.

D. Genetic Algorithm solving process

In this paper, the focus is on the third-order converter, which involves 24 parameters in the volt-second balance equations presented in equation (1) - (3). Obviously, formulas (5) has only 8 equations and cannot be solved directly for 24 unknowns. The solution space consists of 3^{24} possibilities, making exhaustive methods time-consuming. Genetic Algorithm can retain the population characteristics and improve the efficiency of parameter solving through crossover, mutation and other operations [27], which offers significant advantages in solving constraint equations with a large solution space. In addition, Genetic Algorithm can optimize the parameters according to the relevant parameter constraints and parameter optimization indexes, so as to obtain the optimal parameters satisfying the equations [28]. Therefore, this paper proposes the utilization of Genetic Algorithm to solve the optimal parameters $(\alpha_{ij}, \beta_{ij})$.

The parameter combination $(\alpha_{ij}, \beta_{ij})$ is converted into a chromosome with a length of 24, where each gene represents the value of a parameter, and the value range is $\{-1, 0, 1\}$. The solving process of Genetic Algorithm is illustrated in Fig. 7.

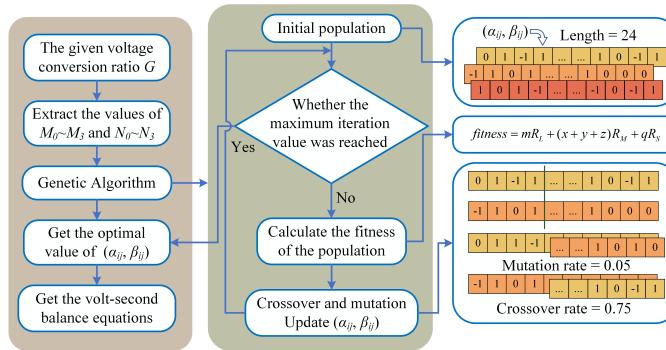


Fig. 7. Genetic Algorithm solving process.

E. Optimal converter topology

The optimal solution is the parameter solution $(\alpha_{ij}, \beta_{ij})$ that meets all the parameter constraints and equations (5). It should also have the highest possible similarity. This solution can

be either a local optimal solution or one of multiple optimal solutions.

The local optimal solution indicates the existence of different parameter solutions $(\alpha_{ij}, \beta_{ij})$ corresponding to different topologies, one converter topology can be obtained for each iteration of the genetic algorithm, and multiple converter topologies may be obtained for multiple iterations, e.g., two converter topologies are given as illustrations for both examples in Section IV.

The multiple optimal solutions indicate the existence of a plurality of parameter solutions corresponding to one converter topology. We further investigated whether there are multiple optimal solutions and if so, what is the number. For an n -order topology, there are K values of $(\alpha_{ij}, \beta_{ij})$ that lead to the different volt-second balance equations [29]. The calculation formula for K is as follows:

$$K = 2^{2n-1} \times n! \times (n-1)! \quad (10)$$

where 2^{2n-1} indicates that the polarities of inductors $L_1 \sim L_n$ and capacitors $C_1 \sim C_{n-1}$ can be assumed in two different ways; $n!$ represents the different ways of naming the order of inductors $L_1 \sim L_n$; $(n-1)!$ represents the different ways of naming the order of capacitors $C_1 \sim C_{n-1}$.

This implies that a third-order DC/DC converter topology ($n = 3$) can correspond to 384 different volt-second balance equation groups. That is to say, there are at least 384 optimal parameter solutions $(\alpha_{ij}, \beta_{ij})$ with the same fitness values for a given third-order voltage conversion ratio.

IV. TOPOLOGY DERIVATION RESULTS

The proposed method has the capability to derive the optimal converter topology that satisfies the requirements based on wide given third-order voltage conversion ratio expression. Since the optimization result of Genetic Algorithm is not necessarily the global optimal solution, different local optimal solutions can be solved several times to obtain different converter topologies. In this paper, the third-order boost converter with voltage conversion ratio $G = 1/(1-D)^3$ and the third-order buck converter with voltage conversion ratio $G = D^3$ are taken as examples to illustrate this function.

A. Calculation speed comparison with exhaustive method

In order to verify the speed of the proposed method, the parameters $(\alpha_{ij}, \beta_{ij})$ are solved by the program using exhaustive and Genetic Algorithm, respectively, with parameter constraints. The solution program was run on a computer equipped with an AMD Ryzen 7 6800H CPU and 16 GB RAM. The parameter configuration of Genetic Algorithm is shown in Table I.

TABLE I
PARAMETERS OF GENETIC ALGORITHM

Parameter	Value	Parameter	Value
Population Size	500	Iterations	4000
Crossover Rate	0.75	Mutation Rate	0.05

The number of calculations of the genetic algorithm is the product of the population size and the number of iterations [27], that is 2×10^6 . It should also be noted that the exhaustive method needs to traverse the entire solution space, so the number of calculations of the exhaustive method is 3^{24} . As can be seen from Table II, Genetic Algorithm has a great advantage in the evaluation metrics of both the number of calculations and solution time in solving 24 parameters.

In addition, in an industrial environment where computational resources and optimization time are limited, before performing the fitness calculation in the genetic algorithm, equation (6) can also be used to pre-judge whether the parameter solution is feasible. This pre-judgment step can quickly eliminate a large number of obviously invalid parameter combinations without going through the entire fitness calculation process, which consumes more resources. Moreover, the solution time in Table II can be further slashed to 23.80s.

TABLE II
COMPARISON OF ALGORITHMS

	Exhaustive Method	Genetic Algorithm
number of calculations	3^{24}	2×10^6
solution time	262509s	31.69s

B. Topology derivation of the third-order boost converter

To derive the topology for a specific voltage conversion ratio expression, it is matched with the general form given in formula (4). In the case of $G = 1/(1 - D)^3$, the coefficients can be determined as follows: $N_0 = 1, N_1 = N_2 = N_3 = 0, M_0 = 1, M_1 = -3, M_2 = 3, M_3 = -1$. By following the solution process outlined in Fig. 7, the third-order boost converter topologies (TOBCT) are obtained, and the topology derivation process is shown in Fig. 8.

In order to illustrate the working principle of the derived converter, taking TOBCT1 in Fig. 8 as an example, the corresponding parameter combination $(\alpha_{ij}, \beta_{ij})$ values are obtained as presented in Table III, and the corresponding volt-second balance equations are shown in equation (11) - (13).

TABLE III
PARAMETER COMBINATIONS OF TOBCT1

Parameter	Value	Parameter	Value	Parameter	Value
α_{10}	0	α_{20}	1	α_{30}	1
α_{11}	1	α_{21}	0	α_{31}	0
α_{12}	1	α_{22}	1	α_{32}	0
α_{13}	0	α_{23}	0	α_{33}	0
β_{10}	0	β_{20}	1	β_{30}	1
β_{11}	1	β_{21}	-1	β_{31}	0
β_{12}	1	β_{22}	-1	β_{32}	-1
β_{13}	-1	β_{23}	0	β_{33}	0

$$\langle V_{L_1} \rangle_{T_s} = (V_{C_1} + V_{C_2}) D + (V_{C_1} + V_{C_2} - V_{C_3}) D' = 0 \quad (11)$$

$$\langle V_{L_2} \rangle_{T_s} = (V_{in} + V_{C_2}) D + (V_{in} - V_{C_1} - V_{C_2}) D' = 0 \quad (12)$$

$$\langle V_{L_3} \rangle_{T_s} = V_{in} D + (V_{in} - V_{C_2}) D' = 0 \quad (13)$$

During the D interval, switches S_1, S_2 , and S_3 are turned on, while switches S_1', S_2' , and S_3' are turned off. On the other hand, during the D' interval, switches S_1, S_2 , and S_3 are turned off, and switches S_1', S_2' , and S_3' are turned on. The circuit functions as a boost circuit. The circuit uses a complementary switch control scheme, as illustrated in Fig. 9(a). The relationship between the boost ratio and the duty cycle is given by:

$$\frac{V_{C_1}}{V_{in}} = \frac{D}{(1 - D)^2} \quad (14)$$

$$\frac{V_{C_2}}{V_{in}} = \frac{1}{1 - D} \quad (15)$$

$$\frac{V_{C_3}}{V_{in}} = \frac{1}{(1 - D)^3} \quad (16)$$

C. Topology derivation of the third-order buck converter

TABLE IV
PARAMETER COMBINATIONS OF TOBCKT1

Parameter	Value	Parameter	Value	Parameter	Value
α_{10}	0	α_{20}	1	α_{30}	0
α_{11}	-1	α_{21}	0	α_{31}	-1
α_{12}	0	α_{22}	-1	α_{32}	1
α_{13}	1	α_{23}	-1	α_{33}	1
β_{10}	0	β_{20}	0	β_{30}	0
β_{11}	0	β_{21}	0	β_{31}	-1
β_{12}	0	β_{22}	-1	β_{32}	0
β_{13}	1	β_{23}	-1	β_{33}	0

To derive the topology for a specific voltage conversion ratio expression, it is matched with the general form given in formula (4). In the case of $G = D^3$, the coefficients can be determined as follows: $N_3 = 1, N_0 = N_1 = N_2 = 0, M_0 = 1, M_1 = M_2 = M_3 = 0$. By following the solution process outlined in Fig. 7, the third-order buck converter topologies (TOBCKT) are obtained, and the topology derivation process is shown in Fig. 10.

In order to illustrate the working principle of the derived converter, taking TOBCKT1 in Fig. 10 as an example, the corresponding parameter combination $(\alpha_{ij}, \beta_{ij})$ values are obtained as presented in Table IV, and the corresponding volt-second balance equations are shown in equation (17) - (19).

$$\langle V_{L_1} \rangle_{T_s} = (-V_{C_1} + V_{C_3}) D + V_{C_3} D' = 0 \quad (17)$$

$$\langle V_{L_2} \rangle_{T_s} = (V_{in} - V_{C_2} - V_{C_3}) D + (-V_{C_2} - V_{C_3}) D' = 0 \quad (18)$$

$$\langle V_{L_3} \rangle_{T_s} = (-V_{C_1} + V_{C_2} + V_{C_3}) D - V_{C_1} D' = 0 \quad (19)$$

During the D interval, switches S_1, S_2 , and S_3 are turned on, while switches S_1', S_2' , and S_3' are turned off. On the other hand, during the D' interval, switches S_1, S_2 , and S_3

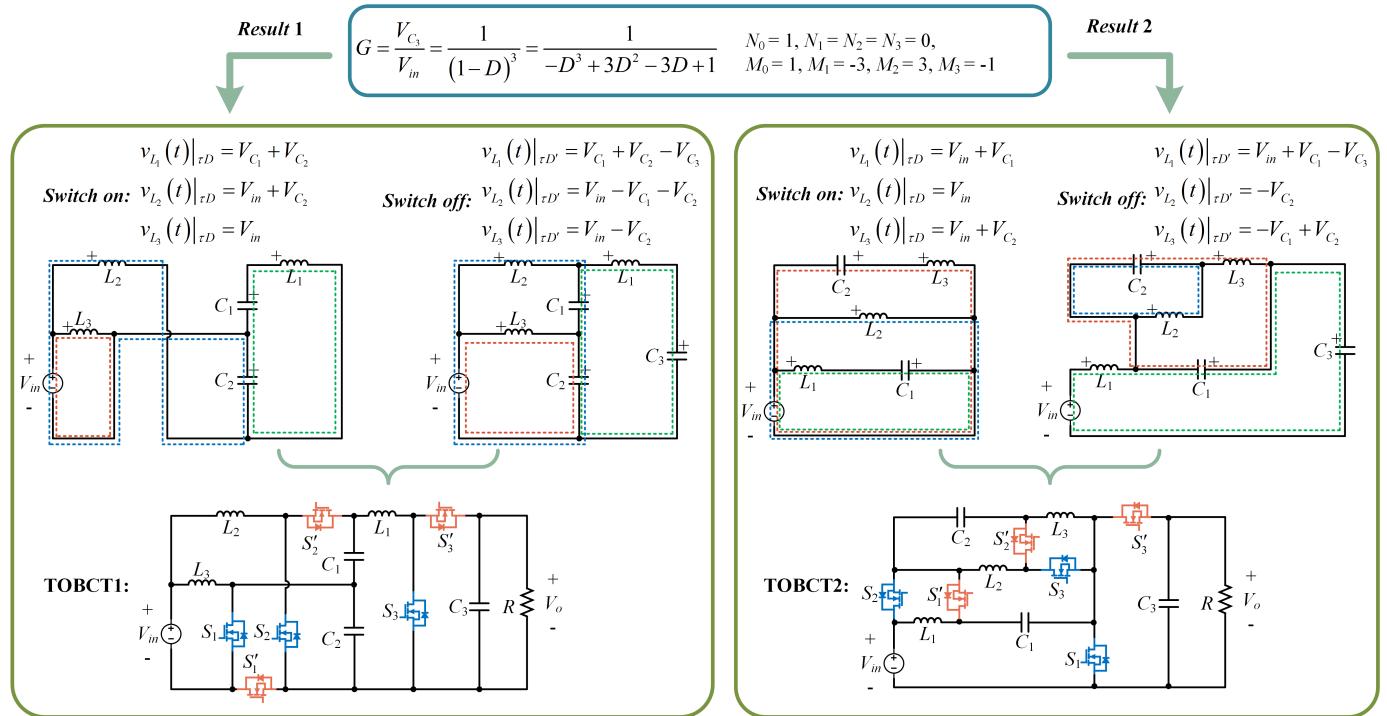


Fig. 8. Topology derivation process of TOBCT.

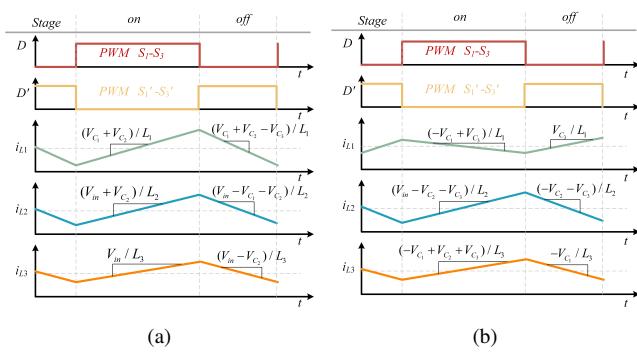


Fig. 9. Switch control scheme. (a)TOBCT1.(b)TOBCKT1

are turned off, and switches S'_1 , S'_2 , and S'_3 are turned on. The circuit functions as a buck circuit. The circuit uses a complementary switch control scheme, as illustrated in Fig. 9(b). The relationship between the step-down ratio and the duty cycle is given by:

$$\frac{V_{C_1}}{V_{in}} = D^2 \quad (20)$$

$$\frac{V_{C_2}}{V_{in}} = D - D^3 \quad (21)$$

$$\frac{V_{C_3}}{V_{in}} = D^3 \quad (22)$$

V. VERIFICATION

A. Simulation verification of the third-order converters

In order to verify the performance of all the converters in Fig. 8 and Fig. 10, Simulink simulations are performed in

this paper. The switching frequencies are all set to 100kHz. The simulation results of the capacitors voltages are shown in Fig. 11 and the simulation results of the inductors currents are shown in Fig. 12.

The Mean Absolute Percentage Error (MAPE) between the simulated values and the theoretical values in Table VI in the Appendix is 4.7%. The simulation results show a close agreement between the simulated and theoretical values. It shows that the converter meets the design requirements and works properly.

B. Experimental verification of TBOCKT1

To validate the compliance of TBOCKT1 in Fig. 10 with the specified voltage specifications, TBOCKT1 has been rigorously validated through printed circuit board (PCB) implementation, as shown in Fig. 13. The experimental settings are as listed in Table V. The inductor values and capacitance values are chosen to ensure the circuit operates under the continuous current mode (CCM) according to the drive signals. The setup entail an input voltage of 24V, a duty cycle D of 0.5, and a switching frequency of 41kHz. The anticipated output voltages are theoretically projected as follows: $V_{C_1} = 6V$, $V_{C_2} = 9V$, $V_{C_3} = 3V$, and $I_o = V_{C_3}/R$. Subsequent to experimental trials, the steady state voltage waveform is shown in Fig. 14(a) and the steady state output current waveform is shown in Fig. 14(b).

From Fig. 14(a), when the output load R is 3Ω, the voltage of C_1 is 5.86V, the voltage of C_2 is 9.07V, and the voltage of capacitor C_3 is 2.90V. From Fig. 14(b), the mean value of I_o is 2.72A for $R = 1\Omega$, the mean value of I_o is 1.42A for $R = 2\Omega$, and the mean value of I_o is 0.96A for $R = 3\Omega$. The gain deviation in the experimental results is caused by the

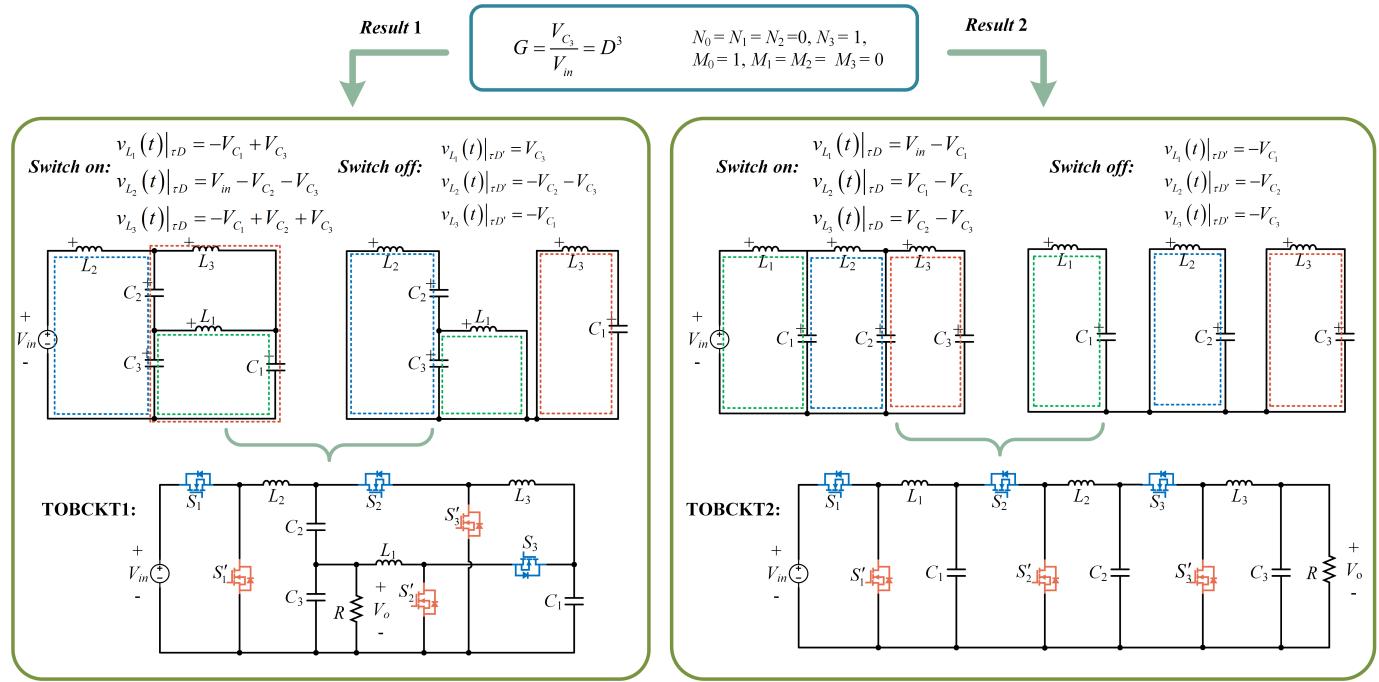


Fig. 10. Topology derivation process of TOBCKT.

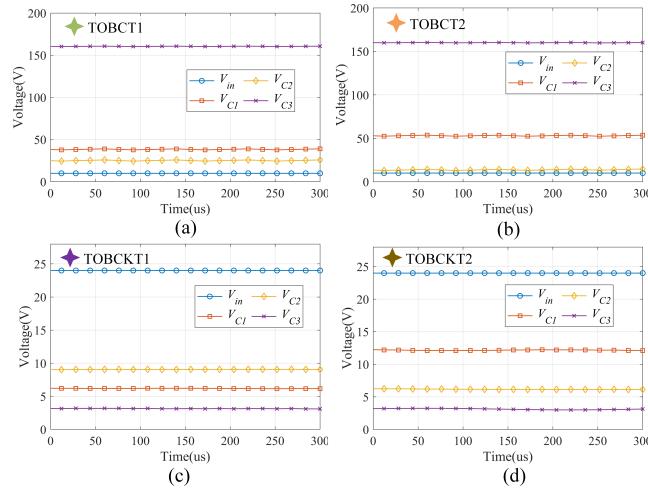


Fig. 11. Simulation results of the capacitors voltages. (a)~(b) $V_{in} = 10V$, $D = 0.6$, $L_1 = L_2 = L_3 = 33\mu H$, $C_1 = C_2 = C_3 = 500\mu F$, $R = 200\Omega$. (c)~(d) $V_{in} = 24V$, $D = 0.5$, $L_1 = L_2 = L_3 = 33\mu H$, $C_1 = C_2 = C_3 = 100\mu F$, $R = 1\Omega$.

TABLE V
PARAMETERS OF THE EXPERIMENTAL CIRCUITS

Parameter	Value	Parameter	Value
L_{1-L_3}	$33\mu H$	$S_1-S_3, S'_1-S'_3$	IRF540NPBF
C_1-C_3	$100\mu F$	Switching Period T_s	$24\mu s$

parasitic resistance of the elements and the forward voltage drop of the diodes.

To further validate the converter, the value of input voltage V_{in} was varied several times to obtain multiple sets of average voltage values of $V_{C_1} \sim V_{C_3}$ as shown in Fig. 15. The

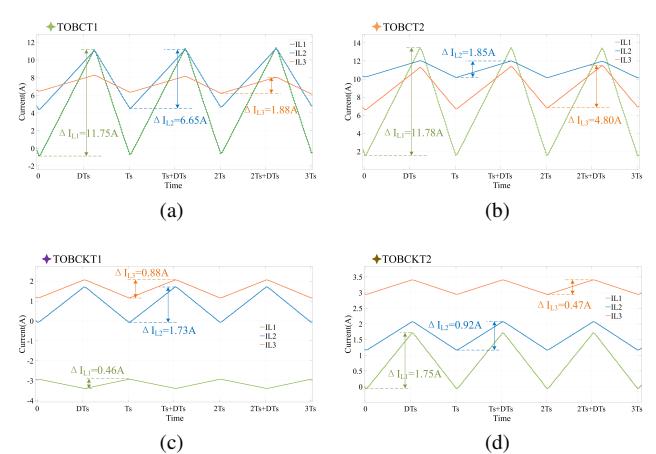


Fig. 12. Simulation results of the inductors currents. (a)~(b) $V_{in} = 10V$, $D = 0.6$, $L_1 = L_2 = L_3 = 33\mu H$, $C_1 = C_2 = C_3 = 500\mu F$, $R = 200\Omega$. (c)~(d) $V_{in} = 24V$, $D = 0.5$, $L_1 = L_2 = L_3 = 33\mu H$, $C_1 = C_2 = C_3 = 100\mu F$, $R = 1\Omega$.

experimental values match well with the mathematical analysis values. This outcome serves as a tangible validation that the proposed methodology empowers engineers to swiftly and effectively design converters that precisely cater to the exigencies of real-world applications.

VI. CONCLUSION

This paper presents a method for determining the topology of a DC/DC converter with wide given third-order voltage conversion ratio. The proposed method involves solving eight equations with 24 unknowns (α_{ij}, β_{ij}). By considering the constraints on the parameters, a suitable combination of (α_{ij}, β_{ij}) is obtained based on Genetic Algorithm. The derived



Fig. 13. PCB photo of fabricated TOBCKT1 prototype.

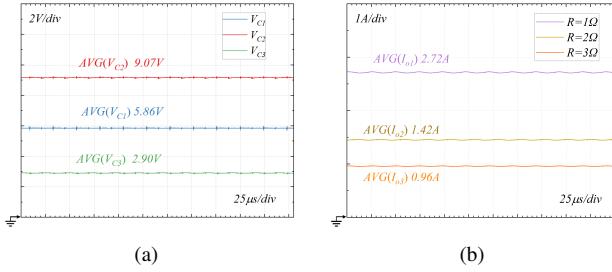


Fig. 14. Steady-state waveform of TOBCKT1. (a)Voltage($R = 3\Omega$). (b)Current($R = 1\Omega/2\Omega/3\Omega$).

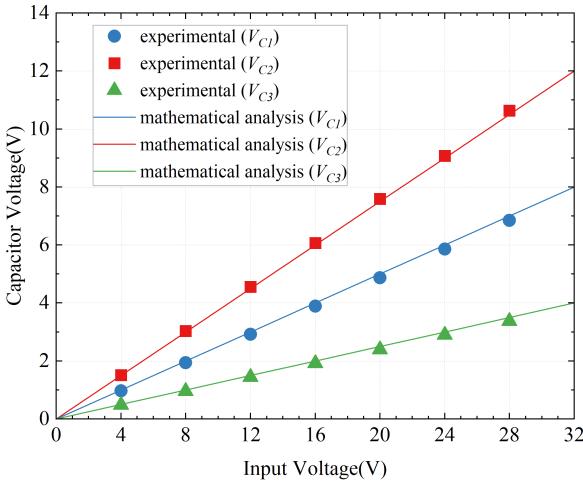


Fig. 15. Operation at different V_{in} of TOBCKT1($R = 3\Omega$).

$(\alpha_{ij}, \beta_{ij})$ values are then used to determine the corresponding converter topology. Compared with the exhaustive method, Genetic Algorithm can not only get the optimal parameters, but also largely improve the speed of parameter solving. To demonstrate the effectiveness of the method, TOBCT with voltage conversion ratio $G = 1/(1 - D)^3$ and TOBCKT with voltage conversion ratio $G = D^3$ are employed as case studies. The steady-state operations of all the topologies obtained are verified by Simulink simulations, and the topology of TOBCKT1 is further verified by PCB implementation.

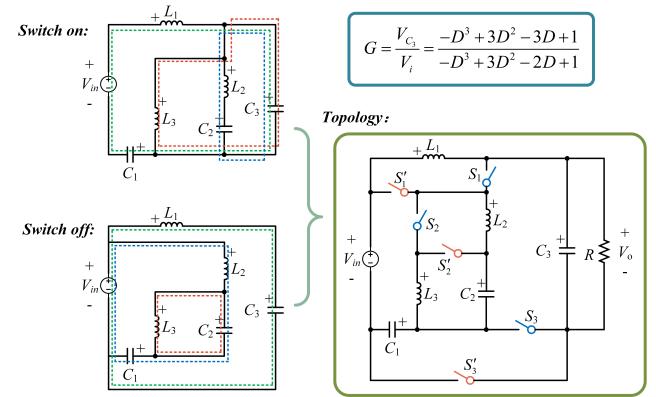


Fig. 16. Derivation process of Example 1.

APPENDIX

COMPARISON OF PERFORMANCE METRICS AND OTHER DERIVATION EXAMPLES

A. Comparison of Performance Metrics

The performance of the deduced converters are analyzed and compared and the results are shown in Table VI. From Table VI, it can be seen that the TOBCT1 converter performs better in terms of inductor current and voltage-current stress on the switch, while the TOBCT2 converter performs better in terms of input-output common ground and intermediate capacitor voltage. Similarly, TOBCKT1 and TOBCKT2 have their own advantages and disadvantages in several evaluation metrics.

B. Other Derivation Examples

In addition to the third-order boost converter and the third-order buck converter, the method can be applied to derive converter topologies for other voltage conversion ratios. Two examples of topology derivation for more complex voltage conversion ratios are shown as follows.

1) *Example 1:* By taking $N_3 = -1, N_2 = 3, N_1 = -3, N_0 = 1, M_3 = -1, M_2 = 3, M_1 = -2, M_0 = 1$, a third-order DC/DC converter topology with a specific voltage conversion ratio can be derived, as shown in Fig. 16.

The volt-second balance equations corresponding to Example 1 are shown in equation (23).

$$\begin{cases} \langle V_{L1} \rangle_{T_s} = (V_{in} - V_{C1} - V_{C3}) D + (V_{in} - V_{C3}) D' = 0 \\ \langle V_{L2} \rangle_{T_s} = (-V_{C2} + V_{C3}) D + (V_{in} - V_{C1} - V_{C2}) D' = 0 \\ \langle V_{L3} \rangle_{T_s} = V_{C3} D + V_{C2} D' = 0 \end{cases} \quad (23)$$

The relationship between the step-down ratio and the duty cycle is given in equation (24).

$$\begin{cases} \frac{V_{C1}}{V_{in}} = \frac{1}{-D^3 + 3D^2 - 2D + 1} \\ \frac{V_{C2}}{V_{in}} = \frac{-D^3 + 2D^2 - D}{-D^3 + 3D^2 - 2D + 1} \\ \frac{V_{C3}}{V_{in}} = \frac{-D^3 + 3D^2 - 3D + 1}{-D^3 + 3D^2 - 2D + 1} \end{cases} \quad (24)$$

TABLE VI
COMPARISON OF THIRD-ORDER CONVERTERS

	TOBCT1	TOBCT2	[30]	TOBCKT1	TOBCKT2	[29]
Voltage conversion ratio	$\frac{1}{(1-D)^3}$	$\frac{1}{(1-D)^3}$	$\frac{1}{(1-D)^3}$	D^3	D^3	D^3
Common ground?	no	yes	yes	yes	yes	yes
Number of switches	6	6	6	6	6	6
V_{C_1}	$\frac{DV_{in}}{(1-D)^2}$	$\frac{(-D^2+2D)V_{in}}{(1-D)^2}$	$\frac{V_{in}}{(1-D)}$	$V_{in} D^2$	$V_{in} D^2$	$-V_{in} D$
V_{C_2}	$\frac{V_{in}}{(1-D)}$	$\frac{DV_{in}}{(1-D)}$	$\frac{V_{in}}{(1-D)^2}$	$V_{in}(D - D^3)$	$V_{in} D^2$	$V_{in}(D^3 - D^2)$
I_{L_1}	$\frac{V_{in}}{(1-D)^3 R}$	$\frac{V_{in}}{(1-D)^4 R}$	$\frac{V_{in}}{(1-D)^6 R}$	$-\frac{V_{in} D^3}{R}$	$\frac{V_{in} D^5}{R}$	$\frac{V_{in} D^4}{R}$
Ripple of I_{L_1}	$\frac{V_{in} DT_s}{(1-D)^2 L_1}$	$\frac{V_{in} DT_s}{(1-D)^2 L_1}$	$\frac{V_{in} DT_s}{L_1}$	$\frac{V_{in}(D^3 - D^4) T_s}{L_1}$	$\frac{V_{in}(D - D^2) T_s}{L_1}$	$\frac{V_{in}(D - D^2) T_s}{L_1}$
I_{L_2}	$\frac{V_{in}}{D(1-D)^3 R}$	$\frac{V_{in}}{(1-D)^6 R}$	$\frac{V_{in}}{(1-D)^5 R}$	$\frac{V_{in} D^5}{R}$	$\frac{V_{in} D^4}{R}$	$\frac{-V_{in}(D^4 - D^5)}{R}$
Ripple of I_{L_2}	$\frac{V_{in}(2-D)DT_s}{(1-D)L_2}$	$\frac{V_{in} DT_s}{L_2}$	$\frac{V_{in} DT_s}{(1-D)L_2}$	$\frac{V_{in}(D - D^2) T_s}{L_2}$	$\frac{V_{in}(D^2 - D^3) T_s}{L_2}$	$\frac{V_{in}(D - D^2) T_s}{L_2}$
I_{L_3}	$\frac{V_{in}}{D(1-D)^3 R}$	$\frac{V_{in}}{(1-D)^5 R}$	$\frac{V_{in}}{(1-D)^4 R}$	$\frac{V_{in} D^4}{R}$	$\frac{V_{in} D^3}{R}$	$\frac{V_{in} D^3}{R}$
Ripple of I_{L_3}	$\frac{V_{in} DT_s}{L_3}$	$\frac{V_{in} DT_s}{(1-D)L_3}$	$\frac{V_{in} DT_s}{(1-D)^2 L_3}$	$\frac{V_{in}(D^2 - D^3) T_s}{L_3}$	$\frac{V_{in}(D^3 - D^4) T_s}{L_3}$	$\frac{V_{in}(D^3 - D^4) T_s}{L_3}$
Voltage stress of S_1	$\frac{V_{in}}{(1-D)}$	$\frac{V_{in}}{(1-D)^3}$	$\frac{V_{in}}{(1-D)}$	V_{in}	V_{in}	V_{in}
Current stress of S_1	$\frac{2V_{in}}{D(1-D)^3 R}$	$\frac{(D^2 - 3D + 3)V_{in}}{(1-D)^6 R}$	$\frac{V_{in}}{(1-D)^6 R}$	$\frac{V_{in} D^5}{R}$	$\frac{V_{in} D^5}{R}$	$\frac{V_{in} D^5}{R}$
Voltage stress of S'_1	$\frac{V_{in}}{(1-D)}$	$\frac{V_{in}}{(1-D)^2}$	$\frac{V_{in}}{(1-D)}$	V_{in}	V_{in}	V_{in}
Current stress of S'_1	$\frac{2V_{in}}{D(1-D)^3 R}$	$\frac{V_{in}}{(1-D)^5 R}$	$\frac{V_{in}}{(1-D)^6 R}$	$\frac{V_{in} D^5}{R}$	$\frac{V_{in} D^5}{R}$	$\frac{V_{in} D^4}{R}$
Voltage stress of S_2	$\frac{V_{in}}{(1-D)^2}$	$\frac{V_{in} D}{(1-D)^3}$	$\frac{V_{in}}{(1-D)^2}$	$V_{in} D$	$V_{in} D$	$V_{in} D$
Current stress of S_2	$\frac{V_{in}}{D(1-D)^3 R}$	$\frac{V_{in}(2-D)}{(1-D)^6 R}$	$\frac{V_{in}}{(1-D)^5 R}$	$\frac{V_{in} D^4}{R}$	$\frac{V_{in} D^4}{R}$	$\frac{V_{in} D^4(1-D)}{R}$
Voltage stress of S'_2	$\frac{V_{in}}{(1-D)^2}$	$\frac{V_{in}}{(1-D)}$	$\frac{V_{in}}{(1-D)^2}$	$V_{in} D^2$	$V_{in} D$	V_{in}
Current stress of S'_2	$\frac{V_{in}}{D(1-D)^3 R}$	$\frac{V_{in}}{(1-D)^6 R}$	$\frac{V_{in}}{(1-D)^5 R}$	$\frac{V_{in} D^3}{R}$	$\frac{V_{in} D^4}{R}$	$\frac{V_{in} D^5}{R}$
Voltage stress of S_3	$\frac{V_{in}}{(1-D)^3}$	$\frac{V_{in} D}{(1-D)^2}$	$\frac{V_{in}}{(1-D)^3}$	$V_{in} D^2$	$V_{in} D^2$	$V_{in} D^2$
Current stress of S_3	$\frac{V_{in}}{(1-D)^3 R}$	$\frac{V_{in}}{(1-D)^6 R}$	$\frac{V_{in}}{(1-D)^4 R}$	$\frac{V_{in} D^3}{R}$	$\frac{V_{in} D^3}{R}$	$\frac{V_{in} D^3}{R}$
Voltage stress of S'_3	$\frac{V_{in}}{(1-D)^3}$	$\frac{V_{in}}{(1-D)^3}$	$\frac{V_{in}}{(1-D)^3}$	$V_{in} D$	$V_{in} D^2$	$V_{in} D^2$
Current stress of S'_3	$\frac{V_{in}}{(1-D)^3 R}$	$\frac{V_{in}}{(1-D)^4 R}$	$\frac{V_{in}}{(1-D)^4 R}$	$\frac{V_{in} D^4}{R}$	$\frac{V_{in} D^3}{R}$	$\frac{V_{in} D^3}{R}$

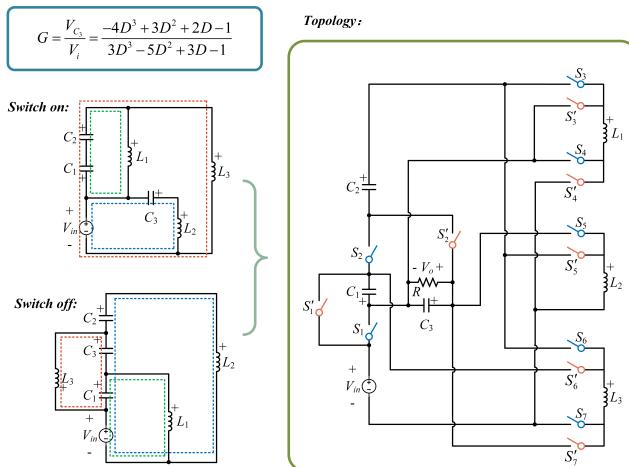


Fig. 17. Derivation process of Example 2.

2) **Example 2:** By taking $N_3 = -4, N_2 = 3, N_1 = 2, N_0 = -1, M_3 = 3, M_2 = -5, M_1 = 3, M_0 = 1$, Fig. 17 shows the derivation of another third-order DC/DC converter topology. The volt-second balance equations corresponding to Example

2 are shown in equation (25).

$$\left\{ \begin{array}{l} \langle V_{L_1} \rangle_{T_s} = (-V_{C_1} + V_{C_2}) D + (V_{in} + V_{C_1}) D' = 0 \\ \langle V_{L_2} \rangle_{T_s} = (V_{in} + V_{C_3}) D + (V_{in} + V_{C_1} + V_{C_2} + V_{C_3}) D' = 0 \\ \langle V_{L_3} \rangle_{T_s} = (V_{in} - V_{C_1} + V_{C_2}) D + (-V_{C_1} - V_{C_3}) D' = 0 \end{array} \right. \quad (25)$$

The relationship between the step-down ratio and the duty cycle is given in equation (26).

$$\left\{ \begin{array}{l} \frac{V_{C_1}}{V_{in}} = \frac{-D^3 + 2D^2 - 3D + 1}{3D^3 - 5D^2 + 3D - 1} \\ \frac{V_{C_2}}{V_{in}} = \frac{D^3 - 3D^2 + 1}{3D^3 - 5D^2 + 3D - 1} \\ \frac{V_{C_3}}{V_{in}} = \frac{-4D^3 + 3D^2 + 2D - 1}{3D^3 - 5D^2 + 3D - 1} \end{array} \right. \quad (26)$$

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