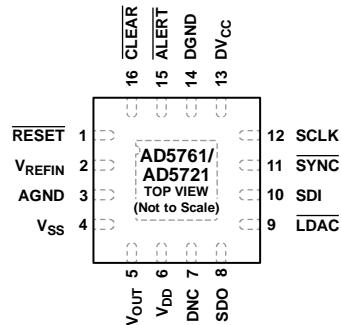


PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

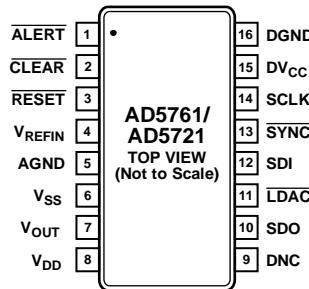


NOTES

1. DNC = DO NOT CONNECT. DO NOT CONNECT TO THIS PIN.
2. EXPOSED PAD. ENSURE THAT THE EXPOSED PAD IS MECHANICALLY CONNECTED TO A PCB COPPER PLANE FOR OPTIMAL THERMAL PERFORMANCE. THE EXPOSED PAD CAN BE LEFT ELECTRICALLY FLOATING.

12840-106

Figure 5. LFCSP Pin Configuration



DNC = DO NOT CONNECT. DO NOT CONNECT TO THIS PIN.

12840-006

Figure 6. TSSOP Pin Configuration

Table 6. Pin Function Descriptions

Pin No.		Mnemonic	Description
LFCSP	TSSOP		
1	3	RESET	Active Low Reset Input. Asserting this pin returns the AD5761/AD5721 to their default power-on status where the output is clamped to ground and the output buffer is powered down. This pin can be left floating because there is an internal pull-up resistor.
2	4	V _{REFIN}	External Reference Voltage Input. For specified performance, V _{REFIN} = 2.5 V.
3	5	AGND	Ground Reference for Analog Circuitry.
4	6	V _{SS}	Negative Analog Supply Connection. A voltage in the range of -16.5 V to 0 V can be connected to this pin. For unipolar output ranges, connect this pin to 0 V. V _{SS} must be decoupled to AGND.
5	7	V _{OUT}	Analog Output Voltage of the DAC. The output amplifier is capable of directly driving a 2 kΩ, 1 nF load.
6	8	V _{DD}	Positive Analog Supply Connection. A voltage in the range of 4.75 V to 30 V can be connected to this pin for unipolar output ranges. Bipolar output ranges accept a voltage in the range of 4.75 V to 16.5 V. V _{DD} must be decoupled to AGND.
7	9	DNC	Do Not Connect. Do not connect to this pin.
8	10	SDO	Serial Data Output. This pin clocks data from the serial register in daisy-chain or readback mode. Data is clocked out on the rising edge of SCLK and is valid on the falling edge of SCLK.
9	11	LDAC	Load DAC. This logic input updates the DAC register and, consequently, the analog output. When tied permanently low, the DAC register is updated when the input register is updated. If LDAC is held high during the write to the input register, the DAC output register is not updated, and the DAC output update is held off until the falling edge of LDAC. This pin can be left floating because there is an internal pull-up resistor.
10	12	SDI	Serial Data Input. Data must be valid on the falling edge of SCLK.
11	13	SYNC	Active Low Synchronization Input. This pin is the frame synchronization signal for the serial interface. While SYNC is low, data is transferred in on the falling edge of SCLK. Data is latched on the rising edge of SYNC.
12	14	SCLK	Serial Clock Input. Data is clocked into the input shift register on the falling edge of SCLK. This pin operates at clock speeds of up to 50 MHz.
13	15	DV _{CC}	Digital Supply. The voltage range is from 1.7 V to 5.5 V. The applied voltage sets the voltage at which the digital interface operates.
14	16	DGND	Digital Ground.
15	1	ALERT	Active Low Alert. This pin is asserted low when the die temperature exceeds approximately 150°C, or when an output short circuit or a brownout occurs. This pin is also asserted low during power-up, a full software reset, or a hardware reset, for which a write to the control register asserts the pin high.
16	2	CLEAR	Falling Edge Clear Input. Asserting this pin sets the DAC register to zero-scale, midscale, or full-scale code (user selectable) and updates the DAC output. This pin can be left floating because there is an internal pull-up resistor.
17	N/A ¹	EPAD	Exposed Pad. Ensure that the exposed pad is mechanically connected to a PCB copper plane for optimal thermal performance. The exposed pad can be left electrically floating.

¹ N/A means not applicable.