

Yilong Zhao (赵恽龙)

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RESEARCH INTEREST

DRAM-based processing-in-memory (PIM), including memory management, task scheduling, and application acceleration for PIM architectures.

EDUCATION

Sep. 2022 – Now	Shanghai Jiao Tong University (SJTU), Shanghai, China <i>Ph.D. Student</i> , Major: Computer Science and Technology Expected Graduation: Jun. 2026	Advisor: Prof. Li Jiang
Sep. 2018 – Mar. 2021	Shanghai Jiao Tong University (SJTU), Shanghai, China <i>M.Eng.</i> , Major: Computer Technology	Advisor: Prof. Li Jiang
Sep. 2014 – Jun. 2018	Shanghai Jiao Tong University (SJTU), Shanghai, China <i>B.Eng.</i> , Major: Electronic Science and Technology	

PUBLICATIONS & PATENT (Full list can be found [here](#))

- **Yilong Zhao**, Mingyu Gao, Huanchen Zhang, Fangxin Liu, Gongye Chen, He Xian, Haibing Guan, and Li Jiang, "PUSHtap: PIM-based In-Memory HTAP with Unified Data Storage Format, " in *Proceedings of the 30th ACM International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS'25)* (Accepted)
- **Yilong Zhao**, Fangxin Liu, Xiaoyao Liang, Mingyu Gao, Naifeng Jing, Chengyang Gu, Qidong Tang, Tao Yang, and Li Jiang, "STAMP: Accelerating Second-order DNN Training Via ReRAM-based Processing-in-Memory Architecture, " in *Proceedings of the 16th International Symposium on Advanced Parallel Processing Technology (APPT'25)*
- **Yilong Zhao**, Mingyu Gao, Fangxin Liu, Yiwei Hu, Zongwu Wang, Han Lin, Ji Li, He Xian, Hanlin Dong, Tao Yang, Naifeng Jing, Xiaoyao Liang, and Li Jiang, "UM-PIM: DRAM-based PIM with Uniform & Shared Memory Space, " in *51st International Symposium on Computer Architecture (ISCA'24)*
- Weidong Cao, **Yilong Zhao (Co-first author)**, Adith Bolor, Yinhe Han, Xuan Zhang, and Li Jiang, "Neural-PIM: Efficient Processing-In-Memory with Neural Approximation of Peripherals, " in *IEEE Transactions on Computers (TC, 2021)*
- **Yilong Zhao**, Zhezhi He, Naifeng Jing, Xiaoyao Liang, and Li Jiang. Re2PIM: A Reconfigurable ReRAM-Based PIM Design for Variable-Sized Vector-Matrix Multiplication. In *Proceedings of the 2021 on Great Lakes Symposium on VLSI (GLSVLSI'21)*

Patent

- Li Jiang, Yilong Zhao, "Reconfigurable Architecture, Accelerator, Circuit Deployment and Dataflow Methods," Authorization No. CN112181895B
- Li Jiang, Yilong Zhao, Xiaosong Cui, Yun Chen, Jianxing Liao, "Neural Network Circuit," Authorization No. CN114004344A

SCIENTIFIC RESEARCH EXPERIENCE

Shanghai Jiao Tong University, ACA-IMPACT Lab,

Shanghai Qizhi Institute

PIM Implementation Towards Optical Communication Project

Mar. 2021 – Jul. 2022

The purpose of the research is to realize the receiver of optical communication and wireless communication based on the integrated technology of storage and calculation. I am responsible for the following tasks:

- Design the overall architecture of optical communication and wireless communication systems based on the integration of storage and calculation, including operator splitting and algorithm reconstruction.
- Realize the circuit simulation of some operators.
- Aiming at the high-power calculation module to achieve a lower calculation amount than the existing numerical algorithm under the conditions of allowable error.

Shanghai Jiao Tong University, ACA Lab

ReRAM-based Efficient and Reliable DNN Accelerator Project

Apr. 2019 – Apr. 2020

The project investigates the enhancement of computational reliability and the utilizes sparsity to improve energy efficiency in ReRAM-based DNN accelerator. I am responsible for the following work:

- Design and code a cycle-accurate simulator for the ReRAM-based NN accelerator. The simulator is built based on GEM5.
- Rewrite the simulator to evaluate the reliability and performance of architecture for pruned NN, The results of the simulator are used as an important metric for the project evaluation.
- Design a ReRAM-based DNN accelerator for pruned NN.