Ordering number : EN4346B

CMOS LSI

LC79400D

Dot Matrix LCD Driver

Overview

The LC79400D is a large-scale dot matrix LCD segment driver LSI. Display data transferred from the controller (4-bit parallel format) is processed through 80-bit latching and a LCD drive signal is generated. The LC79400D can be used in conjunction with common driver LC7943D (QIP80D) as well as LC79430D (QIP100D) and LC79431D (QIP100D) to drive a wide-screen LCD panel.

Features

- On-chip LCD drive circuit (80 bits)
- Display duty selection ranging from 1/64 to 1/256
- Supports use of chip disable pin for lower large panel power supply dissipation
- Supports externally supplied bias voltage
- Operating power supply voltage/operating temperature include

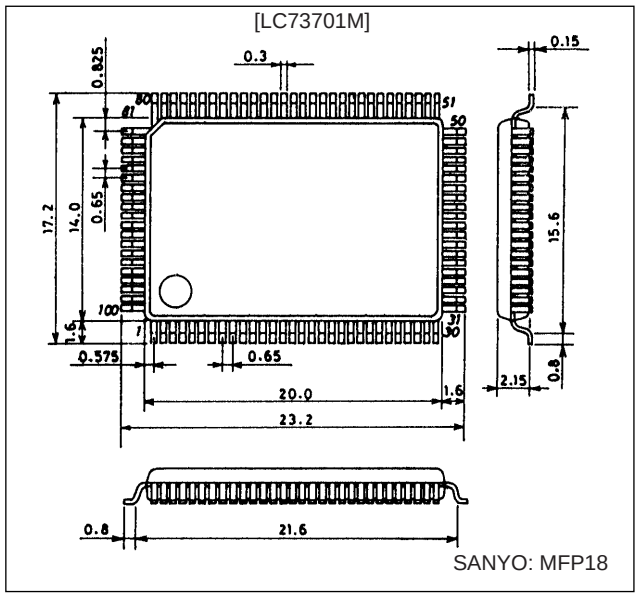
  V_{DD} (logic block) : 5 V ±10 % / –20 to +75 °C

  V_{DD}-V_{EE} (LCD block) : 12 V to 32 V / –20 to +75°C
- Data transfer clock provides maximum 3.0 MHz and supports bidirectional shift
- 4-bit parallel data input
- CMOS process
- 100-pin flat plastic package

Package Dimensions

unit : mm

3180-QFP100D



Specifications

Absolute Maximum Ratings at Ta = 25±2°C, V_{SS} = 0 V

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage (logic)	V_{DD} max		–0.3 to +7.0	V
Maximum supply voltage (LCD)	V_{DD} - V_{EE} max*1		0 to 35	V
Maximum input voltage	V_I max		–0.3 to V_{DD} + 0.3	V
Storage temperature range	Tstg		–40 to +125	°C

Note: 1. The voltages V_1, V_3, V_4, V_7, V_{DD} and V_{EE} must obey the relationships: $V_{DD} \geq V1 > V3 > V4 > V_{EE}$, $V_{DD} - V3 \leq 7V$, $V4 - V_{EE} \leq 7V$.

Allowable Operating Ranges at Ta = –20 to +75°C, V_{SS} = 0 V

Parameter	Symbol	Conditions	min	typ	max	Unit
Supply voltage (logic)	V_{DD}		4.5		5.5	V
Supply voltage (LCD)	V_{DD} - V_{EE}	*2, *3	12		32	V
Input high-level voltage	V_{IH}	DI1 to 4, CP, LOAD, CDR, CDL R/L, M, $\overline{\text{DISP OFF}}$	0.8 V_{DD}			V
Input low-level voltage	V_{IL}	DI1 to 4, CP, LOAD, CDR, CDL R/L, M, $\overline{\text{DISP OFF}}$			0.2 V_{DD}	V
CP (shift clock)	f_{CP}	CP			3.0	MHz
CP (pulse width)	f_{WC}	CP	100			ns
LOAD pulse width	t_{WL}	LOAD	100			ns
Setup time	t_{SETUP}	DI1 to 4 → CP	80			ns
Hold time	t_{HOLD}	DI1 to 4 → CP	80			ns
CP → LOAD	$t_{CL}1$	CP → LOAD	0			ns
	$t_{CL}2$	CP → LOAD	100			ns
LOAD → CP	t_{LC}	LOAD → CP	63			ns
Rise/Fall time	t_R	CP			50	ns
	t_F	CP			50	ns
	t_{RL}	LOAD			50	ns
	t_{FL}	LOAD			50	ns

Note: 2. The voltages V_1, V_3, V_4, V_7, V_{DD} and V_{EE} must obey the relationships: $V_{DD} \geq V1 > V3 > V4 > V_{EE}$, $V_{DD} - V3 \leq 7V$, $V4 - V_{EE} \leq 7V$.

3. When applying power, apply power to the LCD drive block after applying power to the logic block or apply power to both the blocks simultaneously. When turning off power, turn off power to the logic block after turning off power to the LCD drive block or turn off power to both the blocks simultaneously.

Electrical Characteristics at Ta = 25±2°C, V_{SS} = 0 V, V_{DD} = 5 V±10%

Parameter	Symbol	Conditions	min	typ	max	Unit
Input high-level current	I_{IH}	$V_{IN} = V_{DD}$; LOAD, CP, CDR (CDL), R/L, DI1 to DI4, M, $\overline{\text{DISP OFF}}$			1	µA
Input low-level current	I_{IL}	$V_{IN} = V_{SS}$; LOAD, CP, CDR (CDL), R/L, DI1 to DI4, M, $\overline{\text{DISP OFF}}$	–1			µA
Output high-level voltage	V_{OH}	I_{OH} = –400 µA; CDL (CDR)	V_{DD} – 0.4			V
Output low-level voltage	V_{OL}	I_{OL} = 400 µA; CDL (CDR)			0.4	V
Driver on resistor	$R_{ON}1$	$V_{DD} - V_{EE}$ = 30 V, $\lvert V_{DE} - V_O \rvert$ = 0.5 V*4; O1 to O80		1.5	3.0	kΩ
	$R_{ON}2$	$V_{DD} - V_{EE}$ = 20 V, $\lvert V_{DE} - V_O \rvert$ = 0.5 V*4; O1 to O80		2.0	3.5	kΩ
Standby current dissipation	I_{ST}	CDR (CDL) = V_{DD}, $V_{DD} - V_{EE}$ = 30 V CP = 3.0 MHz, no-load output: V_{SS}			200	µA
Operation current dissipation	I_{SS}*5	$V_{DD} - V_{EE}$ = 30 V, CP = 3 MHz, LOAD = 14 kHz, M = 35 Hz; V_{SS}			4.0	mA
	I_{SS}*6	$V_{DD} - V_{EE}$ = 30 V, CP = 3 MHz, LOAD = 14 kHz, M = 35 Hz; V_{EE}			0.1	mA
Input capacity	C_I	f = 3.0 MHz; CP		5		pF

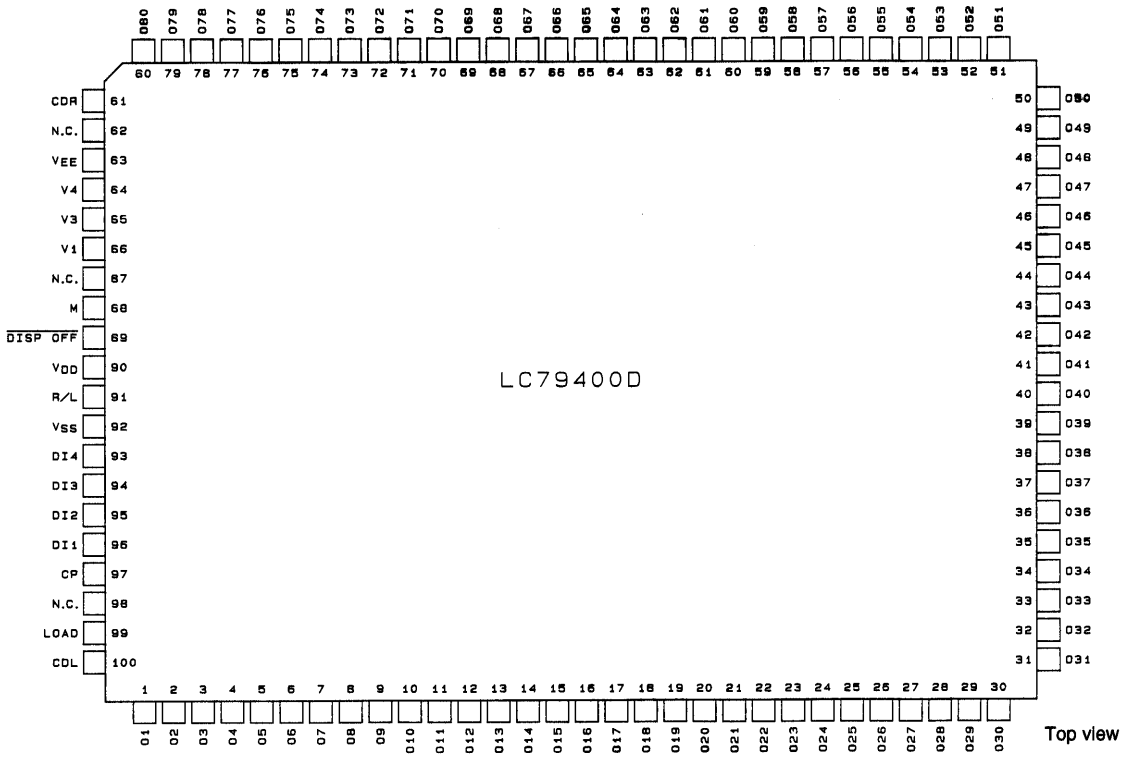
Note: 4. V_{DE} = V1 or V3 or V4 or V_{EE}, V1 = V_{DD}, V3 = 15/17 (V_{DD}-V_{EE}), V4 = 2/17 (V_{DD}-V_{EE})

5. I_{SS} current flows from V_{DD} to V_{SS}.
6. I_{EE} current flows from V_{DD} to V_{EE}.

Switching Characteristics at Ta = 25±2°C, V_{SS} = 0 V, V_{DD} = 5 V±10%

Parameter	Symbol	Conditions	min	typ	max	Unit
Output delay time	t_D	Load = 15 pF; CDR (CDL)			200	ns

Pin Assignment



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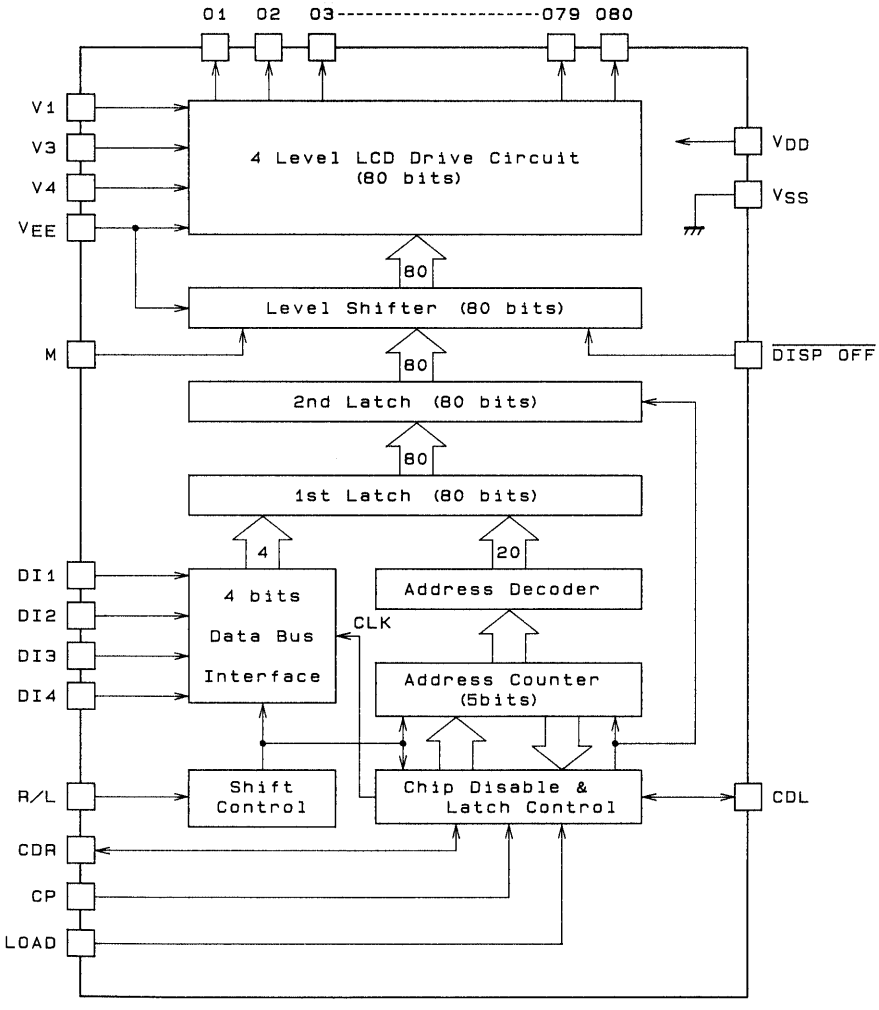
Equivalent Circuit Block Diagram



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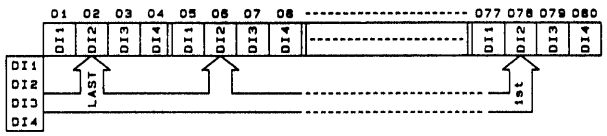
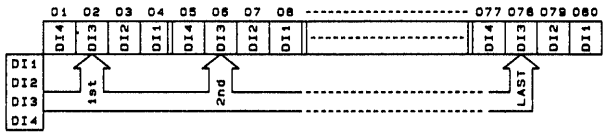
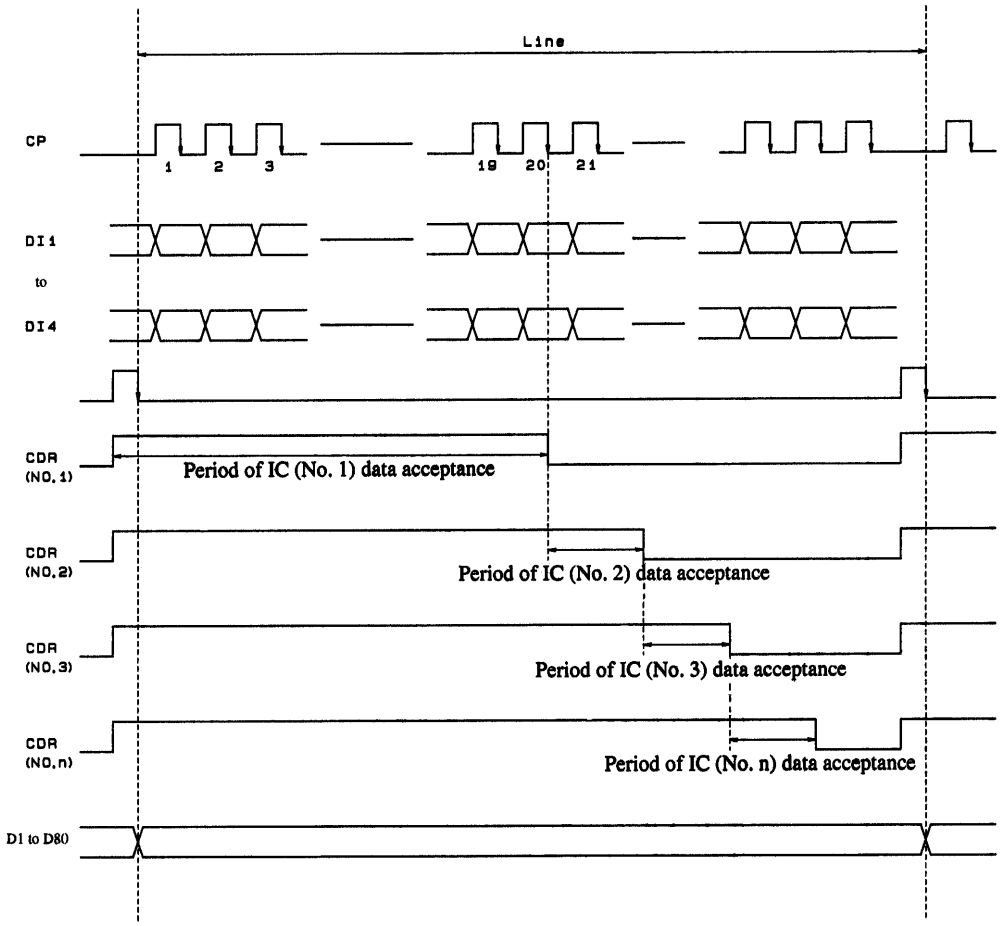
Pin Descriptions

<table>
<tr><th>Pin No</th><th>Pin name</th><th>Input/Output</th><th>Functions</th></tr>
<tr><td>90
92
83</td><td>V_{DD}
V_{SS}
V_{EE}</td><td>Power supply</td><td>V_{DD} and V_{SS}: Power supply for logic section

V_{DD} and V_{EE}: Power supply for LCD drive circuit</td></tr>
<tr><td>86
85
84</td><td>V1
V3
V4</td><td>Power supply</td><td>LCD drive level power supply
V1 and V_{EE} : Select level
V3 and V4 : Nonselect level</td></tr>
<tr><td>97</td><td>CP</td><td>Input</td><td>Display data shift clock (triggering on the trailing edge)</td></tr>
<tr><td>81
100</td><td>CDR
CDL</td><td>Input/Output
Input/Output</td><td>Chip disable pin
H level : Data not accepted
L level : Data accepted
<table>
<tr><th>Pin Name</th><th>Input/Output</th><th>R/L</th><th>Pin Description</th></tr>
<tr><td>CDR</td><td>Input</td><td rowspan="2">L</td><td>Control input pin for the IC's internal disable F/F.</td></tr>
<tr><td>CDL</td><td>Output</td><td>Output pin of the IC's internal disable F/F. Connects to the next stage CDR pin when establishing a cascade connection.</td></tr>
<tr><td>CDL</td><td>Input</td><td rowspan="2">H</td><td>Control input pin for the IC's internal disable F/F.</td></tr>
<tr><td>CDR</td><td>Output</td><td>Output pin of the IC's internal disable F/F. Connects to the next stage CDL pin when establishing a cascade connection.</td></tr>
</table></td></tr>
<tr><td>99</td><td>LOAD</td><td>Input</td><td>Display data latch clock (triggering on the trailing edge). On the trailing edge, output levels switch in response to the particular combination of display data, M and $\overline{\text{DISP OFF}}$ signals.</td></tr>
<tr><td>93
94
95
96</td><td>DI4
DI3
DI2
DI1</td><td>Input</td><td>
<table>
<tr><th>R/L</th><th>Input data and latch address</th></tr>
<tr><td>L</td><td> 
</td></tr>
<tr><td>H</td><td> 
</td></tr>
</table></td></tr>
<tr><td>88</td><td>M</td><td>Input</td><td>LCD drive output alternating signal</td></tr>
<tr><td>91</td><td>R/L</td><td>Input</td><td>Input pin which performs input/output switching for CDR and CDL pins and directional shift for 4-bit parallel input data.</td></tr>
<tr><td>1
2
⋮
79
80</td><td>O1
O2
⋮
O79
O80</td><td>Output</td><td>LCD drive output

The combination of display data, M signal, and $\overline{\text{DISP OFF}}$ signal can be used to create output levels as shown below.
<table>
<tr><th>M</th><th>Q</th><th>$\overline{\text{DISP OFF}}$</th><th>Output</th></tr>
<tr><td>L</td><td>L</td><td>H</td><td>V3</td></tr>
<tr><td>L</td><td>H</td><td>H</td><td>V1</td></tr>
<tr><td>H</td><td>L</td><td>H</td><td>V4</td></tr>
<tr><td>H</td><td>H</td><td>H</td><td>V_{EE}</td></tr>
<tr><td>*</td><td>*</td><td>L</td><td>V1</td></tr>
</table>
*Don't care
(To be set to either "H" or "L")</td></tr>
<tr><td>89</td><td>$\overline{\text{DISP OFF}}$</td><td>Input</td><td>Input pin which controls output pins O1 to O80. V1 level is output from O1 to O80 pin output during the low level input interval (See logic table).</td></tr>
</table>

Operation Timing (for R/L = H)



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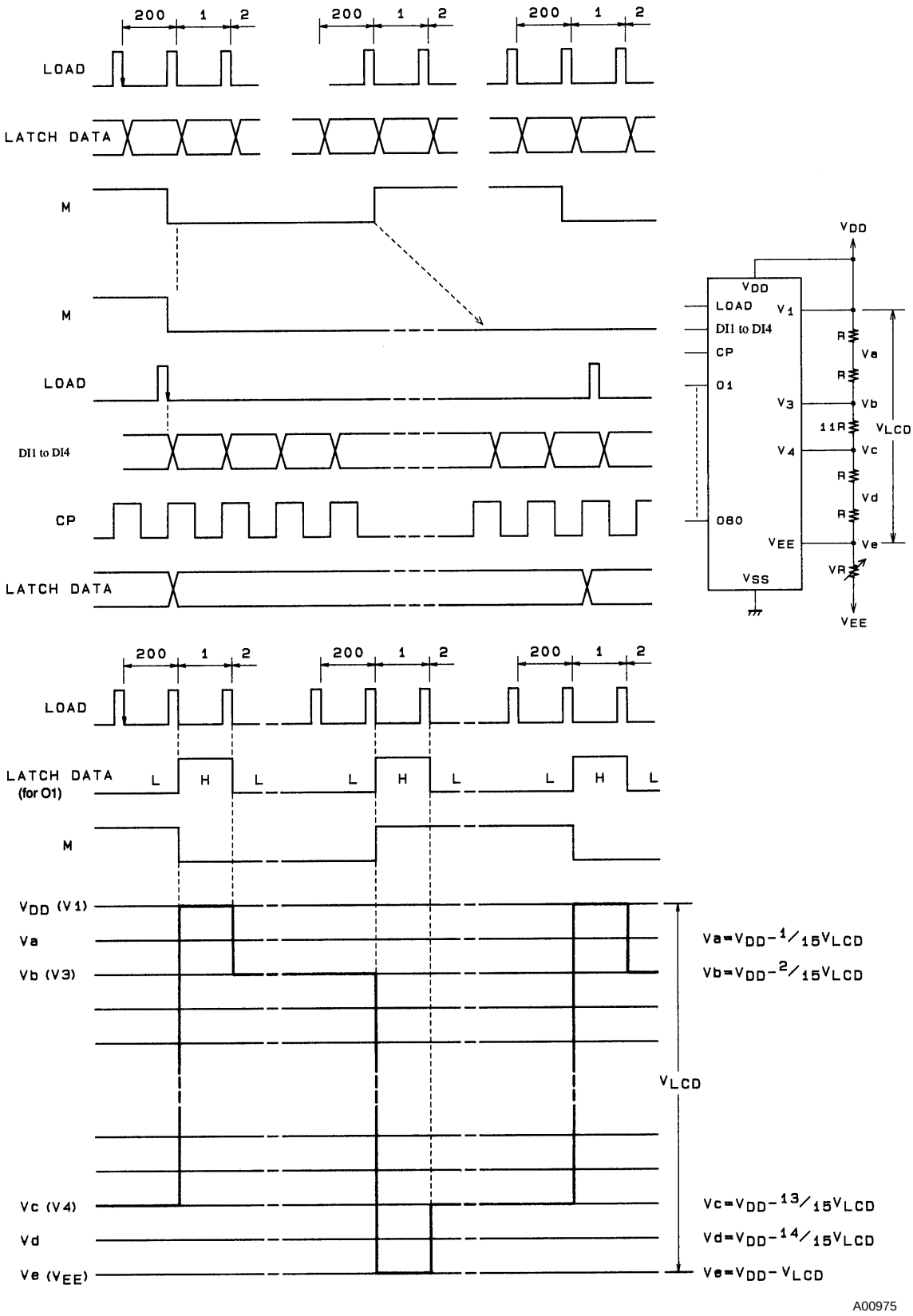
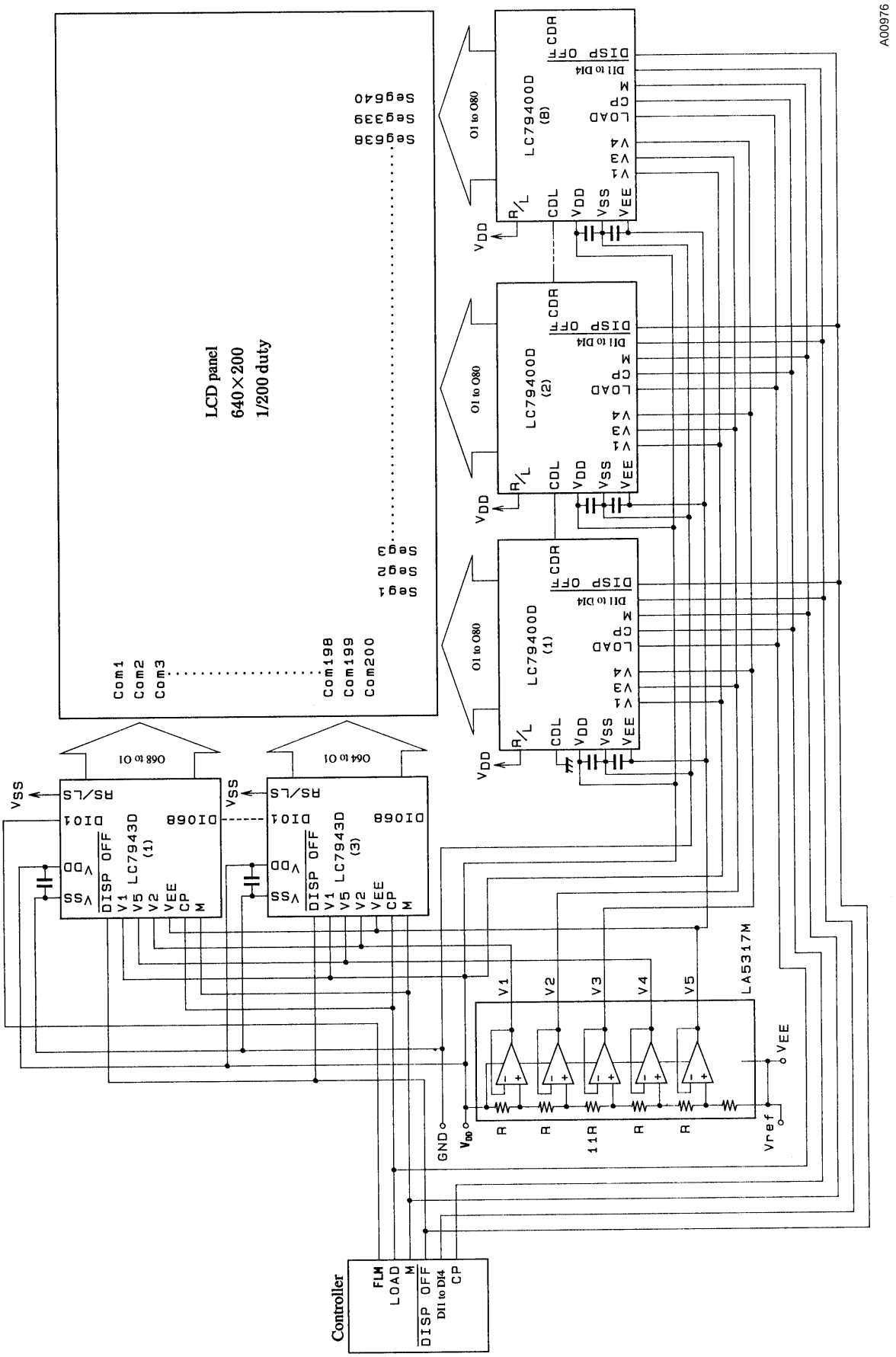
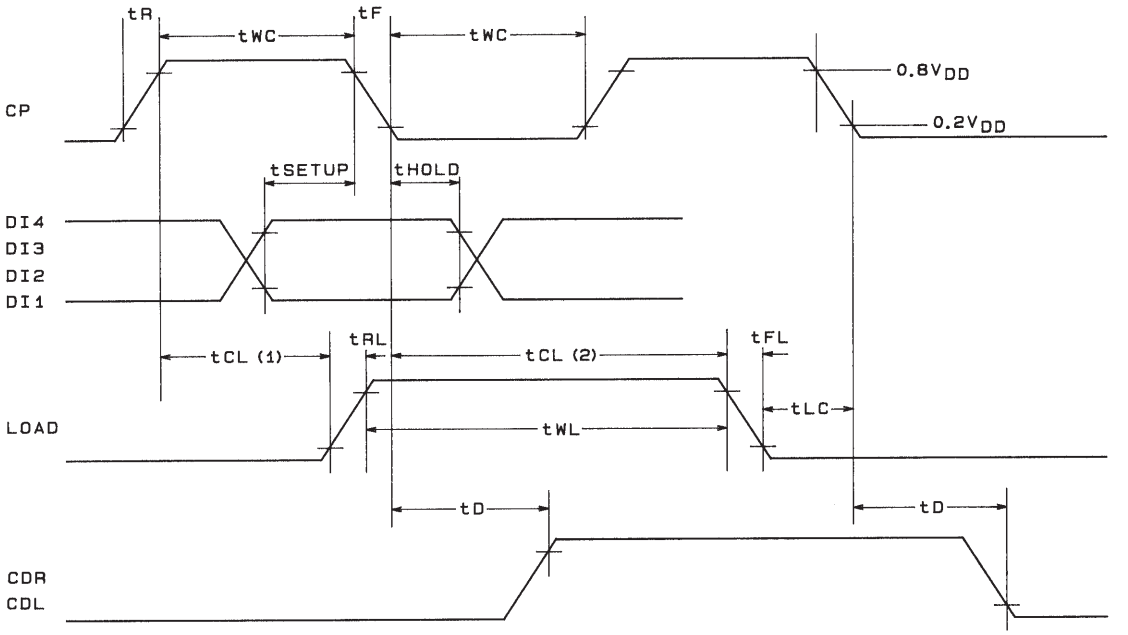
Time Chart (1/200 Duty 1/15 Bias)Switching Characteristics



Sample Application



Switching Characteristics



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