

HD61830B

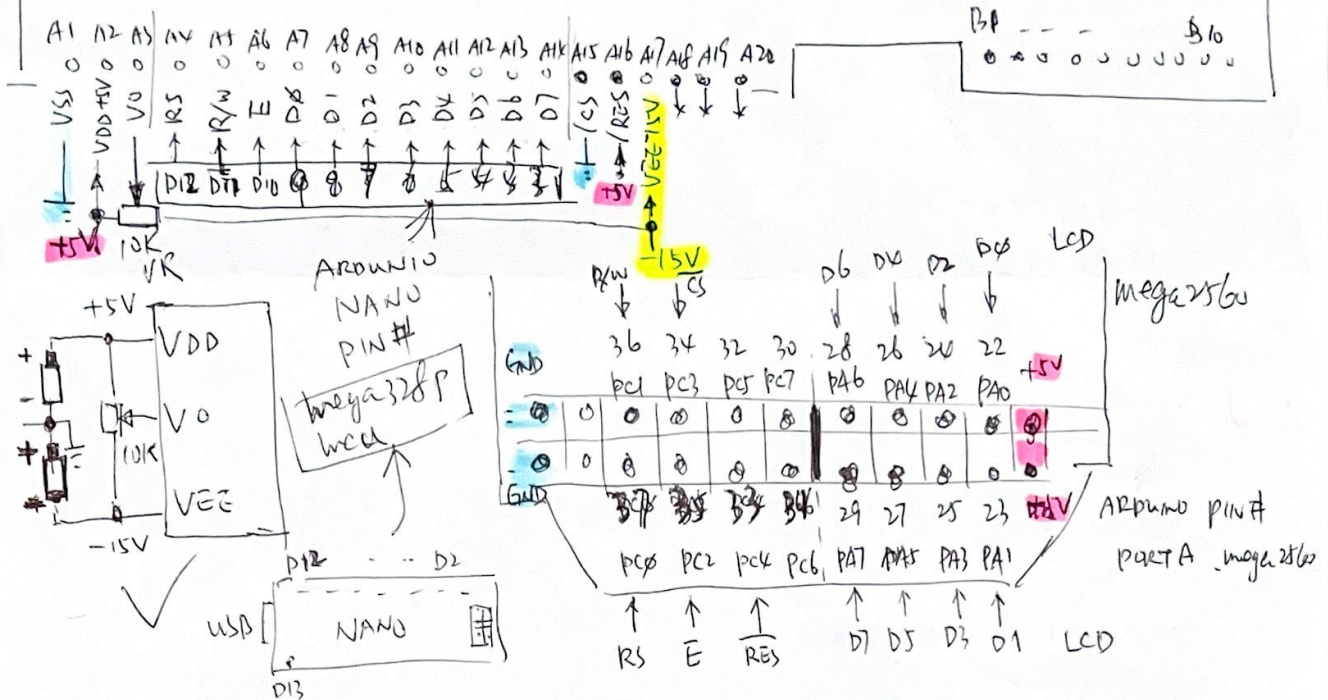
ASCII map INTERNAL ROM
0010.0000 space 0x20 ~ 0xFF C program

HITACHI LMG6401PL4Z

HD61830 / LC7940 / LC7940

240x128 LCM

U8g2 lib



D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	ARDUINO NANO / LUNO PIN#
PD0	PD1	PD2	PD3	PD4	PD5	PD6	PD7	PB0	PB1	PB2	PB3	PB4	mega328 / 16P pin#
CS	RES	RS	R/W	E	D0	D1	D2	D3	D4	D5	D6	D7	HD61830 PIN#
PB3	PB0	PB1	PB2	PD0	PD1	PD2	PD3	PD4	PD5	PD6	PD7		ARDUINO NANO / LUNO PIN#
D11	D12	PD8	PD9	D10	PD0	D1	D2	PD3	PD4	PD5	PD6	PD7	mega328P PIN# ARDUINO PAF
		PORT B / DDRB			PORTD / DDRC								mega port
		LCD_CTRL_PORT			LCD_DATA_PORT								LCD PORT

PD3 PD0 PD1 PD2
D3 D4 D5 D1 D2
PC3 PC6 PC0 PC1 PC2
A3 A4 A5 A1 A2

PORTC / DDRC 168P / 168PA

ATmega328P 16MHz XTAL

efuse = 0x05

hfuse = 0xda

lfuse = 0xff

efuse = 0xFF

hfuse = 0xBF

lfuse = 0x62

efuse = 0xFF

hfuse = 0xB9

lfuse = 0x62

1MHz

cpu

8MHz RC

LMG6401PLGE

240*128 Dots

FEATURES

- ◆ Blue on Grey STN Type
- ◆ Transflective Mode

MECHANICAL DATA

Item	Value	Unit
Module Dimensions	159.4*101*9.5	mm
Viewing Area	126*71	mm
Resolution	240*128	dots
Dot Size	0.47*0.47	mm
Dot Pitch	0.5*0.5	mm
Weight	160	g

OPTICAL DATA

Item	Symbol	Condition	Min	Typ	Max	Unit
Contrast Ratio	K	Ø=10°, θ=0°, Note 1	-	3.0	-	-
Brightness	-	-	-	10	-	cd/m ²
Viewing Direction			6			o'clock
Viewing Angle	Ø2 - Ø1	K=1.4, Note 1	-	40	-	degree
Response Time (Rise)	t _R	Ø=10°, θ=0°, Note 1	-	250	400	ms
Response Time (Fall)	t _F	Ø=10°, θ=0°, Note 1	-	300	450	ms

ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Condition	Min	Max	Unit
Supply Voltage (Logic)	V _{DD} - V _{SS}	-	0	7	V
Supply Voltage (LC Drive)	V _{DD} - V _{EE}	-	0	22	V
Input Voltage	V _I	-	V _{SS}	V _{DD}	V
Operating Temperature	T _{OP}	Note 4,5	0	50	°C
Storage Temperature	T _{ST}	Note 4,5	-20	60	°C

DATA INTERFACE PIN ASSIGNMENT

Pin No	Symbol	Level	Function
A1	VSS (0V)	-	Ground
A2	VDD (+5V)	-	Power supply for logic
A3	V0	-	Power supply for LCD drive
A4	RS	-	Register select
A5	R/W	-	Read / Write
A6	E	-	Enable
A7-A14	DB0 - DB7	-	Data bus
A15	Not CS	-	Chip select
A16	Not RES	-	Reset
A17	VEE (15.0V)	-	Power supply for LCD drive
A18-A20	NC	-	No connection
E1-E2	VEL	-	Power supply for EL driving

- ◆ Low Power EL Backlight
- ◆ Built-in LCD Controller HD61830B

ELECTRICAL CHARACTERISTICS

Item	Symbol	Condition	Min	Typ	Max	Unit
Supply Voltage (Logic)	V _{DD} - V _{SS}	-	4.75	5.0	5.25	V
Supply Voltage (LC Drive)	V _{EE} - V _{SS}	-	-14.5	-15.0	-15.5	V
Supply Current	I _{DD}	Note 2	-	6.0	-	mA
	I _{EE}	Note 2	-	4.0	-	mA
Input Voltage (High Level)	V _{IH}	High Level	0.8* V _{DD}	-	V _{DD}	V
Input Voltage (Low Level)	V _{IL}	Low Level	0	-	0.2* V _{DD}	V
Frame Frequency	f _{FLM}	-	-	75	-	Hz
Duty Ratio		-		1/128		-
Recommended LC Drive Voltage	V _{DD} - V _O	Duty=1/128 T=0°C, Ø=10°, Note 3	-	16.9	-	V
		Duty=1/128 T=25°C, Ø=10°, Note 3	-	15.8	-	V
		Duty=1/128 T=40°C, Ø=10°, Note 3	-	15.4	-	V
Backlight Tile Voltage	V _{EL}	f _{EL} =400Hz	-	100	-	Vrms
Backlight Lamp Frequency	f _{EL}	-	-	400	-	Hz
Backlight Tile Current	I _{EL}	V _{EL} =100Vrms, f _{EL} =400Hz	-	-	160	mA Arms

TIMING CHARACTERISTICS

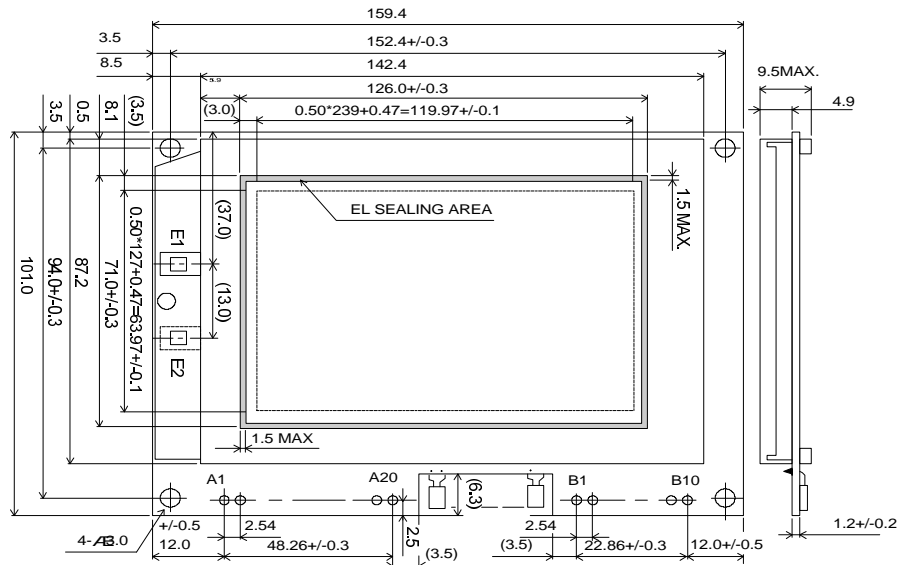
Item	Symbol	Min	Typ	Max	Unit
Enable cycle time	tCYC	1000	-	-	ns
Enable pulse width (High level)	tWEH	450	-	-	ns
Enable pulse width (Low level)	tWEL	450	-	-	ns
Enable rise time	tEr	-	-	25	ns
Enable fall time	tEf	-	-	25	ns
Set up time of CS, R/W, RS	tAS	140	-	-	ns
Set up time of Input Data	tDIS	225	-	-	ns
Data delay time	tDD	-	-	225	ns
Hold time of Data	tH	10	-	-	ns
Hold time of CS, R/W, RS	tAH	10	-	-	ns
Data hold time	tDH	20	-	-	ns

CONNECTORS

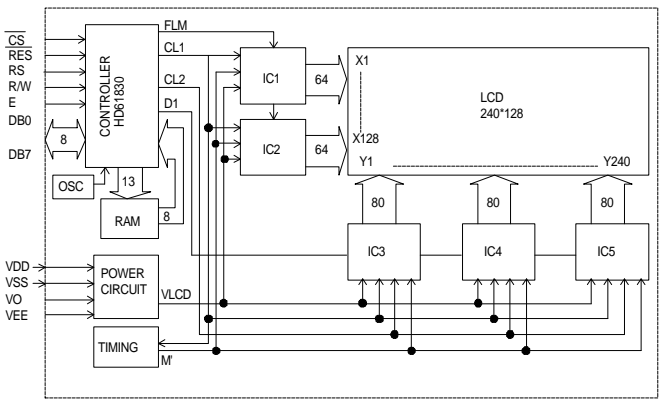
Connector	
No special connector required	

- Note1:Definition of optical data, see page XXX
- Note2:fFLM=75Hz, VDD-V0=15.8V, D=GND(VSS)
- Note3:Recommended LC driving voltage may fluctuate about +- 0.5V by each module
- Note4:Background colour of the LCD changes depending on temperature. Between 40-50°C optical characteristics of the LCD like contrast and viewing angle change but the LCD remains readable.
- Note5:Storage at -20°C < 48 hr.

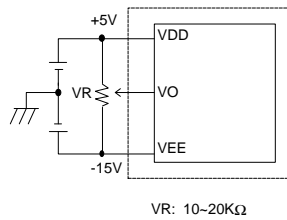
MECHANICAL DIMENSIONS



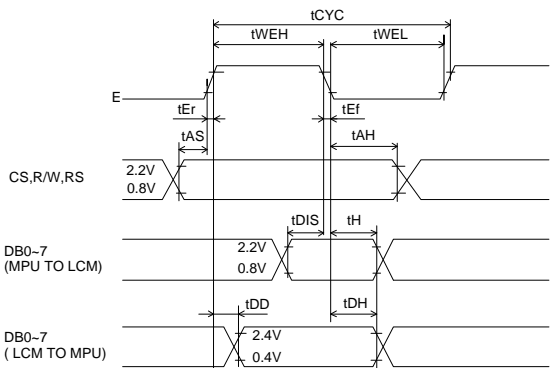
BLOCK DIAGRAM



POWER SUPPLY



INTERFACE TIMING DIAGRAM



POWER UP TIMING DIAGRAM

