On-Chip Power Delivery and Management

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On-Chip Power Delivery and Management

Fourth Edition

Springer

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ISBN 978-3-319-29393-6 ISBN 978-3-319-29395-0 (eBook)
DOI 10.1007/978-3-319-29395-0

Library of Congress Control Number: 2016936678

Printed on acid-free paper

This Springer imprint is published by Springer Nature
The registered company is Springer International Publishing AG Switzerland

To Sasha and Eva
To Victoria and Daniel
To Oksana, Elizabeth, and JulieAnn
To Elizabeth
To the memory of my late father, Nurettin Köse
To Laurie, Joseph, Shlomit, and Samuel

Preface to the Fourth Edition

Novel market segments such as intelligent transportation, revolutionary health care, sophisticated security systems, and smart energy have recently emerged, requiring increasingly diverse functionality such as RF circuits, power control, passive components, sensors/actuators, biochips, optical communication, and microelectromechanical devices. Integration of these non-digital functionalities at the board-level into system platforms such as systems-in-package (SiP), systems-on-chip (SoC), and three-dimensional (3-D) systems is a primary near- and long-term challenge of the semiconductor industry. The delivery and management of high-quality, highly efficient power have become primary design issues in these functionally diverse systems. Integrated in-package and distributed on-chip power delivery is currently under development across a broad spectrum of applications; the power delivery design process, however, is currently dominated by ad hoc approaches.

The lack of methodologies, architectures, and circuits for scalable on-chip power delivery and management is at the forefront of current heterogeneous system design issues. The objective of this book is to describe the many short- and long-term challenges of high-performance power delivery systems, provide insight and intuition into the behavior and design of next-generation power delivery systems, and suggest design solutions while providing a framework for addressing power objectives at the architectural, methodology, and circuit levels.

This book is based on the body of research carried out by the authors of previous editions of this book from 2001 to 2011. The first edition of the book, titled *Power Distribution Networks in High Speed Integrated Circuits*, was published in 2004 by Andrey V. Mezhiba and Eby G. Friedman. This first book focused on on-chip distribution networks, including electrical characteristics, relevant impedance phenomenon, and related design trade-offs. On-chip distributed power delivery, at that time an innovative paradigm shift in power delivery, was also introduced in the book. As the concept of integrated power delivery evolved, the important topic of on-chip decoupling capacitance was added to the book, which was released in 2008 with a new title, *Power Distribution Networks with On-Chip Decoupling Capacitors* by Mikhail Popovich, Andrey V. Mezhiba, and Eby G. Friedman. Later, this book was revised by Renatas Jakushokas, Mikhail Popovich, Andrey V. Mezhiba,

Selçuk Köse, and Eby G. Friedman to address emerging design and analysis challenges in on-chip power networks. This last edition was published with an identical title in 2011. Since the first book was published in 2004, the issue of power delivery has greatly evolved. The concept of on-chip distributed power delivery has been recognized as an important cornerstone to high-performance integrated circuits. A number of ultrasmall on-chip power supplies to support this on-chip focus have also been demonstrated.

While on-chip power integration has become a primary objective for system integration, research has remained focused on developing compact and efficient power supplies, lacking a methodology to effectively integrate and manage in-package and on-chip power delivery systems. The challenge has become greater as the diversity of modern systems increases, and dynamic voltage scaling (DVS) and dynamic voltage and frequency scaling (DVFS) become a part of the power management process. Hundreds of on-chip power domains with tens of different voltage levels have recently been reported, and thousand-core ICs are being considered. Scalable power delivery systems and the granularity of power management in DVS/DVFS multicore systems are limited by existing ad hoc approaches. To cope with this increasing design complexity and the quality and system-wide efficiency challenges of next-generation power delivery systems, enhanced methodologies to design and analyze scalable, hierarchical power management and delivery systems with fine granularity of dynamically controllable voltage levels are necessary. Updating the vision of on-chip power delivery networks, traditionally viewed as a passive network, is the primary purpose for publishing a new (fourth) edition of this book. Emphasis is placed on complex and scalable power delivery systems, system-wide efficiency, quality of power, and intelligent, real-time, fine-grain local power management. A framework that addresses various power objectives at the architectural, methodology, and circuit levels is described, providing a general solution for existing and emerging power delivery challenges and techniques. This book, titled *On-Chip Power Delivery and Management*, is authored by Inna P.-Vaisband, Renatas Jakushokas, Mikhail Popovich, Andrey V. Mezhiba, Selçuk Köse, and Eby G. Friedman as the fourth edition of this series of books.

The chapters of the book are now separated into eight parts. Power networks, inductive properties, electromigration, and decoupling capacitance within integrated circuits are described in Part I (Chaps. 1, 2, 3, 4, 5, and 6). In Part II (Chaps. 7, 8, 9, and 10), the design of on-chip power distribution networks and power supplies is discussed. Circuits for on-chip power delivery and management and integrated power delivery systems are described in Part IV (Chaps. 17, 18, 19, and 20). Closed-form expressions for power grid analysis, modeling and optimization of power networks, and the codesign of power supplies are presented in Part V (Chaps. 21, 22, 23, 24, 25, 26, and 27). Since noise within the power grid is a primary design constraint, this issue is reviewed in Part VI (Chaps. 28, 29, 30, 31, 32, 33, and 34). Multilayer power distribution networks are the focus of Part VII (Chaps. 35, 36, 37, 38, and 39). In Part III (Chaps. 12, 13, 14, and 15), the issue of placing on-chip decoupling capacitors is discussed. In Part VIII (Chaps. 40, 41, 42, and 43), multiple power supply systems are described. The focus of this part is on those integrated

circuits where multiple on-chip power supplies are required. In Part IX, some concluding comments, the appendices, and additional information are provided.

This revised and updated material is based on recent research by Inna P.-Vaisband developed between 2009 and 2015 at the University of Rochester during her doctoral studies under the supervision of Prof. Eby G. Friedman. The new chapters focus on design complexity, system scalability, and system-wide optimization of power delivery and management systems. The concept of intelligent power delivery is introduced, and a framework for on-chip power delivery and management is described that provides local power control and real-time management for sharing energy resources.

The book covers a wide spectrum of issues related to on-chip power networks and systems. The authors believe that this revised edition provides the latest information on a dynamic and highly significant topic of primary importance to both the industrial and academic research and development communities.

Acknowledgments

The authors would like to thank Chuck Glaser for his sincere encouragement and enthusiastic support of the publication of this book. The authors would also like to thank Burt Price and Jeff Fischer from Qualcomm and Avinoam Kolodny from Technion – Israel Institute of Technology for their collaboration and support.

The research described in this book has been supported in part by the Binational Science Foundation under grant no. 2012139; the National Science Foundation under grant nos. CCF-1329374, CCF-1526466, and CNS-1548078; the IARPA under grant no. W911NF-14-C-0089 and by grants from Qualcomm, Cisco Systems, and Intel.

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December 2015

Preface to the Third Edition

The first planar circuit was fabricated by Fairchild Semiconductor Company in 1959. Since then, the evolution of the integrated circuit has progressed, now providing billions of transistors on a single monolithic substrate. These integrated circuits are an integral and nearly essential part of our modern life. The power consumed by a typical $20 \times 20\,\text{mm}^2$ microprocessor is in the range of several hundreds of watts, making integrated circuits one of the highest power consumers per unit area. With such a high rate of power consumption, the problem of delivering power on-chip has become a fundamental issue. The focus of this book is on distributing power within high-performance integrated circuits.

In 2004, the book titled *Power Distribution Networks in High Speed Integrated Circuits* by A. V. Mezhiba and E. G. Friedman was published to describe, for the first time in book form, the design and analysis of power distribution networks within integrated circuits. The book described different aspects of on-chip power distribution networks, starting with a general introduction and ending with a discussion of various design trade-offs in on-chip power distribution networks. Later, the important and highly relevant topic of decoupling capacitance was added to this book. Due to the significant change in size and focus, the book was released in 2008 as a new first edition with a new title, *Power Distribution Networks with On-Chip Decoupling Capacitors* by M. Popovich, A. V. Mezhiba, and E. G. Friedman. Since this revised book was published, new design and analysis challenges in on-chip power networks have emerged.

The rapidly evolving field of integrated circuits has required an innovative perspective on on-chip power generation and distribution, shifting the authors' research focus to these new challenges. Updating knowledge on chip-based power distribution networks is the primary purpose for publishing a second edition of *Power Distribution Networks with On-Chip Decoupling Capacitors*. Focus is placed on complexity issues related to power distribution networks, developing novel design methodologies and providing solutions for specific design and analysis issues. In this second edition, the authors have revised and updated previously

published chapters and added four new chapters to the book. This second edition has also been partitioned into subareas (called parts) to provide a more intuitive flow to the reader.

The organization of the book is now separated into seven parts. A general background, introducing power networks, inductive properties, electromigration, and decoupling capacitance within integrated circuits, is provided in Part I (Chaps. 1, 2, 3, 4, 5, 6, and 7). In Part II (Chaps. 8, 9, 10, 11, and 12), the design of on-chip power distribution networks is discussed. Since noise within the power grid is a primary design constraint, this issue is reviewed in Part III (Chaps. 13, 14, 15, 16, 17, 18, and 19). In Part IV (Chaps. 20, 21, 22, and 23), the primary issue of placing on-chip decoupling capacitors is discussed. Multilayer power distribution networks are the focus of Part V (Chaps. 24, 25, and 26). In Part VI (Chaps. 27, 28, 29, and 30), multiple power supply systems are described. The focus of this part is on those integrated circuits where several on-chip power supplies are required. In Part VII, some concluding comments, the appendices, and additional information are provided.

This revised and updated material is based on recent research by Renatas Jakushokas and Selçuk Köse developed between 2005 and 2010 at the University of Rochester during their doctoral studies under the supervision of Prof. Eby G. Friedman. The emphasis of these newly added chapters is on the complexity of power distribution networks. Models for commonly used meshed and interdigitated interconnect structures are described. These models can be used to accurately and efficiently estimate the resistance and inductance of complex power distribution networks. With these models, on-chip power networks can be efficiently analyzed and designed, greatly enhancing the performance of the overall integrated circuit.

Acknowledgments

The authors would like to thank Charles Glaser from Springer for making this book a reality. The authors are also grateful to Dr. Sankar Basu of the National Science Foundation for his support over many years. We are sincerely thankful to Dr. Emre Salman for endless conversations and discussions, leading to novel research ideas and solutions.

This research has been supported in part by the National Science Foundation under grant nos. CCF-0541206, CCF-0811317, and CCF-0829915; grants from the New York State Office of Science, Technology and Academic Research to the Center for Advanced Technology in Electronic Imaging Systems; and grants from Intel Corporation, Eastman Kodak Company, and Freescale Semiconductor Corporation.

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September 2010

Preface to the Second Edition

The purpose of this book is to provide insight and intuition into the behavior and design of power distribution systems with decoupling capacitors for application to high-speed integrated circuits. The primary objectives are threefold. First is to describe the impedance characteristics of the overall power distribution system, from the voltage regulator through the printed circuit board and package onto the integrated circuit to the power terminals of the on-chip circuitry. The second objective of this book is to discuss the inductive characteristics of on-chip power distribution grids and the related circuit behavior of these structures. Finally, the third primary objective is to present design methodologies for efficiently placing on-chip decoupling capacitors in nanoscale integrated circuits.

Technology scaling has been the primary driver behind the amazing performance improvement of integrated circuits over the past several decades. The speed and integration density of integrated circuits have dramatically improved. These performance gains, however, have made distributing power to the on-chip circuitry a difficult task. Highly dense circuitry operating at high clock speeds has increased the distributed current to many tens of amperes, while the noise margin of the power supply has shrunk consistent with decreasing power supply levels. These trends have elevated the problems of power distribution and allocation of the on-chip decoupling capacitors to the forefront of several challenges in developing high-performance integrated circuits.

This book is based on the body of research carried out by Mikhail Popovich from 2001 to 2007 and Andrey V. Mezhiba from 1998 to 2003 at the University of Rochester during their doctoral studies under the supervision of Professor Eby G. Friedman. It is apparent to the authors that although various aspects of the power distribution problem have been addressed in numerous research publications, no text exists that provides a unified focus on power distribution systems and related design problems. Furthermore, the placement of on-chip decoupling capacitors has traditionally been treated as an algorithmic oriented problem. A more electrical perspective, both circuit models and design techniques, has been used in this

book for presenting how to efficiently allocate on-chip decoupling capacitors. The fundamental objective of this book is to provide a broad and cohesive treatment of these subjects.

Another consequence of higher speed and greater integration density has been the emergence of inductance as a significant factor in the behavior of on-chip global interconnect structures. Once clock frequencies exceeded several hundred megahertz, incorporating on-chip inductance into the circuit analysis process became necessary to accurately describe signal delays and waveform characteristics. Although on-chip decoupling capacitors attenuate high-frequency signals in power distribution networks, the inductance of the on-chip power interconnect is expected to become a significant factor in multi-gigahertz digital circuits. An important objective of this book, therefore, is to clarify the effects of inductance on the impedance characteristics of on-chip power distribution grids and to provide an understanding of related circuit behavior.

The organization of the book is consistent with these primary goals. The first eight chapters provide a general description of distributing power in integrated circuits with decoupling capacitors. The challenges of power distribution are introduced and the principles of designing power distribution systems are described. A general background to decoupling capacitors is presented followed by a discussion of the use of a hierarchy of capacitors to improve the impedance characteristics of the power network. An overview of related phenomena, such as inductance and electromigration, is also presented in a tutorial style. The following seven chapters are dedicated to the impedance characteristics of on-chip power distribution networks. The effect of the interconnect inductance on the impedance characteristics of on-chip power distribution networks is evaluated. The implications of these impedance characteristics on circuit behavior are also discussed. On-chip power distribution grids are described, exploiting multiple power supply voltages and multiple grounds. Techniques and algorithms for the computer-aided design and analysis of power distribution networks are also described; however, the emphasis of the book is on developing circuit intuition and understanding the electrical principles that govern the design and operation of power distribution systems. The remaining five chapters focus on the design of a system of on-chip decoupling capacitors. Methodologies for designing power distribution grids with on-chip decoupling capacitors are also presented. These techniques provide a solution for determining the location and magnitude of the on-chip decoupling capacitance to mitigate on-chip voltage fluctuations.

Acknowledgments

The authors would like to thank Alex Greene and Katelyn Stanne from Springer for their support and assistance. We are particularly thankful to Bill Joyner and Dale Edwards from the Semiconductor Research Corporation and Marie Burnham, Olin Hartin, and Radu Secareanu from Freescale Semiconductor Corporation for

their continued support of the research project that culminated in this book. The authors would also like to thank Emre Salman for his corrections and suggestions on improving the quality of the book. Finally, we are grateful to Michael Sotman and Avinoam Kolodny from Technion – Israel Institute of Technology for their collaboration and support.

The original research work presented in this book was made possible in part by the Semiconductor Research Corporation under contract nos. 99–TJ–687 and 2004–TJ–1207; the DARPA/ITO under AFRL contract F29601–00–K–0182; the National Science Foundation under contract nos. CCR–0304574 and CCF–0541206; grants from the New York State Office of Science, Technology and Academic Research to the Center for Advanced Technology in Electronic Imaging Systems; and by grants from Xerox Corporation, IBM Corporation, Lucent Technologies Corporation, Intel Corporation, Eastman Kodak Company, Intrinsix Corporation, Manhattan Routing, and Freescale Semiconductor Corporation.

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June 2007

Preface to the First Edition

The primary purpose of this book is to provide insight and intuition into the behavior and design of power distribution systems for high-speed integrated circuits. The objective is twofold. First is to describe the impedance characteristics of the overall power distribution system, from the voltage regulator through the printed circuit board and package onto the integrated circuit to the power terminals of the on-chip circuitry. The second objective of this book is to discuss the inductive characteristics of on-chip power distribution grids and the related circuit behavior of these structures.

Technology scaling has been the primary driver behind improving the performance characteristics of integrated circuits over the past several decades. The speed and integration density of integrated circuits have dramatically improved. These performance gains, however, have made distributing power to the on-chip circuitry a difficult task. Highly dense circuitry operating at high clock speeds has increased the distributed current to tens of amperes, while the noise margin of the power supply has been shrunk consistent with decreasing power supply levels. These trends have elevated the problem of power distribution to the forefront of challenges in developing high-performance integrated circuits.

This monograph is based on the body of research carried out by Andrey V. Mezhiba from 1998 to 2003 at the University of Rochester during his doctoral study under the supervision of Professor Eby G. Friedman. It has become apparent to the authors during this period that although various aspects of the power distribution problem have been addressed in numerous research publications, no text provides a unified description of power distribution systems and related design problems. The primary objective of this book is therefore to provide a broad and cohesive, albeit not comprehensive, treatment of this subject.

Another consequence of higher speed and greater integration density has been the emergence of inductance as a significant factor in the behavior of on-chip global interconnect structures. Once clock frequencies exceeded several hundred megahertz, incorporating on-chip line inductance into the circuit analysis process became necessary to accurately describe signal delays and rise times. Although on-chip decoupling capacitors attenuate high-frequency signals in power distribution

networks, the inductance of the on-chip power interconnect is expected to become a significant factor in multi-gigahertz digital circuits. Another objective of this book, therefore, is to describe the effects of inductance on the impedance characteristics of on-chip power distribution grids and to develop an understanding of related circuit behavior.

The organization of the book is consistent with these primary goals. The first eight chapters provide a general description of distributing power in integrated circuits. The challenges of power distribution are introduced and the principles of designing power distribution systems are described. A hierarchy of decoupling capacitors used to improve the impedance characteristics is reviewed. An overview of related phenomena, such as inductance and electromigration, is also presented in a tutorial style. The following six chapters are dedicated to the impedance characteristics of on-chip power distribution networks. The effect of the interconnect inductance on the impedance characteristics of on-chip power distribution networks is evaluated. The implications of these impedance characteristics for the circuit behavior are also discussed. Techniques and algorithms for the computer-aided design and analysis of power distribution networks are also described; however, the emphasis of the book is on developing circuit intuition and understanding the principles that govern the design and operation of power distribution systems.

Acknowledgments

The authors would like to thank Michael Hackett from Kluwer Academic Publishers for his support and assistance. We are particularly thankful to Bill Joyner from the Semiconductor Research Corporation for his continuing support of the research project that culminated in this book. Finally, we are sincerely grateful to Bilyana Boyadjieva for designing the cover of the book.

The original research work presented in this monograph was made possible in part by the Semiconductor Research Corporation under contract no. 99-TJ-687; the DARPA/ITO under AFRL contract F29601-00-K-0182; grants from the New York State Office of Science, Technology and Academic Research to the Center for Advanced Technology-Electronic Imaging Systems and the Microelectronics Design Center; and grants from Xerox Corporation, IBM Corporation, Intel Corporation, Lucent Technologies Corporation, and Eastman Kodak Company.

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Inna Vaisband received the Bachelor of Science degree in computer engineering and the Master of Science degree in electrical engineering from the Technion-Israel Institute of Technology, Haifa, Israel in, respectively, 2006 and 2009, and the Ph.D. degree in electrical engineering from the University of Rochester, Rochester, New York in 2015.

She is currently a post-doctoral researcher with the Department of Electrical Engineering, University of Rochester, Rochester, New York. Between 2003 and 2009, she held a variety of software and hardware R&D positions at Tower Semiconductor Ltd., G-Connect Ltd., and IBM Ltd., all in Israel. In summer 2012, Inna was a Visiting Researcher at Stanford University. Her current research interests include the analysis and design of high performance integrated circuits, analog circuits, and on-chip power delivery and management. Dr. Vaisband is an Associate Editor of the *Microelectronics Journal*.

Renatas Jakushokas was born in Kaunas, Lithuania. He received the B.Sc. degree in electrical engineering from Ort-Braude College, Karmiel, Israel in 2005, and the M.S. and Ph.D. degrees in electrical and computer engineering from the University of Rochester, Rochester, New York in, respectively, 2007 and 2011.

He was previously an intern at Intrinsix Corporation, Fairport, New York, in 2006, working on Sigma Delta ADCs. In the summer of 2007, he interned with Eastman Kodak Company, Rochester, New York, where he designed a high speed and precision comparator for high performance ADCs. During the summer of 2008, he was with Freescale Semiconductor Corporation, Tempe, Arizona where he worked on developing a noise coupling estimation calculator, supporting the efficient evaluation of diverse substrate isolation techniques. In 2011, Renatas joined Qualcomm Inc., where he works on custom high speed circuit design, power and signal integrity, power distribution networks, development/optimization/placement of on-die decoupling capacitors, and power estimation/correlation/optimization.

He currently holds a US patent and is the author of additional disclosed patents. He has authored a book and published over ten journal and conference papers. Dr. Jakushokas participates in conference committees and is currently serving as an editor for the *Microelectronics Journal*. His research interests are in the areas of power distribution, noise evaluation, signal and power integrity, substrate modeling/analysis, and optimization techniques for high performance integrated circuit design.

Mikhail Popovich was born in Izhevsk, Russia in 1975. He received the B.S. degree in electrical engineering from Izhevsk State Technical University, Izhevsk, Russia in 1998, and the M.S. and Ph.D. degrees in electrical and computer engineering from the University of Rochester, Rochester, New York in, respectively, 2002 and 2007.

He was an intern at Freescale Semiconductor Corporation, Tempe, Arizona in the summer of 2005, where he worked on signal integrity in RF and mixed-signal ICs and developed design techniques and methodologies

for placing distributed on-chip decoupling capacitors. His professional experience also includes characterization of substrate and interconnect crosstalk noise in CMOS imaging circuits for Eastman Kodak Company, Rochester, New York. He has authored several conference and journal papers in the areas of power distribution networks in CMOS VLSI circuits, placement of on-chip decoupling capacitors, and the inductive properties of on-chip interconnect. He holds several US patents. In 2007, Mikhail joined Qualcomm Corporation, where he works on power distribution networks, power and signal integrity, low power techniques, and interconnect design including on-chip inductive effects, noise coupling, and placement of on-chip decoupling capacitors.

Mr. Popovich received the Best Student Paper Award at the ACM Great Lakes Symposium on VLSI in 2005, and the GRC Inventor Recognition Award from the Semiconductor Research Corporation in 2007.

Andrey V. Mezhiba graduated from the Moscow Institute of Physics and Technology in 1996 with a Diploma in Physics. He continued his studies at the University of Rochester where he received the Ph.D. degree in electrical and computer engineering in 2004. Andrey authored several conference and journal papers in the areas of power distribution networks, on-chip inductance, circuit coupling, and signal integrity; he holds several patents. Andrey is currently with Intel Corporation working on phase-locked loops and other mixed-signal circuits in advanced CMOS technologies.

Selçuk Köse received the B.S. degree in electrical and electronics engineering from Bilkent University, Ankara, Turkey in 2006, and the M.S. and Ph.D. degrees in electrical engineering from the University of Rochester, Rochester, NY, respectively, in 2008 and 2012.

He is currently an Assistant Professor at the Department of Electrical Engineering, University of South Florida, Tampa, Florida. He was a part-time engineer at the Scientific and Technological Research Council (TÜBİTAK), Ankara, Turkey in 2006. He was with the Central Technology and Special Cir-

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Dr. Köse received the National Science Foundation CAREER Award in 2014, University of South Florida College of Engineering Outstanding Junior Research Achievement Award in 2014, and Cisco Research Award in 2015. He is currently serving on the editorial board of the *Journal of Circuits, Systems, and Computers* and the *Microelectronics Journal*. He is a member of the technical program committee of a number of conferences.

Eby G. Friedman received the B.S. degree from Lafayette College in 1979, and the M.S. and Ph.D. degrees from the University of California, Irvine, in 1981 and 1989, respectively, all in electrical engineering.

From 1979 to 1991, he was with Hughes Aircraft Company, rising to the position of manager of the Signal Processing Design and Test Department, responsible for the design and test of high performance digital and analog ICs. He has been with the Department of Electrical and Computer Engineering at the University of Rochester since 1991, where he is a Distinguished Professor and the Director of the High Performance VLSI/IC Design and Analysis Laboratory. He is also a Visiting Professor at the Technion—Israel Institute of Technology. His current research and teaching interests are in high performance synchronous digital and mixed-signal microelectronic design and analysis with application to high speed portable processors and low power wireless communications.

He is the author of almost 500 papers and book chapters, 13 patents, and the author or editor of 16 books in the fields of high speed and low power CMOS design techniques, 3-D integration, high speed interconnect, and the theory and application of synchronous clock and power distribution networks. Dr. Friedman is the Editor-in-Chief of the *Microelectronics Journal*, a Member of the editorial boards of the *Analog Integrated Circuits and Signal Processing*, *Journal of Low Power Electronics*, and *Journal of Low Power Electronics and Applications*, and

a Member of the technical program committee of numerous conferences. He previously was the Editor-in-Chief and Chair of the steering committee of the *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, the Regional Editor of the *Journal of Circuits, Systems and Computers*, a Member of the editorial board of the *Proceedings of the IEEE*, *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, and *Journal of Signal Processing Systems*, a Member of the Circuits and Systems (CAS) Society Board of Governors, Program and Technical chair of several IEEE conferences, and a recipient of the IEEE Circuits and Systems 2013 Charles A. Desoer Technical Achievement Award, a University of Rochester Graduate Teaching Award, a College of Engineering Teaching Excellence Award, and is a member of the University of California, Irvine Engineering Hall of Fame. Dr. Friedman is a Senior Fulbright Fellow and an IEEE Fellow.