ASM2824 /ASM2812 Schematics

Revision 0.3

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Title: COVER SHEET		
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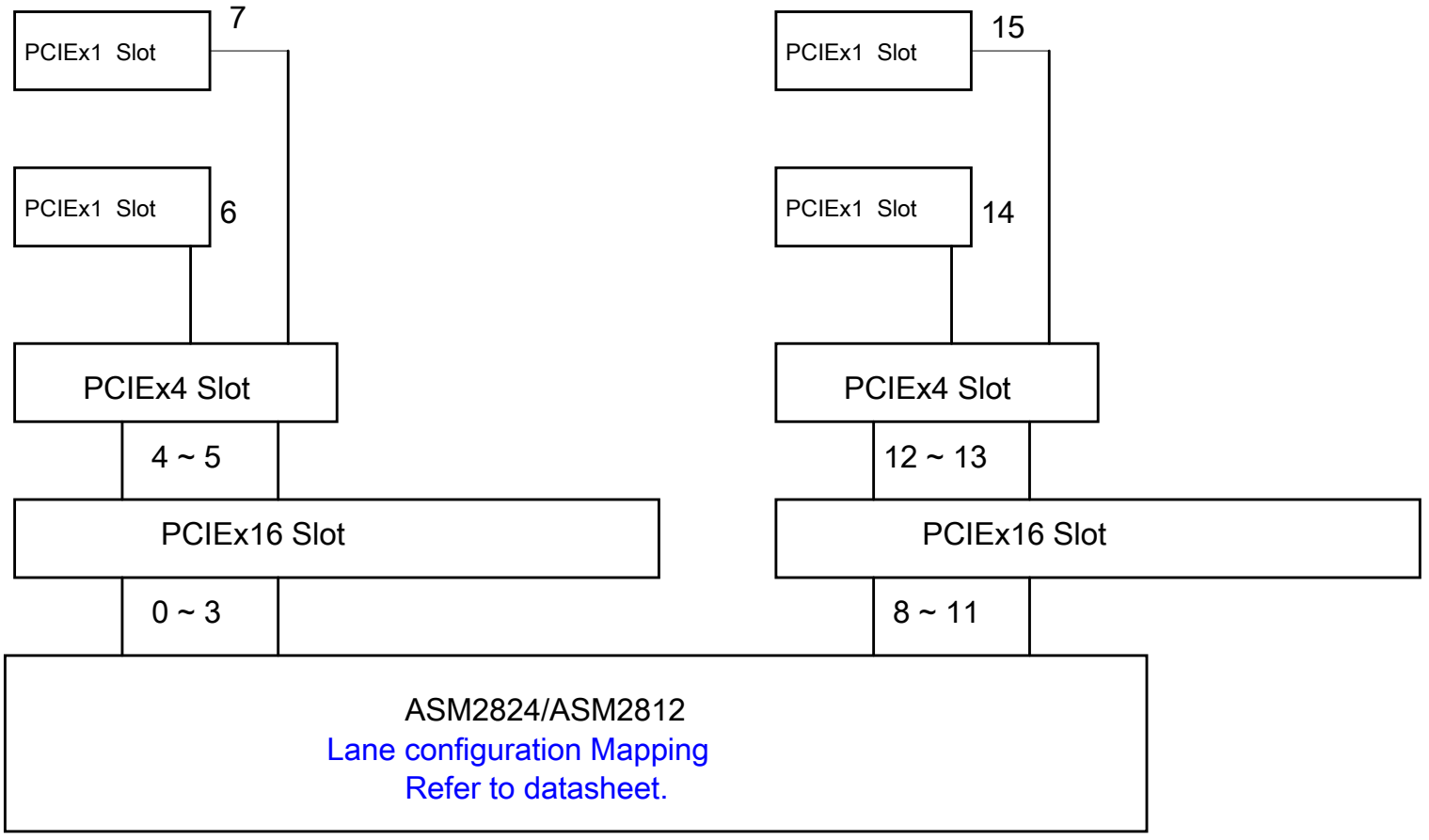

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Title: BLOCK DIAGRAM		
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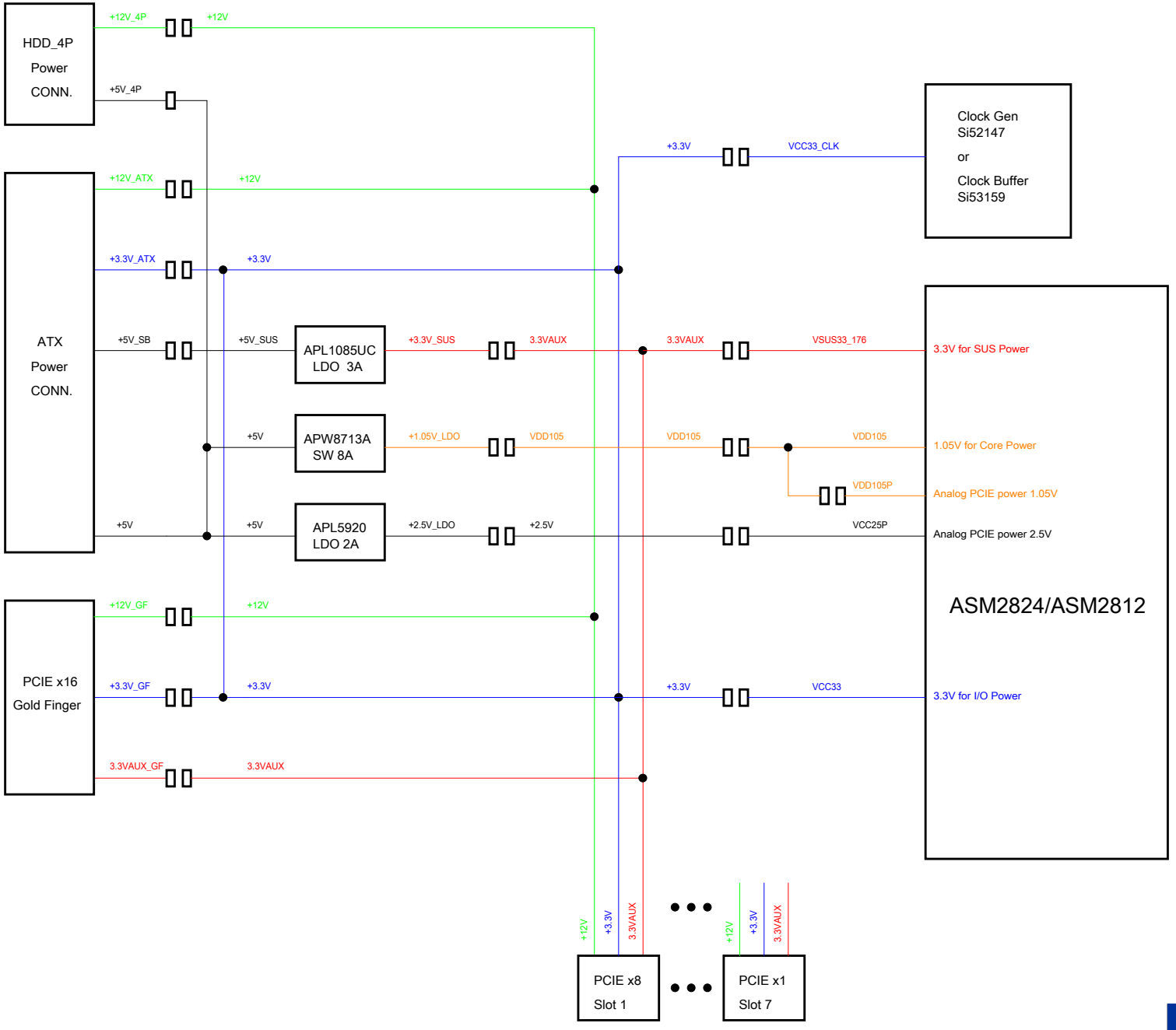

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Title: POWER BLOCK DIAGRAM		
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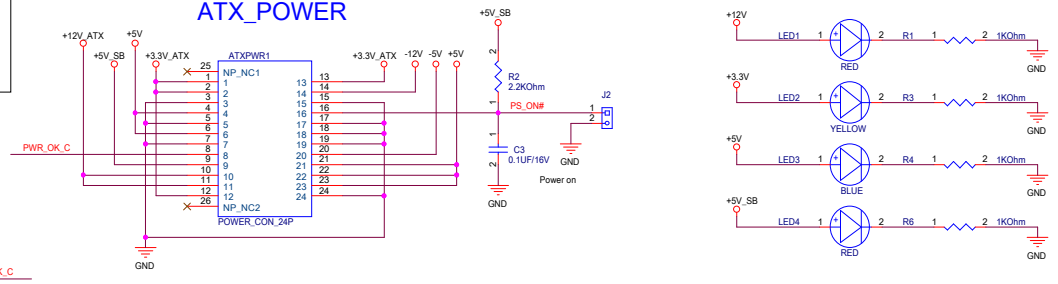
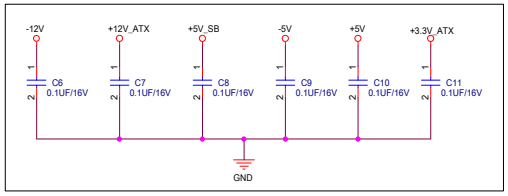
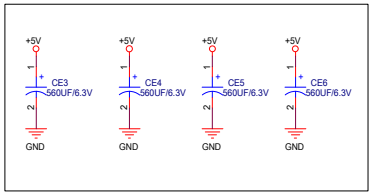
250W ATX
3.3V--->20A
5V----->25A
12V---->18A

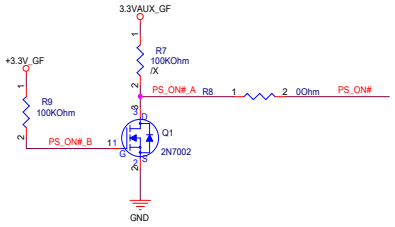
ATX_POWER



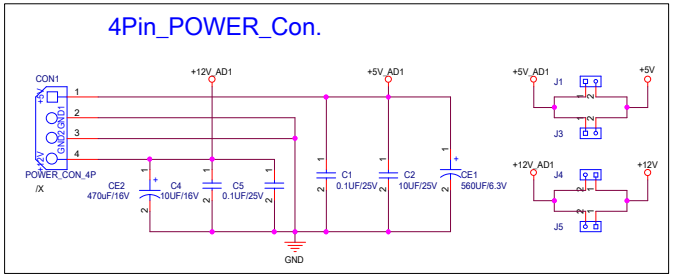
Close to ATX PWR con.



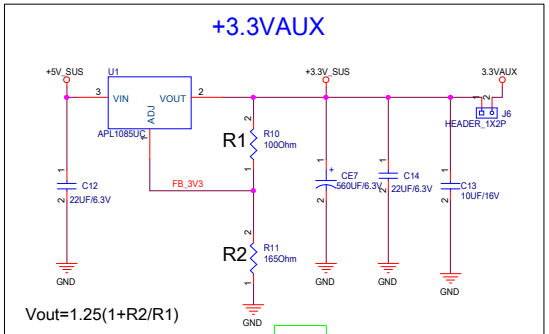




4Pin_POWER_Con.



+3.3VAUX



Vout=1.25(1+R2/R1)

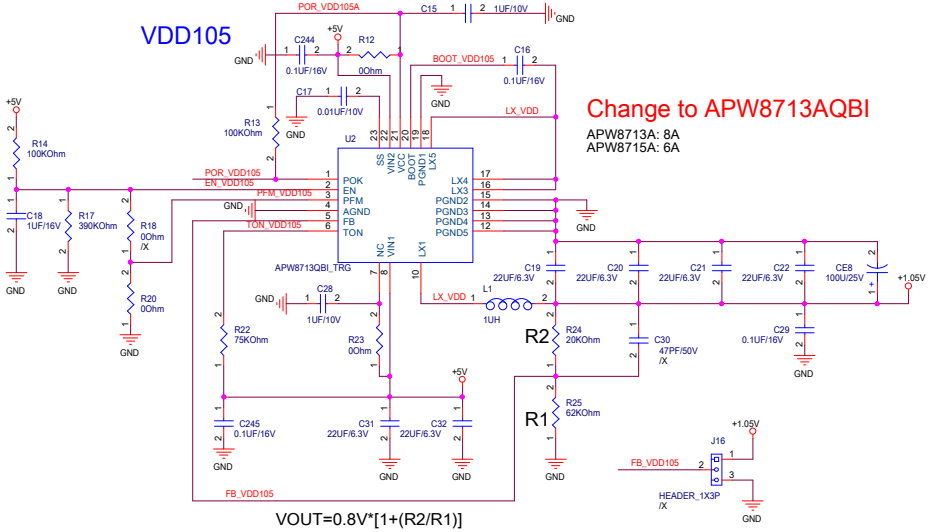
3.3=1.25(1+165/100)

2.5=1.25(1+100/100)

102=165//270

RS2

VDD105



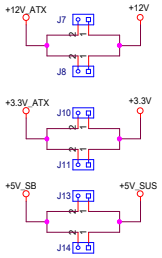
Change to APW8713AQBI

APW8713A: 8A

APW8715A: 6A

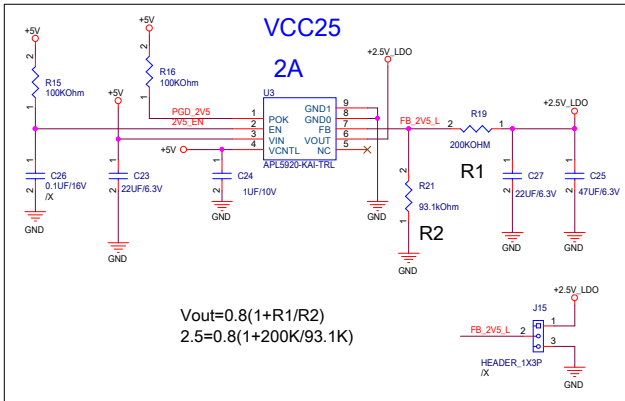
VOUT=0.8V*[1+(R2/R1)]

1.058=0.8(1+20K/62K)



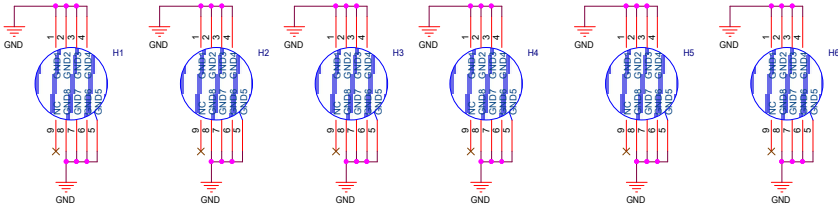
VCC25

2A

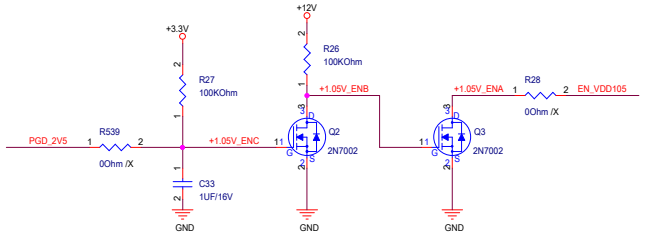


Vout=0.8(1+R1/R2)

2.5=0.8(1+200K/93.1K)



VDD105 Power Sequence



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Title	SYSTEM POWER	
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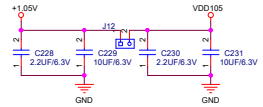
For Power TEST/Short



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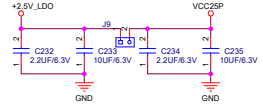

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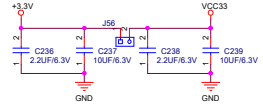
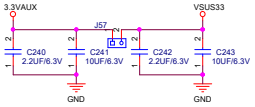
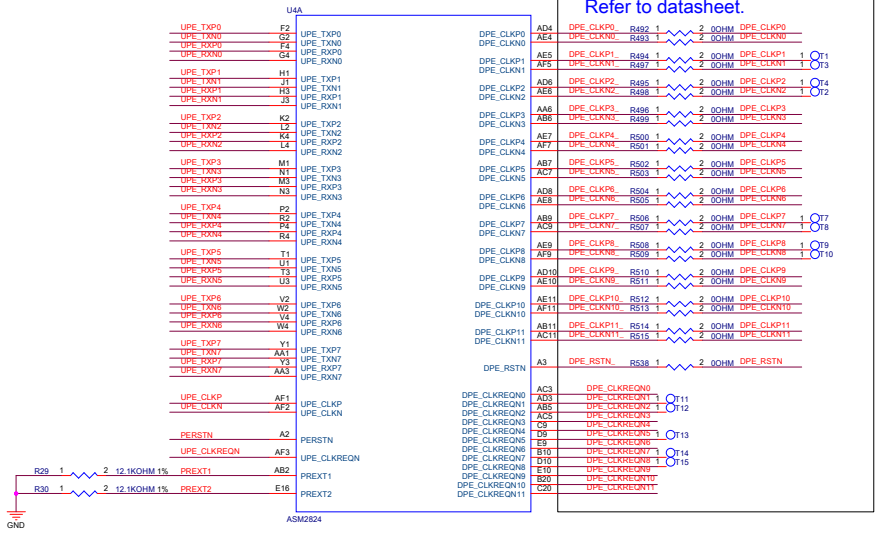
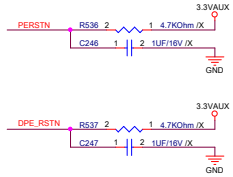
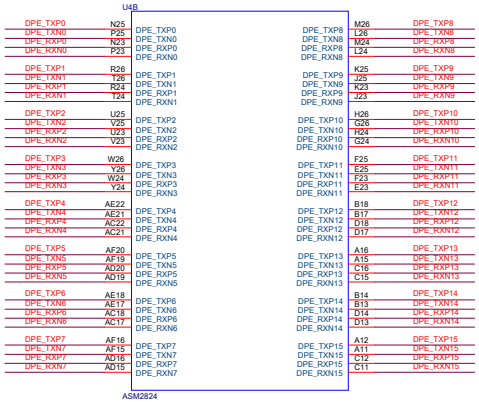


For Power TEST/Short



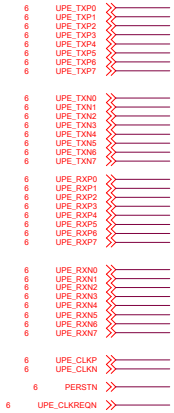




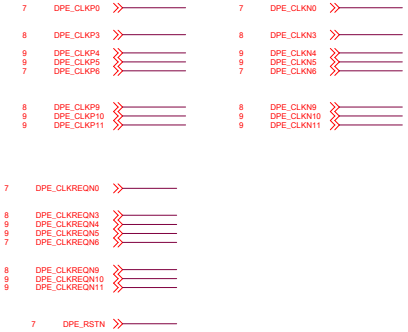


PCIE DOWNSTREAM

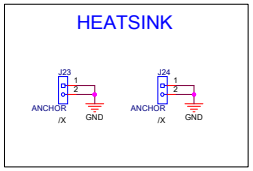
PCIE UPSTREAM



PCIE CLOCK



HEATSINK



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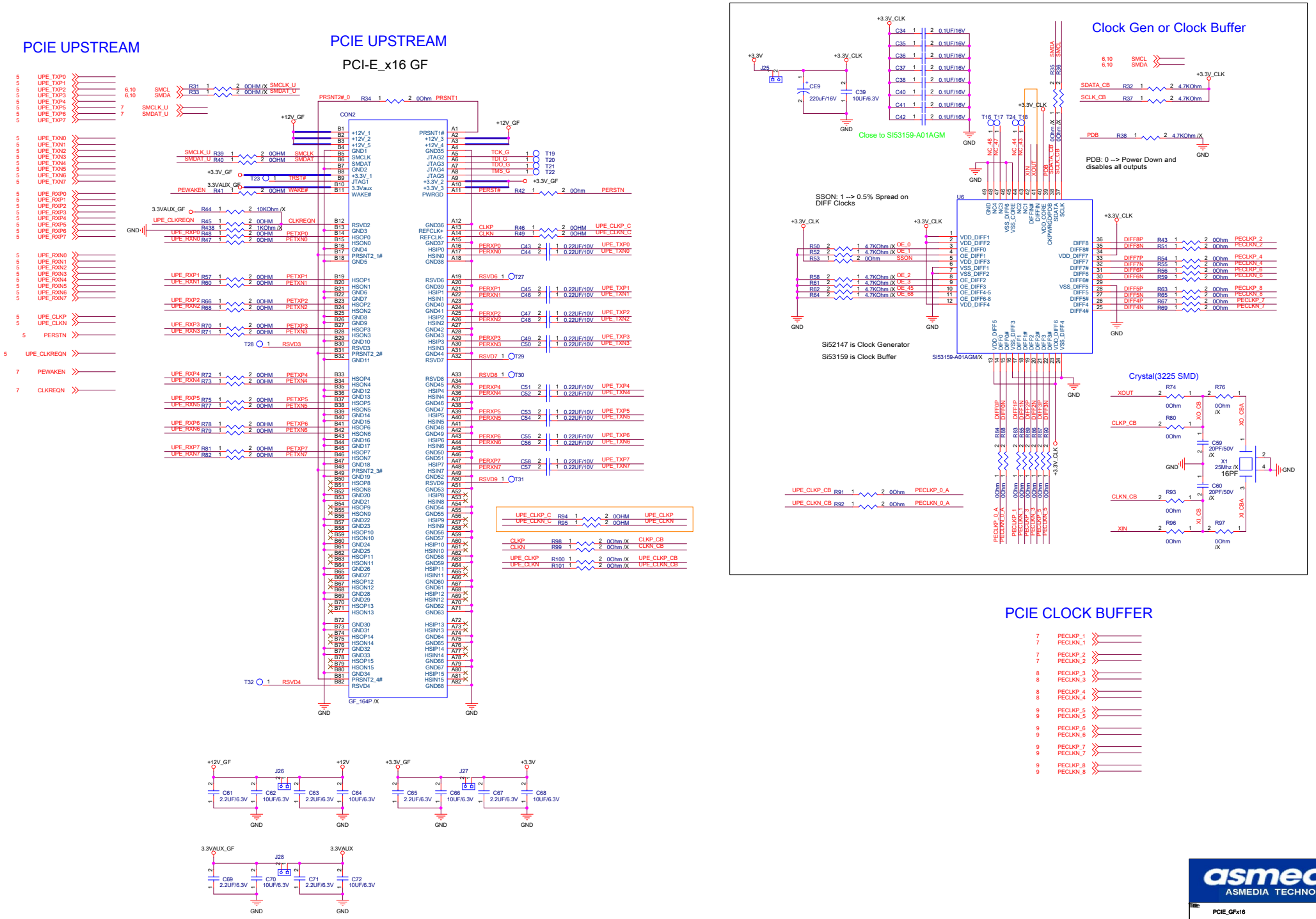
PCIE UPSTREAM
PCIE UPSTREAM
PCI-E_x16 GF
Clock Gen or Clock Buffer
Close to SI53159-A01AGM
PDB: 0 --> Power Down and disables all outputs
SSON: 1 --> 0.5% Spread on DIFF Clocks
Si52147 is Clock Generator
Si53159 is Clock Buffer
Crystal(3225 SMD)
PCIE CLOCK BUFFER
CON2
GF_164P /X
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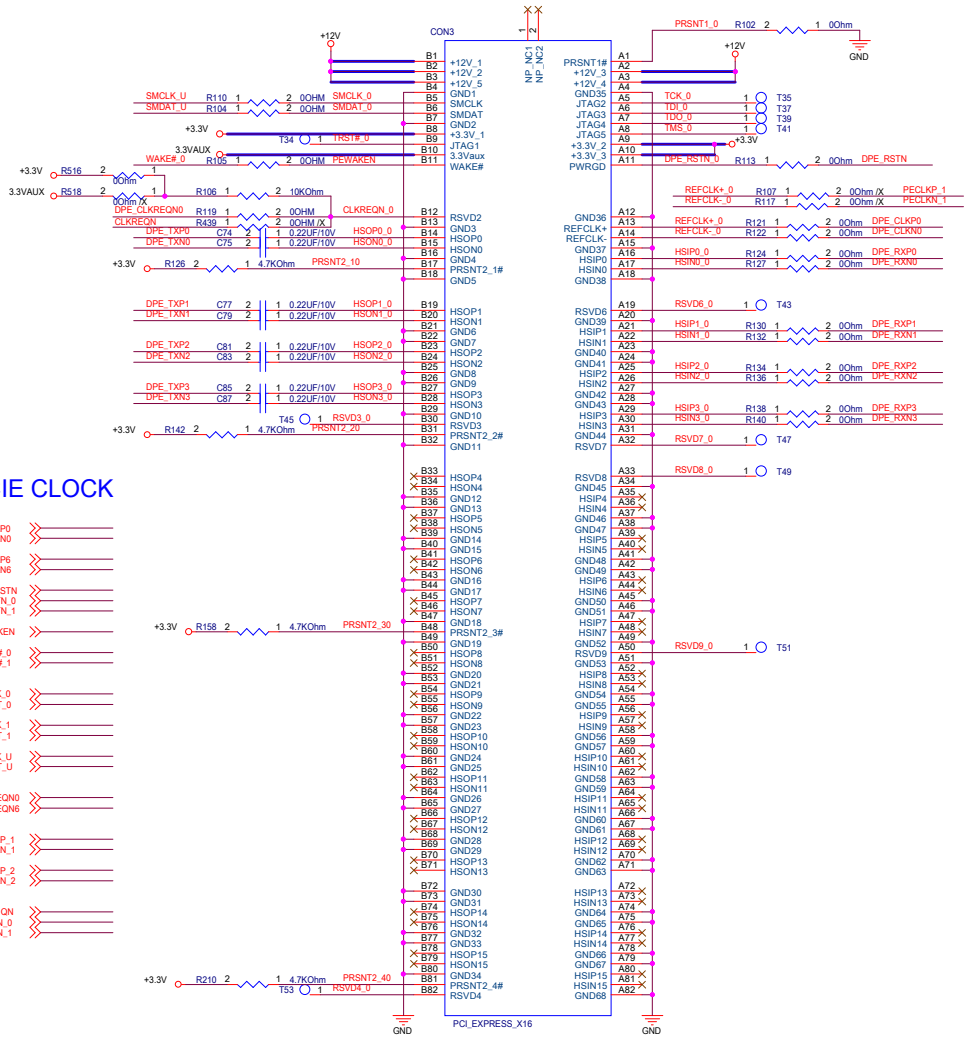
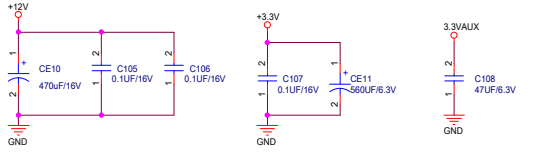
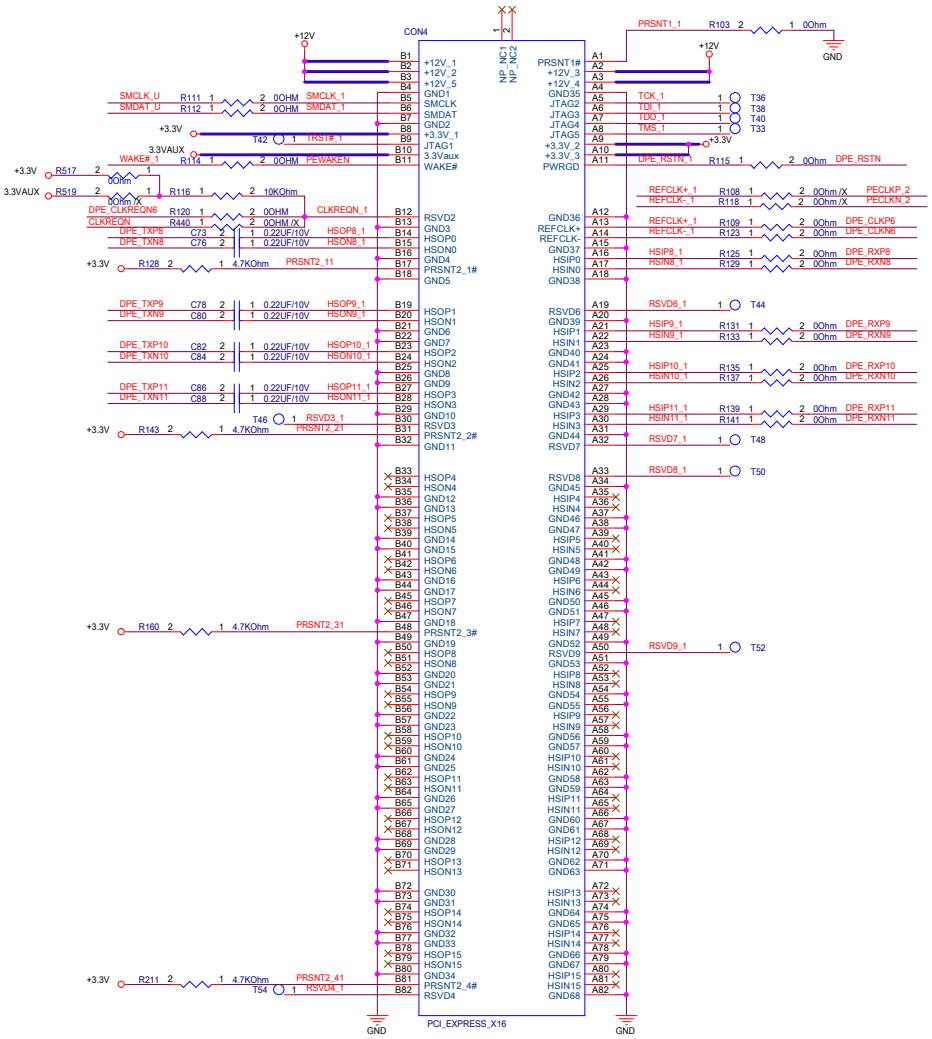
PCIE_GFx16
Friday, July 03, 2020

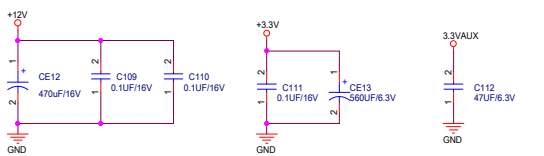
PCIE DOWNSTREAM





PCIE CLOCK





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Title: PCIE_SLOT_x16*2

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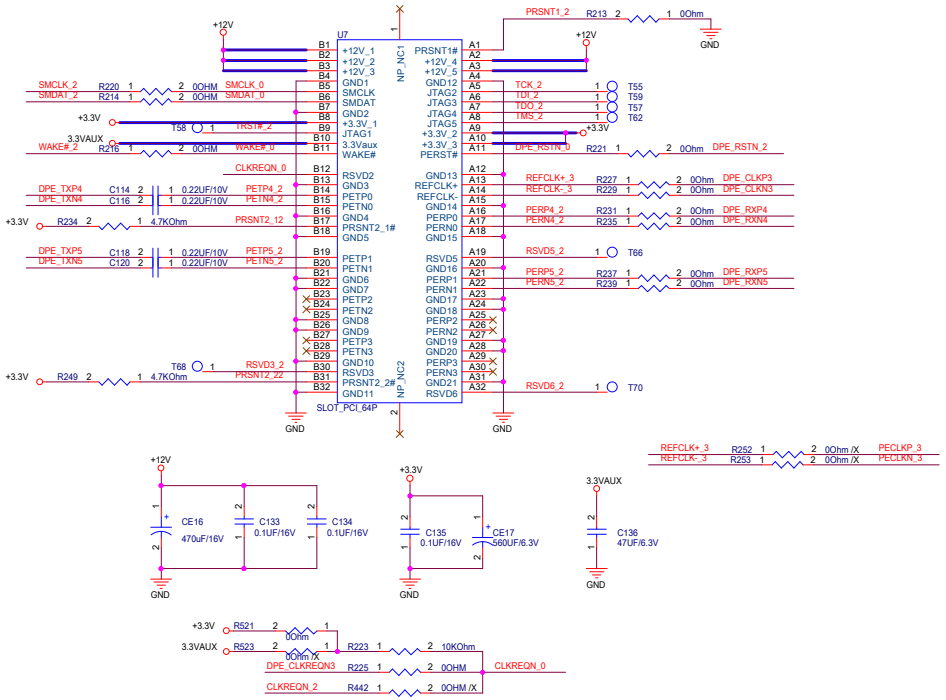
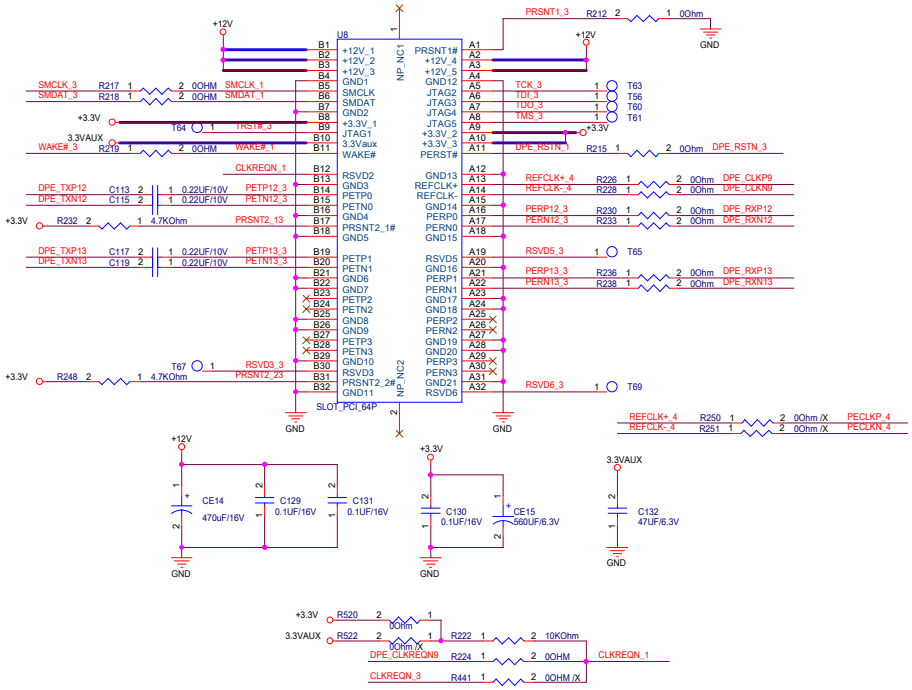
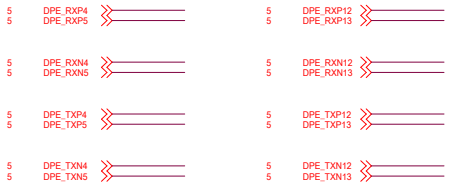
PCIE_X4 Slot



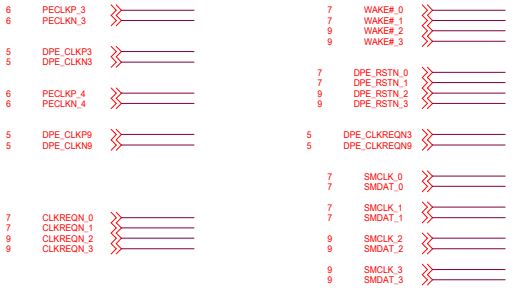
PCIE_X4 Slot



PCIE DOWNSTREAM



PCIE CLOCK



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Title	PCIE_SLOT_x4*2	
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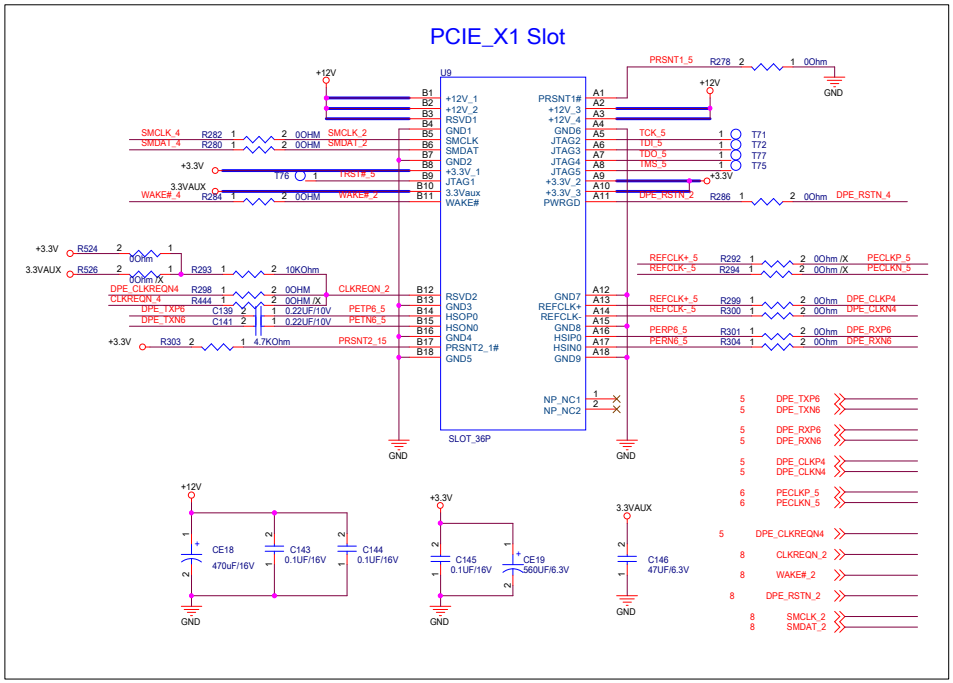

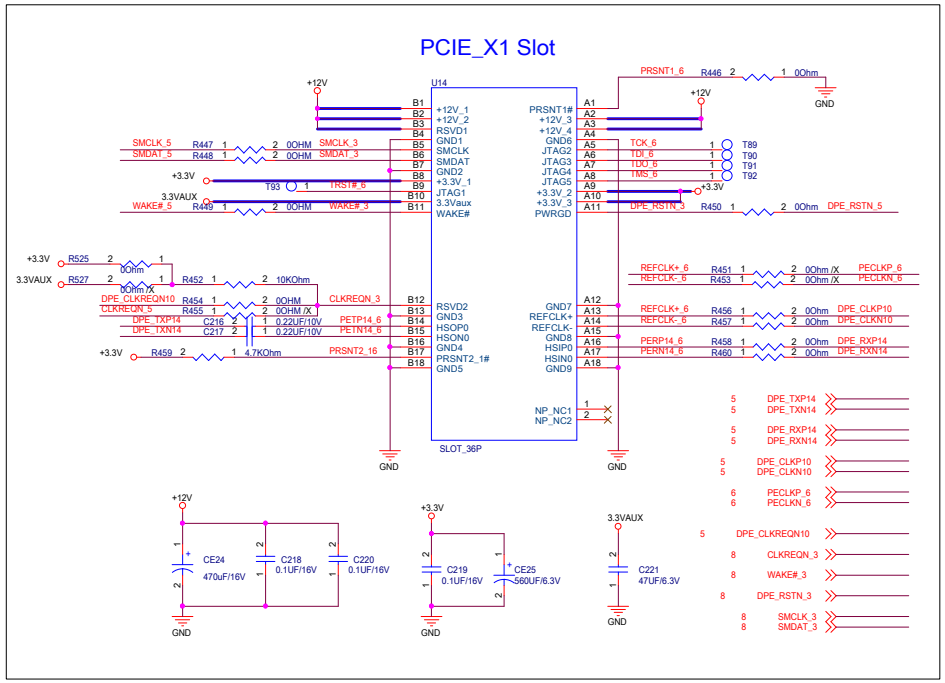

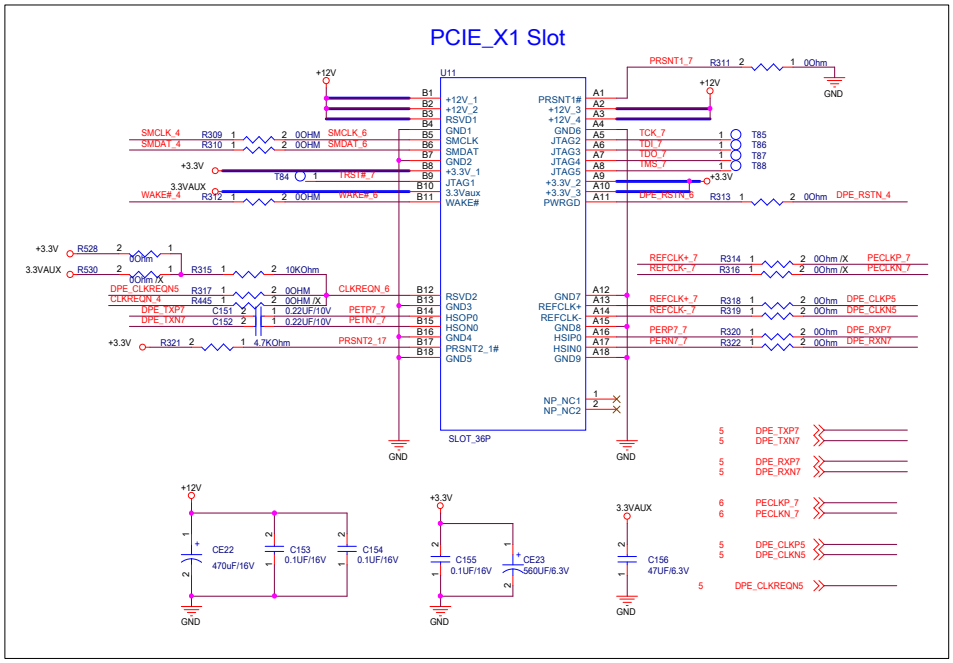

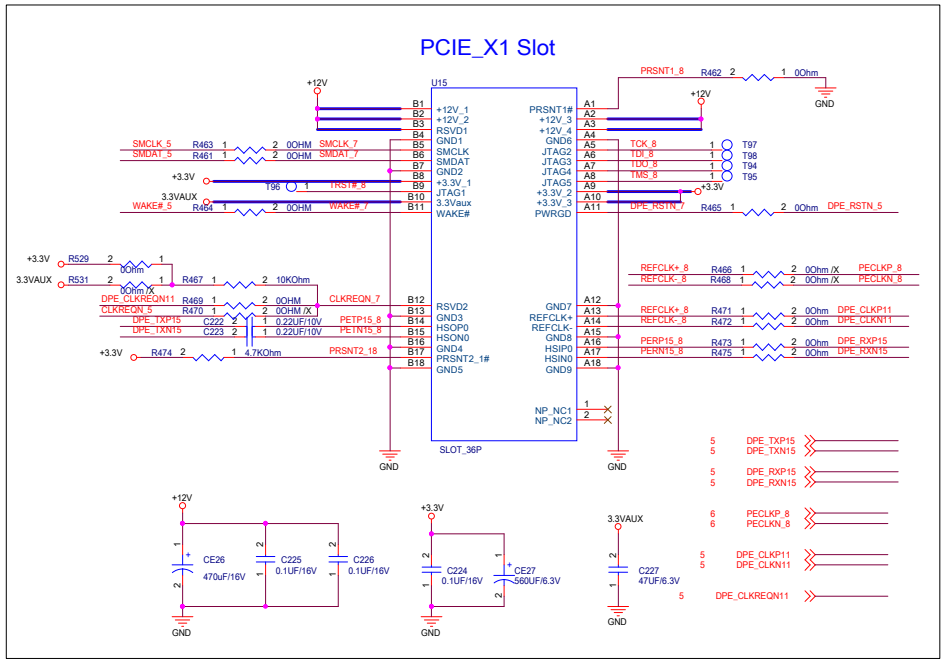

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Title	PCIE_SLOT_x2*1_SLOT_x1*2	
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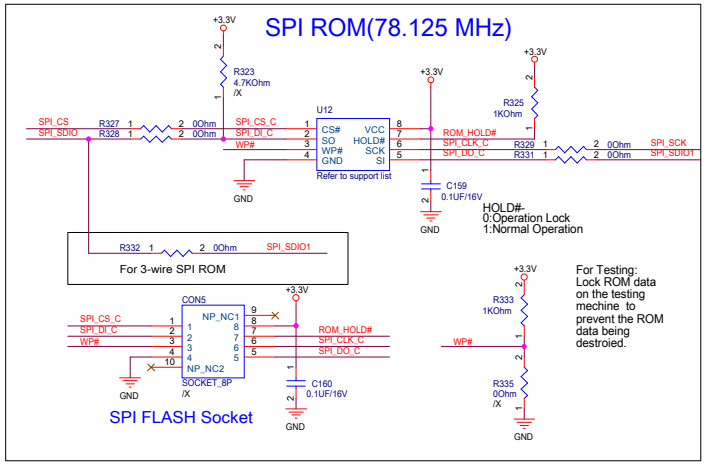
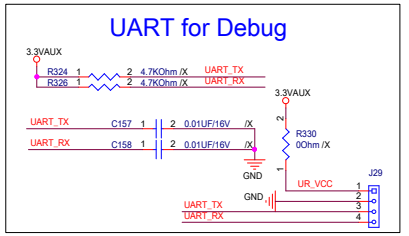
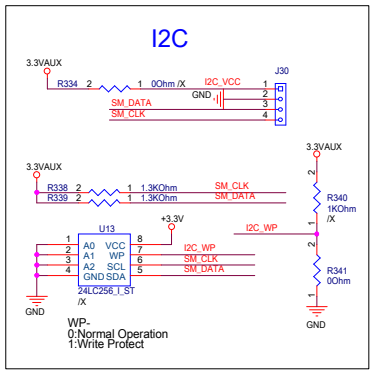
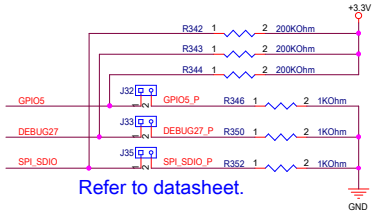




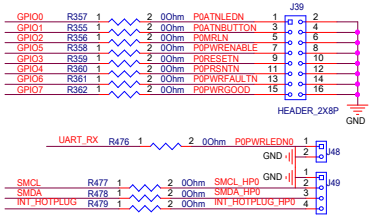


H/W Strapping



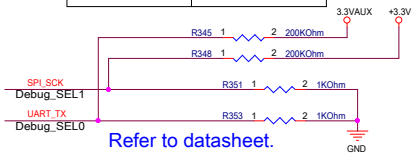
Refer to datasheet.

HOTPLUG Header

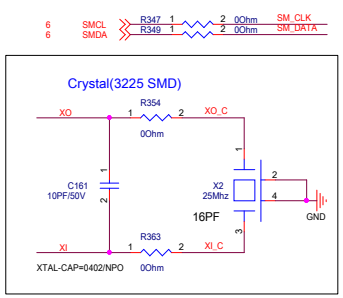


Clock mode select: SPI_SCK, UART_TX

Strapping bit	Upstream Clock
SPI_SCK	0 : 100MHz diff 1 : OSC
Strapping bit	Downstream Clock
UART_TX	0 : 100MHz diff 1 : OSC



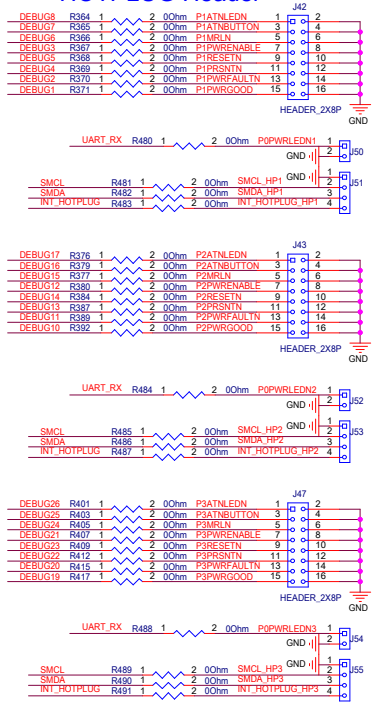
Refer to datasheet.

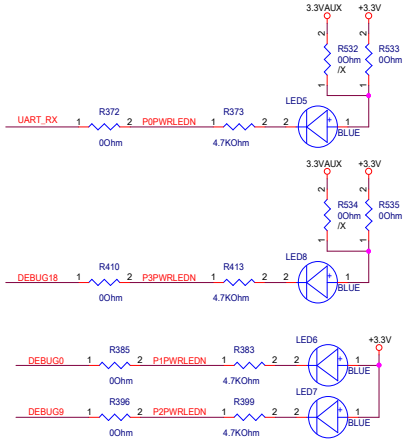


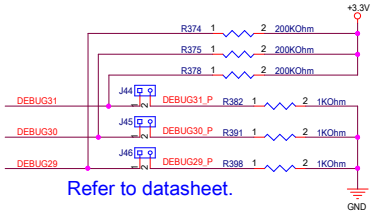
ASM2824 First 8 lane group PCIe lane configuration:

Strapping bits GPIO5,DEBUG27,SPI_SDIO	LANE0	LANE1	LANE2	LANE3	LANE4	LANE5	LANE6	LANE7
PECLK Mapping	LANE0		LANE1	LANE2	LANE3		LANE4	LANE5
0 0 0	x2		x1	x1	x2		x1	x1
0 0 1	x2		x1	x1	x4			
0 1 0	x4				x2		x1	x1
0 1 1	x4				x4			
1 0 0	x8							

HOTPLUG Header







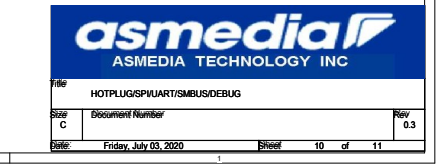
Refer to datasheet.

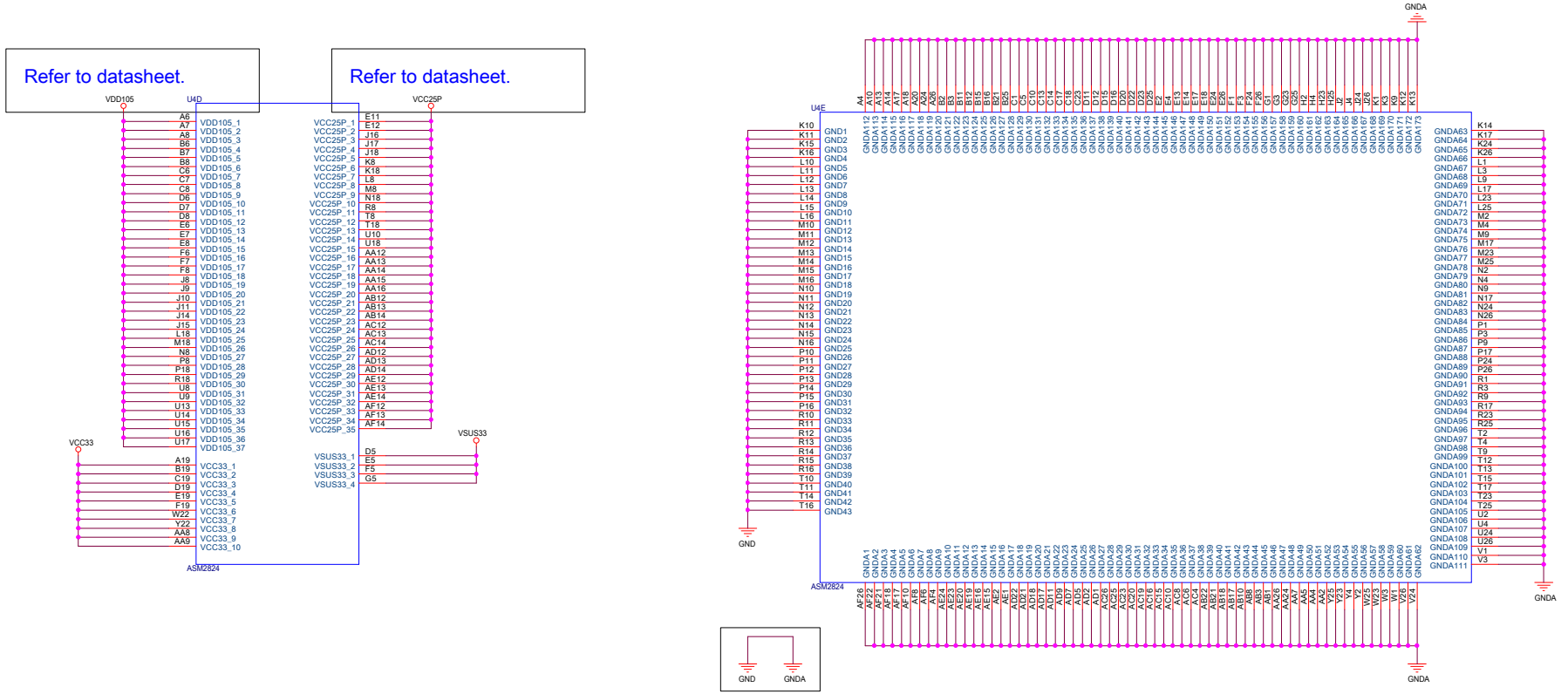
ASM2824 Second 8 lane group PCIe lane configuration:

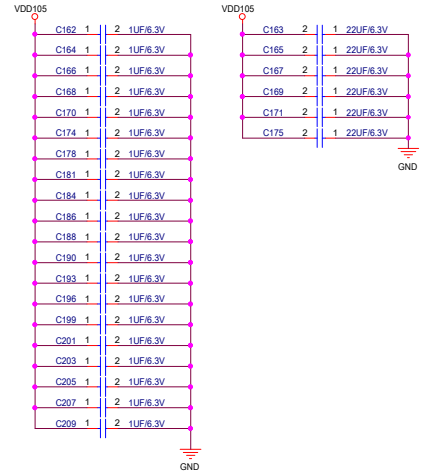
Strapping bits DEBUG31,DEBUG30,DEBUG29	LANE8	LANE9	LANE10	LANE11	LANE12	LANE13	LANE14	LANE15
PECLK Mapping	LANE6		LANE7	LANE8	LANE9		LANE10	LANE11
0 0 0	x2		x1	x1	x2		x1	x1
0 0 1	x2		x1	x1	x4			
0 1 0	x4				x2		x1	x1
0 1 1	x4				x4			
1 0 0	x8							

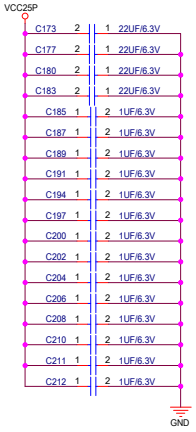
Lane configuration Mapping

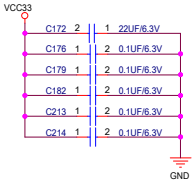
Refer to datasheet.

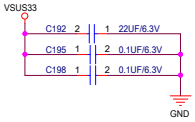












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