Genesys Logic, Inc.

GL3227E

USB 3.1 Gen1
e•MMC Reader Controller

Datasheet

Revision 1.02
Jun. 28, 2019

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Revision History

Revision	Date	Description
1.00	07/06/2017	First release
1.01	08/07/2017	Modify Table 3.1 - QFN48 Pin Description
1.02	06/28/2019	Update CH3.1 QFN 48 Pinout

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CHAPTER 1 GENERAL DESCRIPTION

The GL3227E is an USB 3.1 Gen1 eMMC RAID reader controller, it provides single LUN (Logic Unit Number) which can support *e*•MMC v5.0, 1/4/8bit data bus, High Speed SDR/ High Speed DDR/ HS200/ HS400 mode.

The GL3227E integrates a high speed 8051 microprocessor and a high efficiency hardware engine for the best data transfer performance between USB and various memory card interfaces. It supports Serial Peripheral Interface (SPI) for firmware upgrade to SPI Flash Memory via USB port. It also integrates 5V to 3.3V and 3.3V to 1.8V/1.2V regulators and power MOSFETs which can reduce system BOM cost.

CHAPTER 2 FEATURES

- USB specification compliance
  - Comply with Universal Serial Bus 3.0 Specification rev. 1.0 (USB 3.1 GEN1)
  - Comply with Universal Serial Bus Specification rev. 2.0 (USB 2.0)
  - Comply with USB Mass Storage Class Specification rev. 1.0
  - Support USB Mass Storage Class Bulk-Only Transport (BOT)
  - Support 1 device address and up to 3 endpoints: Control (0) / Bulk Data Read In (1) / Bulk Data Write Out (2)
  - Support 5 Gbps SuperSpeed, 480 Mbps high-speed, and 12 Mbps full-speed transfer rates
- Integrated USB building blocks
  - USB2.0 transceiver macrocell (UTM), Serial Interface Engine (SIE), embedded Power-On Reset (POR)
- Embedded high speed 8051 micro-controller
- High efficient DMA hardware engine improves transfer rate between USB and flash card interfaces
- Support Embedded MultiMediaCard ™ (*e*•MMC)
  - *e*•MMC specification v4.3/ v4.4/ v4.5/ v5.0
  - High Speed SDR/ High Speed DDR/ HS200/ HS400
- Support Serial Peripheral Interface (SPI) for firmware upgrade to SPI Flash Memory via USB interface
- Support firmware stored in eMMC and upgrade firmware via USB interface
- On-Chip 5V to 3.3V, 3.3V to 1.8V/1.2V regulator
- On-Chip power MOSFETs for flash media cards power source
- On-Chip 1.8V power source for VCCQ of *e*•MMC to operate as HS200/HS400 mode.
- On board 25 MHz Crystal driver circuit
- Support USB 2.0 LPM (Link Power Management)
- Support USB 3.0 LTM (Latency Tolerance Messaging)
- Support USB 3.0 U1/U2/U3 low power link state
- Pass the USB-IF Test Procedure for SuperSpeed product (TID: 341010008)
- Support two *e*•MMC chips by RAID 0 to increase the reading/writing performance
- Support one or two *e*•MMC chips by PCB co-layout, flexible for product design
- Support reset control of *e*•MMC for better compatibility
- Support PIA (Partition Information Area) in *e*•MMC to store customized VID/PID, USB device descriptor, SCSI inquiry and EEP configuration to save extra BOM cost
- Support programmable SSC (Spread Spectrum Clocking), clock rate in memory card interface for better EMI test effect
- Support Over-Current protection mechanism
- Support one power/access indicator LED (shared with SPI_MOSI)
- Available in QFN48 pin package (6x6mm)

CHAPTER 3 PIN ASSIGNMENT

3.1 QFN 48 Pinout

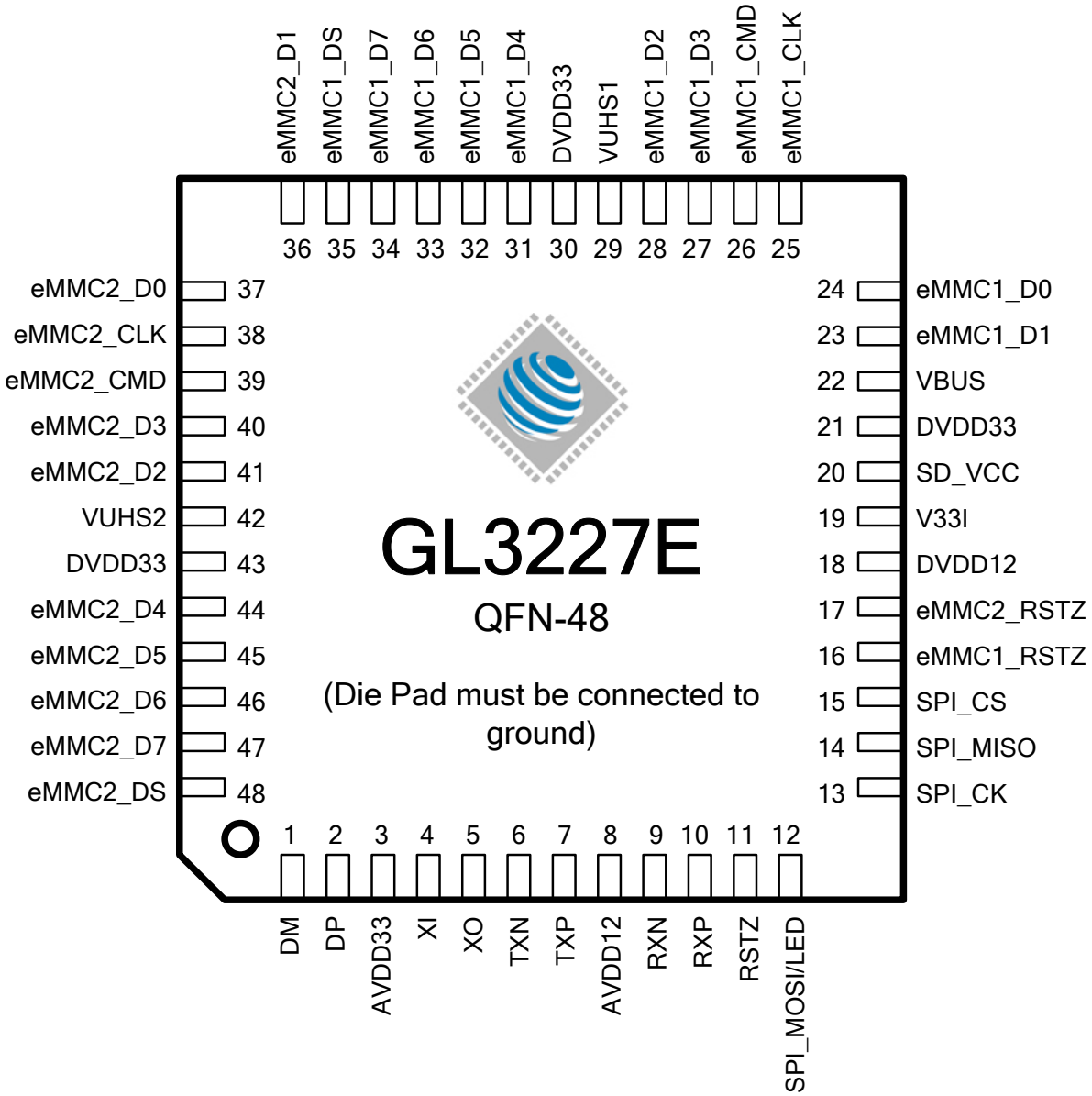


Figure 3.1 - QFN48 Pinout Diagram

3.2 Pin Description

Table 3.1 - QFN48 Pin Description

Pin Name	QFN 48	Type	Description
Power/Ground			
AVDD12	8	P	Analog 1.2V power source
AVDD33	3	P	Analog 3.3V power source
DVDD12	18	P	Digital 1.2V power source
DVDD33	21, 30, 43	P	Digital 3.3V power source
VBUS	22	P	5V power source
V33I	19	P	LDO12 3.3V power input.
VUHS_1	29	P	UltraHighSpeed IO PAD Power, the power source of this pin comes from the internal regulator of GL3227E and no need of external power input
			e•MMC: Connect to VCCQ for *e*•MMC interface power
VUHS_2	42	P	UltraHighSpeed IO PAD Power, the power source of this pin comes from the internal regulator of GL3227E and no need of external power input
			e•MMC: Connect to VCCQ for *e*•MMC interface power
SD_VCC	20	P	*e*•MMC: Connect to VCC for *e*•MMC memory power
USB PHY Interface			
DP	2	A	USB 2.0 D+
DM	1	A	USB 2.0 D-
TXN	6	A	USB 3.0 TX-
TXP	7	A	USB 3.0 TX+
RXN	9	A	USB 3.0 RX-
RXP	10	A	USB 3.0 RX+
X1	4	I	25MHz x'TAL input. It can be connected to external 25MHz clock input
X2	5	O	25MHz x'TAL output
Memory Card Interface			
eMMC1_RSTZ	16	O	eMMC1 reset
eMMC2_RSTZ	17	O	eMMC2 reset
eMMC1_D0	24	B	1st *e*•MMC data pin
eMMC1_D1	23	B	1st *e*•MMC data pin
eMMC1_D2	28	B	1st *e*•MMC data pin

eMMC1_D3	27	B	1st *e*•MMC data pin
eMMC1_D4	31	B	1st *e*•MMC data pin
eMMC1_D5	32	B	1st *e*•MMC data pin
eMMC1_D6	33	B	1st *e*•MMC data pin
eMMC1_D7	34	B	1st *e*•MMC data pin
eMMC1_CLK	25	O	1st *e*•MMC clock
eMMC1_CMD	26	B	1st *e*•MMC command/response
eMMC1_DS	35	I	1st *e*•MMC data strobe
eMMC2_D0	37	B	2nd *e*•MMC data pin
eMMC2_D1	36	B	2nd *e*•MMC data pin
eMMC2_D2	41	B	2nd *e*•MMC data pin
eMMC2_D3	40	B	2nd *e*•MMC data pin
eMMC2_D4	44	B	2nd *e*•MMC data pin
eMMC2_D5	45	B	2nd *e*•MMC data pin
eMMC2_D6	46	B	2nd *e*•MMC data pin
eMMC2_D7	47	B	2nd *e*•MMC data pin
eMMC2_CLK	38	O	2nd *e*•MMC clock
eMMC2_CMD	39	B	2nd *e*•MMC command/response
eMMC2_DS	48	I	2nd *e*•MMC data strobe
Others			
RSTZ	11	I, pu	Chip reset, active low Internal pull-up to DVDD33(3.3V)
SPI_CS/BOOTOP1	15	O	SPI interface: chip select (When SPI is not used, tie low this pin to enable Boot from eMMC)
SPI_CK/BOOTOP2	13	O	SPI interface: clock (When SPI is not used, tie low this pin to define eMMC I/O as 1.8V)
SPI_MISO	14	I	SPI interface: connect to SPI flash data output
SPI_MOSI/LED	12	O	SPI interface: connect to SPI flash data input (When SPI is not used this pin can be configured as LED)

Notation:

Type	**O**	Output
	I	Input
	B	Bi-directional
	pu	internal pull-up when input
	pd	internal pull-down when input
	P	Power / Ground
	A	Analog

CHAPTER 4 BLOCK DIAGRAM

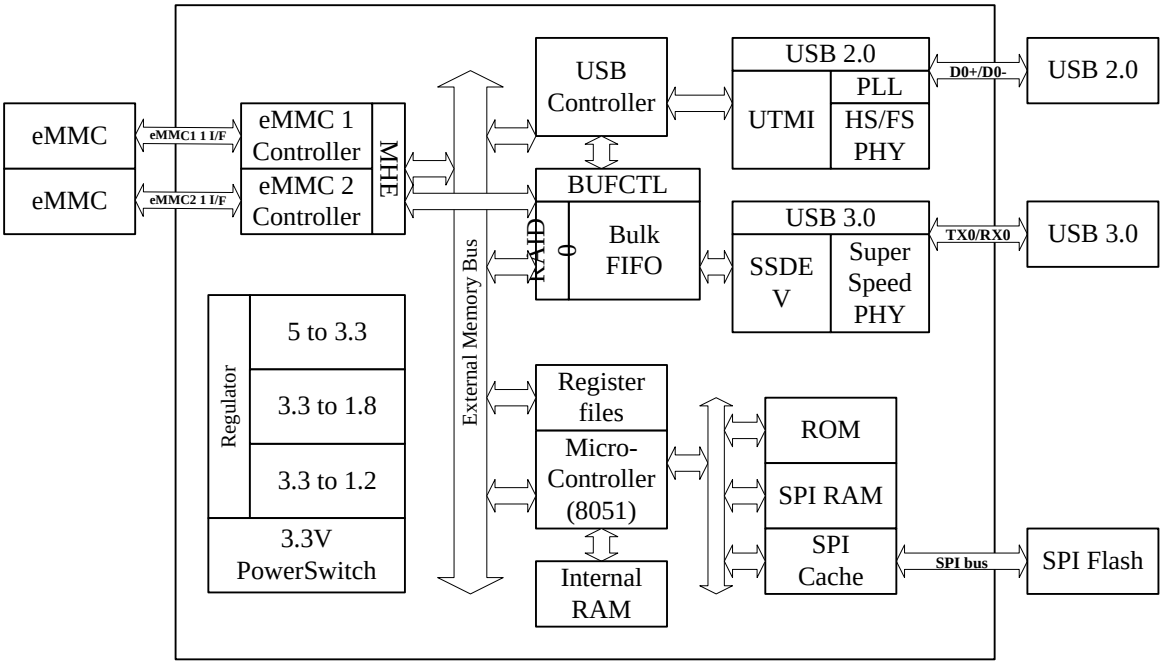


Figure 4.1 - QFN48 Functional Block Diagram

4.1 Super Speed and HS/FS PHY

The transceiver macro cell is the analog circuitry that handles the low level USB protocol and signaling, and shifts the clock domain of the data from the USB to one that is compatible with the general logic.

4.2 USB Controller and SSDEV

The USB Controller, which contains the USB PID and address recognition logic, and other sequencing and state machine logic to handle USB packets and transactions.

4.3 EPFIFO

Endpoint FIFO includes Control FIFO (FIFO0), Bulk In/Out FIFO

- **EP0 FIFO** FIFO of control endpoint 0. It is 512-byte FIFO and used for endpoint 0 data transfer.
- **Bulk In/Out FIFO** It can be in the TX mode or RX mode:
  1. It can be transmit/receive 512-byte data of USB 2.0 and 1K-byte data of USB 3.0 continuously.
  2. It can be directly accessed by micro-controller

4.4 MCU

8051 micro-controller inside.

- **8051 Core** Compliant with Intel 8051 high speed micro-controller
- **ROM** Firmware code on ROM
- **IRAM** Internal RAM area for MCU access
- **EXTRAM** External RAM area for MCU access

4.5 MHE (Media Hardware Engine)

Media Interface: Two eMMC

4.6 Regulator

- **5V to 3.3V** 3.3V Power source
- **3.3V to 1.8/1.2V** 1.8/1.2V Power source

CHAPTER 5 ELECTRICAL CHARACTERISTICS

5.1 Temperature Conditions

Table 5.1 - Absolute Maximum Ratings

Parameter	Value
Storage Temperature	-65°C to +150 °C
Operating Temperature	0°C to +70 °C

5.2 Operating Conditions

Table 5.2 - Operating Conditions

Parameter	Value
Supply Voltage	+4.75V to +5.25V
Ground Voltage	0V
F_{OSC} (Oscillator or Crystal Frequency)	25 MHz ± 0.03%

5.3 DC Characteristics

Table 5.3 - DC Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage		4.75	5.0	5.25	V
V_{IH}	Input High Voltage		2.0			V
V_{IL}	Input Low Voltage				0.4	V
I_I	Input Leakage Current	$0 < V_{IN} <$ DVDD	-10		10	μA
V_{OH}	Output High Voltage	DVDD = 3.3V	2.8			V
V_{OL}	Output Low Voltage				0.4	V
I_{OH}	Output Current High			8		mA
I_{OL}	Output Current Low			8		mA
C_{IN}	Input Pin Capacitance			5		pF
I_{NORMAL}	HS mode			48		mA
	SS mode	U0 state		130		mA
		U1 state		33		mA
		U2 state		16		mA
I_{ACTIVE}	HS mode			65.6		mA
	SS mode	U0 state		146		mA
I_{RESET}				5		mA

I_{SUS}	Suspend current	1.5K pull-up included		1.14		mA
	SS Suspend current	U3 state		0.97		mA
R_{pu}	Reset Pad pull-up			46		KΩ
	eMMC_CMD pull-up			15		KΩ
	eMMC_D[7:0] Pad pull-up			15		KΩ
R_{pd}	eMMC_DS pull-down			15		KΩ

5.4 AC Characteristics of Reset Timing

5.4.1 Reset Timing

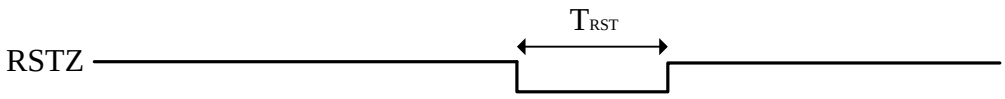


Figure 5.1 - Timing Diagram of Reset Width

5.4.2 *e*•MMC Clock Frequency

Table 5.2 - *e*•MMC Clock Frequency

Parameter	Description	Max.	Unit
F_{ID}	Clock frequency Identification Mode	400	KHz
F_{SDR}	Clock frequency High Speed SDR	52	MHz
F_{DDR}	Clock frequency High Speed DDR	52	MHz
F_{HS200}	Clock frequency HS200	200	MHz
F_{HS400}	Clock frequency HS400	200	MHz

CHAPTER 6 SPI FLASH MEMORY SUPPORT LIST

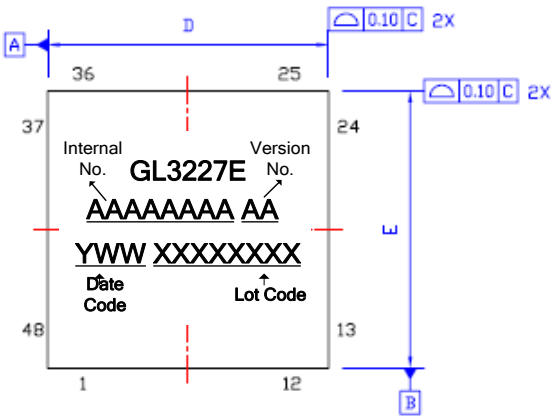
Table 6.1 - SPI Flash Memory Support List

Vendor	Model
GigaDevice	GD25D10B
PMC	PM25LD010
	PM25LD020
WINBOND	W25X10CL
	W25X20CL
MXIC	MX25L1006E
	MX25L4006E
ESMT	F25L01PA(86P)
	F25L01PA(100P)
FMSH	FM25F01

Note :

- GL3227E supports Page-Program SPI Flash Memory only, does not support Byte-program SPI Flash Memory
- The density of SPI Flash Memory shall be larger than or equal to 512Kbit.
- Firmware file (xxxx.bin) which Genesys Logic provided is only used for Genesys Logic's Multi-Tool and MP Tool ISP (In System Programming via USB interface) purpose. If you would like to provide FW to SPI Flash vendor for pre-loading or Flash ROM writer usage, please contact to GL technical support team.

CHAPTER 7 PACKAGE DIMENSION



SYMBOL	DIMENSION MM (MIL)		
	MIN.	NOM.	MAX.
A	0.70 (27.6)	0.75 (29.5)	0.80 (31.5)
A1	---	0.02 (0.8)	0.05 (2.0)
A3		0.203 (8.0) REF	
b	0.13 (5.1)	0.18 (7.1)	0.25 (9.8)
D		6.00 (236.2) BSC	
D2	4.40 (173.2)	4.50 (177.2)	4.60 (181.1)
E		6.00 (236.2) BSC	
E2	4.40 (173.2)	4.50 (177.2)	4.60 (181.1)
e		0.40 (15.7) BSC	
L	0.30 (11.8)	0.40 (15.7)	0.50 (19.7)

NOTE: 1. REFER TO JEDEC STD. MO-220
2. ALL DIMENSIONS IN MILLIMETERS.

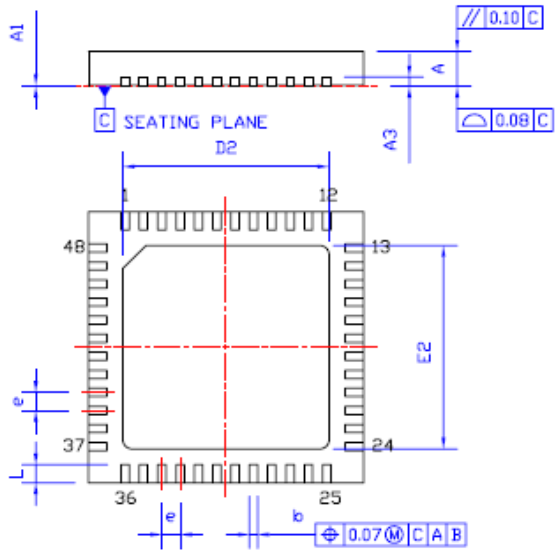


Figure 7.1 - QFN 48 Pin Package

CHAPTER 8 ORDERING INFORMATION

Table 8.1 - Ordering Information

Part Number	Package	Green/Wire Material	Version	Status
GL3227E-ONYXX	QFN 48	Green Package + CU Wire	XX	Available