100V Synchronous Buck DC/DC Controller

1 DESCRIPTION

The MK9218 operates over a wide input voltage range from 6V to 100V. With appropriate high-side and low-side MOSFET and Inductance, the MK9218 delivers up to 30A output current.

The MK9218 adopts a voltage mode control architecture to achieve excellent accurate voltage output. The switching frequency is adjustable up to 1 MHz, which also can be synchronized to an external clock source to eliminate beat frequencies in noise-sensitive applications.

MK9218 support Forced-PWM (FPWM) and Diode Emulation Mode; FPWM operation eliminates switching frequency variation to minimize EMI, while user selectable diode emulation lowers current consumption at light-load condition.

MK9218 is offered with wide duty cycle from 1% to 98% under appropriate switching frequency, so input and output voltage can easy to be choose.

The MK9218 provides a power good (PG) flag pin to indicate output voltage.

2 APPLICATIONS

- POL modules
- High-Power Density DC – DC
- Datacom, Telecom
- Non-isolated PoE and IP cameras

3 FEATURES

- Wide Input Voltage 6V-100V
- Adjustable output from 0.8V to 60V
- 40ns $t_{on(min)}$ for low duty ratio
- 190ns $t_{off(min)}$ for high duty ratio
- Precision ±1% Feedback Reference
- Adjustable F_{SW} from 100kHz to 1MHz
- Configuration diode emulation or FPWM
- 2.5A source and 3.5A sink driver ability
- Prebias start-up
- SYNCI and SYNCO capability
- Open-Drain Power Good Indicator
- Adjustable output voltage soft start
- Input UVLO with hysteresis
- VCC and BOOT UVLO protection
- OC, OT Protection with Hiccup Mode
- QFN20L 4.5mm x 3.5mm Package with Thermal PAD

4 TYPICAL APPLICATION

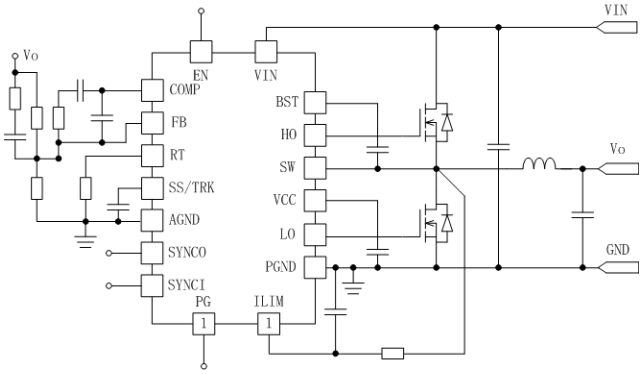


Figure 1. Typical Application Diagram

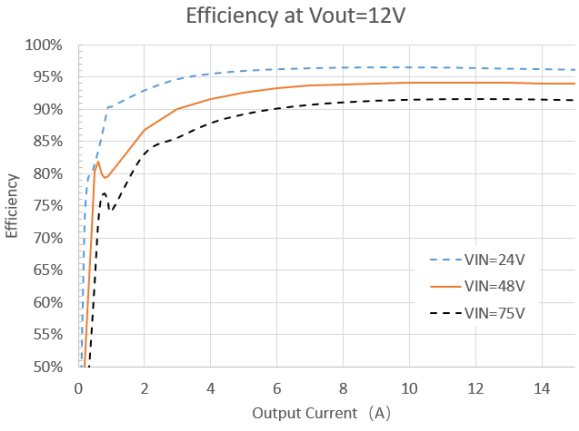


Figure 2.Efficiency at Vout=12V

5 PACKAGE REFERENCE AND PIN FUNCTION

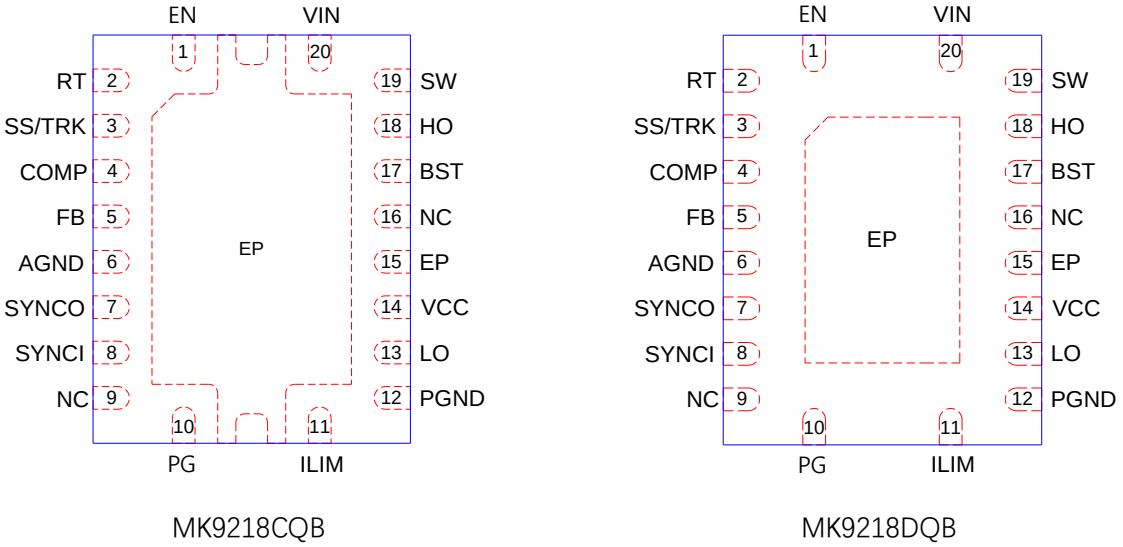


Figure 3. Pin Function (top view)

Order No.	Description
MK9218：MK9218CQB	QFN20L, tape, 3000/reel
MK9218：MK9218DQB	QFN20L, tape, 3000/reel

Pin #	Name	Description
1	EN	Enable input and undervoltage lockout. The device has accurate 1.2V rising threshold and a hysteresis current to programable falling threshold for tri-state（shutdown、standby、operating） to reduce quiescent loss. This pin also can be used for programming the VIN turn on voltage with the resistor divider. V_{EN}＜0.8V，shutdown mode，VIN to VCC LDO shutdown； 0.8V≤V_{EN}＜1.2V，standby mode，VIN to VCC LDO regulated to 7.5V； V_{EN}＞1.2V，operating mode，start to operating；
2	RT	Oscillator frequency set. The internal oscillator is programmed with a single resistor between RT and the AGND.
3	SS/TRK	Soft-start and voltage-tracking. during start-up, Output voltage tracking SS/TRK voltage; After start-up, Output voltage tracking Ref.
4	COMP	Compensation. Low impedance output of the internal error amplifier. Connect the loop compensation network between the COMP pin and the FB pin.
5	FB	Feedback. Connection to the inverting input of the internal error amplifier. Connect this pin to the center point of the output resister divider to program the output voltage: VOUT=0.8×(1+Rf1/Rf2)
6	AGND	Analog ground. Return for the internal 0.8V voltage reference and analog circuits.

7	SYNCO	Synchronization output. Logic output that provides a clock signal that is 180° out-of-phase with the HS FET drive signal.
8	SYNCI	Synchronization input. Tri function: 1.optional external clock input 2.low-side MOSFET diode emulation mode 3.FPWM.
9	NC	No electrical connection.
10	PG	Power good indicator. This pin is an open-drain output pin. Connect to a source voltage through a pull-up resistor.
11	ILIM	Current limit set. Connect a resistor to SW to adjust current limit.
12	PGND	Power ground.
13	LO	LS MOSFET gate driver output. Connect to the gate of the low-side MOSFET through a short, low inductance path.
14	VCC	VCC. Output of the 7.5V bias regulator. Locally decouple to PGND using a low ESR/ESL capacitor located as close as possible to the controller.
15	NC	No electrical connection.
16	NC	No electrical connection.
17	BST	Boot-strap. Decouple this pin to SW pin with a 100nF ceramic capacitor located as close as possible to the controller.
18	HO	HS MOSFET gate driver output. Connect to the gate of the high-side MOSFET through a short, low inductance path.
19	SW	Switching node. Connect to the bootstrap capacitor, the source terminal of the high-side MOSFET and the drain terminal of the low-side MOSFET using short, low inductance paths.
20	VIN	Input. Decouple this pin to PGND with low ESR ceramic capacitor.
-	EP	Exposed pad. Solder the EP to the PGND pin and connect to a large copper plane to reduce thermal resistance.

6 ABSOLUTE MAXIMUM RATINGS (1)

VIN, EN, SW, ILIM to GND ····· -0.3V to 105V
SW to PGND (20ns pulse) ····· -5V to 105V
VCC, SYNCI, SYNCO, PG to AGND ····· -0.3V to 14V
FB, COMP, SS/TRK, RT to AGND ····· -0.3V to 6.6V
BST to GND ····· -0.3V to 115V
BST to VCC ····· 0V to 105V
BST to SW ····· -0.3V to 14V
VCC to BST (20ns pulse) ····· 0V to 14V
LO to GND (20ns pulse) ····· -5V to 14V
Package Thermal Resistance
θ_{JA} (Junction to ambient) ····· TBD℃/W
θ_{JC} (Junction to case) ····· TBD℃/W
Operating Junction Temperature, T_J ····· -40℃ to 160℃
Storage Temperature，T_{stg} ····· -65℃ to 160℃
Soldering Temperature(10 second)，T_{sld} ····· 260℃

Notes:

(1) Stresses beyond the “ABSOLUTE MAXIMUM RATINGS” may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated in “RECOMMENED OPERATING CONDITIONS”. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

7 RECOMMENDED OPERATING CONDITIONS

VIN Voltage ····· 5V to 100V
EN Voltage ····· -0.3V to 100V
SW Voltage ····· -0.3V to 100V
ILIM Voltage ····· -0.3V to 100V
Ambient Temperature ····· -40℃ to 125℃

8 ESD RATINGS

		Value	Units
Electrostatic discharge V_{ESD}	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	TBD	V
	Charged device model (CDM), per JEDEC specification JESD22-C101(2)	±2000	V

Notes:

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process

(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process

9 ELECTRICAL CHARACTERISTICS

V_{IN}=48V, V_{OUT}=12V, L=4.7μH, C_{OUT}=400uF, T_A=25℃, unless otherwise specified

Parameter		Test Conditions	MIN	TYP	MAX	UNIT
Input Voltage						
V_{IN}	Input Voltage		6		100	V
Supply Current						
V_{IN}	Operating voltage		6		100	V
I_{Q-SD}	Shutdown Current	V_{EN}=0V		7.7		μA
I_{Q-STBY}	Standby Current	V_{EN}= 1V, I_{OUT}=0A,		1.5		mA
$I_{Q-OPERAT}$	Operating current, no switching	V_{EN}=1.5V, $V_{SS/TRK}$=0V		1.8		mA
VCC Regulator						
V_{VCC}	VCC regulation voltage	$V_{SS/TRK}$=0V, 9V≤VIN≤100V, 0mA ≤ I_{VCC} ≤ 20mA		7.5		V
$V_{VCC-LDO}$	VIN to VCC dropout	V_{VIN}=6V, $V_{SS/TRK}$=0V, I_{VCC}=20mA		0.25		V
$I_{MAX-LDO}$	VCC max current	$V_{SS/TRK}$=0V, V_{VCC}=0V		30		mA
V_{VCC-UV}	VCC undervoltage Threshold	V_{VCC} rising		4.9		V
$V_{VCC-UVH}$	VCC undervoltage hysteresis	Rising Threshold-falling Threshold		0.26		V
$V_{VCC-EXT}$	Minimum external bias supply voltage	> V_{VCC}	8			V
I_{VCC}	External VCC input	$V_{SS/TRK}$=0V, V_{VCC}=13V				mA
EN						
$V_{EN-STBY}$	EN rising to standby threshold	V_{IN}=48V, I_{OUT}=0.1A		0.8		V
V_{EN-SD}	EN falling to shutdown threshold	V_{IN}=48V, I_{OUT}=0.1A		0.65		V
V_{EN-H}	EN rising to operating threshold	V_{IN}=48V, I_{OUT}=0.1A		1.2		V
I_{EN-HYS}	Hysteresis Input Current	V_{EN}=1.5V		10		μA
Feedback Amplifier						
V_{REF}	Feedback reference voltage	V_{FB}=V_{COMP}		0.8		V
V_{COMP-H}	COMP output high voltage	VFB=0V, COMP sourcing 1 mA		4		V
V_{COMP-L}	COMP output low voltage	COMP sinking 1 mA			0.3	V
$I_{FB-BIAS}$	FB input bias current	V_{FB}=0.8V	-0.1		0.1	uA

SS/TRK						
I_{SS}	SS/TRK charging current	$V_{SS/TRK}$ = 0 V		10		uA
R_{SS}	Discharge FET resistance	V_{EN}=1V, $V_{SS/TRK}$=0.1V		10		Ω
V_{SS-FB}	SS/TRK to FB offset			0		mV
$V_{SS-CLAMP}$	SS/TRK to FB clamp voltage	$V_{SS/TRK}$-V_{FB} (0.8V)		115		mV
PG						
PG_{UTH}	FB upper threshold for PG high to low	% of VREF, V_{FB} rising		108		%
PG_{LTH}	FB lower threshold for PG high to low	% of VREF, V_{FB} falling		92		%
PG_{HYS_U}	PG upper threshold hysteresis	% of VREF		3		%
PG_{HYS_L}	PG lower threshold hysteresis	% of VREF		2		%
$T_{PG-RISE}$	PG rising filter	FB to PG rising edge		25		us
$T_{PG-FALL}$	PG falling filter	FB to PG falling edge		25		us
V_{PG-L}	PG low state output	V_{FB}=0.9V, I_{PG}=2mA			150	mV
I_{PG-H}	PG high state leakage current	V_{FB}=0.8V, V_{PG}=13V			100	nA
Frequency						
F_{SW}	Programmable Switching Frequency	$F_{SW}(kHz) = \frac{10^4}{R_T(K\Omega)}$	100		1000	kHz
SYNCI and SYNCO						
F_{SYNCI}	SYNCI external Fsw	% of F_{SW} set by R_{RT}	-20		50	%
$V_{SYNC-IH}$	SYNCI input logic high		2			V
$V_{SYNC-IL}$	SYNCI input logic low				0.4	V
R_{SYNCI}	SYNCI input resistance	V_{SYNCI}=3V		20		kΩ
t_{SYNCI}	SYNCI input minimum pulse width	Minimum high/low state duration	50			ns
$V_{SYNCO-OH}$	SYNCO input logic high	I_{SYNCO}=-1mA(sourcing)	3			V
$V_{SYNCO-OL}$	SYNCO input logic low	I_{SYNCO}=1mA(sink)			0.4	V
t_{SYNCI}	Delay from SYCNI leading edge to HO rising	50% to 50%		150		ns
t_{SYNCO}	Delay from HO rising to SYNCO leading edge	V_{SYNCI}=0, T_S=1/F_{SW}, 50% to 50%		T_S/2-140		ns
PWM CONTROL						
$t_{ON(MIN)}$	Minimum on-time	HO rising to falling, VBST-VSW=7V,50% to		40		ns

		50%				
$T_{OFF(MIN)}$	Minimum off-time	HO falling to rising, VBST-VSW=7V,50% to 50%		190		ns
D_{100K}	Maximum duty cycle	F_{SW}=100kHz, 6V≤V_{VIN}≤60V		98		%
D_{400K}	Maximum duty cycle	F_{SW}=400kHz, 6V≤V_{VIN}≤60V		93		%
V_{RAMP}	Minimum Ramp valley	COMP at 0% duty cycle		300		mV
k_{FF}	Feedforward gain	V_{IN}/V_{RAMP}, 6V ≤ V_{VIN} ≤ 60V		15		V/V
ILIM-OCP						
I_{RS}	ILIM source current, R_{SENSE} mode	Low voltage detected at ILIM		100		uA
$I_{RDS(on)-LS}$	ILIM source current, $R_{DS(ON)}$ mode	SW voltage detected at ILIM		200		uA
$TC_{I-RDS(on)}$	ILIM current tempco	$R_{DS(on)}$ mode		4500		ppm/℃
TC_{I-RS}	ILIM current tempco	R_{SENSE} mode		0		ppm/℃
$V_{ILIM-TH}$	ILIM comparator threshold at ILIM			0		mV
SCP						
V_{CLAMP_OS}	Clamp offset voltage, no current limit	CLAMP to COMP steady state offset voltage		0.2+V_{VIN}/75		V
V_{CLAMP_MIN}	Clamp offset voltage, no current limit	CLAMP voltage with continuous current limiting		0.3+V_{VIN}/75		V
HICCUP						
$C_{HICC-DEL}$	Hiccup mode activation delay	Clock cycle with current limiting before hiccup off-time activated		512		cycles
C_{HICCUP}	Hiccup mode off-time after activation	Clock cycle with no switching followed by SS/TRK release		8192		cycles
DIODE EMULATION MODE						
V_{ZCD-SS}	ZCD soft-start ramp	ZCD threshold measured at SW pin 50 clock cycles after first HO pulse		0		mV
$V_{ZCD-DIS}$	ZCD disable threshold(CCM)	ZCD threshold measured at SW pin 50 clock cycles after first HO pulse		200		mV
V_{DEM-TH}	Diode emulation	Measured at SW with		0		mV

	ZC threshold	V_{SW} rising				
DRIVERS						
R_{HO-UP}	HO high-state resistance HO to BST	V_{BST}-V_{SW}=7V, I_{HO}=-100mA		1.5		Ω
$R_{HO-DOWN}$	HO low-state resistance HO to SW	V_{BST}-V_{SW}=7V, I_{HO}=100mA		0.9		Ω
$R_{LO-DOWN}$	LO high-state resistance LO to VCC	V_{BST}-V_{SW}=7V, I_{LO}=-100mA		1.5		Ω
$R_{LO-DOWN}$	LO low-state resistance LO to PGND	V_{BST}-V_{SW}=7V, I_{HO}=100mA		0.9		Ω
I_{HOH}, H_{LOH}	HO, LO source current	V_{BST}-V_{SW}=7V, HO=SW LO=AGND		2.5		A
I_{HOL}, H_{LOL}	HO, LO sink current	V_{BST}-V_{SW}=7V, HO=BST LO=VCC		3.5		A
THERMAL SHUTDOWN						
T_{SD}	Thermal shutdown threshold	T_J rising		175		℃
T_{SD-HYS}	Thermal shutdown hysteresis			20		℃

10 BLOCK DIAGRAM

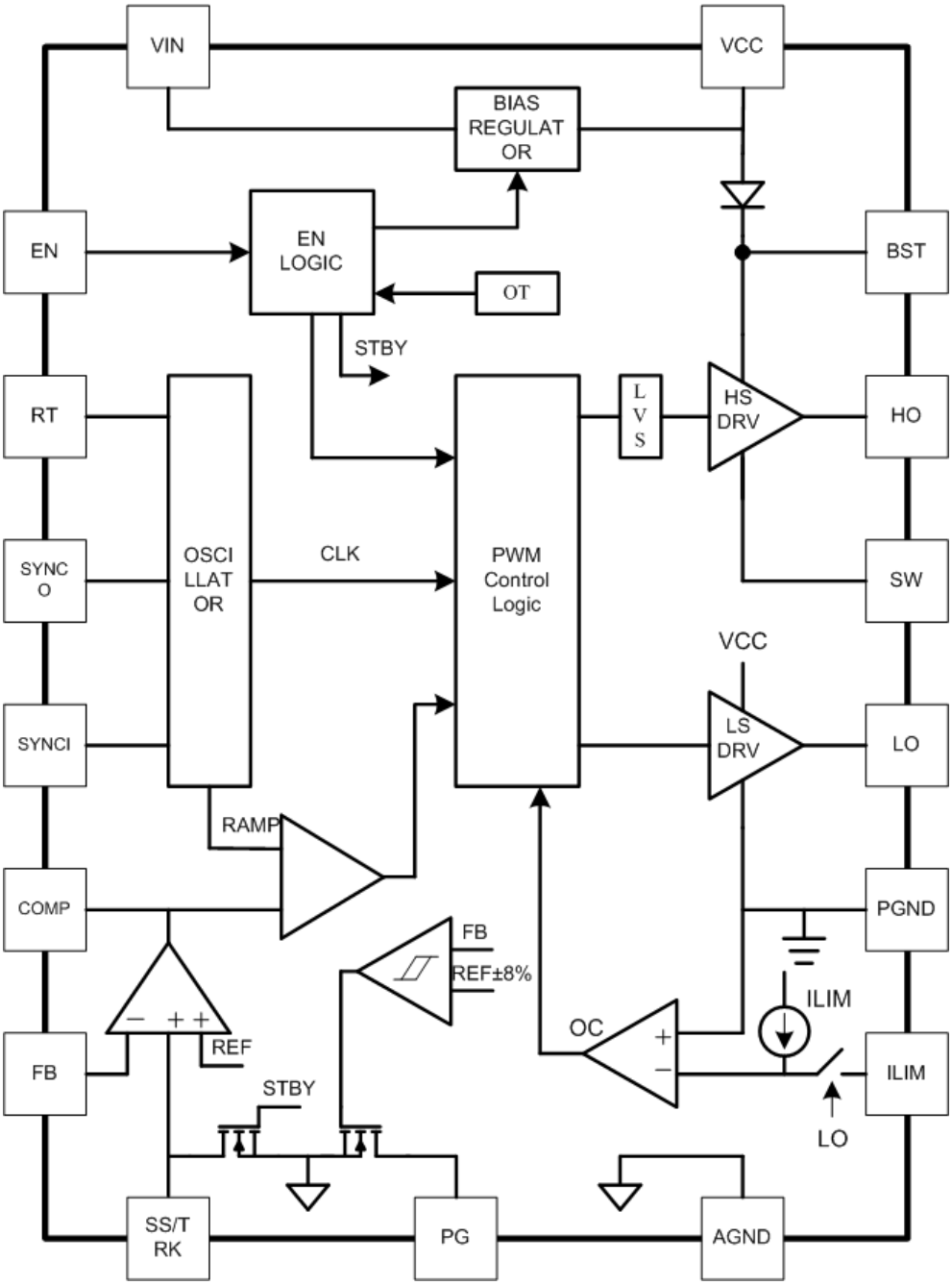


Figure 4. Block Diagram

11 TYPICAL CHARACTERISTICS

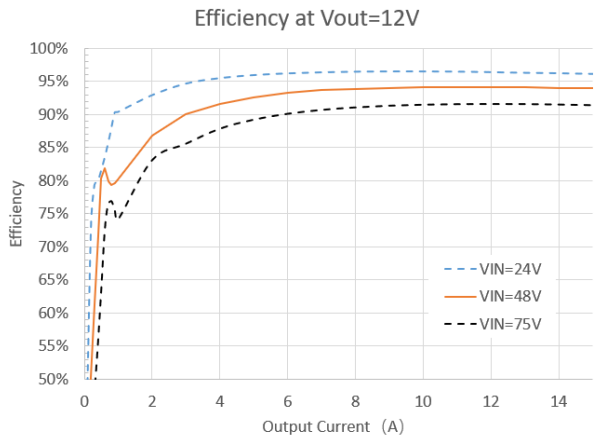


Figure 5. Efficiency at 12V-Vout（400kHz）

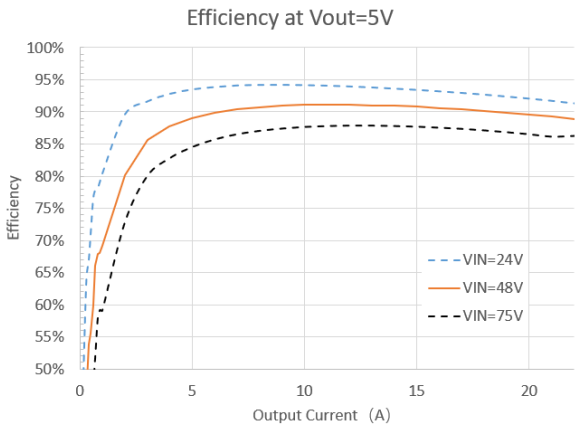
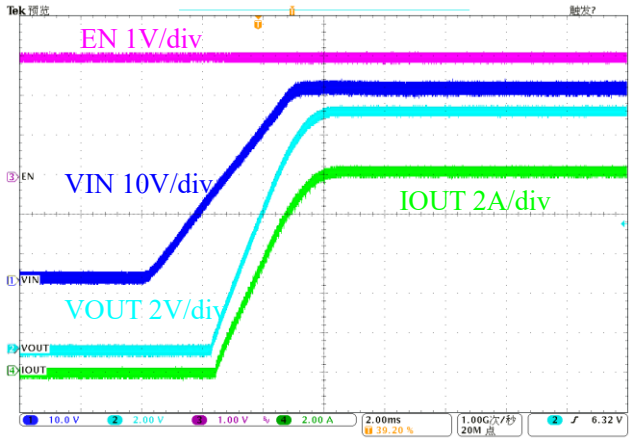
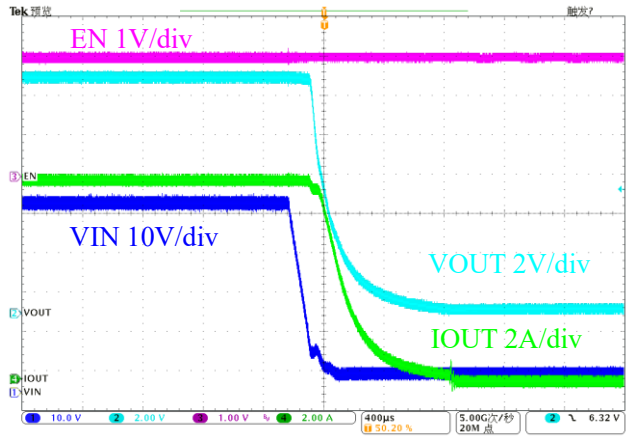


Figure 6. Efficiency at 5V-Vout（230kHz）



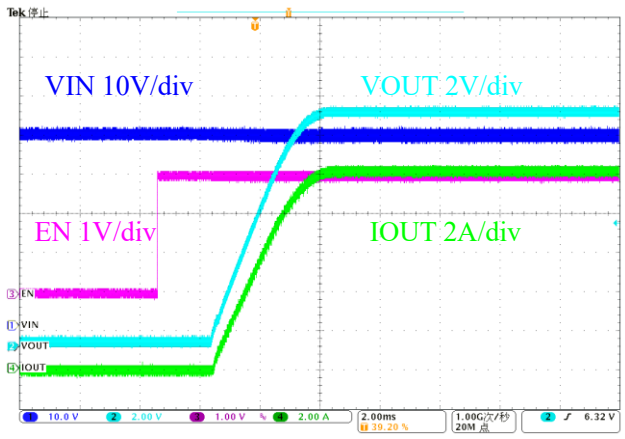
V_{IN}=48V Time(2ms/div) V_{OUT}=12V I_{OUT}=10A

Figure 7. Startup by VIN



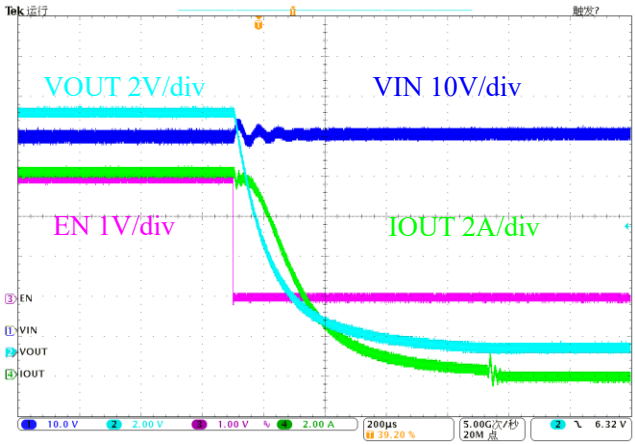
V_{IN}=48V Time(0.4ms/div) V_{OUT}=12V I_{OUT}=10A

Figure 8. Shutdown by VIN



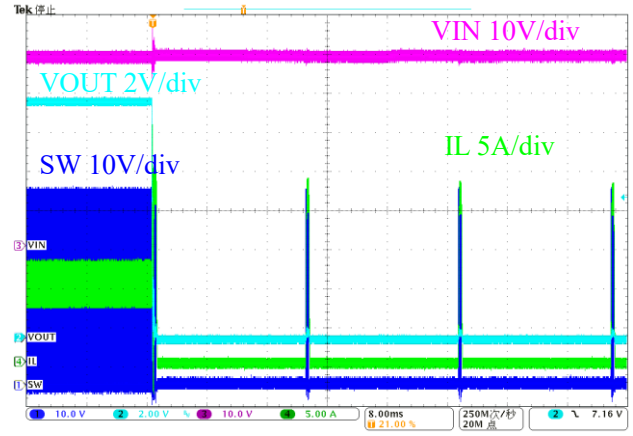
V_{IN}=48V Time(2ms/div) V_{OUT}=12V I_{OUT}=10A

Figure 9. Startup by EN



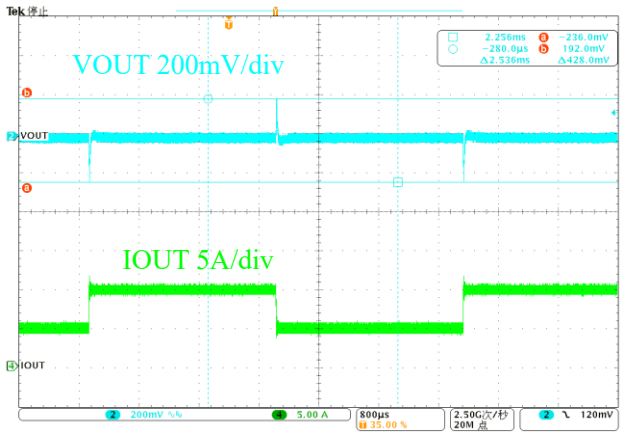
V_{IN}=48V Time(0.2ms/div) V_{OUT}=12V I_{OUT}=10A

Figure 10. Shutdown by EN



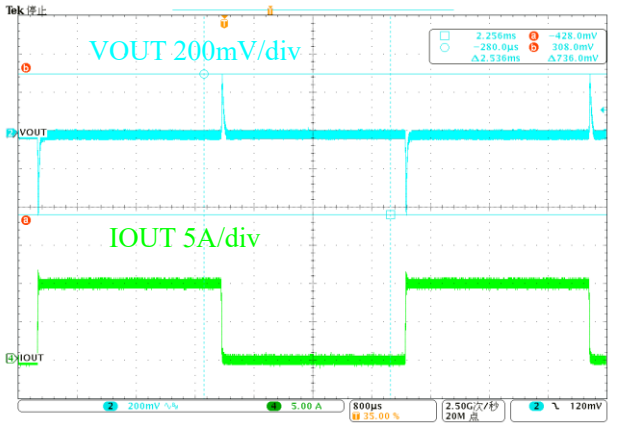
V_{IN}=48V Time(8ms/div) V_{OUT}=12V I_{OUT}=10A

Figure 11. Short Protection and Recovery



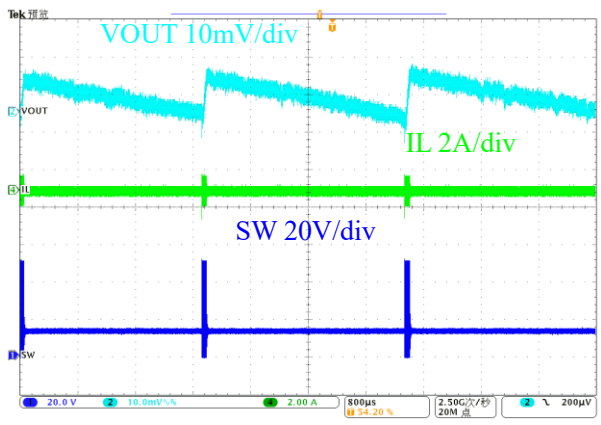
V_{IN}=48V Time(0.8ms/div) V_{OUT}=12V I_{OUT}=5A~10A

Figure 12. Load Transient



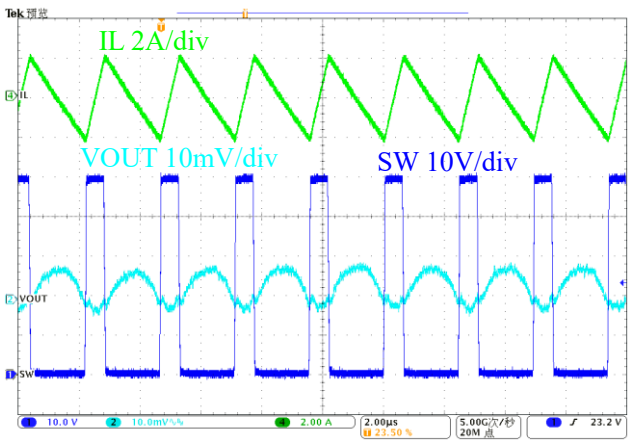
V_{IN}=48V Time(0.8ms/div) V_{OUT}=12V I_{OUT}=0A~10A

Figure 13. Load Transient



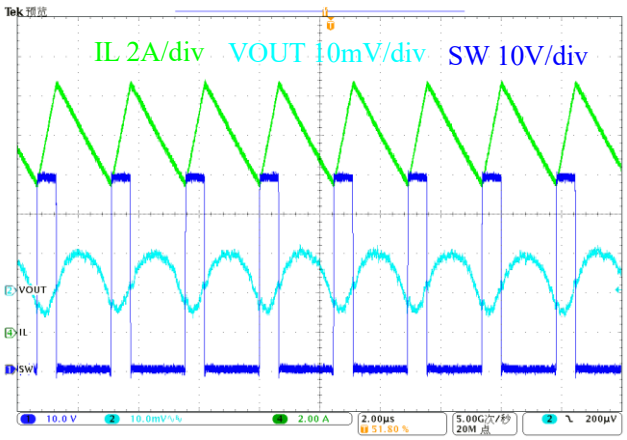
V_{IN}=48V Time(0.8ms/div) V_{OUT}=12V I_{OUT}=0A

Figure 14. Output Ripple (Diode Emulation Mode)



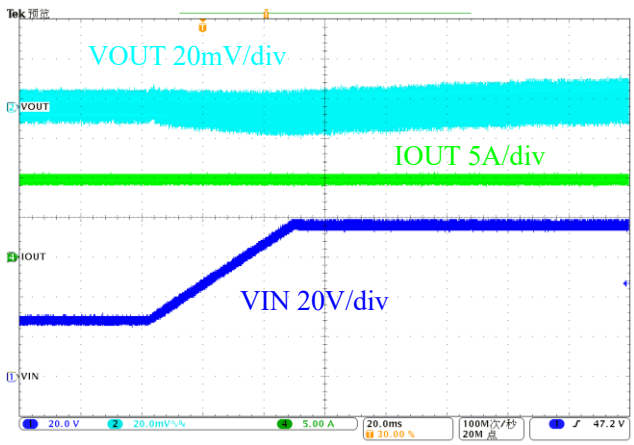
V_{IN}=48V Time(2us/div) V_{OUT}=12V I_{OUT}=0A

Figure 15. Output Ripple (FPWM)



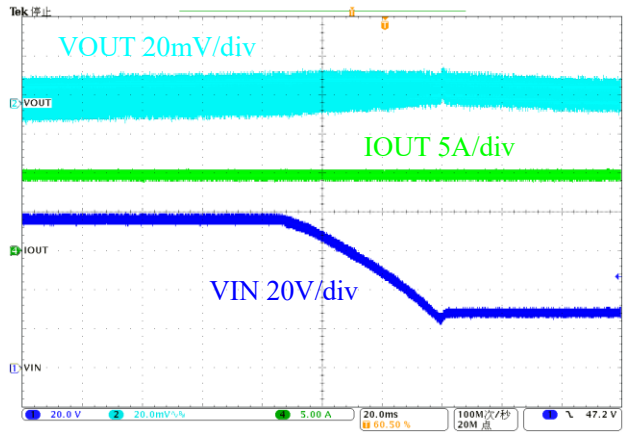
V_{IN}=48V Time(2us/div) V_{OUT}=12V I_{OUT}=10A

Figure 16. Output Ripple



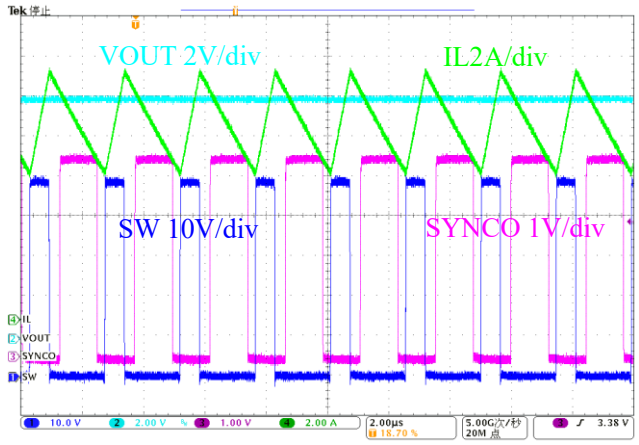
V_{IN}=48V Time(20ms/div) V_{OUT}=12V I_{OUT}=10A

Figure 17. Line Transient Response, 25 V to 75 V



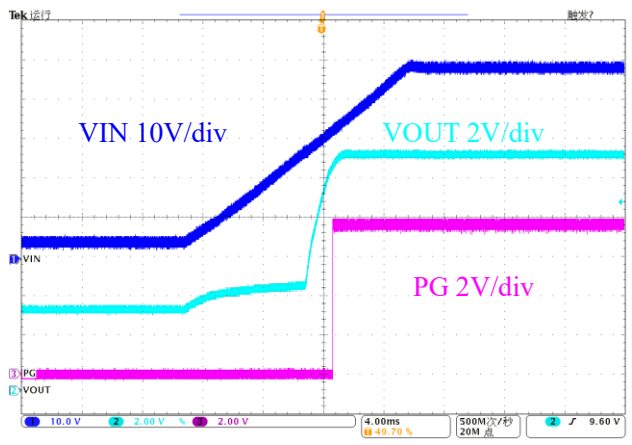
V_{IN}=48V Time(20ms/div) V_{OUT}=12V I_{OUT}=10A

Figure 18. Line Transient Response, 75 V to 25 V



V_{IN}=48V Time(2us/div) V_{OUT}=12V I_{OUT}=10A

Figure 19. SYNCO and SW and IL



V_{IN}=48V Time(4ms/div) V_{OUT}=12V I_{OUT}=0A

Figure 20. Pre-bias Startup

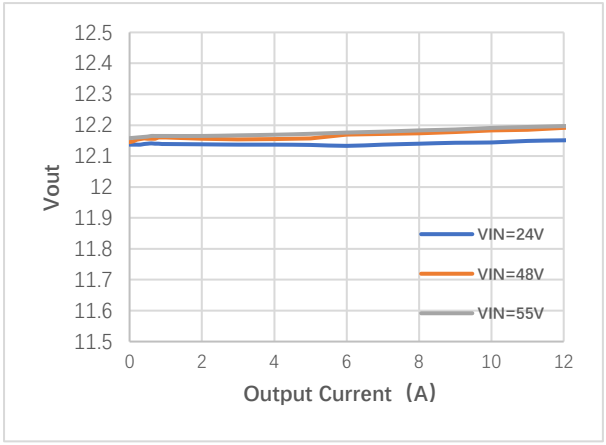


Figure 21. Load and Line Regulation

12 APPLICATIONS

12.1 Operation Overview

The MK9218 operates over a wide input voltage range from 6V to 100V. With appropriate high-side and low-side MOSFET and Inductance, the MK9218 delivers up to 30A output current.

The MK9218 adopts a voltage mode control architecture to achieve excellent accurate voltage output. The switching frequency is adjustable up to 1 MHz, which also can be synchronized to an external clock source to eliminate beat frequencies in noise-sensitive applications.

MK9218 support Forced-PWM (FPWM) and Diode Emulation Mode; FPWM operation eliminates switching frequency variation to minimize EMI, while user selectable diode emulation lowers current consumption at light-load condition.

MK9218 is offered with wide duty cycle from 1% to 98% under appropriate switching frequency, so input and output voltage can easy to be choose.

The MK9218 provides a power good (PG) flag pin to indicate output voltage.

12.2 Enable (EN)

Enable input and undervoltage lockout.
V_{EN} < 0.8V， shutdown mode， VIN to VCC LDO shutdown；
0.8V≤V_{EN} < 1.2V， standby mode， VIN to VCC LDO regulated to 7.5V；
V_{EN} > 1.2V， operating mode， start to operating；
The device has accurate 1.2V rising threshold and a hysteresis current to programable falling threshold for tri-state to reduce quiescent loss. This pin also can be used for programming the VIN turn on voltage with the resistor divider. The UVLO turn-on voltage can be calculated as:

$$V_{UVLO} = (1 + \frac{R_{EN-H}}{R_{EN-L}}) \times V_{EN-H}$$

V_{EN-H} is EN rising threshold voltage, typical is 1.2V.
The UVLO hysteresis is accomplished with an internal 10μA current source that is switched on or off into the impedance of the set-point divider. When the voltage at the EN pin exceeds the rising threshold, the current source is activated to quickly raise the voltage at the EN pin. The hysteresis can be calculated as:

$$V_{hys}(\mathrm{V}) = R_{EN-H} \times 10\mu\mathrm{A}$$

12.3 Switching Frequency (R_T、SYNCI)

When SYNCI is floating or tie to GND, the switch frequency of MK9218 is set by the frequency resistor RT. As shown below, 24.9kΩ resistor sets the switching frequency at 400kHz.

$$F_{SW}(kHz) = \frac{10^4}{R_T(k\Omega)}$$

When SYNCI is connect to an external clock synchronization signal, the switching Frequency is determined by the external clock signal.
Note that the final switching frequency is affected by component tolerant.

Note that the external clock signal frequency must between 0.8× F_{SW} to 1.5× F_{SW}.

12.3 Soft Start and Tracking (SS/TRK)

A capacitor from the SS/TRK pin to GND defines the SS/TRK time, T_{SS}. The MK9218 enters into soft-start immediately after EN exceeds its rising threshold of 1.2 V. Tss is set by Css as shown below:

$$T_{SS} = \frac{V_{REF}(0.8V) \times C_{SS}}{I_{SS}(10uA)}$$

If an external voltage source is connected to the SS/TRK pin, the external soft-start capability of the MK9218 is disabled. The regulated output voltage level is rising follow the external SS/TRK rising slope, when the SS/TRK pin reaches the 0.8V reference voltage level. The regulated output voltage is following the external REF (0.8V).

12.4 Voltage-Mode Control Loop (COMP)

The MK9218 integrates the voltage mode control loop implementation and feeds the input voltage forward to eliminate the input voltage dependence of the PWM modulator gain. for more detail design application information please refer MK9218 reference design parameter; The loop calculation is refer the 12.18 Control Loop Compensation.

12.5 Feed Back (FB)

Feedback input, which connect to the internal voltage EA negative input, choose appropriate R_{F1} and R_{F2} to program the output voltage. For target V_{OUT} setpoint, calculate R_{F1} and R_{F2} using below equation:

$$V_{OUT} = 0.8\text{V} \times (1 + \frac{R_{F2}}{R_{F1}})$$

R_{F1} in the range of 2kΩ to 5kΩ is recommended for most applications. Larger feedback resistors consume less DC current, which is important if light-load efficiency is critical. But too large resistors are not recommended as the feedback path would become more susceptible.

The feedforward capacitor C_{FF} is strongly recommended, which can improve the system stability and transient responses.

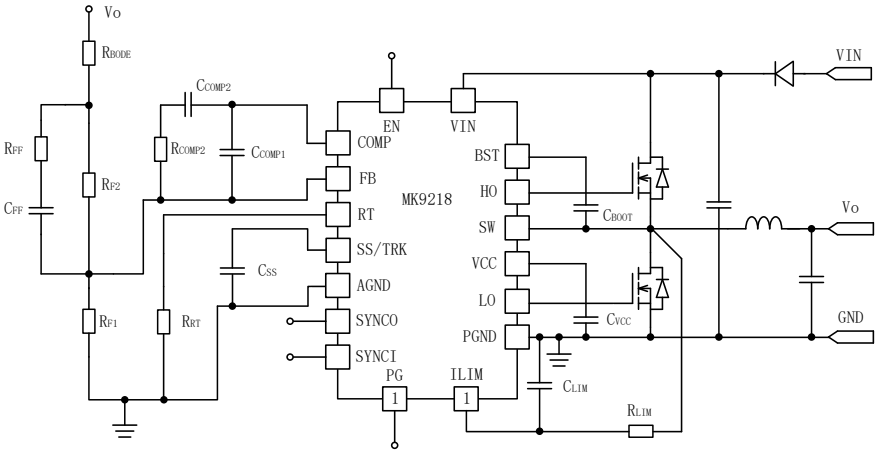


Figure 22. FB connection

12.6 Clock Synchronization and Diode Emulation Mode (SYNCI、SYNCO)

There are 3 functions of SYNCI.
When SYNCI is floating or tie to GND, the switch frequency of MK9218 is set by the frequency resistor RT and works in diodes emulation mode.
When SYNCI is connect to an external clock synchronization signal, the switching Frequency is determined by the external clock signal and works in FPWM mode.
When SYNCI is connect to VCC, it works in FPWM mode;
SYNCO is the output of MK9218, the output of SYNCO is nearly delay 180° of the HO.

12.7 Power Good (PG)

MK9218 provides a PG flag pin to indicate whether the output voltage is within the regulation level. PG is an open-drain output that requires a pullup resistor to a DC source which voltage is less than 14V (If necessary, use a resistor divider to decrease the voltage from a higher voltage pullup rail). The typical range of pullup resistance is about 10kΩ to 100 kΩ. When the FB voltage exceeds 95% of the reference, the internal switch will be turned off and PG can be pulled high by the pullup resistor. If the FB voltage falling below 92% of the reference or rising greater 108% of the reference, the switch will be turned on and PG is pulled low to indicate the output voltage is out of regulation. The function of PG is to set start-up sequencing of downstream converters, fault protection, and output monitoring.

12.8 Current Sensing and OCP (ILIM)

The MK9218 use the negative drop across the low-side FET or current sense resistor at the end of the "OFF" time to measure the inductor current. Allowing for 30% over the minimum current limit for transient recovery and 20% rise in $R_{DS(on)-LS}$ for self-heating of the MOSFET, the voltage drop across the low-side FET at current limit and application diagram is given by below:

$$R_{LIM} = \frac{I_o - \delta I_L/2}{I_{RDS(on)-LS}} \times R_{DS(on)-LS}$$

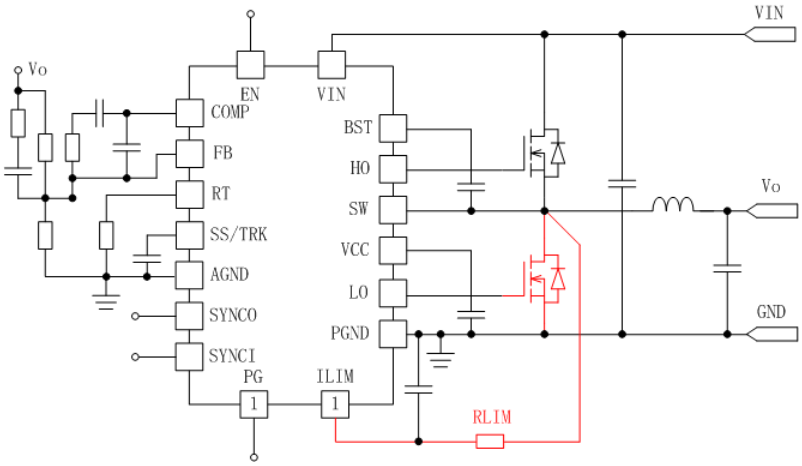


Figure 23. Low-side FET current sense

When use current sense resistor, the voltage drop across the current sense resistor at current limit and application diagram is given by below:

$$R_{LIM} = \frac{I_o - \delta I_L/2}{I_{RS}} \times R_{RS}$$

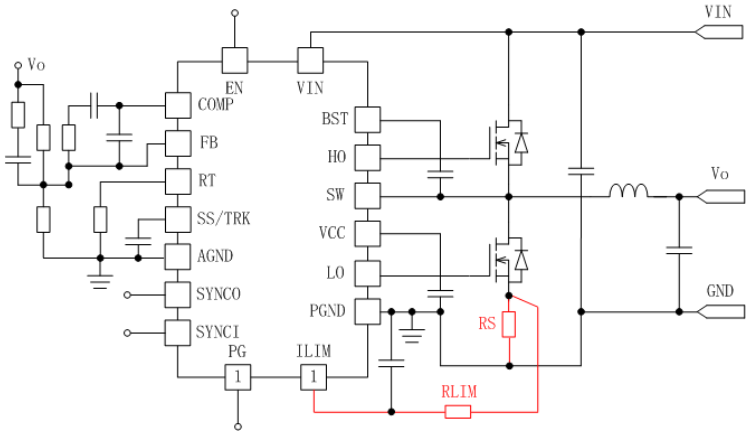


Figure 24. RS current sense

12.9 Gate Drivers (LO, HO)

The MK9218 provide high drive capability up to 2.5A/3.5A, select suitable Rg to reduce switching speed;

12.10 High-Voltage Bias Supply Regulator (VCC)

MK9218 support 100V High-voltage input, it is the high voltage LDO output PIN, output voltage is 7.5V, Connect a ceramic decoupling capacitor between 1 μF and 5 μF from VCC to AGND for stability. Place the capacitor as close as possible to the MK9218 VCC and GND pins.

When application Vout voltage is between 8.5V to 14V,or the system board has 8.5V to 14V voltage rail, this voltage can be connect to VCC through a diodes instead of internal high-voltage LDO, which can reduce internal high voltage LDO power loss, This is very helpful to reduce chip loss and heat generation, especially in scenarios where the input bus voltage is high (for example, applications with an input greater than 60V), application diagram is given by below:

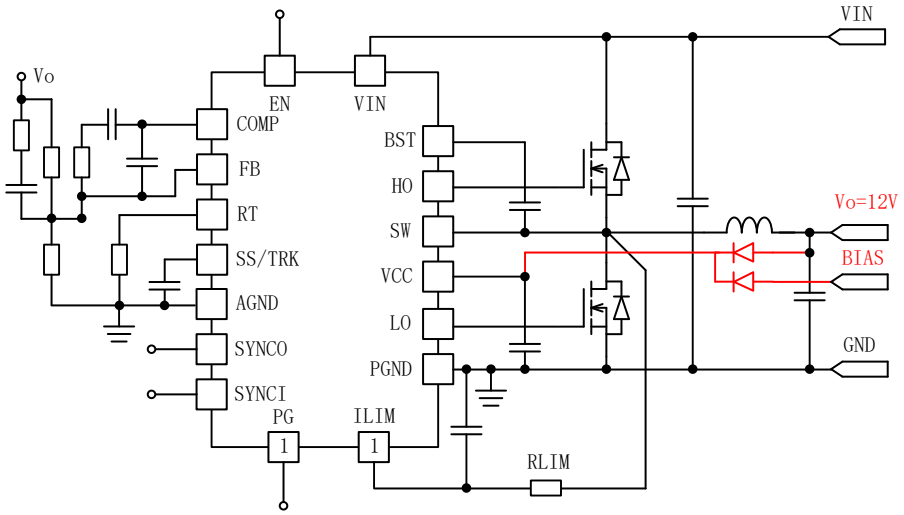


Figure 25. external VCC supply

Notes that if used BIAS voltage to provide VCC supply, VIN is also need to connect to VIN-BUS to

offer startup voltage and current.

Notes that if used BIAS voltage to provide VCC supply and VIN voltage is less than the BIAS voltage, an extra diodes is needed to connect between VIN and VIN-BUS show as below:

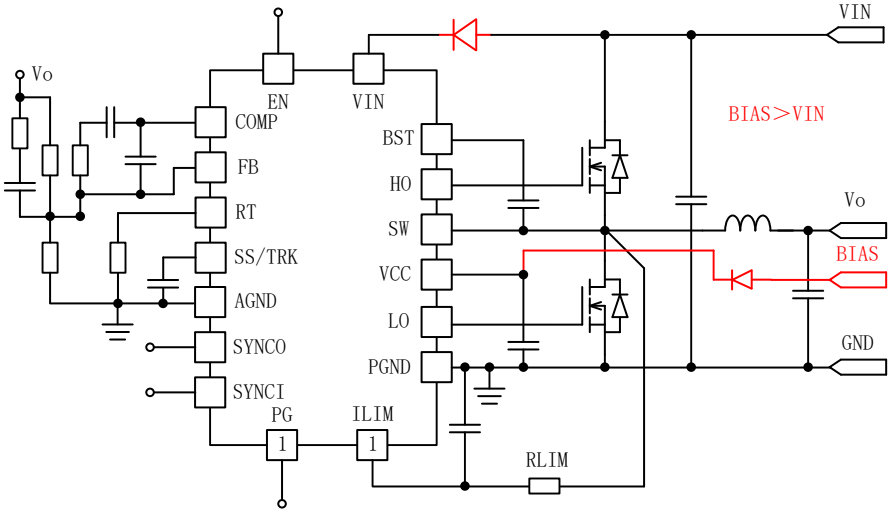


Figure 26. BIAS VCC supply（BIAS＞VIN）

12.11 Boot-strap For High-side MOSFET (BST)

This capacitor provides the energy for high-side gate driver. A high-quality COG 100nF ceramic capacitor connected between the BS pin and the SW pin is recommended. Also, a RC series net can be used for slow down the turn-on speed of high side MOSFET.

12.12 Switching Node (SW)

Switching node. Connect to the bootstrap capacitor, the source terminal of the high side MOSFET and the drain terminal of the low-side MOSFET using short, low inductance paths. It also can be connected to one end of the inductance. Pay attention to this area to be a thermal pad when PCB layout.

12.13 High-Voltage Input (VIN)

MK9218 support 100V High-voltage input, it is the high voltage LDO input PIN, an input capacitor and Resistance is necessary to limit the input ripple voltage ensure the LDO work stability

VIN is also used to provide PWM feedforward Gain(VIN/V_{RAMP}),so VIN is must connected to VIN-BUS..

12.14 OTP

MK9218 support OTP(over temperature protection),The thermal shutdown threshold is about 175℃ which is T_J, The OTP is a non-latching protection, thermal shutdown hysteresis is about 20℃.

12.15 Input Capacitor (C_{IN})

An input capacitor is necessary to limit the input ripple voltage while providing AC current to the buck converter at every switching cycle. The input ripple voltage ΔV_{IN} at input capacitor is calculated as:

$$\Delta V_{IN} = \frac{I_{OUT} \times D \times (1 - D)}{F_{SW} \times C_{IN}} + I_{OUT} \times R_{ESR}$$

The capacitance of input capacitor is calculated as:

$$C_{IN} \geq \frac{I_{OUT} \times D \times (1 - D)}{F_{SW} \times (\Delta V_{IN} - I_{OUT} \times R_{ESR})}$$

To minimize the potential noise problem, a X5R or better grade capacitor with sufficient voltage rating is recommended. This capacitor should be close to the VIN and GND pins to minimize the loop area formed by C_{IN} and VIN/GND pins. In this application, a 0.1µF low ESR ceramic capacitor is recommended.

12.16 Output Inductor (L)

It is recommended to choose the ripple current of inductor between 30% to 50% of the rated load current I_{OUT} (max) for most applications. The inductance is calculated as:

$$L = \frac{V_{OUT}}{F_{SW} \times \Delta I_L} \times (1 - \frac{V_{OUT}}{V_{IN}})$$

And the peak current of inductor is calculated as:

$$I_L(\text{peak}) = I_{OUT}(max) + \frac{\Delta I_L}{2}$$

The saturation current rating of the inductor must greater than the I_L (peak). An inductor whose saturation current is above the current limit setting of the MK9218 will be best choice. Note that inductor saturation current levels generally decrease as the inductor temperature increase.

12.17 Output Capacitor (C_{OUT})

The output capacitor limits the capacitive voltage ripple at the converter output. This voltage ripple which is generated from the triangular inductor current ripple flowing into and out of the capacitor can be calculated as:

$$\Delta V_{OUT} = \frac{\Delta I_L}{8 \times F_{SW} \times C_{OUT}}$$

Above equation only take the steady state ripple into consideration. The transient requirements also must be taken into consideration when selecting the output capacitor. The X7R or better grade ceramic capacitor larger than 220µF is recommended.

12.18 Control Loop Compensation

The MK9218 integrates the voltage mode control loop implementation and feeds the input voltage forward to eliminate the input voltage dependence of the PWM modulator gain. The voltage mode buck control loop is show as below:

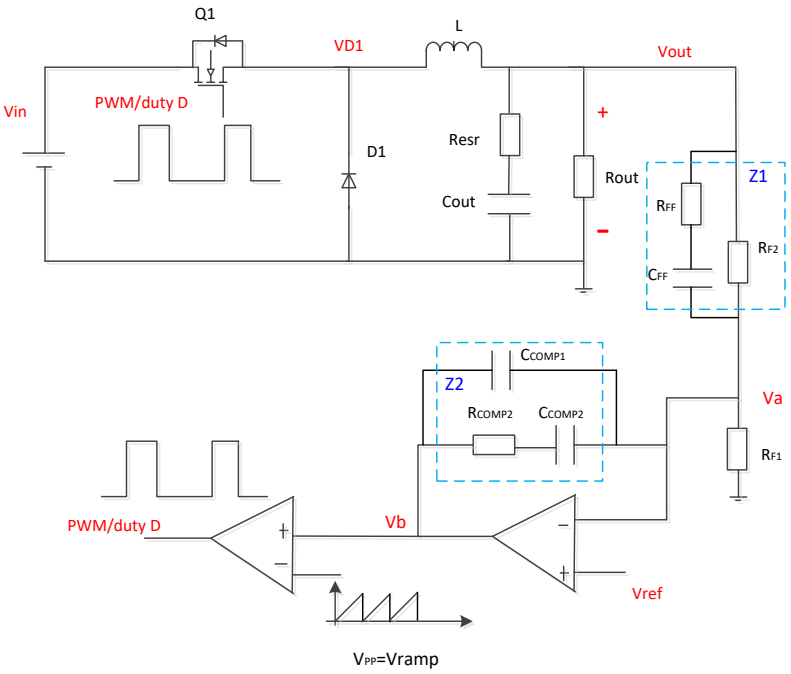


Figure 27. Buck circuit voltage loop control diagram

It is the equivalent control block diagram. kf and Gv(s) are the transfer function of the regulator; kd is the transfer function from the regulator output to the duty cycle; Kpwm is the transfer function from the duty cycle to the diode voltage VD1; G1(s) is the transfer function from VD1 to the output voltage.

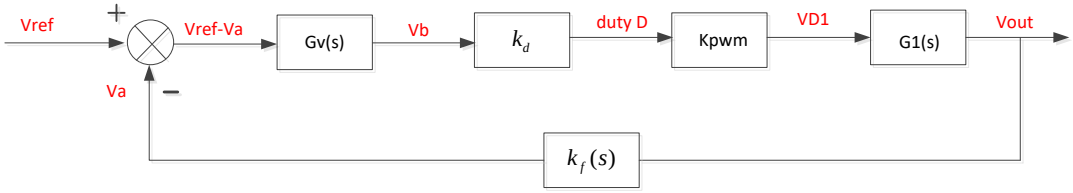


Figure 28. Buck equivalent control block diagram

Step1、calculate $k_f(s) \times G_v(s)$

$$\begin{cases} V_a = \dfrac{R_{F1}}{R_{F1}+Z_1}V_{out} \;\Rightarrow\; V_{ref}-V_a = V_{ref} - \dfrac{R_{F1}}{R_{F1}+Z_1}V_{out} = \dfrac{(R_{F1}+Z_1)V_{ref} - R_{F1}V_{out}}{R_{F1}+Z_1} \\ \dfrac{V_{out}-V_{ref}}{Z_1} = \dfrac{V_{ref}}{R_{F1}} + \dfrac{V_{ref}-V_b}{Z_2} \Rightarrow \dfrac{(Z_1+R_{F1})V_{ref} - R_{F1}V_{out}}{Z_1 R_{F1}} = \dfrac{-V_{ref}+V_b}{Z_2} \end{cases}$$

then

$$\begin{cases} G_v(s) = \dfrac{V_b}{(V_{ref}-V_a)} = \dfrac{Z_2 \times (Z_1+R_{F1})}{Z_1 R_{F1}} \\ k_f(s) = \dfrac{R_{F1}}{Z_1+R_{F1}} \end{cases}$$

Get the loop compensation function result

$$k_f(s) \times G_v(s) = \frac{Z_2}{Z_1}$$

Step2、calculate K_d

The regulator output voltage Vb is compared with the sawtooth wave of amplitude Vramp to get the duty cycle D, and the transfer function of this link is Kd.

$$k_d = \frac{D}{V_b} = \frac{1}{V_{ramp}}$$

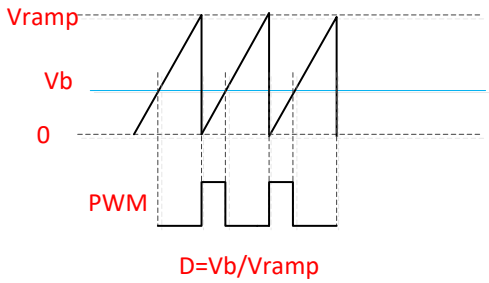


Figure 29. V_{RAMP} wave

Step3、calculate Kpwm

The PWM signal is applied to the switch Q1

0~DT period (T is the switching period): Q1 is turned on, and the voltage across the diode D1 is Vin;

During DT~T: Q1 is off, the inductor current flows through D1, and the voltage across the diode D1 is 0.

Therefore, the average value of the voltage across the diode D1 is DVin.

$$k_{pwm} = \frac{V_{D1}}{D} = \frac{DV_{in}}{D} = V_{in}$$

Step4、calculate G1(s):

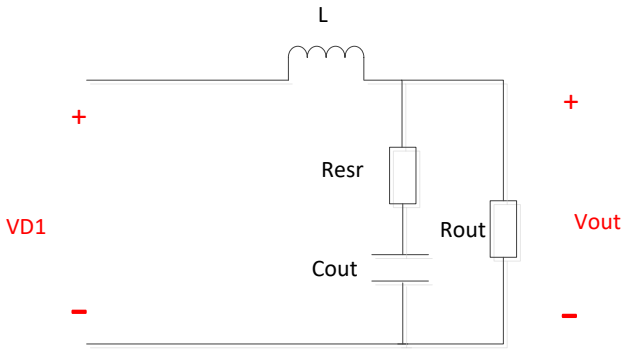


Figure 29. Vout Vs V_{D1}

$$G_1(s) = \frac{V_{out}(s)}{V_{D1}(s)} = \frac{1 + R_{esr}C_{out}s}{\frac{L * R_{out}C_{out} + L * R_{esr}C_{out}}{R_{out}}s^2 + \frac{L + R_{out}R_{esr}C_{out}}{R_{out}}s + 1}$$

Resr<<Rout, to further simplify the transfer function,

$$G_1(s) = \frac{V_{out}(s)}{V_{D1}(s)} = \frac{1 + R_{esr}C_{out}s}{L * C_{out}s^2 + \frac{L}{R_{out}}s + 1}$$

The transfer function has a zero point and a double pole.

Zero frequency:

$$f_{ESR} = \frac{1}{2\pi \times R_{esr}C_{out}}$$

Double pole frequency:

$$f_{LC} = \frac{1}{2\pi\sqrt{L * C_{out}}}$$

Step5、Regulator parameter design

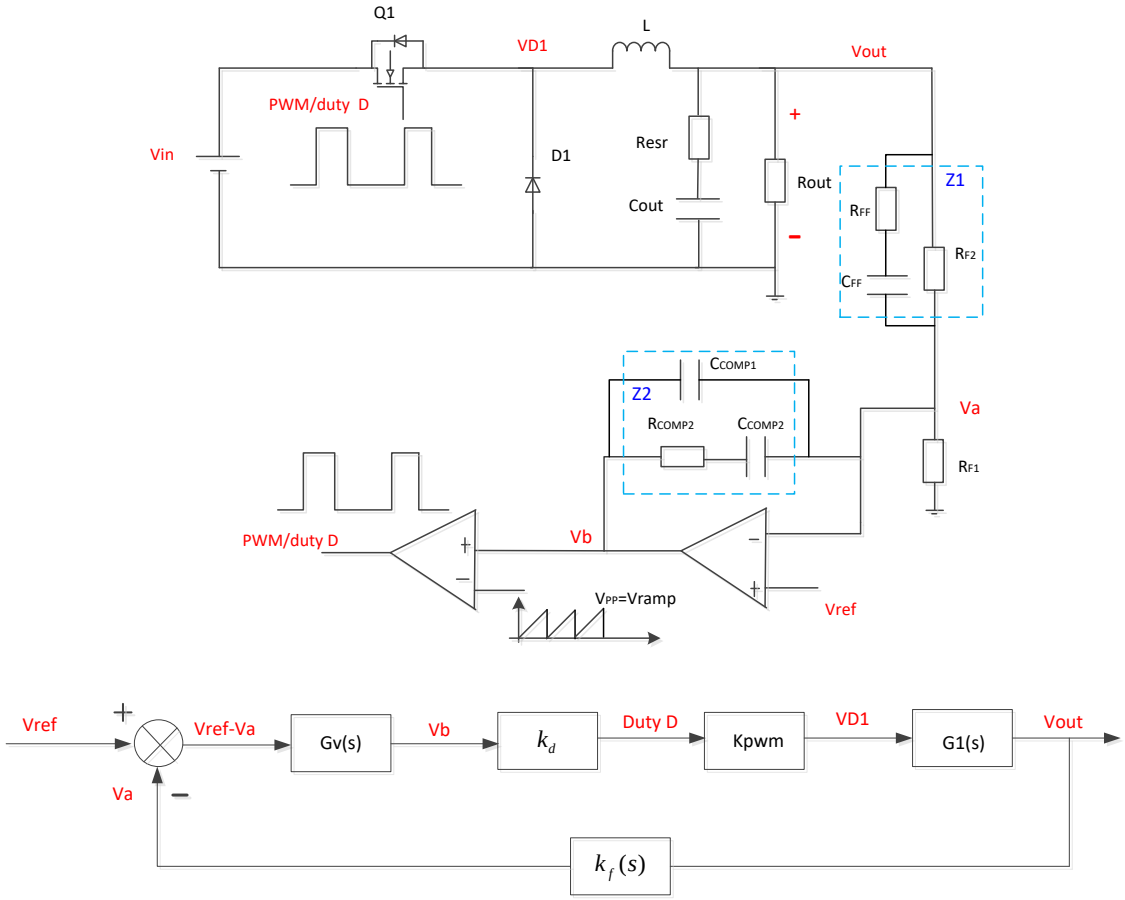


Figure 30. control loop and equivalent control block

Obtain the open-loop transfer function of the system:

$$G_o(s) = k_f(s) \times G_v(s) \times k_d \times k_{pwm} \times G_1(s)$$

$$G_o(s) = \frac{Z_2(s)}{Z_1(s)} \times \frac{k_{pwm}}{V_{ramp}} \times \frac{1 + R_{esr}C_{out}s}{L * C_{out}s^2 + \frac{L}{R_{out}}s + 1}$$

$$\frac{Z_2(s)}{Z_1(s)} = \frac{1}{sR_{F2}(C_{COMP2}+C_{COMP1})} \times \frac{(R_{COMP2}C_{COMP2}s+1)((R_{F2}+R_{FF})C_{FF}s+1)}{(\frac{R_{COMP2}C_{COMP2}C_{COMP1}}{C_{COMP2}+C_{COMP1}}s+1)(R_{FF}C_{FF}s+1)}$$

In order to simplify the regulator transfer function design process, when designing regulator parameters, take C_{COMP2}>>C_{COMP1}. then

$$\frac{Z_2(s)}{Z_1(s)} = \frac{1}{sR_{F2}C_{COMP2}} \times \frac{(R_{COMP2}C_{COMP2}s+1)((R_{F2}+R_{FF})C_{FF}s+1)}{(R_{COMP2}C_{COMP1}s+1)(R_{FF}C_{FF}s+1)}$$

The regulator has two poles:

$$f_{p1} = \frac{1}{2\pi \times R_{FF}C_{FF}},\quad f_{p2} = \frac{1}{2\pi \times R_{COMP2}C_{COMP1}}$$

Two zeros:

$$f_{z1} = \frac{1}{2\pi \times R_{COMP2}C_{COMP2}},\quad f_{z2} = \frac{1}{2\pi \times (R_{F2}+R_{FF})C_{FF}}$$

The two poles and two zeros show as below:

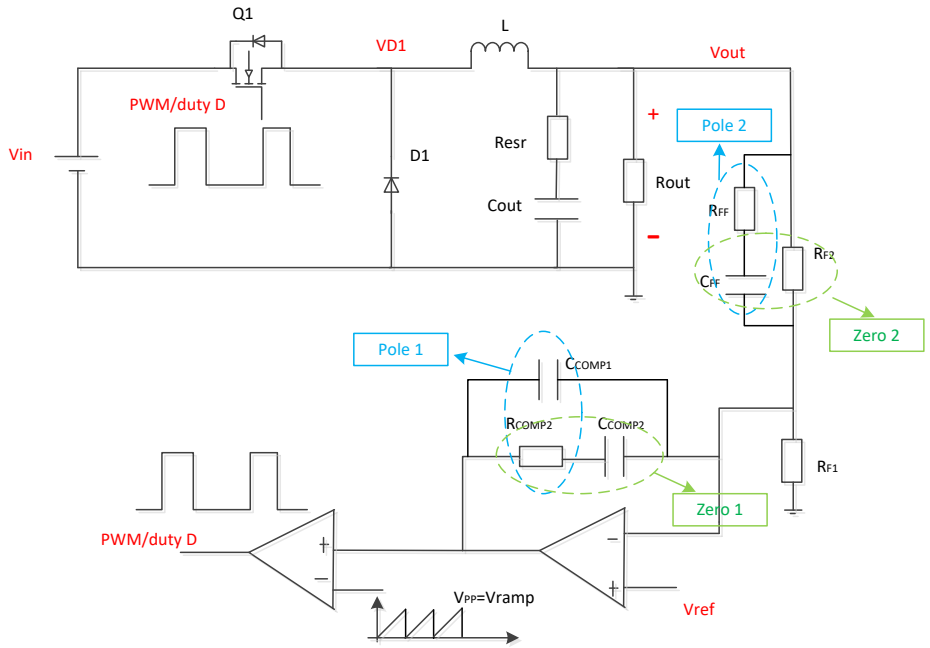


Figure 30. control loop with poles and zeros

And the final Open loop transfer function:

$$G_o(s) = \frac{1}{sR_{F2}C_{COMP2}} \times \frac{(R_{COMP2}C_{COMP2}s+1)((R_{F2}+R_{FF})C_{FF}s+1)}{(R_{COMP2}C_{COMP1}s+1)(R_{FF}C_{FF}s+1)} \times \frac{V_{\text{in}}}{V_{ramp}} \times \frac{1+R_{esr}C_{out}s}{L*C_{out}s^2+\frac{L}{R_{out}}s+1}$$

$$= \frac{V_{\text{in}}}{V_{ramp}} \times \frac{1}{R_{F2}C_{COMP2}} \times \frac{1}{s} \times \frac{(R_{COMP2}C_{COMP2}s+1)((R_{F2}+R_{FF})C_{FF}s+1)}{(R_2C_3s+1)(R_3C_2s+1)} \times \frac{1+R_{esr}C_{out}s}{L*C_{out}s^2+\frac{L}{R_{out}}s+1}$$

Step6、calculate Compensation component parameters:

The crossover frequency of the open loop gain is set to 1/5~1/10 of the switching frequency;

$f_c = (\frac{1}{10}\sim\frac{1}{5})f_{sw}$ f_c is crossover frequency, f_{sw} is switching frequency;

$\frac{V_{in}}{V_{ramp}} \times \frac{1}{R_{F2}C_{COMP2}} \times \frac{1}{k_1} = 2\pi f_c$ （$f_{LC} << f_c$， get k_1）

Usually RF2 and RF1 can be set first according to Vout, so

$C_{COMP2} = \frac{V_{IN}}{V_{ramp} \times \pi f_c \times R_{F2} \times 2k_1}$ ①

The first pole is equal to the zero caused by the out capacitor esr：

$f_{p1} = \frac{1}{2\pi \times R_{FF}C_{FF}} = f_{esr} = \frac{1}{2\pi \times R_{esr}C_{out}}$ ②

The second pole is equal to half of the switching frequency：

$f_{p2} = \frac{1}{2\pi \times R_{COMP2}C_{COMP1}} = f_{p2} = \frac{1}{2} f_{sw}$ ③

Two zero points of the regulator (f_{Z1}: compensate the first zero point, f_{Z2}: compensate the second zero point)

$f_{z1} = \frac{1}{2\pi \times R_{COMP2}C_{COMP2}} = k_1 f_{LC}$ （$k_1 = 0.5 \sim 1$） ④

$f_{Z2} = \frac{1}{2\pi \times (R_{F2}+R_{FF})C_{FF}} = f_{LC}$ ⑤

By the formula ①－⑤， calculate the Compensation component parameters：

$C_{COMP2} = \frac{V_{IN}}{V_{ramp} \times \pi f_c \times R_{F2} \times 2k_1}$

$R_{COMP2} = \frac{V_{ramp}}{V_{IN}} \frac{f_c}{f_{LC}} R_{F2}$

$C_{COMP1} = \frac{1}{\pi \times R_{COMP2} \times f_{sw}}$

$R_{FF} = \frac{f_{LC}}{f_{esr} - f_{LC}} R_{F2}$

$C_{FF} = \frac{1}{2\pi \times f_{esr} \times R_{FF}}$

For example：

Vin=6.5-100V, Vout=5V, Iout=0-20A, Fsw=230kHz, V_{IN}/V_{RAMP}=15， L=3.3uH, Cout=549uF, ESR=3mΩ, R_{F2}=23.2kΩ， R_{F1}=4.42kΩ。

$f_{LC} = \frac{1}{2\pi\sqrt{L*C_{out}}}$=3.74kHz

$f_{ESR} = \frac{1}{2\pi \times R_{esr}C_{out}}$=97kHz

$f_c = \frac{1}{8.6} f_{sw} = 27\text{kHz}$ （f_c *is usually* （$\frac{1}{10} \sim \frac{1}{5}$） of f_{sw};

$C_{COMP2} = \frac{V_{IN}}{V_{RAMP} \times \pi f_c \times R_{F2} \times 2k_1}$=4.8nF （$k_1$ 取 0.8）

$R_{COMP2} = \frac{V_{RAMP}}{V_{IN}} \frac{f_c}{f_{LC}} R_{F2}$=11k

$$C_{COMP1} = \frac{1}{\pi \times R_{COMP2} \times f_{sw}} = 126pF \quad (150\text{pF})$$

$$R_{FF} = \frac{f_{LC}}{f_{esr} - f_{LC}} R_{F2} = 930 \quad (1000)$$

$$C_{FF} = \frac{1}{2\pi \times f_{esr} \times R_{FF}} = 1.6nF \quad (1.8nF)$$

13 LAYOUT

13.1 Layout Guideline

To achieve high performance of the MK9218, the following layout tips must be followed.

(1) At least one low-ESR ceramic bypass capacitor VCC must be used. Place the capacitor as close as possible to the MK9218 VCC and GND pins.

(2) Minimize the loop area formed by C_{IN} connections to VIN and GND pins, refer to figure 25.

(3) Inductor must be placed close to the SW pin. Minimize the area of SW trace to avoid the potential noise problem.

(4) Maximize the PCB area connecting to the GND pin and thermal pad. If it is allowed, a ground plane can be used as noise shielding and heat dissipation path.

(5) Place the feedback resistors, R_{f1} and R_{f2}, close to the FB pin. Route the feedback V_{OUT} sense path away from noisy nodes such as the SW net.

(6) The RT pin is sensitive to noise. The on-time set resistor R_T must be close to the device.

(7) BST capacitor to high-side MOS gate path width is better wider than 15mil(demo is 20mil);

(8) VCC capacitor to low-side MOS gate path width is better wider than 15mil(demo is 20mil),it recommended that 2 vias placed near to VCC capacitor GND to reduce driver path resistance.

13.2 Layout Example

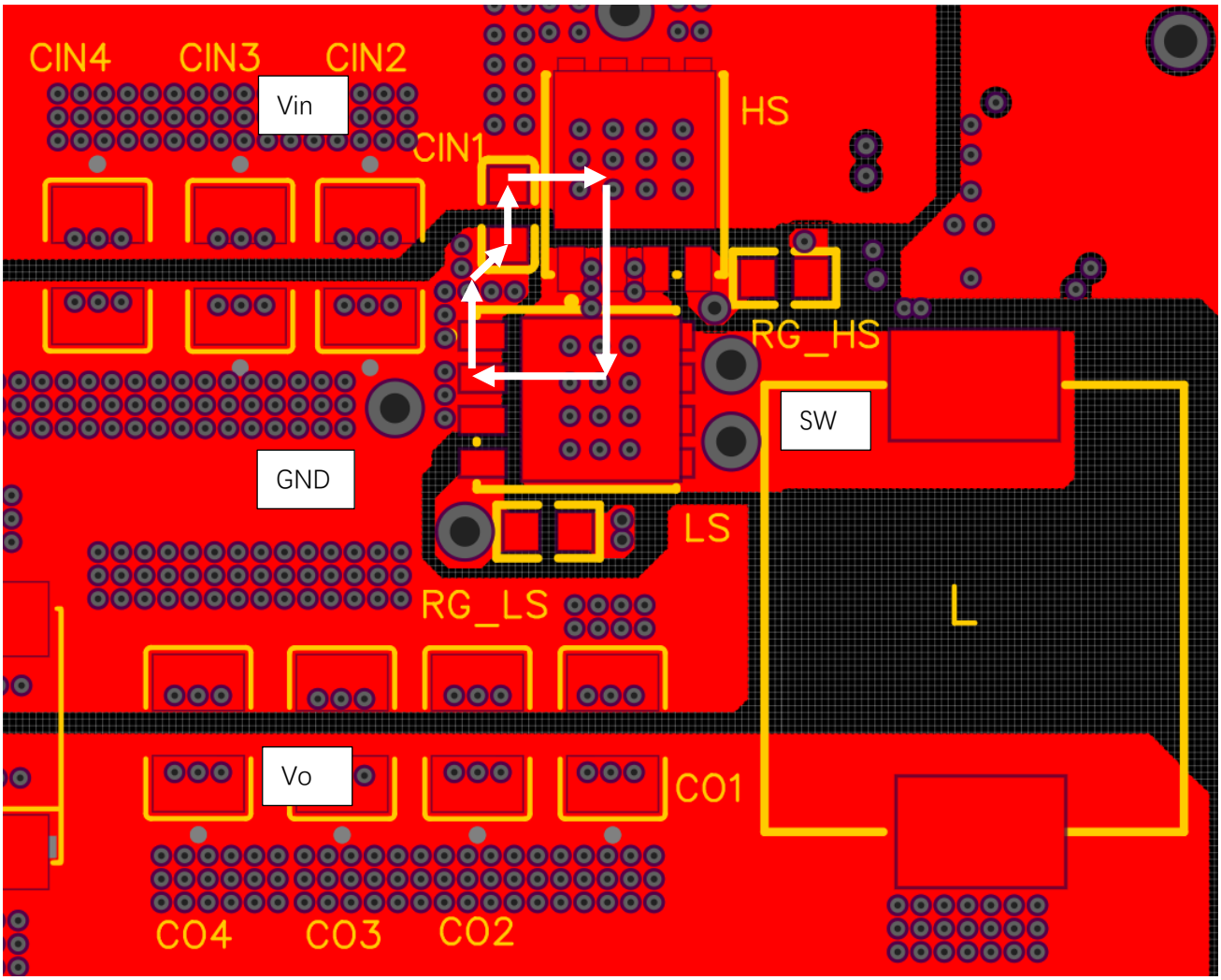


Figure 31. MK9218 Power Loop Layout Example

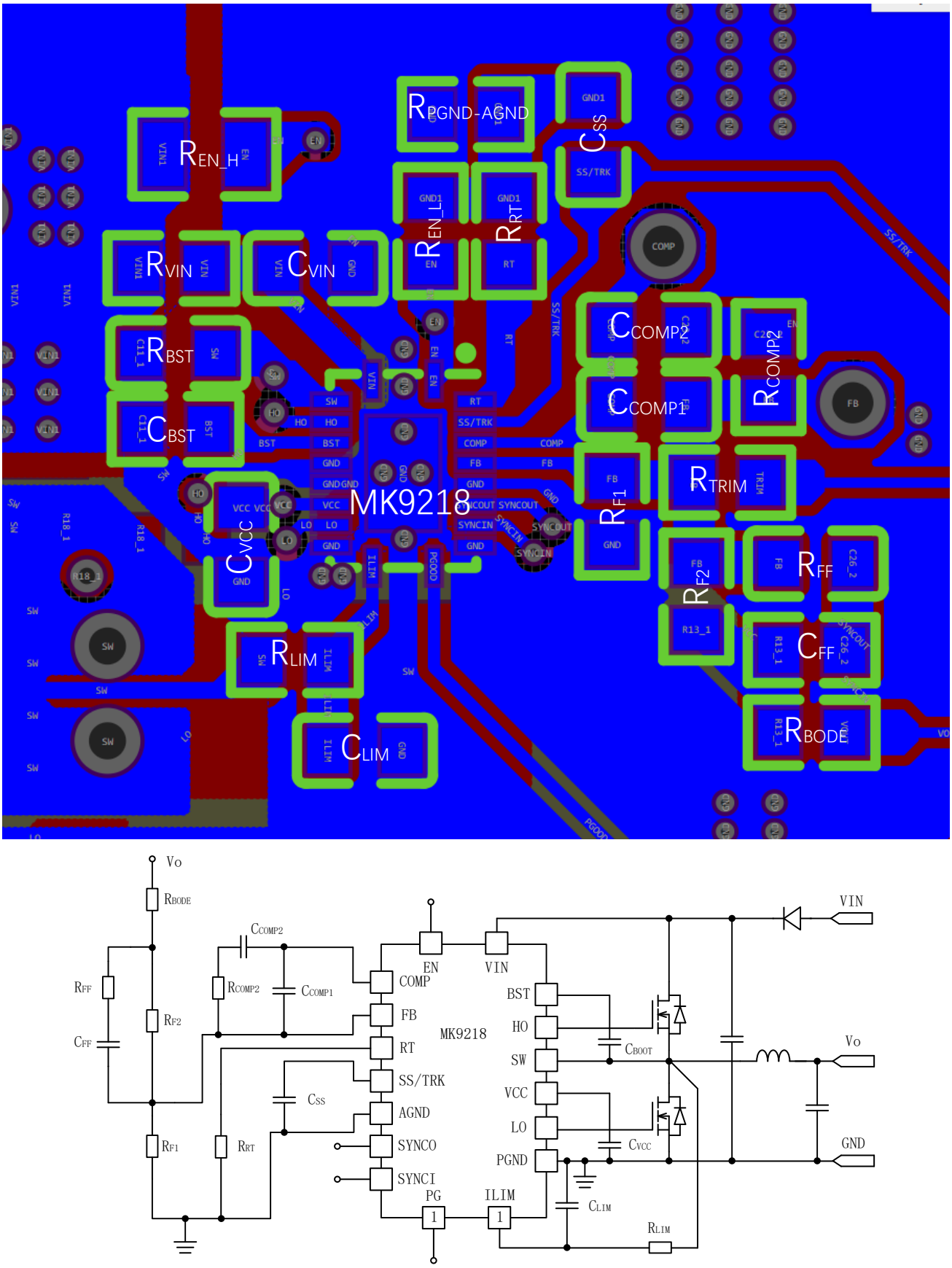


Figure 32. MK9218 controller Loop Layout Example

14 REFERENCE DESIGN

14.1 Reference design 1

Vin=6.5-100V
Vout=5V
Iout=0-20A
Fsw=230kHz

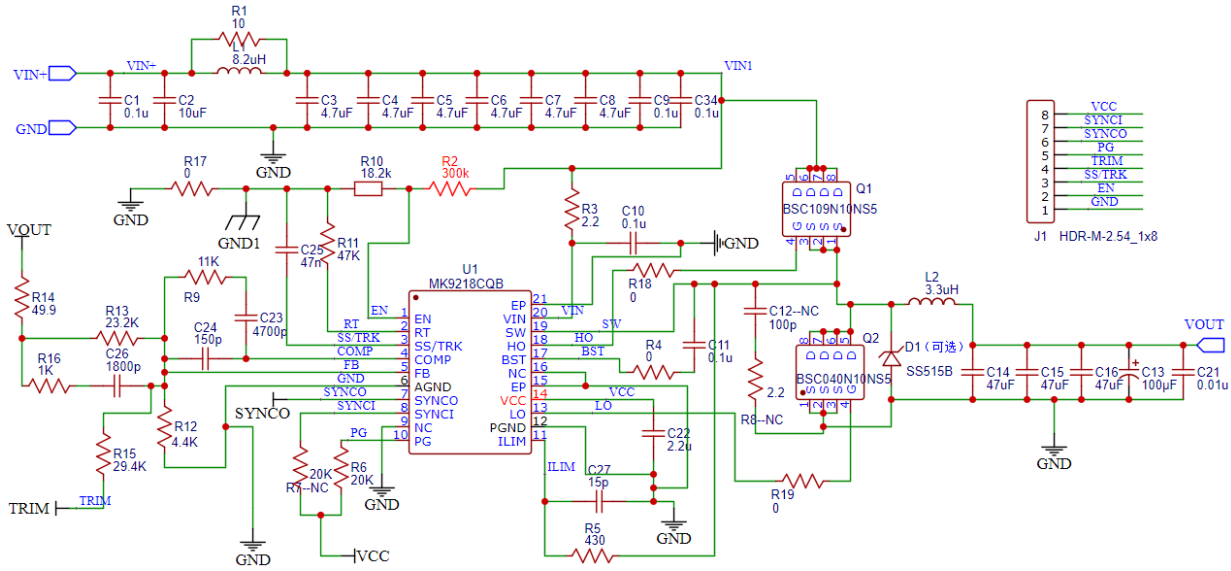


Figure 33. Reference design 1

14.2 Reference design 2

Vin=15-100V
Vout=12V
Iout=0-12A
Fsw=400kHz

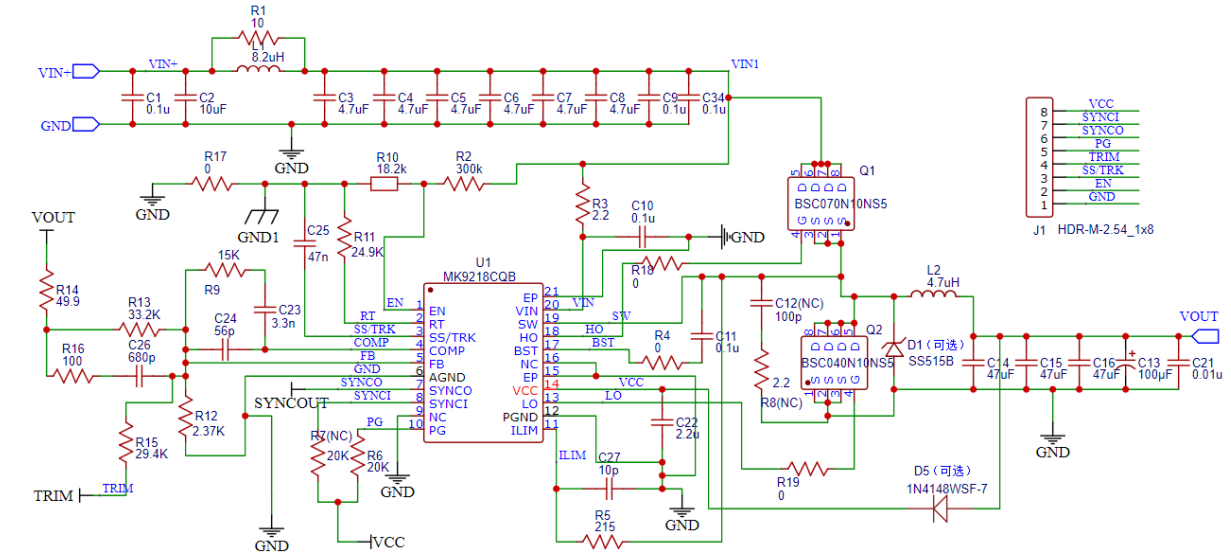


Figure 34. Reference design 2

14.3 Reference design 3

Vin=28-100V
Vout=24V
Iout=0-6A
Fsw=400kHz

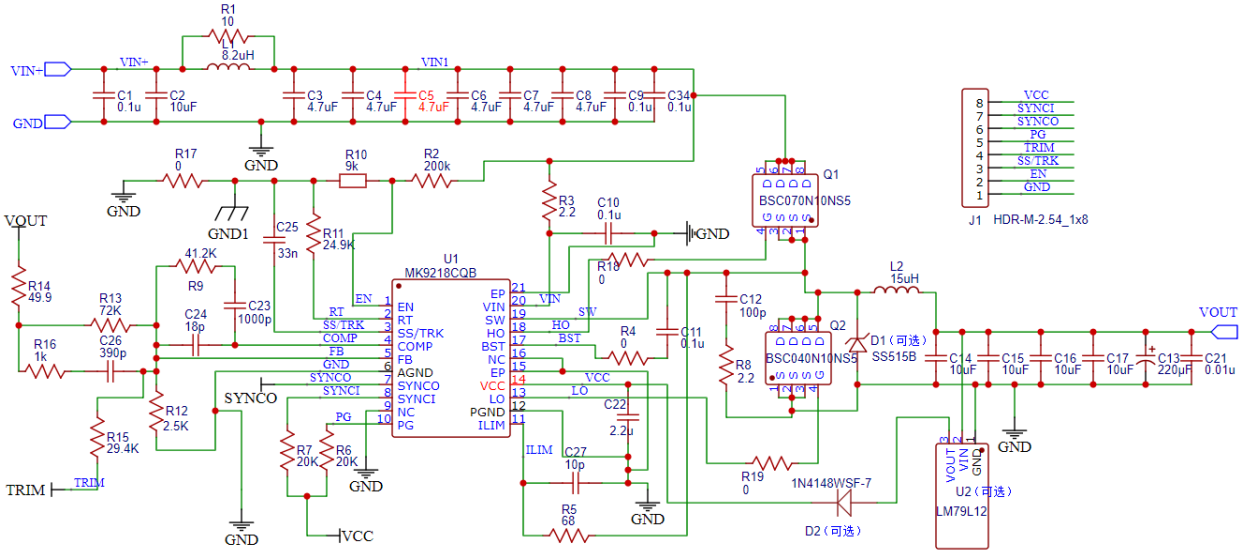


Figure 35. Reference design 3

15 PACKAGE

15.1 Package Size

15.1.1 MK9218CQB package size

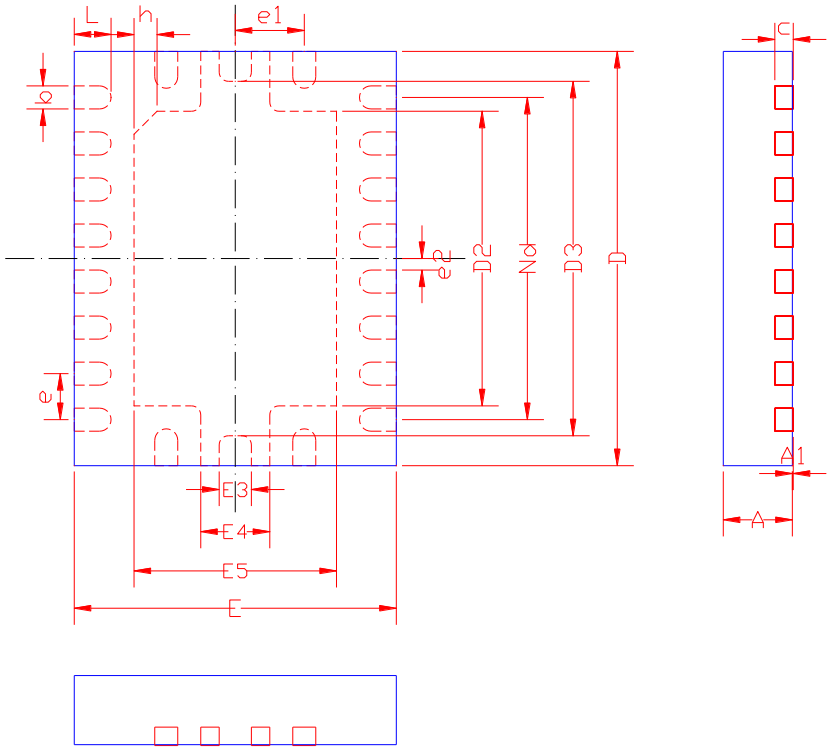


Figure36. package dimensions

SYMBOL	Dimensions(mm)		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	-	0.01	0.05
b	0.18	0.25	0.30
c	0.18	0.20	0.25
D	4.40	4.50	4.60
D2	3.10	3.20	3.30
D3	3.85REF		
e	0.50BSC		
e1	0.75BSC		
e2	0.25BSC		
Nd	3.50BSC		
E	3.40	3.50	3.60
E3	0.35REF		
E4	0.75REF		
E5	2.10	2.20	2.30
L	0.35	0.40	0.45
h	0.20	0.25	0.30

NOTES:

1. This drawing is subject to change without notice
2. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

15.1.2 MK9218DQB package size

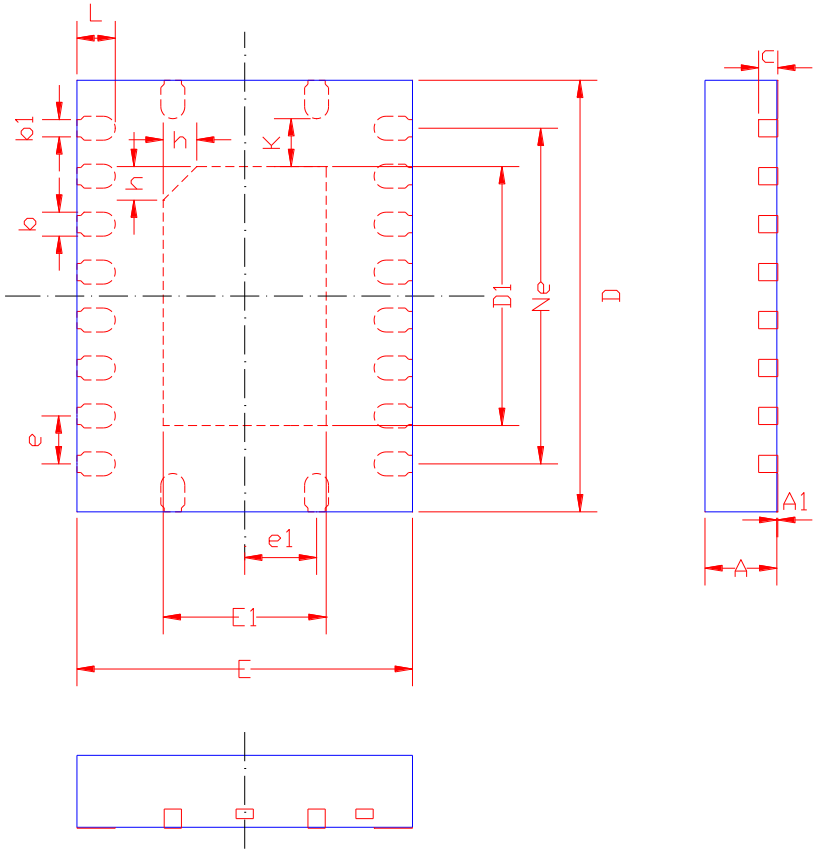


Figure37. package dimensions

SYMBOL	Dimensions(mm)		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	-	0.02	0.05
b	0.20	0.25	0.30
b1		0.18REF	
c		0.203REF	
D	4.40	4.50	4.60
D1	2.60	2.70	2.80
e		0.50BSC	
e1		0.75BSC	
Ne		3.50BSC	
E	3.40	3.50	3.60
E1	2.10	1.80	2.30
L	0.35	0.40	0.45
h	0.30	0.35	0.40
K		0.5REF	

NOTES:

3. This drawing is subject to change without notice
4. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

15.2 Recommended Land Pattern

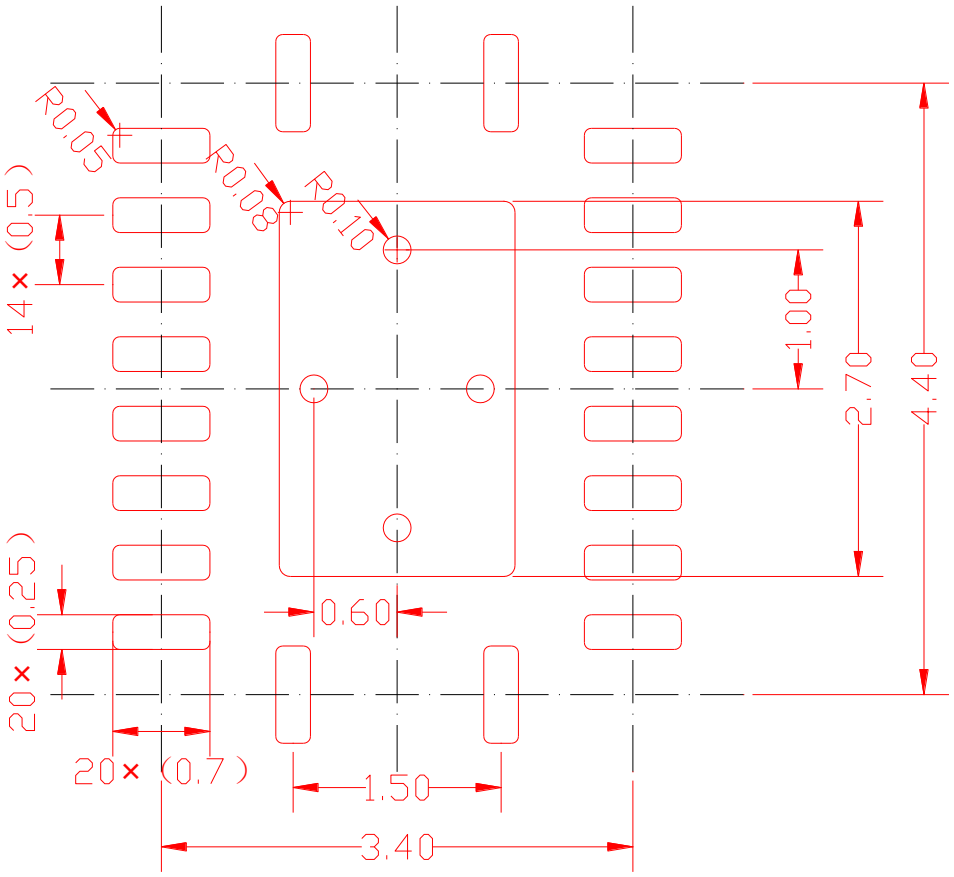


Figure38. Recommended Land Pattern

Notes:

1. All linear dimensions are in millimeters.
2. It is recommended that vias under paste be filled, plugged or tented.

15.3 Recommended Stencil Design

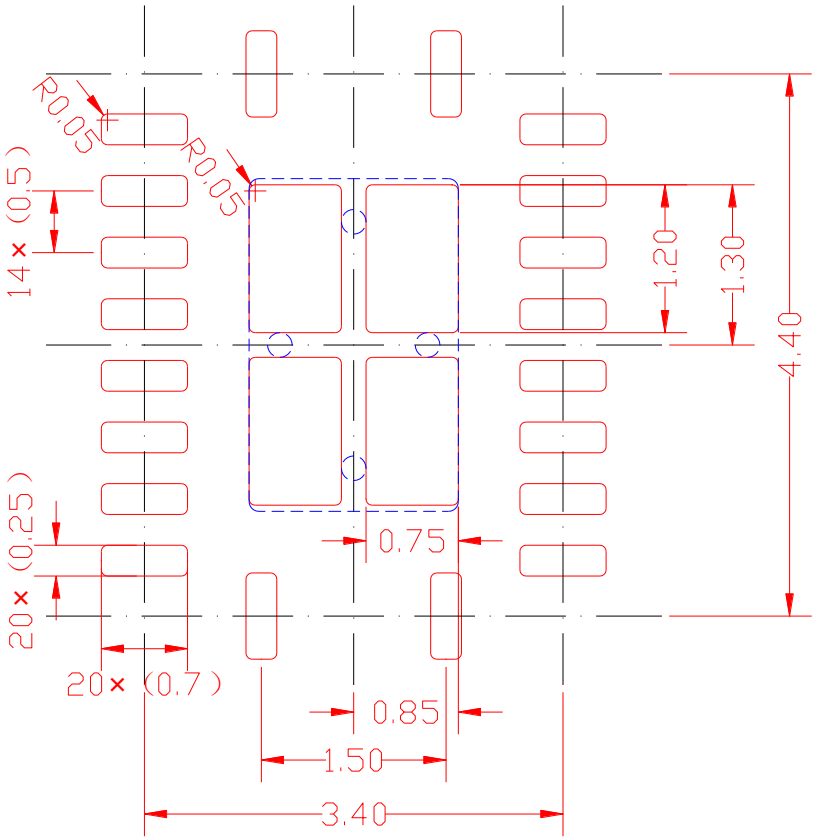


Figure39. Recommended Stencil Design

Notes:

1. All linear dimensions are in millimeters.

16 REEL AND TAPE INFORMATION

REEL DIMENSIONS

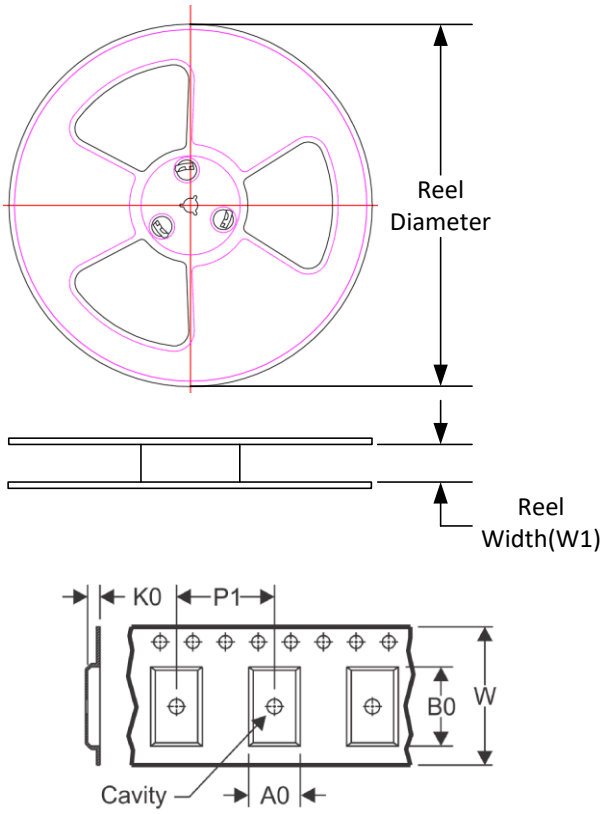


Figure40. Tape Dimensions

SYMBOL	Dimensions(mm)		
	MIN	NOM	MAX
W	11.70	12.00	12.30
W1	12.20	12.50	12.80
A0	3.70	3.80	3.90
B0	4.70	4.80	4.90
K0	1.08	1.18	1.28
P1	7.90	8.00	8.10

Device	Package Type	Pins	Quantities	Reel Diameter (mm)	Reel Width W1(mm)
MK9218	QFN20L	20	4000	332	12.5
A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	
3.8	4.8	1.18	8.0	12.0	

17 REEL BOX DIMENSIONS

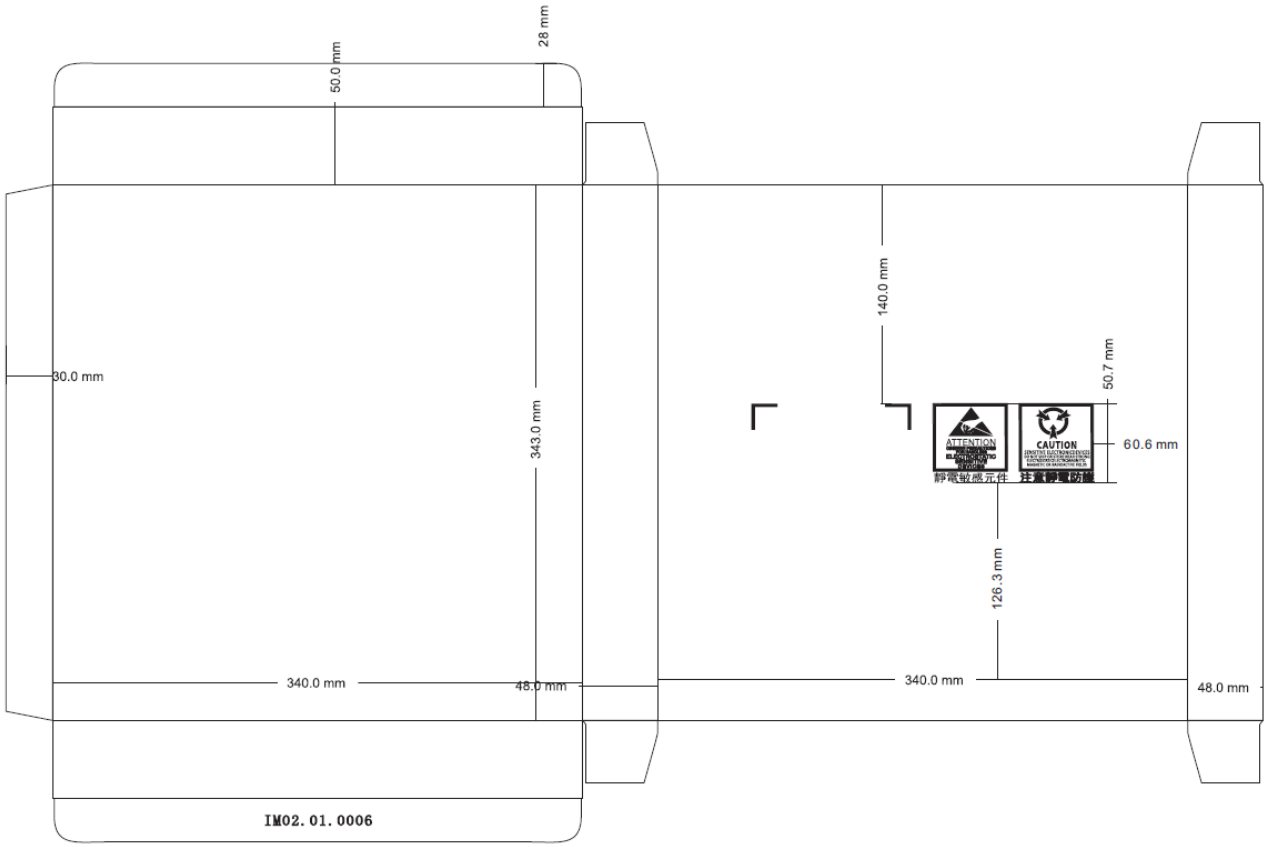


Figure41. Rell Box Dimensions