Embedded Storage

SM2259XT2

SATA Solid-State Drive Controller

Datasheet

Revision 0.1 **Apr 2021**

Revision History

Revision	Date	Description
0.1	Apr 14, 2021	Initial release

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1. Overview

1.1 Product Description

The SM2259XT2 is a high-performance SATA 6Gb/s SSD controller ideally suited for notebook, desktop personal computers, and a growing number of client SSD applications. The controller fully supports high-speed Toggle and ONFI NAND flash up to DDR800 800 MT/s, enabling the realization of fast, reliable, and feature-wise SSDs on the market.

Incorporated Silicon Motion's proprietary NANDXtend® error-correcting code (ECC) technology, the SM2259XT2 provides comprehensive data protection and enhances the endurance and retention of TLC and QLC NAND, achieving longer durability for SSD.

1.2 Key Features

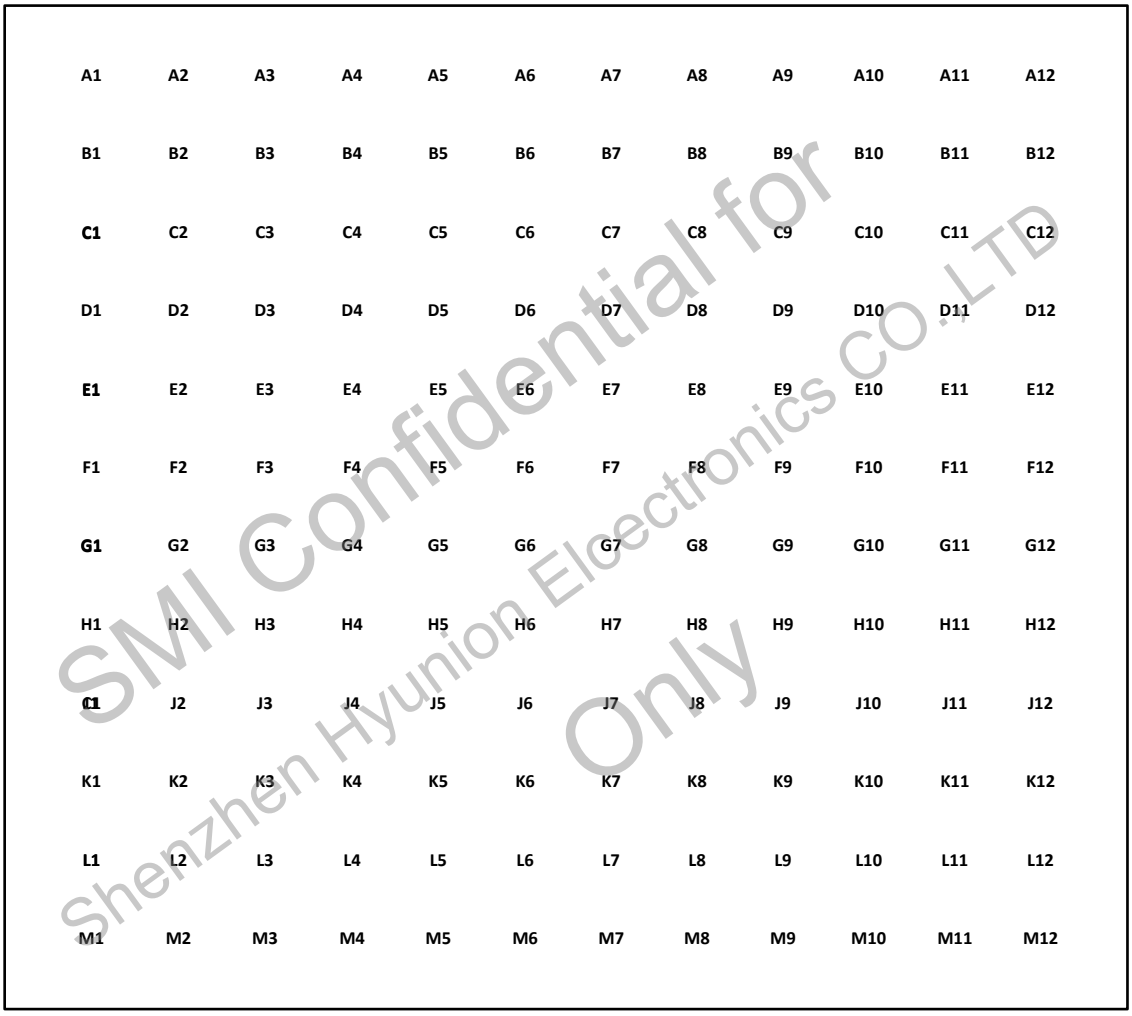
- Host Interface
  - Industrial Standard SATA Revision 3.1 compliant
  - Industrial Standard ATA/ATAPI-8 and ACS-3 command compliant
  - Supports SATA interface rate of 6Gb/s (backward compatible to 1.5Gb/s and 3Gb/s)
  - Native Command Queuing up to 32 commands
  - Supports SATA device sleep mode (DevSleep)
  - Data Set Management command (TRIM support)
  - Self-Monitoring, Analysis, and Reporting Technology (S.M.A.R.T.)
  - Supports 28-bit and 48-bit LBA (Logical Block Addressing) mode commands
- NAND Flash Support
  - Supports ONFI 4.0 and Toggle 2.0 interface
  - Supports SDR, NV-DDR2, NV-DDR3, and Toggle DDR/DDR2 NAND flash
  - 2-channel flash interface supports up to 16 NAND flash devices
  - Supports 1.2V/1.8V Flash I/O
  - Supports 8KB and 16KB page size
  - Supports 1-plane, 2-plane, 4-plane, and 8-plane operation
- Data Protection and Reliability
  - End-to-End Protection
  - Supports ATA8 security feature set
  - Hardware LDPC ECC engine with hard-decision and soft-decision decoding
  - RAID engine offers additional level of data protection
  - Internal data shaping technique increases data endurance
  - StaticDataRefresh technology ensures data integrity
  - Early weak block retirement option
  - Global wear leveling algorithm evens program/erase count and extends SSD lifespan

- Architecture
  - 32-bit RISC CPU
  - High-efficiency 64-bit system bus
  - Automatic sleep and wake-up mechanism to save power
  - Built-in voltage detectors for power failure protection
  - Built-in power-on reset and voltage regulators
  - Built-in temperature sensor for SSD temperature detection
  - Supports JTAG interface and UART (RS-232) interface
- Enhanced Security
  - Real time full drive encryption with Advanced Encryption Standard (AES)
  - Trusted Computing Group (TCG) Opal protocol
  - Hardware SHA 256 and True Random Number Generator (TRNG)
  - eFuse Memory (OTP)
- Package
  - 144-ball TFBGA
  - Lead-free and RoHS compliant

2. Signal Descriptions

2.1 Ball Assignments

Figure 1: 144-Ball TFBGA Assignments (Top View)



2.2 Signal Descriptions

Table 1: SATA Interface Signals

Signal	Ball NO.	Type	Description
RX0_P	A11	CMOS input	SATA Rx Differential Pair
RX0_M	A10	CMOS input	
TX0_P	A8	CMOS output	SATA Tx Differential Pair
TX0_M	A7	CMOS output	
RESREF	B6	Input	External reference for output drive calibration. Attach a 200Ω (±1%) precision resistor-to-ground on the board.

Table 2: Flash Interface Signals

Signal	Ball NO.	Type	Description
P_FSH0_DAT[0]	M3	CMOS I/O	Flash data bus – channel 0
P_FSH0_DAT[1]	K4	CMOS I/O	
P_FSH0_DAT[2]	L4	CMOS I/O	
P_FSH0_DAT[3]	K5	CMOS I/O	
P_FSH0_DAT[4]	L5	CMOS I/O	
P_FSH0_DAT[5]	L6	CMOS I/O	
P_FSH0_DAT[6]	M6	CMOS I/O	
P_FSH0_DAT[7]	L7	CMOS I/O	
P_FSH1_DAT[0]	L8	CMOS I/O	Flash data bus – channel 1
P_FSH1_DAT[1]	K8	CMOS I/O	
P_FSH1_DAT[2]	M9	CMOS I/O	
P_FSH1_DAT[3]	L9	CMOS I/O	
P_FSH1_DAT[4]	K9	CMOS I/O	
P_FSH1_DAT[5]	L10	CMOS I/O	
P_FSH1_DAT[6]	K10	CMOS I/O	
P_FSH1_DAT[7]	L11	CMOS I/O	
P_FSH0_ALE	K6	CMOS output	Flash address latch enable – channel 0
P_FSH1_ALE	J8	CMOS output	Flash address latch enable – channel 1
P_FSH0_CLE	K7	CMOS output	Flash command latch enable – channel 0
P_FSH1_CLE	J9	CMOS output	Flash command latch enable – channel 1

Table 2: Flash Interface Signals (continued)

Signal	Ball NO.	Type	Description
P_FSH0_CEN[0]	K2	CMOS output	Flash chip enable – channel 0
P_FSH0_CEN[1]	L2	CMOS output	
P_FSH0_CEN[2]	K3	CMOS output	
P_FSH0_CEN[3]	J5	CMOS output	
P_FSH0_CEN[4]	L1	CMOS output	
P_FSH0_CEN[5]	L3	CMOS output	
P_FSH0_CEN[6]	M1	CMOS output	
P_FSH0_CEN[7]	M2	CMOS output	
P_FSH1_CEN[0]	L12	CMOS output	Flash chip enable – channel 1
P_FSH1_CEN[1]	G10	CMOS output	
P_FSH1_CEN[2]	K11	CMOS output	
P_FSH1_CEN[3]	J10	CMOS output	
P_FSH1_CEN[4]	G12	CMOS output	
P_FSH1_CEN[5]	J11	CMOS output	
P_FSH1_CEN[6]	H12	CMOS output	
P_FSH1_CEN[7]	H11	CMOS output	
P_FSH0_DQS_P	M4	CMOS I/O	P_FSHx_DQS_P/P_FSHx_DQS_N: Flash data strobe/Flash data strobe complement. • For SDR access mode, these signals are not used (no connect). • For NV-DDR2/NV-DDR3 and Toggle DDR 2.0 access modes, P_FSHx_DQS_P indicates the data valid window. P_FSHx_DQS_P is paired with differential signal P_FSHx_DQS_N to provide differential pair signaling to the system during reads and writes.
P_FSH0_DQS_N	M5	CMOS I/O	
P_FSH1_DQS_P	M11	CMOS I/O	
P_FSH1_DQS_N	M10	CMOS I/O	
P_FSH0_RE_P	M7	CMOS output	P_FSHx_RE_P/P_FSHx_RE_N: Flash read enable/read enable complement • For SDR access mode, the P_FSHx_RE_P enables serial data output. • For NV-DDR2/NV-DDR3 and Toggle DDR 2.0 access mode, the P_FSHx_RE_P signal is the serial data-out control, and when active, drives the data onto the DQ buses. Data is valid after tDQSRE of rising edge and falling edge of P_FSHx_RE_P, which also increments the internal column address counter by each one. Read enable P_FSHx_RE_N is paired with differential signal P_FSHx_RE_P (only in NV-DDR2 and Toggle DDR 2.0 modes) to provide differential pair signaling to the system during reads.
P_FSH0_RE_N	M8	CMOS output	
P_FSH1_RE_P	J12	CMOS output	
P_FSH1_RE_N	K12	CMOS output	

Table 2: Flash Interface Signals (continued)

Signal	Ball NO.	Type	Description
P_FSH_WP	J6	CMOS output	Flash write protect signal directly connected to the flash memory write protect signal.
P_GPIO_FRB	J7	CMOS input	Flash ready/busy signals indicating the state, ready or busy of flash memory.
P_FSH0_WE_N	H9	CMOS output	Flash write enable • For SDR access mode, the write enable signal controls the latching of output data. Data, commands, and addresses are latched on the rising edge of P_FSHx_WE_N. • For NV-DDR2/NV-DDR3 and Toggle DDR 1.0/2.0 access modes, this signal controls writes to the DQ bus. Commands and addresses are latched on the rising edge of the WE pulse.
P_FSH1_WE_N	H10	CMOS output	
P_FSH_ZQCL	G11	CMOS I/O	Reference pin for Flash output drive calibration. Attach a 24Ω precision resistor (with 1% tolerance) on board to calibrate Flash ODT and driving strength.
FSH_VDTF	E10	Analog input	Voltage detection for NAND core power supply
VREFIO_FSH	M12	CMOS I/O	External Flash I/O reference voltage (0.5 x VCCFQ)

Table 3: Power Signals

Signal	Ball NO.	Type	Description
VDD	D7, E6, F6, G6, H6	Power input	Core power supply 0.9V
VCCGQ	A5	Power input	Power supply for general I/O 1.8V/3.3V
VCCFQ	G8, G9, H7, H8	Power input	Power supply for Flash I/O 1.2V/1.8V
VPTX0	D8	SATA power	Power supply 0.9V for SATA PHY
VPH	C9	SATA power	Power supply 1.8V/3.3V for SATA PHY
VCCAH	C10	Analog power input	Power supply 1.8V/3.3V for SATA PHY and Analog IP (AIP)
V09A_PAD	D9	Analog power input	Power supply 0.9V for SATA PHY core and AIP
VBG_PAD	E11	Analog input	Bandgap buffer output voltage 1.2V
VCCGQ_33C	D1	Output	This pin is used to connect 1uF capacitor on board to stabilize output voltage of internal LDO.
VQPS	C6	Input	High voltage for fuse programming (CP stage 64-bit)
VDTFIO_VIN	F12	Analog input	Flash I/O power detection
VDT5V_0D4VIN	E12	Analog input	Voltage detection for VBUS 5V power. This signal shall connect to a resistor divider to keep the maximum input voltage under 1V.
VSS	A6, A9, A12, B7-B11, C7, C8, C11, D12	Ground	Core ground and crystal pad connection
VSS33	D10, D11, E7-E9, F3, F7-F11, G7	Ground	GPIO and Flash I/O ground connection

Table 4: Miscellaneous Signals

Signal	Ball NO.	Type	Description
P_EXRSTN	C5	CMOS input	Chip Global Reset
P_EXCLK	C3	CMOS input	Chip External Clock
P_EX_PWD_N	D6	CMOS output	External Power Control Signal
P_DEVSLP	B3	CMOS input	Enter/Exit device sleep
XOUT	B12	CMOS output	Crystal Out
XIN	C12	CMOS input	Crystal In
P_JTAG_TRST_N	H4	CMOS input	JTAG signal
P_JTAG_TMS	J4	CMOS input	JTAG signal
P_JTAG_TDI	K1	CMOS input	JTAG signal
P_JTAG_TDO	J3	CMOS output	JTAG signal
P_JTAG_TCK	J2	CMOS input	JTAG signal
P_TEST0	A2	CMOS input	Test signal. Tie to ground for normal operation.
P_TEST1	B4	CMOS input	Test signal. Tie to ground for normal operation.
P_TEST2	A3	CMOS input	Test signal. Tie to ground for normal operation.
P_SPI_HOLDN	G2	CMOS output	SPI signal
P_SPI_CSN	G1	CMOS output	SPI signal
P_SPI_CLK	G4	CMOS output	SPI signal
P_SPI_MOSI	H1	CMOS output	SPI signal
P_SPI_MISO	H2	CMOS input	SPI signal
P_I2C_SCL	J1	CMOS I/O	I^2C signal
P_I2C_SDA	H3	CMOS I/O	I^2C signal
P_P0[0]	F2	CMOS I/O	General Purpose I/O
P_P0[1]	F1	CMOS I/O	General Purpose I/O
P_P0[2]	E5	CMOS I/O	General Purpose I/O
P_P0[3]	F4	CMOS I/O	General Purpose I/O
P_P0[4]	F5	CMOS I/O	General Purpose I/O
P_P0[5]	G5	CMOS I/O	General Purpose I/O
P_P0[6]	H5	CMOS I/O	General Purpose I/O
P_P0[7]	G3	CMOS I/O	General Purpose I/O
P_P1[0]	D4	CMOS I/O	General Purpose I/O
P_P1[1]	C1	CMOS I/O	General Purpose I/O
P_P1[2]	E3	CMOS I/O	General Purpose I/O
P_P1[3]	D3	CMOS I/O	General Purpose I/O

Table 4: Miscellaneous Signals (continued)

Signal	Ball NO.	Type	Description
P_P1[4]	E4	CMOS I/O	General Purpose I/O
P_P1[5]	D2	CMOS I/O	General Purpose I/O
P_P1[6]	E2	CMOS I/O	General Purpose I/O
P_P1[7]	E1	CMOS I/O	General Purpose I/O
P_P2[0]	C2	CMOS I/O	General Purpose I/O
P_P2[1]	D5	CMOS I/O	General Purpose I/O
P_P2[2]	B5	CMOS I/O	General Purpose I/O
P_P2[3]	B2	CMOS I/O	General Purpose I/O
P_P2[4]	A1	CMOS I/O	General Purpose I/O
P_P2[5]	A4	CMOS I/O	General Purpose I/O
P_P2[6]	C4	CMOS I/O	General Purpose I/O
P_P2[7]	B1	CMOS I/O	General Purpose I/O

Note: For more information on GPIO, please contact project manager or local support personnel.

3. Electrical Specifications

3.1 Recommended Operating Conditions

Table 5: Recommended/Typical Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Core Power Supply	VDD	0.837	0.9	0.99	V
I/O Pad Power Supply	VCCGQ	1.7	1.8	1.95	V
		2.7	3.3	3.6	
Flash I/O Power Supply	VCCFQ	1.14	1.2	1.26	V
		1.7	1.8	1.95	V
Flash I/O Reference Voltage	VREFIO_FSH	0.49 x VCCFQ	0.5 x VCCFQ	0.51 x VCCFQ	V
Analog Power Supply	V09A_PAD	0.81	0.9	0.99	V
	VCCAH	1.62	1.8	1.98	V
SATA PHY Power Supply	VPTX0	0.837	0.9	0.99	V
	VP	0.837	0.9	0.99	V
	VPH	3.069	3.3	3.63	V
eFuse Power Voltage	VQPS	1.8	1.8	1.98	V

3.2 DC Electrical Characteristics

Table 6: Digital DC Electrical Characteristics (VCCGQ of 3.3V)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (V_{IO})	VCCGQ	2.7	3.3	3.47	V
High Level Output Voltage	V_{OH}	0.75 * V_{IO}			V
Low Level Output Voltage	V_{OL}			0.125 * V_{IO}	V
High Level Input Voltage	V_{IH}	1.62		V_{IO} + 0.3	V
Low Level Input Voltage	V_{IL}	V_{SS33} - 0.3		0.25 * V_{IO}	V
Pull-up Resistance	R_{PU}	30	58	95	kΩ
Pull-down Resistance	R_{PD}	31	60	100	kΩ

Table 7: Digital DC Electrical Characteristics (VCCGQ of 1.8V)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (V_{IO})	VCCGQ	1.7	1.8	1.95	V
High Level Output Voltage	V_{OH}	VCCGQ - 0.1			V
Low Level Output Voltage	V_{OL}			0.1	V
High Level Input Voltage	V_{IH}	0.8 * V_{IO}		V_{IO} + 0.3	V
Low Level Input Voltage	V_{IL}	V_{SS33} - 0.3		0.2 * V_{IO}	V
Pull-up Resistance	R_{PU}	30	58	95	kΩ
Pull-down Resistance	R_{PD}	31	59	100	kΩ

Table 8: Digital DC Electrical Characteristics (VCCFQ of 1.8V)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (V_{IO})	VCCFQ	1.7	1.8	1.95	V
High Level Output Voltage	V_{OH}	VCCFQ - 0.1			V
Low Level Output Voltage	V_{OL}			0.1	V
High Level Input Voltage	V_{IH}	0.8 * V_{IO}		V_{IO} + 0.3	V
Low Level Input Voltage	V_{IL}	V_{SS33} - 0.3		0.2 * V_{IO}	V
Pull-up Resistance	R_{PU}	34	49.7	72	kΩ
Pull-down Resistance	R_{PD}	23	50	86	kΩ

Table 9: Digital DC Electrical Characteristics (VCCFQ of 1.2V)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (V_{IO})	VCCFQ	1.14	1.2	1.26	V
High Level Output Voltage	V_{OH}	VCCFQ - 0.1			V
Low Level Output Voltage	V_{OL}			0.1	V
High Level Input Voltage	V_{IH}	0.8 * V_{IO}		V_{IO} + 0.3	V
Low Level Input Voltage	V_{IL}	V_{SS33} - 0.3		0.2 * V_{IO}	V
Pull-up Resistance	R_{PU}	59	90.3	133	kΩ
Pull-down Resistance	R_{PD}	28	89.4	161	kΩ

3.3 Flash Interface Timing Characteristics

3.3.1 SDR (Legacy NAND) Interface

Table 10: AC Timing Characteristics of SDR Mode

Parameter	Symbol	Min	Max	Unit
CE# Setup Time	tCS	15.0		ns
CE# Hold Time	tCH	5.0		ns
CLE Setup Time	tCLS	10.0		ns
CLE Hold Time	tCLH	5.0		ns
ALE Setup Time	tALS	10.0		ns
ALE Hold Time	tALH	5.0		ns
Write Cycle Time	tWC	20.0		ns
WE# Pulse Width	tWP	10.0		ns
WE# High Hold Time	tWH	7.0		ns
Write Data Setup Time	tDS	7.0		ns
Write Data Hold Time	tDH	5.0		ns
Read Cycle Time	tRC	20.0		ns
Ready to RE# Low	tRR	20.0		ns
RE# Pulse Width	tRP	10.0		ns
RE# High Hold Time	tREH	7.0		ns

Figure 2: Command Latch Timing

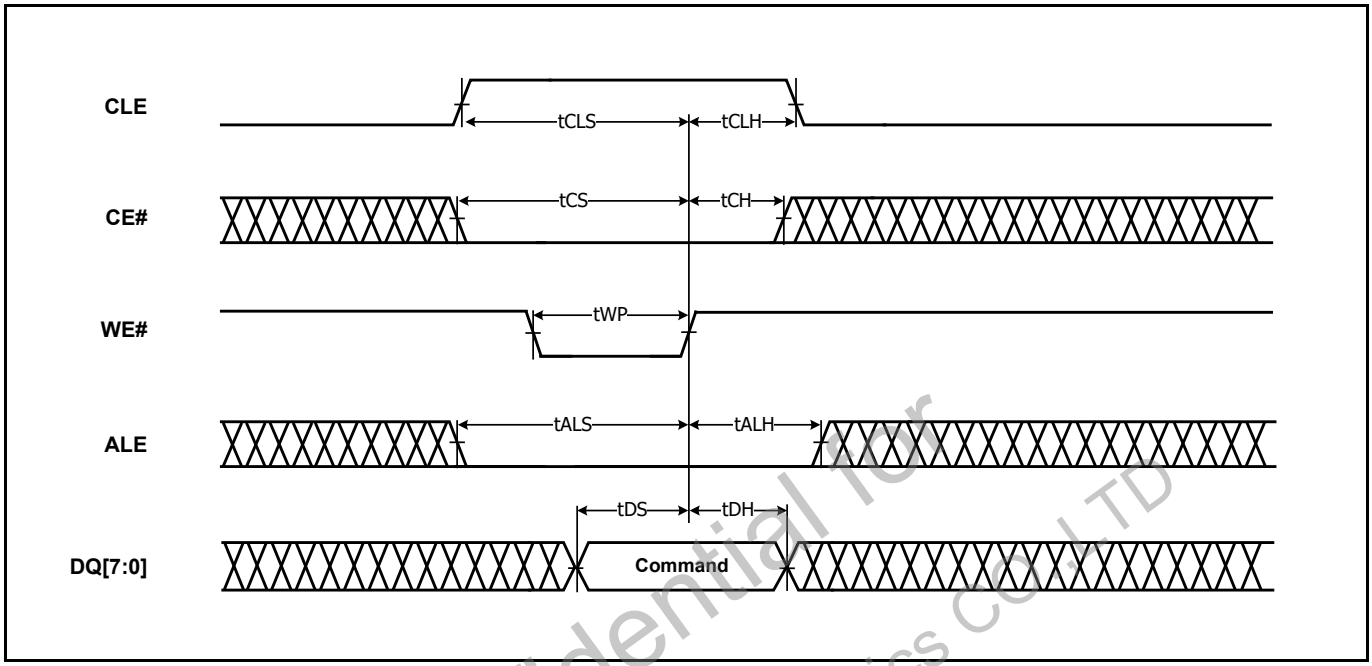


Figure 3: Address Latch Timing

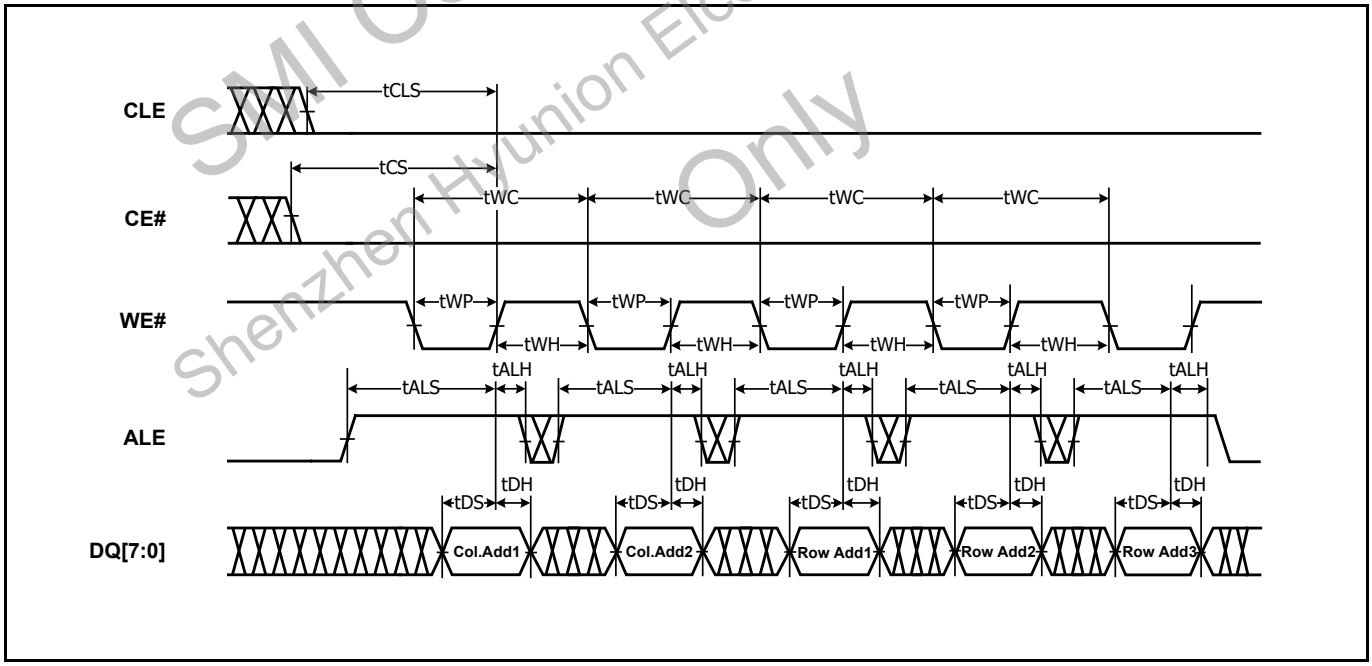


Figure 4: Data Output (Write) Cycle Timing

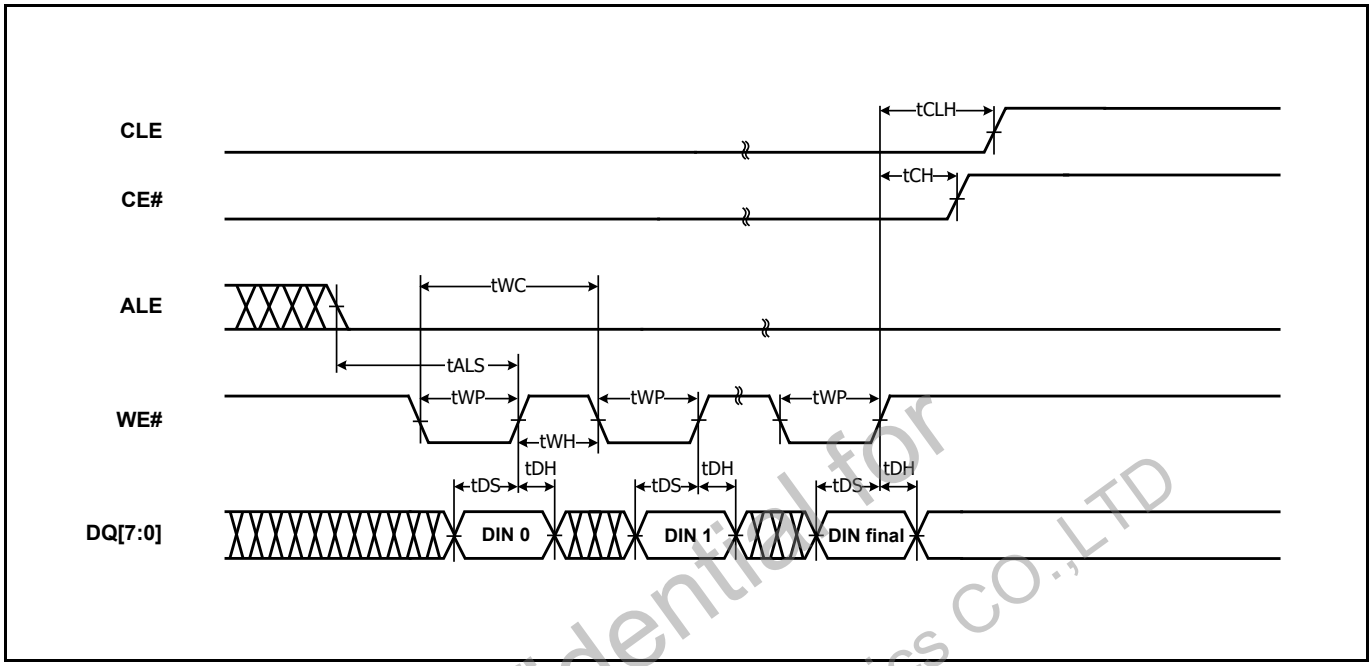
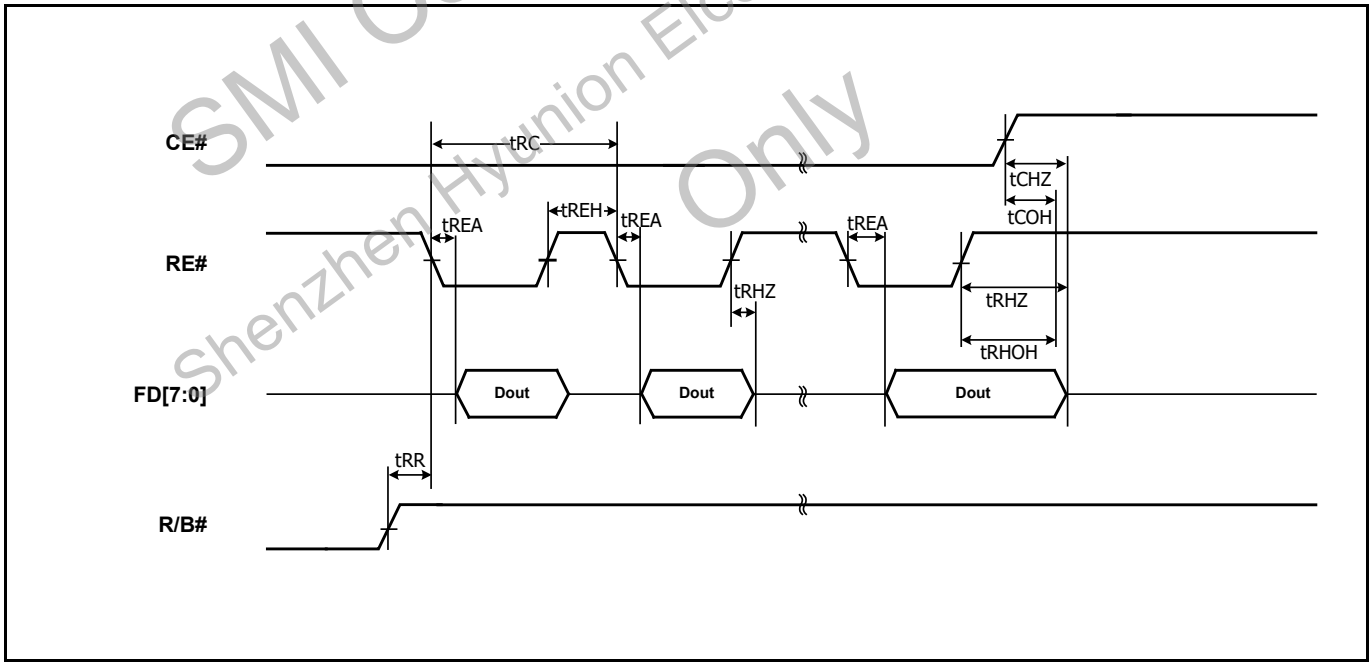


Figure 5: Data Input (Read) Cycle Timing



3.3.2 NV-DDR2/NV-DDR3 Interface

Table 11: AC Timing Characteristics of NV-DDR2/NVDDR3 Mode

Parameter	Symbol	Min	Max	Unit
Address to Data Loading Time	tADL	400		ns
Command/Address Hold Time	tCAH	5		ns
Command/Address Setup Time	tCAS	5		ns
CLE/ALE Hold Time	tCALH	5		ns
CLE/ALE Setup Time	tCALS	15		ns
CLE/ALE Setup Time when ODT is enabled	tCALS2	25		ns
CE# Hold Time	tCH	5		ns
CE# Setup Time	tCS	40		ns
Write Cycle Time	tWC	25		ns
WE# High Pulse Width	tWH	11		ns
WE# Low Pulse Width	tWP	11		ns
WE# High to RE# Low	tWHR	120		ns
WE# High to RE# Low for Random Data out	tWHR2	300		ns
Data Strobe Cycle Time	tDSC	5		ns
Data Setup Time	tDS	0.2		ns
Data Hold Time	tDH	0.2		ns
DQS Output High Pulse Width	tDQSH	0.45 * tRC	0.55 * tRC	ns
DQS Output Low Pulse Width	tDQSL	0.45 * tRC	0.55 * tRC	ns
Read Cycle Time	tRC	2.5		ns
RE# High Pulse Width	tREH	0.45 * tRC	0.55 * tRC	ns
RE# Low Pulse Width	tRP	0.45 * tRC	0.55 * tRC	ns
Read Preamble	tRPRE	15		ns
Read Preamble when ODT is enabled	tRPRE2	25		ns
Read Postamble	tRPST	tDQSRE + 6 * tRC		ns
Read Postamble Hold Time	tRPSTH	5		ns
Write Preamble	tWPRE	15		ns
Write Preamble when ODT is enabled	tWPRE2	25		ns
Write Postamble	tWPST	6.5		ns
Write Postamble Hold Time	tWPSTH	5		ns

Note: Table 12 provides the parameters of NV-DDR2 and NV-DDR3 data interface mode 10. Refer to ONFI specification for more details.

Figure 6: NV-DDR2/NVDDR3 Command Cycle Timing

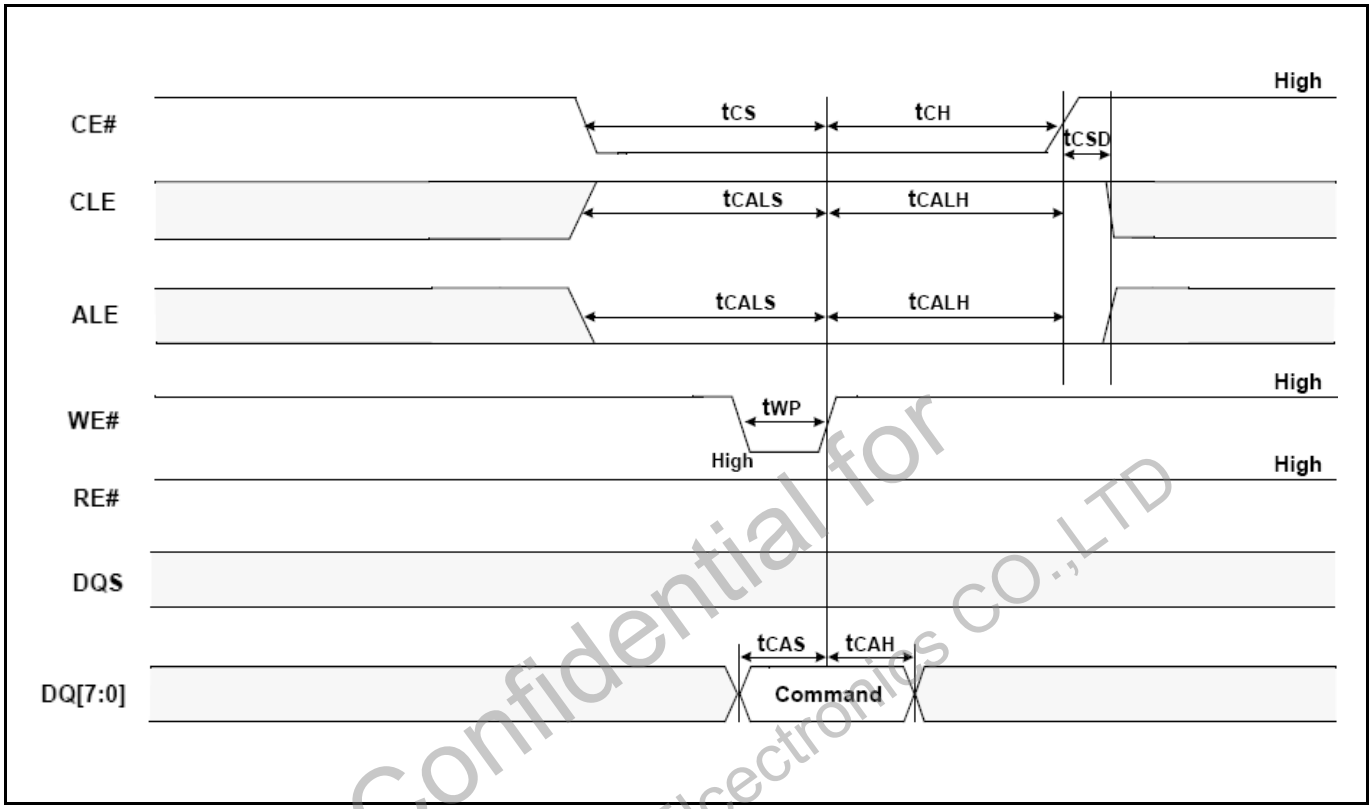


Figure 7: NV-DDR2/NVDDR3 Address Cycle Timing

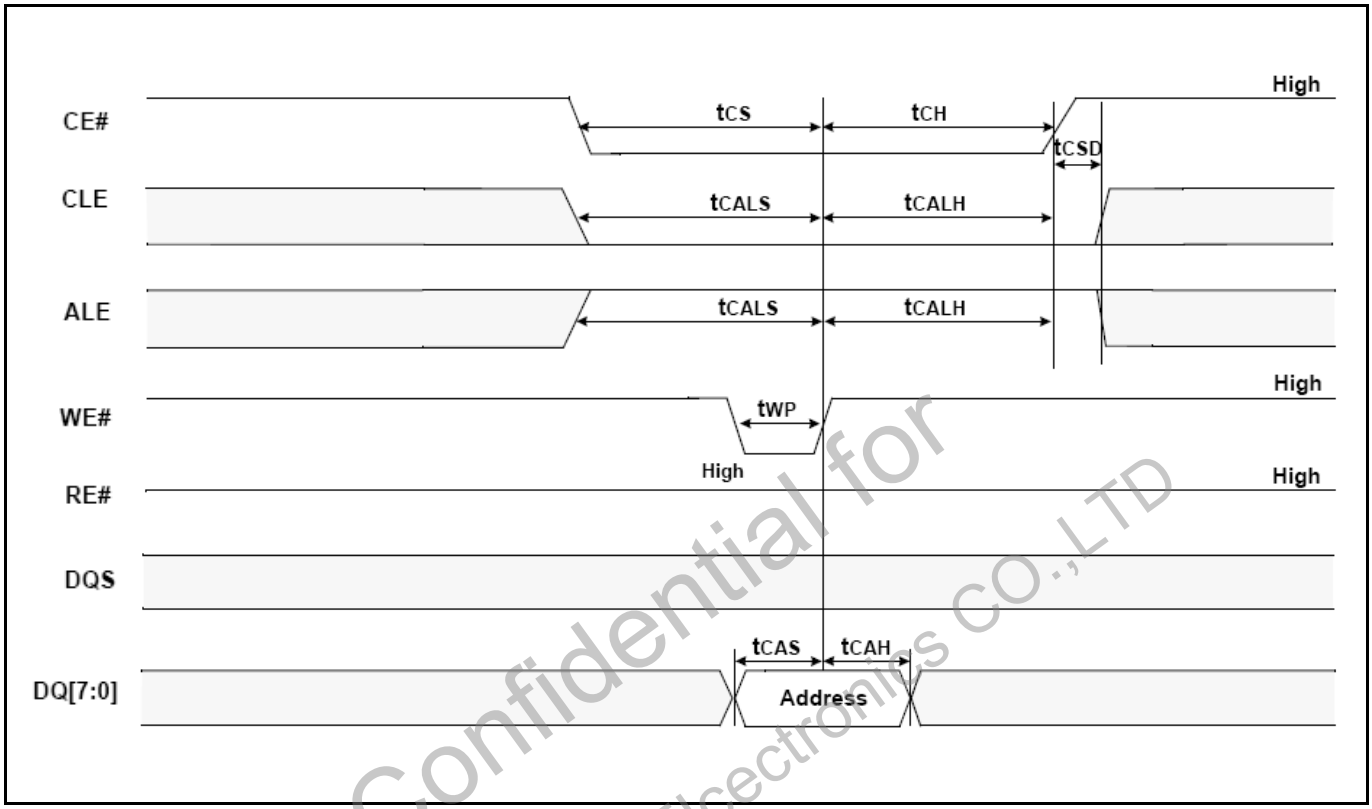


Figure 8: NV-DDR2/NVDDR3 Data Output (Write) Cycle Timing

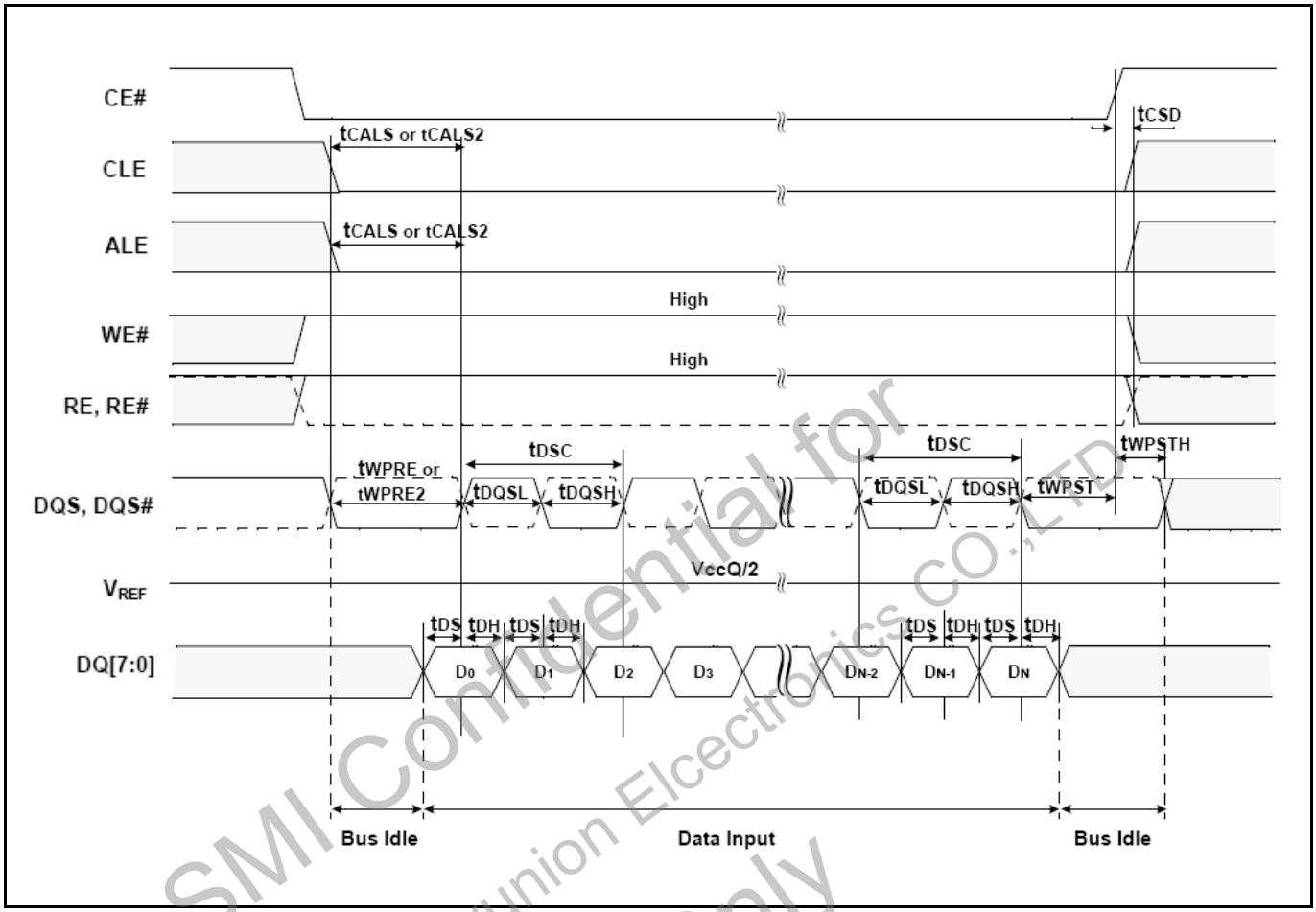
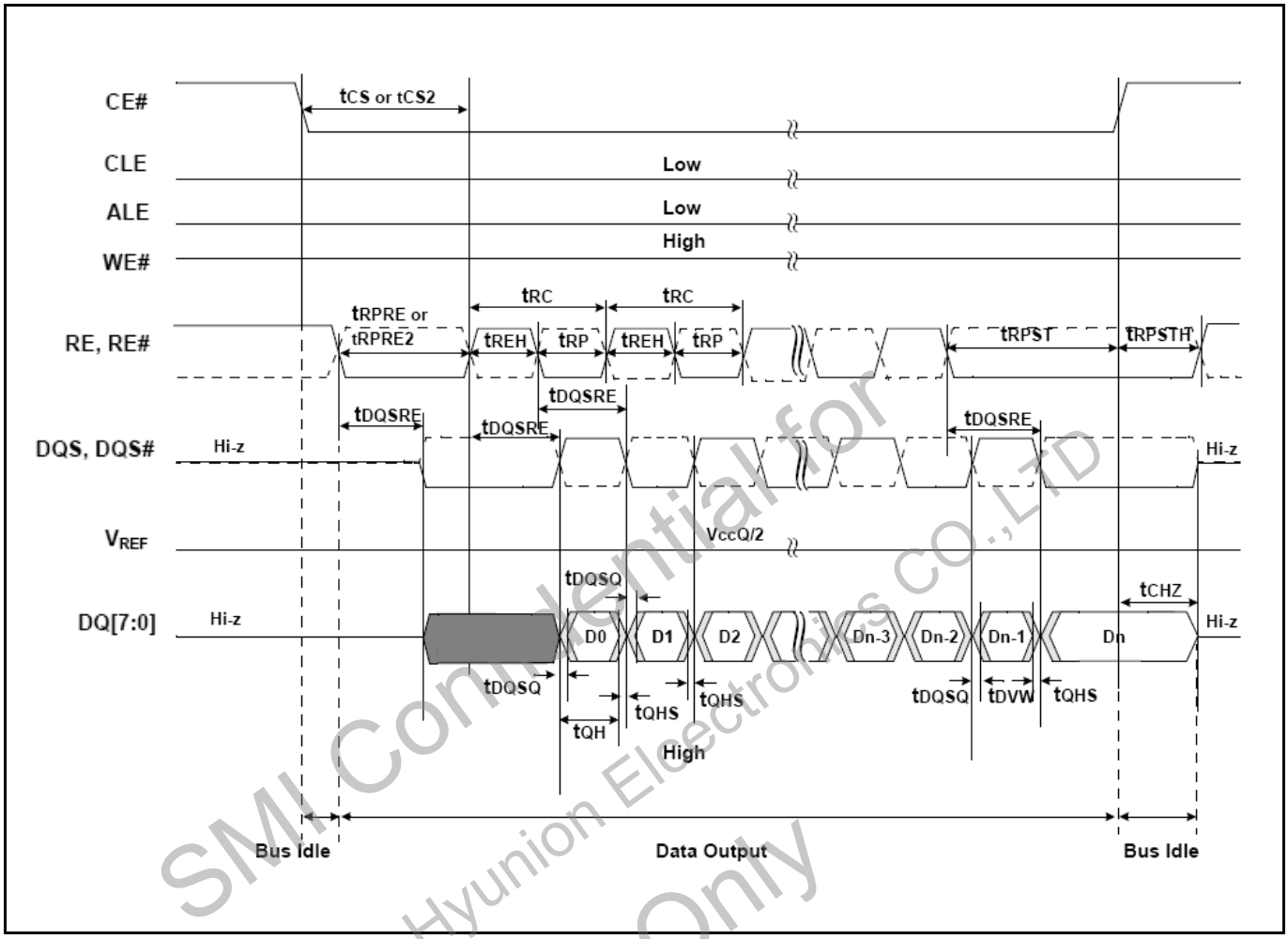
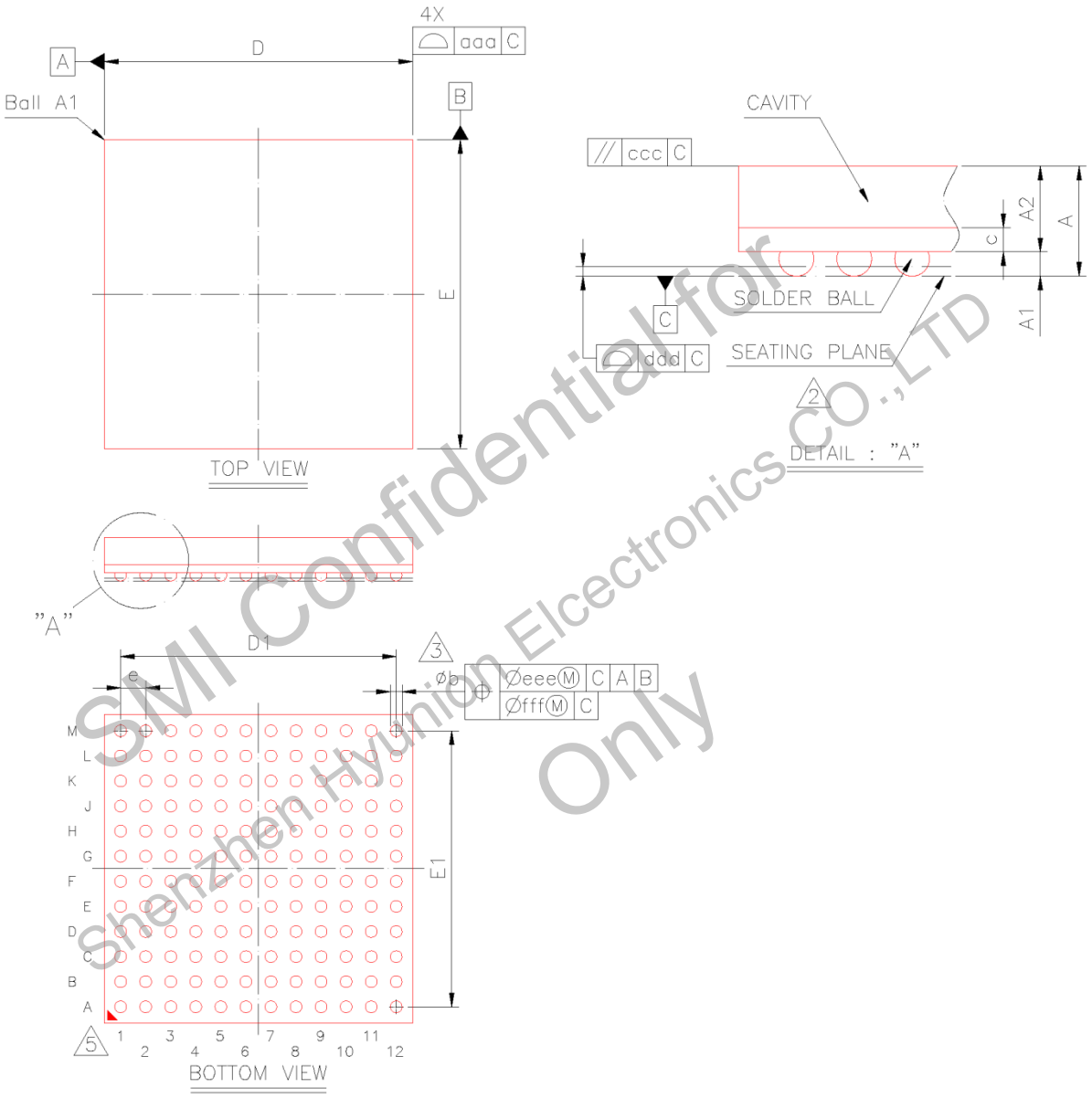


Figure 9: NV-DDR2/NVDDR3 Data Input (Read) Cycle Timing



4. Package Information

Figure 10: 144-Ball TFBGA Package (8x8mm)



Symbol	MIN	NOM	MAX	Symbol	MIN	NOM	MAX
A	1.05	1.12	1.19	e	---	0.65	---
A1	0.16	0.21	0.26	b	0.25	0.30	0.35
A2	0.86	0.91	0.96	aaa	0.15		
c	0.17	0.21	0.25	ccc	0.10		
D	7.90	8.00	8.10	ddd	0.08		
E	7.90	8.00	8.10	eee	0.15		
D1	---	7.15	---	fff	0.08		
E1	---	7.15	---	MD/ME	12/12		

Notes:
1. Controlling Dimension: Millimeter.
2. Primary datum C and seating plane are defined by the spherical crowns of the solder balls.
3. Dimension b is measured at the maximum solder ball diameter, parallel to primary datum C.
4. Special characteristics C class: ccc, ddd.
5. The pattern of Pin 1 fiducial is for reference only.

5. Product Ordering Information

5.1 Ordering Information

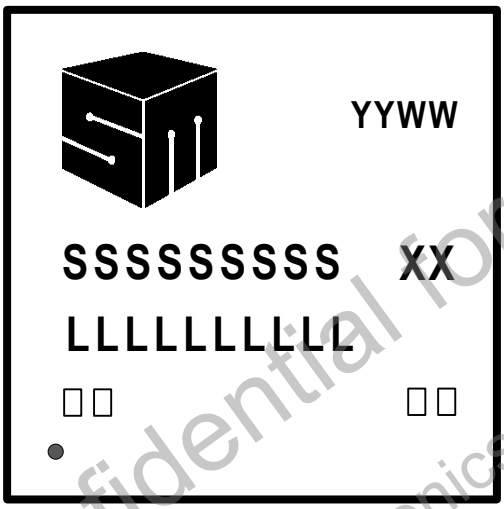
Table 12: Ordering Information

Ordering Number	Operating Temperature	Package Description
SM225GX0900X2-AA	0°C ~ 70°C	144-ball BGA, 8x8x1.19 (mm)

Note: The suffix “XX” denotes the IC revision.

5.2 Top Marking

Figure 11: Top Marking



Top Marking Guidelines:

Line 1: **Date Code**
YY: Last two digits of current year
WW: Assembly work week

Line 2: **Product Type + Space + Product Revision**
Product Type "SSSSSSSSS": SM2259XT2G
Product Revision "XX" (AA for example)

Line 3: **ASIC Lot Number**
LLLLLLLLLL: 10 characters at maximum

Line 4A: **Assembly Location**
□□ (Left; TW for example)

Line 4B: **Process Technology + Assembly Supplier**
□□ (Right;1D for example)
Note that the code may vary due to different suppliers.