Synchronous, Bi-directional Buck-Boost Charger Controller with NVDC PowerPath management and I2C interface

1 Descriptions

SC8886S is a synchronous buck-boost charger, which supports buck mode, boost mode and buck-boost mode during forward charging or reverse discharging operation. SC8886S manages 1 to 4 cells battery charging from wide input range from 3.5V to 24V, supporting pre-charge, constant current charge, constant voltage charge. The battery discharging mode supports wide output range from 3V to 24V with 8mV resolution. SC8886S is compliant with Intel IMVP8/IMVP9 specification including system power, input current, charging or discharging current monitoring and processor hot indication. SC8886S adopts Narrow-VDC power path management, which automatically regulates the current and voltage and controls the flow of power.

Through I2C interface, user can set the charging/discharging mode easily, and program the charging current, charging voltage, VINREG voltage, input current limit, reverse output voltage adjustment, current limits, switching frequency and other parameters flexibly. Besides, input current limit, charge voltage could be set by external resistors.

SC8886S supports pass through mode to reduce switching losses during forward charging. The device also supports Vmin active mode to absorb system peak power when only battery powers the system. 10-bit ADC is integrated to monitor voltage, current and power. SC8886S can operate in learn mode and ship mode to meet the user's demands. Full protection is supported including input over voltage protection/undervoltage, system and battery over-voltage protection, MOSFETs over-current protection. over-temperature protection.

SC8886S is available in a 4mm x 4mm QFN-32 Package.

2 Features

- Wide input range: 3.5V to 24V, 29V sustainable
- High efficiency Buck-Boost conversion
- Buck-Boost battery charger for 1 to 4 cell batteries
- Charging management including precharge, fast charge, constant voltage charge, auto-wake up
- Reverse discharging mode, output voltage range: 3V to 24V with 8 mV resolution, comply with USB PD 3.0 standards
- NVDC PowerPath management and dynamic power management
- I2C interface
- Input current limit set by external resistor and internal register
- Switching frequency: 800kHz /1.2MHz
- Integrated PSYS/IADPT/IBAT pin for power and current monitor, compliant with Intel IMVP8/9 standard
- Integrated processor hot indication(/PROCHOT) pin
- Pass through mode (PTM)
- Integrated VMIN active protection (VAP) to supplement system peak power when only battery exists
- 2-Level input current limit for CPU peak power
- Input current optimizer (ICO) algorithm for maximum adapter power capacity
- Learn mode and ship mode for system application
- Integrated high accuracy ADC
- Integrated independent comparator for system voltage monitoring
- Protection including UVP, OVP, OCP, SCP, OTP
- QFN-32 Package

3 Applications

- Ultra-Books, Notebooks, Tablet PCs
- Power Banks
- Industrial Equipment
- Equipment with Rechargeable Batteries

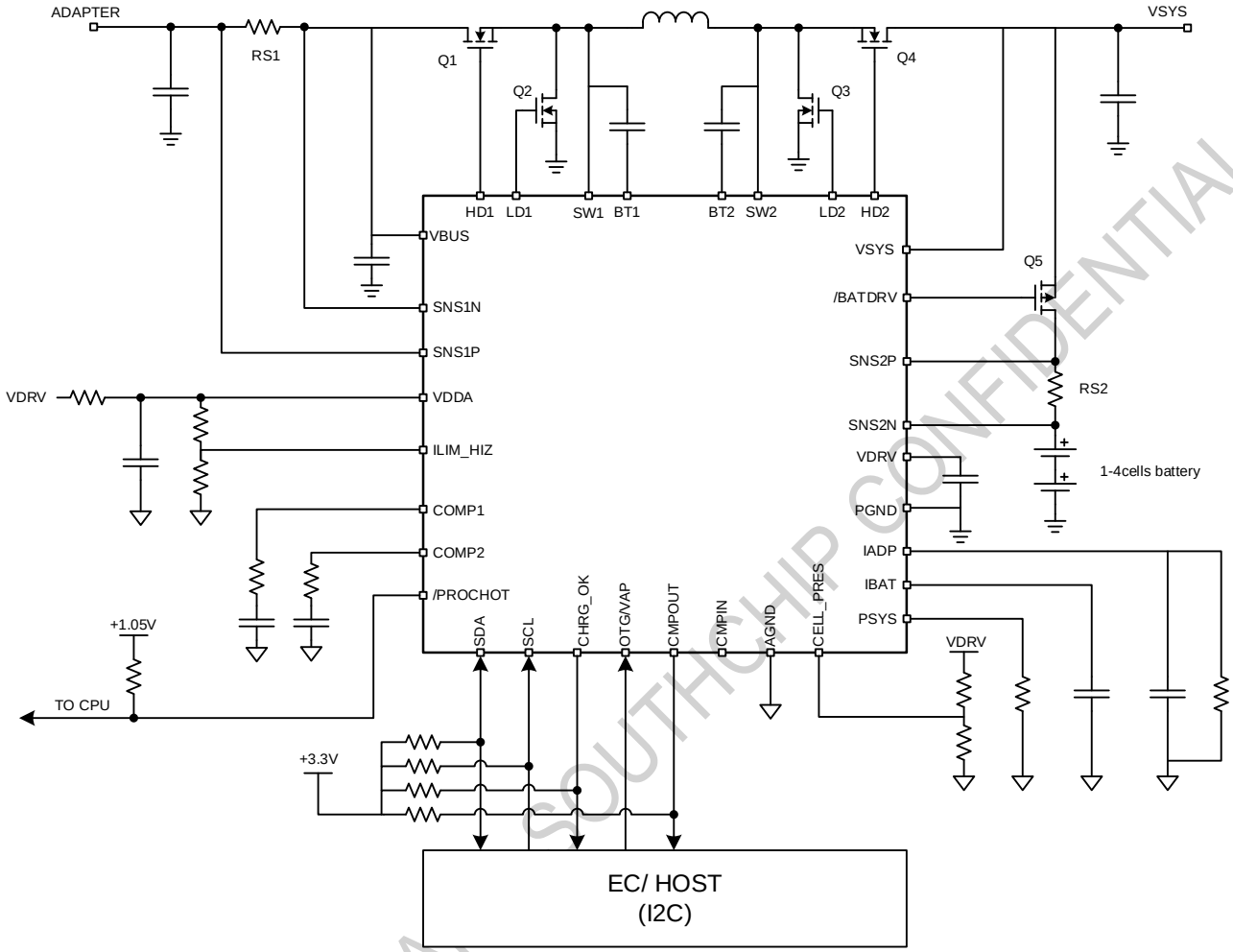
4 Device Information

ORDER NUMBER	PACKAGE	BODY SIZE
SC8886SQDER	32 pin QFN	4mm x 4mm x 0.75mm

DATASHEET DRAFT SOUTHCHIP CONFIDENTIAL

Copyright © 2022, Southchip Semiconductor Technology (Shanghai) Co., Ltd.

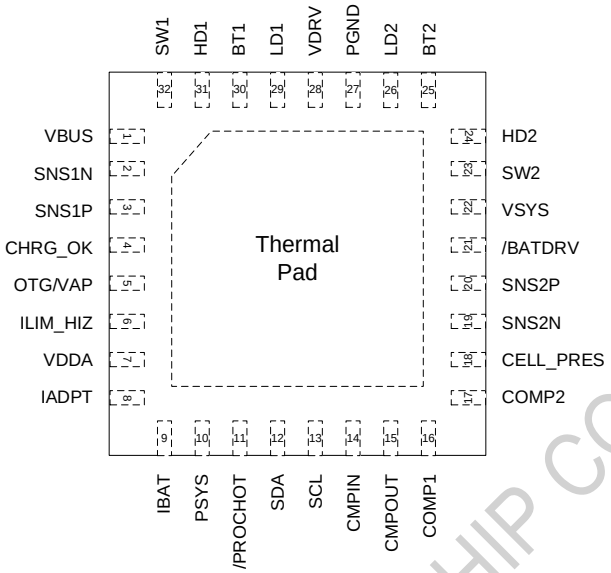
5 Typical Application Circuit



DATASHEET DRAFT SOUTHCHIP CONFIDENTIAL

6 Terminal Configuration and Functions

TOP VIEW



TERMINAL		I/O	DESCRIPTION
NUMBER	NAME		
1	VBUS	I/O	The power input node of charger in charging mode and the power output node of the converter in discharging node.
2	SNS1N	I	Negative input of a current sense amplifier. Connect to one pad of the current sense resistor (typical 10mΩ) on the power path to sense the current into or out from VBUS
3	SNS1P	I	Positive input of a current sense amplifier. Connect to one pad of the current sense resistor (typical 10mΩ) on the power path to sense the current into or out from VBUS
4	CHRG_OK	O	Open drain active high output. CHRG_OK outputs logic high indicating VBUS is in the range of 3.5V to 24V and no fault occurs.
5	OTG/VAP	I	OTG mode or VAP mode enable pin.
6	ILIM_HIZ	I	Input current limit setting pin. Program ILIM_HI-Z voltage by connecting a resistor divider from VDRV supply rail to ILIM_HI-Z pin to ground.
7	VDDA	I	Internal reference bias pin. Connect a 10Ω resistor from VDRV to VDDA and a 1μF ceramic capacitor from VDDA to AGND.
8	IADPT	O	Input current monitoring output pin. Connect a 100 pF or less decoupling capacitor from IADPT to AGND.
9	IBAT	O	Battery current monitoring output pin. Connect a 100 pF or less decoupling capacitor from IBAT to AGND.
10	PSYS	O	System power monitoring output pin. The output current is proportional to the total power from the adapter and the battery. Connect a resistor between this pin and AGND.

DATASHEET DRAFT, SOUTHCHIP CONFIDENTIAL

11	/PROCHOT	O	Active low open drain output of processor hot indicator.
12	SDA	I/O	I2C open-drain data I/O. Connect to data line from the host controller or smart battery. Connect a 10kΩ pullup resistor.
13	SCL	I	I2C clock input. Connect to clock line from the host controller or smart battery. Connect a 10kΩ pullup resistor.
14	CMPIN	I	Input of independent comparator
15	CMPOUT	O	Open drain output of independent comparator.
16	COMP1	I	Connect RC network with this pin to compensate the control loop.
17	COMP2	I	Connect RC network with this pin to compensate the control loop.
18	CELL_PRES	I	1s to 4s battery configuration pin or battery present input. Connect this pin to a resistor divider between VDDA and AGND which sets the target voltage and VSYS over-voltage threshold.
19	SNS2N	I	Negative input of a current sense amplifier. Connect to one pad of the current sense resistor (typical 10mΩ) on the power path to sense the current into or out from battery.
20	SNS2P	I	Positive input of a current sense amplifier. Connect to one pad of the current sense resistor (typical 10mΩ) on the power path to sense the current into or out from battery.
21	/BATDRV	O	P-channel battery FET(BATFET) gate driver output. It is shorted to VSYS to fully turn off the BATFET and goes 10V below VSYS to fully turn on BATFET.
22	VSYS	O	Charger system supply output.
23	SW2	O	Switching node 2. Connect this pin to the inductor
24	HD2	I/O	Gate driver output to control the external high side power MOSFET(Q4).
25	BT2	I/O	Connect a 47nF capacitor between BT2 pin and SW2 pin to bootstrap a bias voltage for high side MOSFET driver.
26	LD2	I/O	Gate driver output to control the external low side power MOSFET(Q3).
27	PGND	I/O	Power ground.
28	VDRV	O	Output of an internal regulator. Connect a 2.2 μF ceramic capacitor from VCC to PGND pin close to the IC. The regulator provides supply for internal gate drivers.
29	LD1	I/O	Gate driver output to control the external low side power MOSFET(Q2).
30	BT1	I/O	Connect a 47nF capacitor between BT1 pin and SW1 pin to bootstrap a bias voltage for high side MOSFET driver.
31	HD1	I/O	Gate driver output to control the external high side power MOSFET(Q1).
32	SW1	O	Switching node 1. Connect this pin to the inductor

DATASHEET DRAFT, SOUTHCHIP CONFIDENTIAL

Copyright © 2022, Southchip Semiconductor Technology (Shanghai) Co., Ltd.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	Unit
Voltage range at terminals(2)	VBUS, VSYS, /BATDRV, SNS1N, SNS1P, SNS2N, SNS2P	-0.3	29	V
	SW1, SW2	-0.3	29	V
	SW1, SW2(10ns)	-4	29	V
	BT1, BT2, HD1, HD2	-0.3	34	V
	HD1, HD2 (25ns)	-4	34	V
	ILIM_HIZ, COMP1, COMP2, SDA, SCL, CHRG_OK, OTG/VAP, CMPIN, CMPOUT, CELL_PRES	-0.3	6.5	V
	VDRV, VDDA, LD1, LD2	-0.3	6.5	V
	LD1, LD2 (25ns)	-4	6.5	V
	/PROCHOT	-0.3	5.5	V
	PSYS, IADP, IBAT	-0.3	3.6	V
	SNS1P to SNS1N, SNS2P to SNS2N	-0.5	0.5	V
	VBUS- SNS1P, VBUS- SNS1N	-1	1	V
	BT1 to HD1, BT2 to HD2, HD1 to SW1, HD2 to SW2	-0.3	6.5	V
T_J	Operating junction temperature range	-40	150	°C
T_{stg}	Storage temperature range	-65	150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values are with respect to network ground terminal.

7.2 Thermal Information

THERMAL RESISTANCE(1)		QFN-32 (4mmX4mm)	UNIT
θ_{JA}	Junction to ambient thermal resistance	35	°C/W
θ_{JC}	Junction to case resistance	7	°C/W

(1) Measured on JESD51-7, 4-layer PCB.

7.3 Handling Ratings

PARAMETER	DEFINITION		MIN	MAX	UNIT
ESD(1)	Human body model (HBM) ESD stress voltage(2)	All pins except	-2	2	kV
	Charged device model (CDM) ESD stress voltage(3)		-750	750	V

(1) Electrostatic discharge (ESD) to measure device sensitivity and immunity to damage caused by assembly line electrostatic discharges into the device.

(2) Level listed above is the passing level per ANSI, ESDA, and JEDEC JS-001. JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(3) Level listed above is the passing level per EIA-JEDEC JESD22-C101. JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

DATASHEET DRAFT, SOUTHCHIP CONFIDENTIAL

7.4 Recommended Operating Conditions

		MIN	TYP	MAX	UNIT
VBUS	VBUS voltage range	3.5		24	V
VBAT	VBAT voltage range	2.55		24	V
VSYS	System voltage range			24	V
C_{VBUS}	VBUS valid capacitance	30			μF
C_{VSYS}	VSYS valid capacitance	30			μF
C_{VBAT}	VBAT valid capacitance	10			μF
L	Inductance	1	2.2	3.3	μH
R_{S1}	current sense resistor 1	5	10		mΩ
R_{S2}	current sense resistor 2	5	10		mΩ
T_A	Operating ambient temperature	-40		125	°C
T_J	Operating junction temperature	-40		150	°C

DATASHEET DRAFT, SOUTHCHIP CONFIDENTIAL

Copyright © 2022, Southchip Semiconductor Technology (Shanghai) Co., Ltd.

7.5 Electrical Characteristics

T_J= -40°C to 125°C, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE						
I_{Q_VBAT}	VBAT supply current	VBAT = 18V, REG0x01[7] = 1, in low power mode		52	90	μA
		VBAT = 18V, REG0x01[7] = 1, in low power mode, REG0x31[4]=1, VDRV off.		54	95	μA
		VBAT = 18V, REG0x01[7] = 0 (performance mode) REG0x31[4]=0，VDRV on. DIS_PSYS		1.2	1.5	mA
		VBAT = 18V, REG0x01[7] = 0 (performance mode), REG0x31[4]=1，VDRV on, EN_PSYS		1.45	1.75	mA
$I_{Q\_BAT\_OTG}$	Quiescent current into VBAT and SYS pins in OTG mode	VBAT = 8.4V, VBUS = 5V, no load, Fsw = 800kHz REG0x01[2]=0 (no OOA mode) MOSFET Qg=4nC		3		mA
		VBAT = 8.4V, VBUS = 12V , no load, Fsw = 800kHz REG0x01[2]=0 (no OOA mode) MOSFET Qg=4nC		5		mA
		VBAT = 8.4V, VBUS = 20V, no load, Fsw = 800kHz REG0x01[2]=0 (no OOA mode) MOSFET Qg=4nC		9		mA
I_{Q_VBUS}	Quiescent current into VBUS pin	VBUS = 20V, VSYS = 12.76V, no load, Fsw = 800kHz REG0x01[2]=0 (no OOA mode) MOSFET Qg=4nC		3.4		mA
		VBUS = 5V, VSYS = 8.56V, no load, Fsw = 800kHz REG0x01[2]=0 (no OOA mode) MOSFET Qg=4nc		6		mA
		VBUS = 12V, VSYS = 12.16V, no load, Fsw = 800kHz REG0x01[2]=0 (no OOA mode) MOSFET Qg=4nC		4		mA
POWER SUPPLY						
V_{UVLO_VBUS}	VBUS under-voltage lockout threshold	VBUS rising	2.3	2.55	2.8	V
		VBUS falling	2.2	2.4	2.6	V
V_{VBUS_CONV}	VBUS converter switching voltage	VBUS rising	3.2	3.5	3.9	V
		VBUS falling	2.9	3.2	3.5	V

DATASHEET DRAFT SOUTHCHIP CONFIDENTIAL

Copyright © 2022, Southchip Semiconductor Technology (Shanghai) Co., Ltd.

V_{UVLO_VBAT}	VBAT under-voltage lockout threshold	VBAT rising	2.3	2.55	2.8	V
		VBAT falling	2.2	2.4	2.6	V
V_{OTG_CONV}	OTG converter switching voltage	VBAT rising	3.25	3.55	3.85	V
		VBAT falling	2.2	2.4	2.6	V
VSYS Regulation						
V_{SYSMAX_REG}	System voltage regulation range, measured on VSYS, VBAT>VSYSMIN		1.184		19.36	V
V_{SYSMAX_ACC}	System voltage regulation accuracy	REG0x05/04() = 0x41A0 ChargeVoltage =16.800V Vsysmax=16.96V	-2		2	%
		REG0x05/04() = 0x3138 ChargeVoltage =12.600V Vsysmax=12.76V	-2		2	%
		REG0x05/04() = 0x20D0 ChargeVoltage =8.400V Vsysmax=8.56V	-3		3	%
		REG0x05/04() = 0x1068 ChargeVoltage =4.200V Vsysmax=4.36V	-3		3	%
V_{SYSMAX_REG}	System voltage regulation range, measured on VSYS, VBAT<VSYSMIN		1.184		19.36	V
V_{SYSMIN_ACC}	System voltage regulation accuracy (VBAT<VSYSMIN)	REG0x0D/0C() = 0x3000 4s setting, default value Vsysmin=12.448V	-2		2	%
		REG0x0D/0C() = 0x2400 3s setting, default value Vsysmin=9.376V	-2		2	%
		REG0x0D/0C() = 0x1800 2s setting, default value Vsysmin=6.304V	-3		3	%
		REG0x0D/0C() = 0x0E00 1s setting, default value Vsysmin=3.744V	-4		4	%
Charge Voltage Regulation						
V_{BATREG}	Charge Voltage regulation range		1.024		19.2	V
V_{BATREG_ACC}	Charge Voltage accuracy	REG0x05/04() = 0x41A0H ChargeVoltage=16.8V	-0.5		0.5	%
		REG0x05/04() = 0x3138H (ChargeVoltage=12.6V	-0.5		0.5	%
		REG0x05/04() = 0x20D0 ChargeVoltage=8.400V	-0.5		0.5	%

DATASHEET DRAFT SOUTHCHIP CONFIDENTIAL

Copyright © 2022, Southchip Semiconductor Technology (Shanghai) Co., Ltd.

		REG0x05/04() = 0x1068 ChargeVoltage=4.200V	-1	1	%
Charge Current Regulation					
I_{CHG_REG}	Charge Current regulation range	V_{SNS2P}-V_{SNS2N}	0.5	81.28	mV
I_{CHG_ACC}	Charge current regulation accuracy with 10mΩ SNS1P/SNS1N series resistor (0℃ to +85℃)	REG0x03/02() = 0x1000H ICHG=4096mA	-2	2	%
		REG0x03/02() = 0x0800H ICHG=2048mA	-3	3	%
		REG0x03/02() = 0x0400H ICHG=1024mA	-5	5	%
		REG0x03/02() = 0x0200H ICHG=512mA	-10	10	%
I_{PRECHG_REG}	Precharge current clamp	CELL=1s, Vsys<3V		384	mA
		CELL=1s, 3V<Vsys<Vsysmin		2	A
		CELL=2s-4s, Vsys<Vsysmin		384	mA
I_{PRECHG_ACC}	Precharge current regulation accuracy with 10mohm SNS1P/SNS1N series resistor (0℃ to +85℃)	CELL=2s-4s, Iprecharge=384mA REG0x03/02() = 0x1080H	-15	15	%
		CELL=1s，Iprecharge=384mA REG0x03/02() = 0x1080H	-25	25	%
		CELL=2s-4s, Iprecharge=256mA REG0x03/02() = 0x1080H	-20	20	%
		CELL=1s, Iprecharge=256mA REG0x03/02() = 0x1080H	-30	30	%
Input Current Regulation					
I_{INLIM_REG}	Input current regulation differential voltage range	V_{SNS1P}-V_{SNS1N}	0.5	64	mV
I_{INLIM_ACC}	Input current regulation accuracy with 10mΩ SNS1P/SNS1N series resistor	REG0x0F/0E() = 0x4FFF, IIN=4000mA	3800	3900 4000	mA
		REG0x0F/0E() = 0x3BFF, IIN=3000mA	2800	2900 3000	mA
		REG0x0F/0E() = 0x1DFF, IIN=1500mA	1300	1400 1500	mA
		REG0x0F/0E() = 0x09FF, IIN=500mA	300	400 500	mA
$I_{LIM\_HIZ\_ACC}$	Input current regulation accuracy on ILIM_HIZ pin, V_{ILIM_HIZ} = 1 V + 40 × I_{INLIM_REG} × (V_{SNS1P}- V_{SNS1N}), with 10mΩ SNS1P/SNS1N series resistor	V_{LIM_HIZ} = 2.6V	3800	4000 4200	mA
		V_{LIM_HIZ} = 2.2V	2800	3000 3200	mA
		V_{LIM_HIZ} = 1.6V	1300	1500 1700	mA
		V_{LIM_HIZ} = 1.2V	300	500 700	mA
Input Voltage Regulation					
V_{INDPM_REG}	Input voltage regulation range	Voltage on VBUS	3.2	19.52	V
V_{INDPM_ACC}	Input voltage regulation accuracy	REG0x0B/0A() = 0x3C80	-2	2	%

DATASHEET DRAFT, SOUTHCHIP CONFIDENTIAL

		VINDPM=18688mV				
		REG0x0B/0A() = 0x1E00 VINDPM=10880mV	-2.5		2.5	%
		REG0x0B/0A() = 0x12C0 VINDPM=8000mV	-3		3	%
		REG0x0B/0A() = 0x0500 VINDPM=4480mV	-5		5	%
OTG Current Regulation						
$V_{OTG\_CUR\_REG}$	Output current regulation differential voltage range	V_{SNS1N}-V_{SNS1P}	0.5		64	mV
I_{OTG_ACC}	Reverse discharge current regulation accuracy with 10mohm series resistor	REG0x09/08() = 0x6300	4900	5000	5100	mA
		REG0x09/08() = 0x3C00	2900	3000	3100	mA
		REG0x09/08() = 0x1E00	1400	1500	1600	mA
		REG0x09/08() = 0x0A00	400	500	600	mA
OTG Voltage Regulation						
V_{OTG_REG}	Reverse discharge current regulation differential voltage range	Voltage on VBUS	3		24	V
$V_{OTG\_REG\_ACC}$	Reverse discharge voltage regulation accuracy	REG0x07/06() = 0x2490 REG0x34[2] = 0 VOTG=20V	-2		2	%
		REG0x07/06() = 0x1D4C REG0x34[2] = 1 VOTG=15V	-2		2	%
		REG0x07/06() = 0x1770 REG0x34[2] = 1 VOTG=12V	-2		2	%
		REG0x07/06() = 0x1194 REG0x34[2] = 1 VOTG=9V	-2		2	%
		REG0x07/06() = 0x09C4 REG0x34[2] = 1 VOTG=5V	-3		3	%
VDRV DRIVER						
V_{DRV}	VDRV regulation voltage	VBUS= 10V, VDRV=5.25V	5	5.25	5.5	V
I_{DRV_LIM}	VDRV current limit	VBUS = 10V, VDRV=4V	50	70		mA
C_{DRV}	VDRV output capacitor required for stability	VDRV load current= 100μA to 50mA		2.2		μF
/BATDRV DRIVER						
V_{BATDRV_ON}	Gate driver clamp voltage on BATFET		8.5	10	11.5	V
R_{BATDRV_ON}	BATDRV turn on resistance		4	5.3	6	kΩ

DATASHEET DRAFT, SOUTHCHIP CONFIDENTIAL

R_{BATDRV_OFF}	BATDRV turn off resistance		0.3	0.55	0.8	kΩ
Power Driver(Q1)						
$R_{DRV\_ON\_Q1}$	High side driver turn on resistance	VBT1 - VSW1 = 5V		2.5		Ω
$R_{DRV\_OFF\_Q1}$	High side driver turn off resistance	VBT1 - VSW1 = 5V		1		Ω
$V_{BT1\_REFRESH}$	Bootstrap refresh comparator falling threshold voltage	VBT1 - VSW1		3.2		V
	Rising hysteresis	VBT1 - VSW1		3.4		V
Power Driver(Q2)						
$R_{DRV\_ON\_Q2}$	Low side driver turn on resistance			2.5		Ω
$R_{DRV\_OFF\_Q2}$	Low side driver turn off resistance			1		Ω
Power Driver(Q3)						
$R_{DRV\_ON\_Q3}$	Low side driver turn on resistance			2.5		Ω
$R_{DRV\_OFF\_Q3}$	Low side driver turn off resistance			1		Ω
Power Driver(Q4)						
$R_{DRV\_ON\_Q4}$	High side driver turn on resistance	VBT2 – VSW2 = 5V		2.5		Ω
$R_{DRV\_OFF\_Q4}$	High side driver turn off resistance	VBT2 – VSW2 = 5V		1		Ω
$V_{BT2\_REFRESH}$	Bootstrap refresh comparator falling threshold voltage	VBT2 – VSW2		3.2		V
	Rising hysteresis	VBT2 – VSW2		3.4		V
Switching Frequency						
F_{SW}	Switching frequency	Fsw=1200kHz, REG0x01[1] = 0	1050	1200	1350	kHz
		Fsw=800kHz, REG0x01[1] = 1	750	800	950	kHz
Current Monitor (IADP)						
V_{ADP_CLAMP}	IADPT output clamp voltage		3.1	3.2	3.3	V
I_{ADP}	IADPT output current			2		mA
A_{IADP_ACC}	Input current sensing gain	$V_{IADPT}/(V_{SNS1P}-V_{SNS1N})$, REG0x00[4] = 0.		20		V/V
		$V_{IADPT}/(V_{SNS1P}-V_{SNS1N})$, REG0x00[4] = 1.		40		V/V
V_{IADP_ACC}	Input current monitor accuracy	$V_{SNS1P}-V_{SNS1N}$=40.96mV	-2		2	%
		$V_{SNS1P}-V_{SNS1N}$=20.48mV	-3		3	%
		$V_{SNS1P}-V_{SNS1N}$=10.24mV	-6		6	%
		$V_{SNS1P}-V_{SNS1N}$=5.12mV	-10		10	%
Current Monitor (IBAT)						
V_{BAT_CLAMP}	IBAT output clamp voltage		3.1	3.2	3.3	V
I_{BAT}	IBAT output current			2		mA

DATASHEET DRAFT, SOUTHCHIP CONFIDENTIAL

A_{IBAT_ACC}	Input current sensing gain	$V_{IADPT}/(V_{SNS1P}-V_{SNS1N})$, REG0x00[3] = 0.		8		V/V
		$V_{IADPT}/(V_{SNS1P}-V_{SNS1N})$, REG0x00[3] = 1.		16		V/V
V_{IBAT_ACC}	Charge and discharge current monitor accuracy	$V_{SNS2P}-V_{SNS2N}$=40.96mV	-2		2	%
		$V_{SNS2P}-V_{SNS2N}$=20.48mV	-4		4	%
		$V_{SNS2P}-V_{SNS2N}$=10.24mV	-7		7	%
		$V_{SNS2P}-V_{SNS2N}$=5.12mV	-15		15	%
Power Monitor (PSYS)						
V_{PSYS_CLAMP}	PSYS output clamp voltage		3	3.2	3.3	V
I_{PSYS}	PSYS output current			2		mA
A_{PSYS_ACC}	PSYS gain	$I_{PSYS}/(P_{IADPT}+P_{BAT})$, REG0x31[1] = 1, RS1=RS2=10mΩ		1		μA/W
		$I_{PSYS}/(P_{IADPT}+P_{BAT})$, REG0x31[1] = 0, RS1=RS2=10mΩ		0.25		μA/W
V_{PSYS_ACC}	PSYS gain accuracy	Adapter only with system power = 19V/45W (-40°C to 85°C)	-4		4	%
		Adapter only with system power = 12V/24W (-40°C to 85°C)	-6		6	%
		Battery only with system power = 11V/44W (-40°C to 85°C)	-5		5	%
		Battery only with system power = 7.4V/30W (-40°C to 85°C)	-7		7	%
OTG_UV/OV Protections						
V_{OTG_UV}	Output undervoltage fall threshold during OTG mode	As percentage of REG0x07/06()	83%	87%	90%	
$t_{OTG\_UV\_dg}$	OTG undervoltage deglitch time during OTG mode			8.5		ms
V_{OTG_OV}	Output overvoltage rise threshold during OTG mode	As percentage of REG0x07/06()	102%	107%	112%	
$t_{OTG\_OV\_dg}$	OTG overvoltage deglitch time during OTG mode			10		ms
PRE-CHARGE to FAST CHARGE TRANSITION						
$V_{BAT\_SYSMIN\_R}$	Pre-charge to fast charge threshold, VSNS1N rising	As percentage of REG0x0D/0C()	98%	100%	102%	
	falling edge	As percentage of REG0x0D/0C()	96%	97.5%	99%	
$V_{BAT\_LOWV\_R}$	1 cell pre-charge LOWV threshold rising		2.8	3	3.2	V
	falling edge		2.6	2.8	3	V
Cell configuration						
V_{CELL_4S}	Voltage on CELL_PRES pin, configured as cell 4s	with respect to VDRV	0.7	0.75		
V_{CELL_3S}	Voltage on CELL_PRES pin, configured as cell 3s	with respect to VDRV	0.52	0.55	0.64	

DATASHEET DRAFT, SOUTHCHIP CONFIDENTIAL

Copyright © 2022, Southchip Semiconductor Technology (Shanghai) Co., Ltd.

V_{CELL_2S}	Voltage on CELL_PRES pin, configured as cell 2s	with respect to VDRV	0.35	0.4	0.48	
V_{CELL_1S}	Voltage on CELL_PRES pin, configured as cell 1s	with respect to VDRV	0.185	0.25	0.32	
V_{CELL_PRES}	Battery present rising threshold	with respect to VDRV	0.18			
$V_{CELL\_REMOVAL}$	Battery present falling threshold	with respect to VDRV			0.15	
PROCHOT_VDPM						
V_{VDPM}	VBUS voltage falling edge to trigger VDPM PROCHOT, with respect to VDPM (Reg0x0B/0A)	Reg0x36[0]=0	97%	100%	103%	
		Reg0x36[0]=1, Reg0x37[0]=1	87%	90%	93%	
		Reg0x36[0]=1, Reg0x37[0]=0	77%	80%	83%	
PROCHOT_CMP						
V_{CMP_REF}	Independent comparator reference	CMP_REF=0 (Reg0x30[7]=0), falling edge	1.17	1.2	1.23	V
		CMP_REF=1 (Reg0x30[7]=1), falling edge	2.26	2.3	2.33	V
		Rising hysteresis		100		mV
PROCHOT_ICRIT						
I_{ICRIT}	Input current rising threshold to trigger ICRIT PROCHOT	with respect to ILIM2 (Reg0x37[7:3])	105%	110%	117%	
PROCHOT_INORM						
I_{NORM}	Input current rising threshold to trigger INORM PROCHOT	with respect to ILIM1 (Reg0x0F/0E)	105%	110%	115%	
PROCHOT_IDCHG						
I_{DCHG}	Battery discharge current rising threshold trigger IDCHG PROCHOT	Reg0x39[7:2] = 001100b IDCHG=6272mA	-3		3	%
		Reg0x39[7:2] = 011000b IDCHG=12288mA	-3		3	%
PROCHOT_VSYS						
V_{SYS_TH2}	VSYS voltage falling threshold to trigger VSYS PROCHOT	Reg0x36[3:2] = 10b Cell = 2s to 4s	6.38	6.5	6.62	V
		Reg0x36[3:2] = 10b Cell = 1s	3.38	3.5	3.62	V
PROCHOT_Adapter Removal						
$V_{Adapter\_Removal}$	VBUS voltage falling threshold to trigger Adapter removal PROCHOT		2.95	3.2	3.45	V
PROCHOT_Battery Removal						
$V_{Battery\_Removal}$	CELL_PRES pin voltage falling threshold to trigger Battery removal PROCHOT	with respect to VDRV			15	%

DATASHEET DRAFT, SOUTHCHIP CONFIDENTIAL

Copyright © 2022, Southchip Semiconductor Technology (Shanghai) Co., Ltd.

Protections						
V_{ACOV}	Input overvoltage threshold	VBUS rising	25	26	27	V
		VBUS falling	23.5	24.5	25	V
t_{ACOV}	Input overvoltage deglitch time	VBUS rising		100		µs
		VBUS falling		1		ms
V_{ACOC}	SNS1P to SNS1N rising threshold, with respect to ILIM2 setting in REG0x37[7:4]	REG0x32[2] = 1	180	200	220	%
		REG0x32[2] = 0	120	133	146	%
V_{SYSOVP}	System overvoltage rising threshold to turn off the converter	Cell = 1s	4.85	5	5.1	V
		Cell = 2s	11.3	12	12.7	V
		Cell = 3s/4s	19	19.5	20	V
	Falling edge	Cell = 1s		4.8		V
		Cell = 2s		11.5		V
		Cell = 3s/4s		18.7		V
I_{SYS_OVP}	VSYS over voltage discharge current			30		mA
V_{BAT_OVP}	VBAT OVP rising threshold	Rising edge, over VBAT target	102.5%	104%	106%	
		Hysteresis, over VBAT target		2%		
I_{BAT_OVP}	VBAT over voltage discharge current			10		mA
V_{SYS_SHORT}	VSYS short threshold	VSYS falling, to stop switching	2.2	2.4	2.6	V
		VSYS rising, to recover		2.7		V
LOGIC OUTPUT OPEN DRAIN (SDA, CHRG_OK, CMPOUT)						
I_{OUT_LO}	Output saturation voltage	5 mA drain current			0.4	V
Logic Output /PROCHOT						
I_{OUT_LO}	Output saturation voltage	50 Ω pullup to 1.05V / 5-mA			300	mV
Analog Input ILIM_HIZ						
V_{HIZ_HI}	Voltage to get out of HIZ mode	ILIM_HIZ pin rising	0.8			V
V_{HIZ_LO}	Voltage to enable HIZ mode	ILIM_HIZ pin falling			0.4	V
I2C INTERFACE AND IO LOGIC						
R_{PD}	OTG pin internal pull-down resistor		0.75	1	1.25	MΩ
V_{IL}	OTG, SCL, SDA input low voltage				0.4	V
V_{IH}	OTG, SCL, SDA input high voltage		0.85			V
f_{SCL}	I2C clock frequency				400	kHz
THERMAL SHUTDOWN						
T_{SD}	Thermal shutdown temperature	Temperature rising, 155°C setting		155		°C
		Hysteresis		20		°C

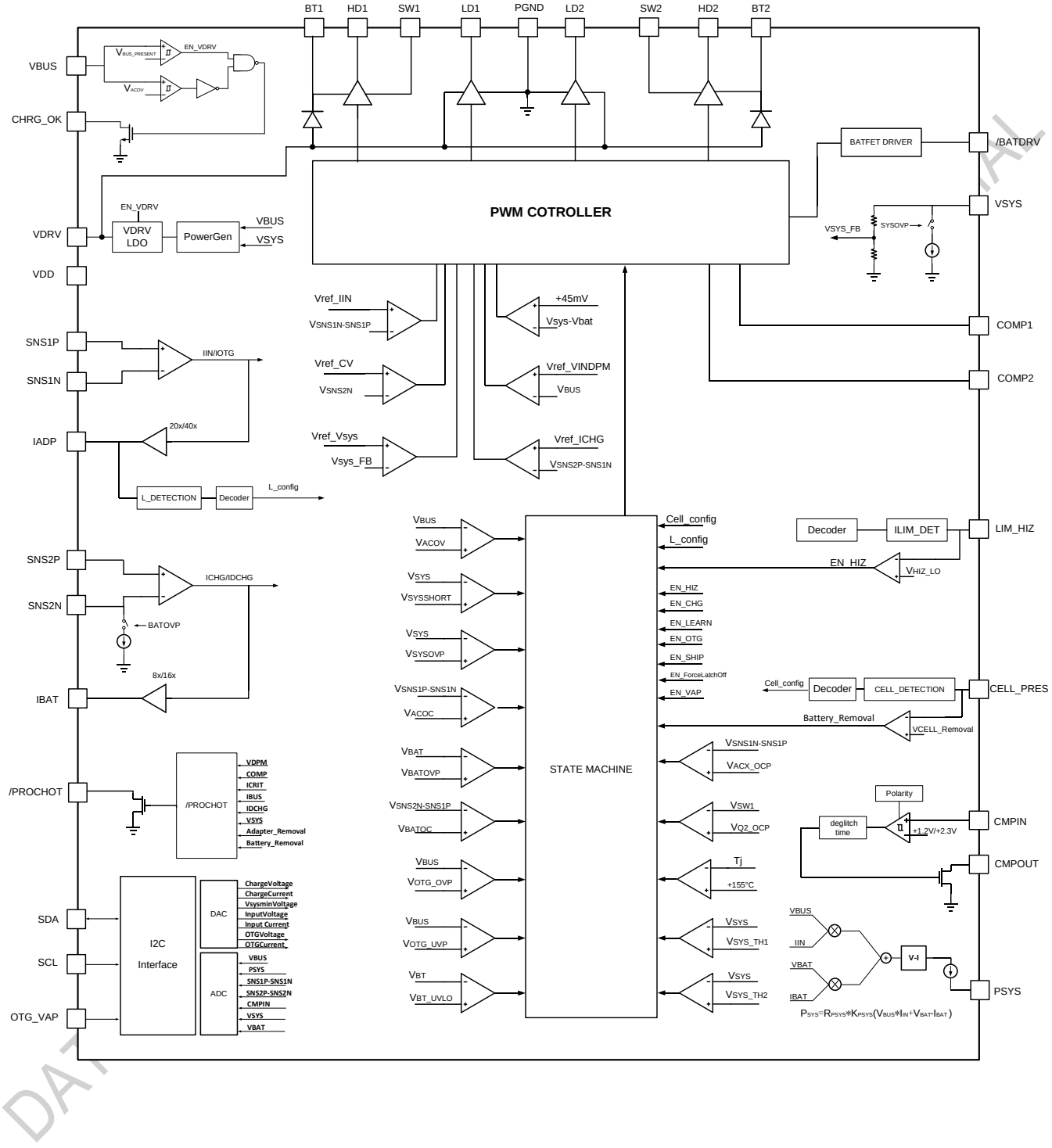
DATASHEET DRAFT SOUTHCHIP CONFIDENTIAL

Copyright © 2022, Southchip Semiconductor Technology (Shanghai) Co., Ltd.

t_{SD}	Thermal shutdown deglitch time	Temperature rising	100	μs
		Temperature falling	12	ms

DATASHEET DRAFT , SOUTHCHIP CONFIDENTIAL

8 Functional Block Diagram



DRAFT

9 Feature Description

SC8886S is a bi-direction buck-boost charger controller with NVDC power path management function, which is suitable for 1-4 cell rechargeable battery application.

SC8886S supports both charging and discharging working mode. The current and voltage can be set by host through I2C.

With NVDC powerpath function, SC8886S realizes plug-and-play function by regulating system voltage at minimum system voltage even when a depleted battery is applied. When system load increases and adapter's capability is not enough, the dynamic power management works by automatically reducing charging current to meet the system power first.

9.1 Power up

9.1.1 Power up from battery only

When only battery plugs in and $V_{BAT} > V_{BAT\_UVLO}$, SC8886S powers up and enters low power mode by default.

In low power mode, the IC consumes low quiescent current. The BATFET is s turned on to supply system. The VDRV LDO works at low power mode. The independent comparator can be enabled by set Reg0x31[6:5]

When Reg0x01[7]=0, IC enters performance mode. In performance mode, The VDRV LDO is on to provide accurate voltage reference and bias. Current monitor IBAT and power monitor PSYS can be enabled. Processor hot indication function can be also enabled.

9.1.2 Power up from VBUS

When adapter plugs in and $VBUS>V_{VBUS\_CONV}$, SC8886S starts poor source detection if HI-Z mode is not asserted.

The power up sequence is as follow:

1. 50ms after $VBUS>V_{VBUS\_CONV}$ and $VBUS<V_{ACOV}$, CHRG_OK is pulled high.
2. Setup Input current limit and Input regulation voltage.
3. Cell detection set by CELL_PRES pin and set charging voltage and minimum system voltage.
4. after 150ms debounce time, converter powers up and decides whether to enter into auto-wake mode based on the battery voltage

9.1.2.1 Hi-Z mode

When ILIM_HI-Z pin is pulled down or EN_HI-Z =1, SC8886S enters into Hi-Z mode. In Hi-Z mode, even when adapters exist, IC still stops switching and consumes low quiescent current from adapter. The BATFET is turned on to supply system.

9.1.2.2 Input current limit (IDPM) setting

SC8886S provides both external and internal current limit setting. The actual current limit is decided by the lower setting of IIN_HOST (set by REG0x0F/0E) and ILIM_HIZ pin.

a) Internal register setting:

The default setting of IIN_HOST is 3.3A. the IIN_HOST register is a 7-bit DAC register and with 50mA resolution.

b) External ILIM_HIZ pin setting:

IC detects ILIM_HI-Z voltage by one-shot ADC sampling at the start-up phase.

The input current is decided by ILIM_HI-Z pin voltage as follow:

$$V_{ILIM\_HIZ} = 1\ V + 40\times IDPM \times RS1$$

When ILIM_HIZ pin voltage is below 0.4V, IC enters Hi-Z mode with low quiescent current. When ILIM_HIZ pin is above 0.8V, IC is out of HIZ mode.

External ILIM_HIZ pin can be disabled by set Reg0x32[7] =0 or pull the ILIM_HIZ above 4V.

9.1.2.3 Input regulation voltage (VDPM) setting

SC8886S detects VBUS voltage under no load before converter switching. The input regulation voltage is set as follow:

$$VDPM = VBUS - 1.28V$$

The input regulation voltage is loaded to Reg0x0A/0B and VDPM voltage can be rewrite by host through Reg0x0A/0B.

9.1.2.4 Cell detection

When VDRV LDO is activated, SC8886S detects the battery configuration through CELL_PRES pin bias voltage. After cell detection is finished, Charge Voltage, Vsysmin voltage and SYSOVP threshold is loaded if the register value is not written by host. Otherwise, the charge voltage and vsysmin voltage shall not be loaded.

The charge voltage and vsysmin voltage can be modified by writing corresponding register. SYSOVP cannot be modified once configured successfully.

The cell detection configuration based on CELL_PRES pin is as follow:

DATASHEET DRAFT, SOUTHCHIP CONFIDENTIAL

Cell Detection	CELL_PRES Voltage	Charge Voltage	Vsysmin Voltage	SYSOVP Threshold
4 cell	75%* VDRV	16.800V	12.29V	19.5V
3 cell	55%* VDRV	12.592V	9.216V	19.5V
2 cell	40%* VDRV	8.400V	6.144V	12V
1 cell	25%* VDRV	4.192V	3.584V	5V

9.1.2.5 Inductor detection

When VDRV LDO is activated, SC8886S detects the inductor configuration through IADP pin's resistor. The resistor connected to IADP pin must be configured correctly before input source plugs in

Resistor of IADP pin	Inductor applied
93kΩ	1μH
137kΩ	2.2μH
169kΩ	3.3μH

9.2 NVDC Power Path Management

The SC8886S deploys Narrow VDC architecture (NVDC) with BATFET separating system from battery. When only battery exists, the BATFET is fully on to supply system and maximize battery power capability. System voltage is regulated between Vsysmin+160mV and Vsysmax+160mV when VBUS exists.

9.2.1 System Voltage Regulation

9.2.1.1 Charger is enabled

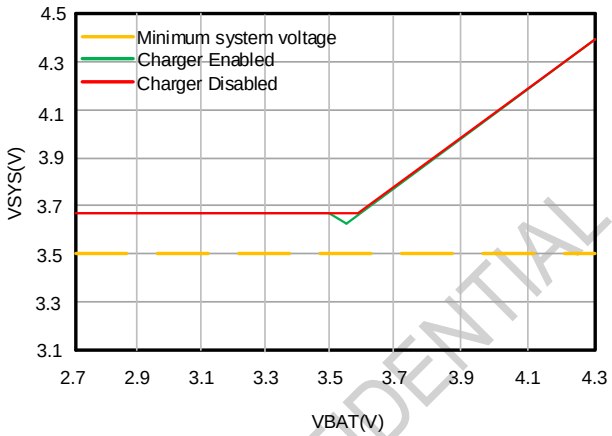
When VBAT<Vsysmin, the system voltage is regulated at Vsysmin+160mV. the BATFET works at LDO mode. The charging current is clamped to 384mA.

When ChargeVoltage >VBAT>Vsysmin, the BATFET is fully on, the system voltage is IR drop above battery voltage caused by charging current.

9.2.1.2 Charger is disabled

When VBAT<Vsysmin, the system voltage is regulated at Vsysmin+160mV. the BATFET is turned off.

When VBAT>Vsysmin, the BATFET is turned off, the system voltage is regulated at 160mV above VBAT.



9.2.2 Dynamic Power Management

When input source is over-loaded, either the current exceeds the input current limit (IDPM) or the voltage falls below the input voltage limit (VDPM). The device then reduces the charge current until the input current falls below the input current limit and the input voltage rises above the input voltage limit.

When the charge current is reduced to zero, but the input source is still overloaded, the system voltage starts to drop, and Once the system voltage falls below the battery voltage, the device automatically enters the supplement mode where the BATFET turns on and battery starts discharging so that the system is supported from both the input source and battery.

9.2.3 Supplement Mode

When BATFET is not fully on under some conditions, such as VBAT is below Vsysmin or charging is disabled, the battery supplies system by regulating BATFET at ideal diode mode. When the system voltage falls below the battery voltage, the BATFET turns on to supplement system. The BATFET gate is regulated so that the VDS of BATFET stays at 45 mV. when the current is low. This prevents oscillation from entering and exiting the supplement mode.

9.3 Charging Mode

SC8886S support 1-4 cells battery charging management. Charger can be disabled by writing ChargeCurrent to 0mA or set Reg0x00[0]=1.

9.3.1 Auto Wake-up Charge

if battery voltage is below Vsysmin (minimum system voltage) upon adapter plugs in, the SC8886S will automatically enable 128mA-charging current for 30 mins. The following condition will exit IC from auto-wake-up charging:

DATASHEET DRAFT SOUTHCHIP CONFIDENTIAL

- Writing auto_wake_up mode enable bit to 0
- Writing value command to charge_current register
- Battery voltage is charged up above Vsysmin
- 30-mins time out

When above condition occurs, the auto_wake_up bit and charge current is reset to 0 automatically. Then waits for command from host.

9.3.2 Pre-charge

When Battery is lower than Vsysmin, SC8886S is working at pre-charge phase.

9.3.2.1 (LDO enable mode)

The BATFET is regulated at LDO mode by default and pre-charge current is clamped.

For 1 cell configuration, if battery voltage is below 3V, charge current is clamped to 384mA. If battery voltage is between 3V and Vsysmin, the current is clamped to 2A.

For 2-4 cells configuration, if battery voltage is below Vsysmin, charge current is always clamped to 384mA.

9.3.2.2 No BATFET mode (LDO disabe mode)

LDO disable mode should be enabled to corporate with no BATFET application. Before the converter starts operation, LDO mode needs to be disabled. The following sequence is required to configure charger without BATFET.

1) Before adapter plugs in, put the charger into HI-Z mode. (either pull ILIM_HIZ pin to ground, or set REG0x35[7] to 1)
2) Set 0x00[2] to 0 to disable LDO mode.
3) Set 0x30[0] to 0 to disable auto-wakeup mode.
4) Check if battery voltage is properly programmed (REG0x05/04)
5) Set pre-charge/charge current (REG0x03/02)
6) Put the device out of HIZ mode. (Release ILIM_HIZ from ground and set REG0x35[7]=0).

No current clamp is applied in LDO disable mode. Thus, to ensure safety of battery charging, the charge current should be set properly by host when battery is below Vsysmin voltage.

9.3.3 Fast Charge

When battery voltage is above Vsysmin, IC enters fast charge phase. BATFET is fully on in fast charge phase. charge current is regulated at setting register value. To ensure the smooth of current adjustment, slew rate control is adopted in fast charge current regulation.

Charge current can be set by write Reg0x03/02. The charge current register is reset to 0, when following events occur:

- Adapter is removed
- BAT_CONFG is pulled down
- Write Charge Voltage register to 0

The charger fault will not reset charge current.

9.3.4 Constant Voltage Charge

When battery voltage is close to charge voltage, charge current is reduced under charge voltage loop regulation automatically. By default, SC8886S works in no termination mode and BATFET is fully on. Though the charging path is still on, battery shall not be overcharged due to the high gain charge voltage loop. Or the host can terminate charging by set the charge current to 0A or set Reg0x00[0] =1 to inhibit charging.

Charge voltage is set by Charge_Voltage Reg0x05/04. Writing REG0x05/04 to 0 will set REG0x05/04 to the default value based on CELL_PRES pin, and force REG0x03/02 to zero to disable charge.

9.4 OTG Mode

SC8886S also supports reverse discharging OTG mode to deliver power from the battery to other portable devices through USB port.

The supported OTG voltage range is from 3V~24V and OTG current range is from 50mA to 6400mA, which is complied with PD device output standard. Besides, to avoid voltage overshoot, slew rate control is adopted in OTG voltage control to avoid voltage overshoot.

The discharging operation can be enabled if the conditions are valid:

1) OTG output voltage is set REG0x07/06.
2) OTG output current limit is set in REG0x09/08.
3) EN_OTG pin is pulled up HIGH, REG0x35[4] =1 and REG0x34[5] = 1.
4) VBUS is below VBUS_UVLO.
5) 10 ms after the above conditions are valid, converter starts and VBUS voltage ramps up to target voltage. CHRG_OK pin goes HIGH if REG0x01[3] = 1.

In OTG mode, if output voltage is 10% higher than setting OTG voltage, OTG_OV protection is triggered. if output voltage is 15% lower than setting OTG voltage, OTG_UV

DATASHEET DRAFT, SOUTHCHIP CONFIDENTIAL

protection is triggered. OTG_OV and OTG_UV both cause SC8886S exits from OTG mode and reset the EN_OTG bit to 0.

If BATOC, force latchoff and Tshut is tripped, the converter is stopped but the EN_OTG bit is not reset to 0. Once above fault disappears, the OTG operation resumes.

9.5 PFM Mode

In order to improve converter light-load efficiency, IC switches to PFM operation at light load. There are two kind of PFM mode: Out of audio PFM mode and regular PFM mode

Set Reg0x01[2] to 1, OOA PFM mode is enabled. The minimum frequency can be limit to 25 kHz which is out of audio frequency. Thus, the converter can switch silently under any load condition.

Set Reg0x01[2] to 0, regular PFM mode is enabled. There is no minimum limit on switching frequency. The switching frequency may be lower than OOA mode, but light load efficiency is improved due to reduced switching loss.

9.6 PSYS

The charger monitors total instantaneous system power by PSYS pin. the PSYS function is disabled by default, to minimize the quiescent current. PSYS function can be enabled by setting REG0x31[4] to 1.

During charging mode, the input adapter powers system, system power is input power minus battery charging power.

During reverse OTG mode, the battery powers the system and VBUS output. The system power is the battery discharging power minus VBUS output power. Another PSYS option is provided in OTG mode by writing Reg0x34[0]=1, the system power is the battery discharging power only.

PSYS outputs a current source and the power information is converted to voltage by resistor R_{PSYS}. The PSYS voltage can be calculated as:

$$V_{PSYS} = K_{PSYS} * (V_{BUS}*I_{IN} + V_{BAT}*I_{BAT}) *R_{PSYS}$$

- K_{PSYS} is the gain of system power monitor, can be programmed in REG0x31[1] with default 1μA/W, and 0.25μA/W option is available. K_{PSYS} is based on current -sensing resistor Rs1 and Rs2. So Rs1 and Rs2 must be selected with right value according the actual value on application board. SC8886S provides both 10mΩ and 5mΩ for option.
- V_{BUS} is the adapter voltage.
- V_{BAT} is the battery voltage.
- I_{IN} is the adapter current, IIN >0 in the forward charging mode and IIN<0 in reverse discharging mode.
- I_{BAT} is the battery current, IBAT<0 in the forward charging mode and IBAT>0 in reverse discharging mode.
- R_{PSYS} is the resistor connected with PSYS with GND.

9.7 Current Monitor (IADPT/IBAT)

SC8886S provides two dedicated pins IADPT pin for adapter current/OTG current and IBAT pin for monitoring battery charging current/battery discharging current. The voltage can be calculated as:

V_{IADPT}=20 or 40 *(V_{SNS1P}-V_{SNS1N}) during charging mode

V_{IADPT}=20 or 40 *(V_{SNS1N}-V_{SNS1P}) during discharging mode

V_{IBAT}=8 or 16 *(V_{SNS2P}-V_{SNS2N}) during charging mode

V_{IBAT}=8 or 16 *(V_{SNS2N}-V_{SNS2P}) during discharging mode

IBAT functionality can be enabled or disabled through Reg0x31[7] bit.

The gain of IADPT can be programmed in REG0x00[4] with 20 by default and 40 is available for option.

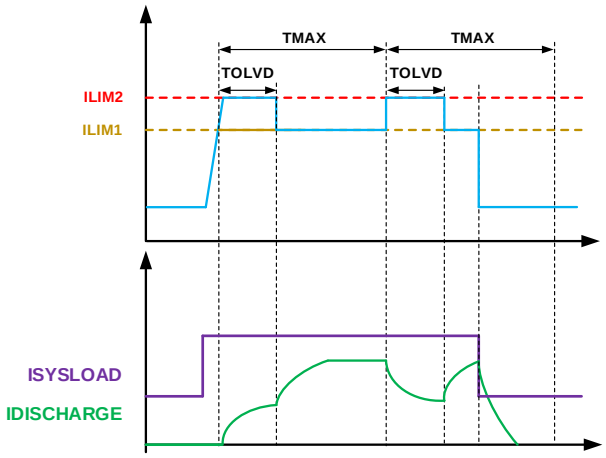
The gain of IBAT can be programmed in REG0x00[3] with 16 by default and 8 is available for option.

The direction of IBAT pin can be also set by Reg0x32[6]. IBAT pin monitors battery discharging current by default.

9.8 Two-Level Current Limit (Peak Power Mode)

Peak power usually occurs in power system but not last for long time which is normally on longer than milliseconds. On the other hand, the adapter can be overload for few milliseconds during which adapter is capable for supplying current higher than its DC rating. Based on above consideration, the SC8886S employs two-level input current limit, or peak power mode, to fully utilize the adapter surge capability and minimize battery discharge power when CPU peak power occurs. The two current limit level is shown as follow:

DATASHEET DRAFT SOUTHCHIP CONFIDENTIAL



Peak power mode can be enabled set by REG0x33[5:4]. When battery discharge or system voltage starts to drop, the peak power mode is triggered. The current limit switches between ILIM1 and ILIM2 as system load changes.

ILIM1: The DC current limit is the same as adapter DC current, set in REG0x0F/0E().

ILIM2: The overloading current is set in REG0x37[7:3], as a percentage of ILIM1.

- 110%-230%, 5%/step
- 250%-450%, 50%/step

Firstly, as the system load increases, the adapters current reaches ILIM1 firstly, the current limit is set to ILIM2 and IC enters overload cycle for TOVLD. TOVLD is the overload cycle duration, which is set in Reg0x33[7:6].

Then, ILIM1 is set for current limit when overload cycle is finished, IC enters relax cycle. The relax cycle duration is TMAX-TOVLD. The TMAX is set in REG0x33[1:0]

After TMAX, if the load is still high, another peak power cycle starts.

If TOVLD is programmed to be equal to TMAX, then peak power mode is always on.

9.9 Vmin Active Protection

When running on battery only, with a 1 or 2 cell system, Vmin Active Protection is a required feature designed to absorb power peaks during periods of high demand. The main purpose of this feature is to keep the system voltage from drooping below the minimum system level and cause the system to black screen.

Follows the steps below to enter VAP operation.:

1) Set the voltage limit to charge VBUS in REG0x07/06().
2) Set the current limit to charge VBUS in REG0x09/08() and REG0x39[7:2].
3) Set the system voltage regulation point in REG0x0D/0C, when the input cap supplements battery, the VSYSMIN regulation loop will maintain VSYS at this regulation point.
4) Set the PROCHOT_VSYS_TH1 threshold to trigger the VAP discharging VBUS in REG0x36[7:4].
5) Set the PROCHOT_VSYS_TH2 threshold to assert /PROCHOT active low signal to throttle SoC in REG0x36[3:2].
6) Enable the VAP mode by setting REG0x34[5] = 0, REG0x35[4] = 0, and pulling the OTG/VAP pin to high.

Writing REG0x34[5] = 1 or pull low the OTG/VAP pin to low both exit IC from VAP operation.

If any fault of ACOV, SYSOVP, THSUT, BATOC and force latchoff occurs, SC8886S will reset REG0x34[5] = 1, and the charger will exit VAP mode automatically.

9.10 PROCHOT (Processor Hot Indication)

Once any of the following events is detected, SC8886S outputs low at /PROCHOT pin.

- ICRIT: adapter peak current, as 110% of I_{LIM2}
- INOM: adapter average current, as110% of I_{LIM1}
- IDCHG: battery discharge current exceeds IDCHG_VTH (REG0x39[7:3])
- VSYS: system voltage on VSYS falls below VSYS_TH2 (REG0x36[3:2])
- Adapter Removal: AC_STAT 1 to 0
- Battery Removal: upon battery removal (CELL_PRES pin goes LOW)
- CMPOUT: Independent comparator output (CMPOUT pin HIGH to LOW)
- VINDPM: input voltage on VBUS lower than 80%/90%/100% of VINREG threshold.
- EXIT_VAP: Every time when the charger exits VAP mode.

The threshold of ICRIT, IDCHG, VSYS or VINREG, and the deglitch time of ICRIT, INOM, IDCHG or CMPOUT are programmable through commands. Except the PROCHOT_EXIT_VAP is always enabled, the other triggering events can be individually enabled in REG0x38[7:0]. When any enabled event in PROCHOT

DATASHEET DRAFT, SOUTHCHIP CONFIDENTIAL

profile is triggered, /PROCHOT is asserted low for a single pulse with minimal width programmable in REG0x23[5:4]. At the end of the single pulse, if the PROCHOT event is still active, the pulse gets extended until the event is removed.

Extension mode: If the /PROCHOT pulse extension mode is enabled by setting REG0x23[6] = 1, the /PROCHOT pin will be kept as low until host writes REG0x23[3] = 0, even if the triggering event has been removed.

If the PROCHOT_VDPM or PROCHOT_EXIT_VAP is triggered, /PROCHOT pin will always stay low until the host clears it, no matter the /PROCHOT is in one pulse mode or in extended mode.

9.10.1 PROCHOT During Low Power Mode

During low power mode (REG0x01[7] = 1), the charger offers a low power PROCHOT function with very low quiescent current consumption, which uses the independent comparator to monitor the system voltage, and assert /PROCHOT to CPU if the system power is too high.

Below lists the register setting to enable PROCHOT monitoring system voltage in low power mode.

- REG0x01[7] = 1 to enable charger low power mode.
- REG0x38[7:0] = 00
- REG0x30[6:4] = 100

Independent comparator threshold is always 1.2 V

Connect CMPIN to voltage proportional to system and set REG0x31[6:5] = 10, charger monitors system voltage. When CMPIN voltage falls below 1.2 V, the /PROCHOT triggers from HIGH to LOW

9.10.2 /PROCHOT Status

REG0x22[7:0] and REG0x23[0] reports which event in the profile triggers PROCHOT if the corresponding bit is set to 1. The status bit can be reset back to 0 after it is read by host, when the current /PROCHOT event is not active anymore. Assume there are two /PROCHOT events, event A and event B. Event A triggers /PROCHOT first, but event B is also active. Both status bits will be HIGH. At the end of the 10 ms /PROCHOT pulse, if any of the /PROCHOT event is still active (either A or B), the /PROCHOT pulse is extended.

9.11 Pass Through Mode

The charger can be operated in the pass through mode (PTM) to improve efficiency. In PTM, the buck and boost high side FETs Q1 and Q4 are both turned on, while the buck and boost low side FETs are both turned off. The input power is directly passed through the charger to the system. The switching losses of MOSFETs and the inductor core loss are saved.

SC8886S will be transition from normal buck-boost operation to PTM operation by:

- Set REG0x32[7] = 0, to disable the ILIM_HIZ pin.
- Set REG0x31[0] = 1, LIM_HIZ pin function is selected as PTM enable pin.
- Set REG0x30[2] = 1 to enable PTM mode.
- Ground ILIM_HIZ pin.

SC8886S will transition out of PTM mode with host control by:

- Set REG0x30[2] = 0.
- Pull ILIM_HIZ pin to high.

If any fault of ACOC, BATOC, SYSOVP, THSUT and force latch off fault occurs, SC8886S will reset REG0x30[2] to 0 and exits PTM to buck-boost operation.

9.12 Input Current Optimizer (ICO)

The SC8886S provides Input Current Optimizer (ICO) algorithm to identify maximum power point without overload the input source. The algorithm automatically identifies maximum input current limit of power source without entering VINDPM to avoid input source overload.

The ICO function is disabled default and can be enabled by set REG0x35[3] to 1.

The actual input current limit used by the Dynamic Power Management is reported in register IIN_DPM set in Reg0x24/25, while ICO is enabled. If the EN_ICO_MODE bit is set to 0, IIN_DPM register reports IINLIM register value.

In addition, even when EN_ICO_MODE=1, the current limit is still clamped by ILIM pin unless EN_EXTILIM bit is 0 to disable ILIM_HIZ pin function.

9.13 Force Latch off Mode

SC8886S enables force latch off function by set Reg0x30[3] =1. When independent comparator output COMPOUT toggles down, converter is latched off. SC8886S turns off Q1 and Q4 (same as disable converter) so that the system is disconnected from the input source. The VDRV LDO is still on but CHRG_OK is pulled down.

The force latch off fault can be cleared by writing REG0x30[3] to 0.

DATASHEET DRAFT SOUTHCHIP CONFIDENTIAL

Copyright © 2022, Southchip Semiconductor Technology (Shanghai) Co., Ltd.

9.14 Ship Mode

When ship mode is enabled (REG0x30[1] = 1), A 30mA discharging current is pulled down from VSYS pin in 120ms. When 120ms is over, REG0x30[1] is reset to 0.

9.15 Learn Mode

Learn mode function allows the battery to discharge while the adapter is present. It calibrates the battery gas gauge over a complete discharge/charge cycle. Learn mode is enabled by set Reg0x00[5] =1.

In learn mode, SC8886S turns off buck-boost converter regardless of whether the adapter is present. The BATFET is turned on to discharging power to system.

Once SC8886S exits from learn mode and resumes switching immediately to supply power to the system bus from adapter in order to prevent system voltage drop. The following is the ways to exits learn mode:

- Set Reg0x00[5] =0 to disable learn mode.
- When CELL_PRES pin voltage falls, battery removal is detected.

9.16 Protection

SC8886S supports full protections including watchdog timer, input overvoltage protection, input overcurrent protection, system overvoltage protection, battery overvoltage protection, battery short, system short and over temperature protection.

9.16.1 Watchdog Timer

The charger includes watchdog timer to terminate charging if the charger does not receive a write ChargeVoltage() or write ChargeCurrent() command within 175 s (adjustable via REG0x01[6:5]).

When watchdog timeout occurs, all register values are kept unchanged except ChargeCurrent resets to zero. Battery charging is suspended. Write ChargeVoltage or write ChargeCurrent commands must be re-sent to reset watchdog timer and resume charging. Writing REG0x01[6:5] = 00 to disable watchdog timer also resumes charging.

9.16.2 ACOV

Once VBUS voltage is detected higher than input over-voltage threshold, SC8886S outputs low at CHRG_OK pin and disable the converter. BATFET will be turned on to supply system from battery. When VBUS voltage falls below ACOV, CHRG_OK is pulled high again and the converter resumes.

9.16.3 BATOC

When battery discharging current exceeds 1.33x or 2x of I_{DCHG}, BATOC protection is triggered. SC8886S stops switching and BATOC fault status is reported to host.

BATOC function can be disabled by writing REG0x32[1] =0.

9.16.4 ACOC

Once input overcurrent (1.33x or 2x of I_{LIM2_VTH}) is detected, ACOC protection is triggered. SC8886S stops switching and CHRG_OK is pulled down to indicate and ACOC fault status is reported to host.

ACOC function can be disabled by writing REG0x32[3] =0.

9.16.5 SYSOVP

After cell detection is finished, SYSOVP threshold is set according to cell configuration (5V for 1 cell, 12V for 2 cells, 19.5V for 3cells/4cells). Once Vsys voltage is above sysovp threshold, SYSOVP is triggered. The SC8886S will stop converter switching and SYSOVP fault is reported by setting REG0x20[4] to 1. SYSOVP latch-off fault can be cleared by writing 0 to the REG0x20[4]. After system voltage falls down, the converter starts again.

9.16.6 BATOVP

Battery over-voltage may happen when battery is removed during charging or the user plugs in a wrong battery. The BATOVP threshold is 104% of charge voltage set in REG0x05/04.

Once BATOVP event is detect, SC8886S stops switching.

9.16.7 Battery Short

If voltage at SNS2N pin falls below SYSMIN during charging, the maximum charging current is limited to 384mA.

9.16.8 System Short

Once VSYS is lower than 2.4V for 2ms deglitch time, sys short protection is triggered. SC8886S adopts hiccup protection mode which will shut down converter for 500ms and then restart. This hiccup mode will be tried continuously, if the charger restart is failed for 7 times in 90s timer, the charger will be latched off. System short fault is reported by setting REG0x20[3] =1. The charger only can be enabled again once the host writes REG0x20[3] to 0.

Sys short hiccup protection can be disabled by writing REG0x00[6] to 0.

9.16.9 Thermal Shutdown

Whenever the junction temperature exceeds the 155°C, SC8886S stops switching and stays off. When the

DATASHEET DRAFT, SOUTHCHIP CONFIDENTIAL

Copyright © 2022, Southchip Semiconductor Technology (Shanghai) Co., Ltd.

temperature falls below 135°C, SC8886S can be resumed with soft start.

9.17 I2C

9.17.1 I2C Interface

The IC features I2C interface, so the MCU or controller can control the IC flexibly. The 7-bit I2C address of the chip is 0x6B (8-bit address is 0xD6 for write command, 0xD7 for read command). The SDA and SCL pins are open drain and must be connected to the positive supply voltage via a current source or pull-up resistor. When the bus is free, both lines are HIGH. The I2C interface supports both standard mode (up to 100kbits) and fast mode (up to 400k bits with 5 kΩ pull up resistor at SCL pin and SDA pin respectively).

9.17.1.1 Data Validity

The data on the SDA line must be stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW. One clock pulse is generated for each data bit transferred.

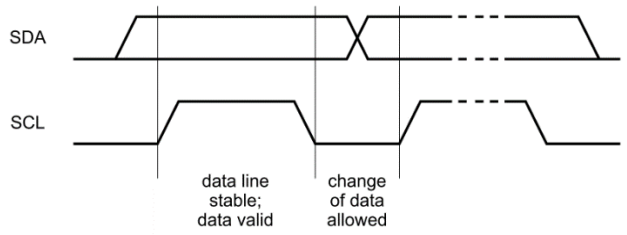


Figure 1 Bit transfer on the I2C bus

9.17.1.2 START and STOP Conditions

All transactions begin with a START (S) and are terminated by a STOP (P). A HIGH to LOW transition on the SDA line while SCL is HIGH defines a START condition. A LOW to HIGH transition on the SDA line while SCL is HIGH defines a STOP condition.

START and STOP conditions are always generated by the master. The bus is considered to be busy after the START condition. The bus is considered to be free again a certain time after the STOP condition.

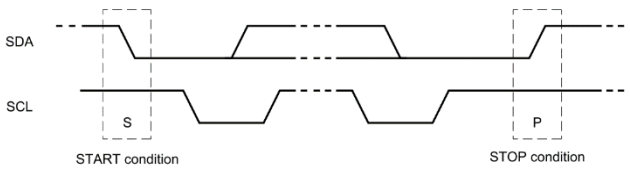


Figure 2 START and STOP conditions

9.17.1.3 Byte Format

Every byte put on the SDA line must be eight bits long. The number of bytes that can be transmitted per transfer is unrestricted. Each byte must be followed by an Acknowledge bit. Data is transferred with the Most Significant Bit (MSB) first. If a slave cannot receive or transmit another complete byte of data until it has performed some other function, for example servicing an internal interrupt, it can hold the clock line SCL LOW to force the master into a wait state. Data transfer then continues when the slave is ready for another byte of data and releases clock line SCL.

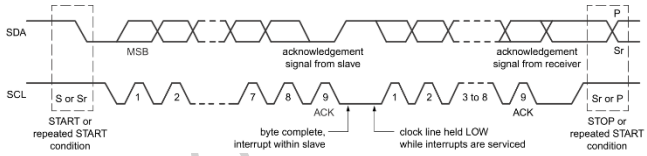


Figure 3 Data transfer on the I2C bus

9.17.1.4 Acknowledge (ACK) and Not Acknowledge (NACK)

The acknowledge takes place after every byte. The acknowledge bit allows the receiver to signal the transmitter that the byte was successfully received and another byte may be sent. During data is transferred, the master can either be the transmitter or the receiver. No matter what it is, the master generates all clock pulses, including the acknowledge ninth clock pulse.

The transmitter releases the SDA line during the acknowledge clock pulse so the receiver can pull the SDA line LOW and it remains stable LOW during the HIGH period of this clock pulse.

When SDA remains HIGH during this ninth clock pulse, this is defined as the Not Acknowledge signal. The master can then generate either a STOP condition to abort the transfer, or a repeated START condition to start a new transfer.

9.17.1.5 The slave address and R/W bit

Data transfers follow the format shown in below. After the START condition (S), a slave address is sent. This address is seven bits long followed by an eighth bit which is a data direction bit (R/W) — a 'zero' indicates a transmission (WRITE), a 'one' indicates a request for data (READ). A data transfer is always terminated by a STOP condition (P) generated by the master. However, if a master still wishes to communicate on the bus, it can generate a repeated START condition (Sr) and address another slave without first generating a STOP condition.

DATASHEET DRAFT, SOUTHCHIP CONFIDENTIAL

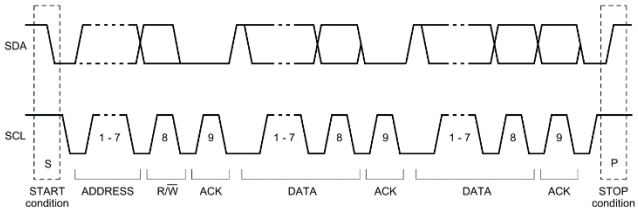


Figure 4 A complete data transfer

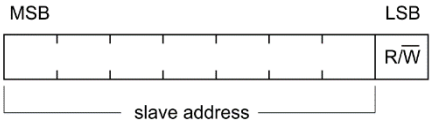


Figure 5 The first byte after the START procedure

9.17.1.6 Single Read and Write

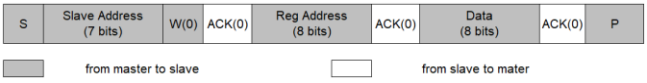


Figure 6 Single Wite

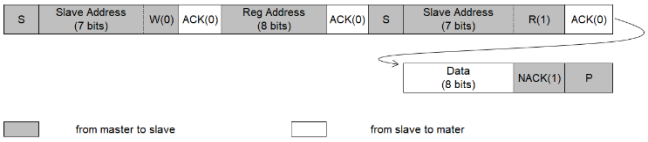


Figure 7 Single Read

If the register address is not defined, the charger IC send back NACK and go back to the idle state.

9.17.1.7 Multi-Read and Multi-Write

The IC supports multi-read and multi-write for continuous registers.

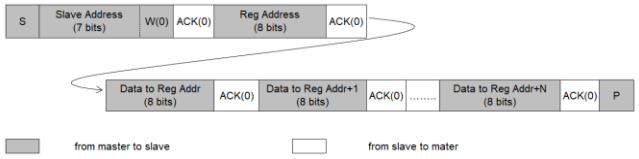


Figure 8 Multi-Write

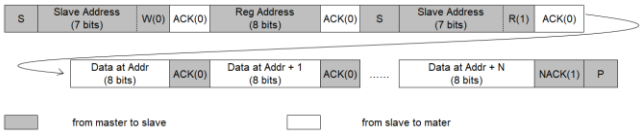


Figure 9 Multi-Read

DATASHEET DRAFT, SOUTHCHIP CONFIDENTIAL

10 Register Map (Address: 0x6B)

Addr	Register	Type	Default value @POR	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00H	Charge option0()	R/W	0x0E		SYS_SHORT_DISABLE	EN_LEARN	IADPT_GAIN	IBAT_GAIN	EN_LDO	EN_IDPM	CHRG_INHIBIT
01H		R/W	0XE7	EN_LWPWR	WDTMR_ADJ		IDPM_AUTO_DISABLE	OTG_ON_CHRGOK	EN_OOA	PWM_FREQ	LOW_PTM_RIPPLE
02H	Charge Current()	R/W	0x00								
03H		R/W	0x00	7-bit charge current setting LSB 64 mA, Range 0 mA – 8128 mA							
04H	Charge Voltage()	R/W	0x00								
05H		R/W	0x00	12-bit charge voltage setting LSB 8 mV, Default: 1S-4200mV, 2S-8400mV, 3S-12600mV, 4S-16800mV							
06H	OTG Voltage()	R/W	0x00								
07H		R/W	0x00	12-bit OTG voltage setting LSB 8 mV, Range: 3000 mV – 20800 mV							
08H	OTG Current()	R/W	0x00								
09H		R/W	0x00	7-bit OTG output current setting LSB 50 mA, Range: 0 A – 6350 mA							
0AH	VINDPM Setting()	R/W	0x00								
0BH		R/W	0x00	8-bit input voltage setting LSB 64 mV, Range: 3200 mV – 19520 mV							
0CH	Vsysmin Voltage()	R/W	0x00								
0DH		R/W	0x0E	6-Bit minimum system voltage setting LSB: 256 mV, Range: 1024 mV - 16182 mV Default: 1S-3.584V, 2S-6.144V, 3S-9.216V, 4S-12.288V							
0EH	IINREG Settting()	R/W	0x00								
0FH		R/W	0x41	7-bit Input current limit set by host LSB: 50-mA, Range: 50 mA - 6400 mA with 50mA offset							
20H	ChargerStatus()	R/W	0x00	Fault ACOV	Fault BATOC	Fault ACOC	SYSOVP_STAT	SYSshort_STAT	Fault Latchoff	Fault OTG_OVP	Fault OTG_UVP
21H		R/W	0x00	AC_STAT	ICO_Done	IN_VAP	IN_VINDPM	IN_IINDPM	IN_FCHRG	IN_PreCHRG	IN_OTG
22H	ProchotStatus()	R	0x00	STAT_VDPM	STAT_COMP	STAT_ICRIT	STAT_INORM	STAT_IDCHG	STAT_VSYS	STAT_battery_removal	STAT_Adapter_removal
23H		R	0x00		EN_PROCHOT _EXT	PROCHOT _WIDTH		PROCHOT _CLEAR		STAT_VAP_FAIL	STAT_EXIT_VAP
24H	IIN_DPM()	R	0x00								
25H		R	0x41	7-bit Input current limit in use LSB: 50-mA, Range: 50 mA - 6400 mA with 50mA offset							
26H	ADC_VBUS/PSYS()	R	0x00	8-bit Digital Output of PSYS output PSYS: Full range: 3.06 V, LSB: 12 mV							

DATASHEET DRAFT, SOUTHCHIP CONFIDENTIAL

Copyright © 2022, Southchip Semiconductor Technology (Shanghai) Co., Ltd.

27H		R	0x00	8-bit Digital Output of Input Voltage VBUS: Full range: 3.2 V - 19.52 V, LSB 64 mV							
28H	ADC_IDCHG/ICHG	R	0x00		7-bit Digital Output of Battery DisCharge Current IDCHG: Full range: 32.512 A, LSB: 256 mA						
29H		R	0x00		7-bit Digital Output of Battery Charge Current ICHG: Full range 8.128 A, LSB 64 mA						
2AH	ADC_IIN/CMPIN()	R	0x00	8-bit Digital Output of CMPIN voltage CMPIN: Full range: 3.06 V, LSB: 12 mV							
2BH		R	0x00	8-bit Digital Output of Input Current IIN: Full range: 12.75 A, LSB: 50 mA							
2CH	ADC_VSYS/VBAT()	R	0x00	8-bit Digital Output of Battery Voltage VBAT: Full range: 2.88 V to 19.2 V, LSB: 64 mV							
2DH		R	0x00	8-bit Digital Output of System Voltage VSYS: Full range: 2.88 V to 19.2 V, LSB: 64 mV							
2EH	ManufactureID()	R	0x03								
2FH	DeviceID()	R	0x66								
30H	ChargeOption1()	R/W	0x11	CMP_REF	CMP_POL	CMP_DEG		FORCE_LATCHOFF	EN_PTM	EN_SHIP_DCHG	AUTO_WAKEUP_EN
31H		R/W	0x02	EN_IBAT	EN_PROCHOT_LPWR		EN_PSYS	RSNS_RAC	RSNS_RSR	PSYS_RATIO	PTM_PINSEL
32H	ChargeOption2()	R/W	0XB7	EN_EXTILIM	EN_ICHG_IDCHG	Q2_OCP		EN_ACOC	ACOC_VTH	EN_BATOC	BATOC_VTH
33H		R/W	0x02	PKPWR_TOVLD_DEG		EN_PKPWR_IDPM	EN_PKPWR_VSYS	PKPWR_OVLD_STAT	PKPWR_RELAX_STAT	PKPWR_TMAX[1:0]	
34H	ChargeOption3()	R/W	0x30		EN_CON_VAP	OTG_VAP_MODE	IL_AVG		OTG_RANGE_LOW	BATFETOFF_HIZ	PSYS_OTG_IDCHG
35H		R/W	0x00	EN_Hiz	RESET_REG	RESET_VINDPM	EN_OTG	EN_ICO_MODE			
36H	ProchotOption0()	R/W	0x65	VSYS_TH1				VSYS_TH2		INOM_DEG	LOWER_PROCHOT_VDPM
37H		R/W	0x4A	ILIM2_VTH					ICRIT_DEG		PROCHOT_VDPM_80_90
38H	ProchotOption1()	R/W	0xA0	PROCHOT_VDPM	PROCHOT_COMP	PROCHOT_ICRIT	PROCHO_INORM	PROCHOT_IDCHG	PROCHOT_VSYS	PROCHOT_BATPRES	PROCHOT_ACOK
39H		R/W	0x81	IDCHG_VTH						IDCHG_DEG	
3AH	ADCOption()	R/W	0x00	EN_ADC_CMPIN	EN_ADC_VBUS	EN_ADC_PSYS	EN_ADC_IIN	EN_ADC_IDCHG	EN_ADC_ICHG	EN_ADC_VSYS	EN_ADC_VBAT
3BH		R/W	0x20	ADC_CONV	ADC_START	ADC_FULLSCALE					

DATASHEET DRAFT, SOUTHCHIP CONFIDENTIAL

Copyright © 2022, Southchip Semiconductor Technology (Shanghai) Co., Ltd.

Table 1 0x00H Charge Option0() Register_0 (Default value=0x0E)

Bit	Mode	Bit Name	Default value @POR	Description	Notes
7	R/W	Reserved	0	**Internal use. Don't overwrite this bit.**	
6	R/W	SYSSHORT_DIS	0	Sysshort hiccup disable bit 0: sysshort hiccup protection is enabled (default) 1: sysshort hiccup protection is disabled When this bit is set to 1, If Vsys< 2.4V, sysshort hiccup is disabled.	
5	R/W	EN_LEARN	0	Learn mode enable bit 0: learn mode is disabled (default) 1: learn mode is enabled When this bit is to 1, IC enters learn mode. The battery supply system by turning on BATFET and DCDC switching is stopped.	
4	R/W	IADPT_GAIN	0	Input current gain selection bit 0: 20x (default) 1: 40x When this bit is to set 0, the IADPT pin outputs 20X (SNS1P-SNS1N).	
3	R/W	IBAT_GAIN	1	Battery current gain selection bit 0: 8x 1: 16x (default) When this bit is set to 1, the IBAT pin outputs 16X (SNS2P-SNS2N).	
2	R/W	EN_LDO	1	BATFET LDO mode enable bit 0: LDO mode is disabled 1: LDO mode is enabled (default) When this bit is 0, the BATFET is kept fully-on, the charge current is not clamped to 384mA in the precharge phase. The host need to set proper ChargeCurrent register value.	
1	R/W	EN_IDPM	1	IINDPM enable bit 0: IINDPM loop is disabled 1: IINDPM loop is enabled (default)	
0	R/W	CHRG_INHIBIT	0	Charger enable bit 0: Charging is enabled (default) 1: charging is disabled	

DATASHEET DRAFT, SOUTHCHIP CONFIDENTIAL

Table 2 0x01H Charge Option0() Register_1(Default value=0xE7)

Bit	Mode	Bit Name	Default value @POR	Description	Notes
7	R/W	EN_LWPWR	1	Low power mode enable bit 0: performance mode 1: low power mode (default) When this bit is set to 1, IC enters low power mode automatically when only battery exists and consumes lower quiescent current. The VDRV LDO and ADC is off, but independent comparator can be enabled by corresponding control bit.	
6-5	R/W	WDT_ADJ	11	Watchdog timer adjust 00: watchdog is disabled 01: 5s 10: 88s 11: 175s (default) When watchdog timer expires, the charge current is reset to 0. Host need to write setting value to ChargeCurrent register to reset timer before it expires.	
4	R/W	IDPM_AUTO_DISABLE	0	IDPM auto disable bit 0: disabled (default) 1: enabled When this bit is set to 1, IDPM loop is disabled automatically when cell removal is detected.	
3	R/W	OTG_ON_CHRGOK	0	CHRG_OK in OTG mode enable bit 0: CHRG_OK is disabled (default) 1: CHRG_OK is enabled When this bit is set 1, CHRG_OK is internally pulled high to indicating OTG is in normal regulation.	
2	R/W	EN_OOA	1	OOA PFM enable bit 0: OOA is disabled 1: OOA is enabled (default) When this bit is set to 1, OOA out of audio PFM is enabled. IC works at least 25kHz PFM mode to avoid audio noise.	
1	R/W	PWM_FREQ	1	Frequency selection bit 0: 1200kHz 1: 800kHz (default)	
0	R/W	LOW_PTM_RIPPLE	1	Pass through low-ripple mode 0: disabled 1: enabled (default)	

DATASHEET DRAFT , SOUTHCHIP CONFIDENTIAL

Copyright © 2022, Southchip Semiconductor Technology (Shanghai) Co., Ltd.

Table 3 0x03H Charge Current() Register_1 (Default value=0x00)

Bit	Mode	Bit Name	Default value @POR	Description	Notes
7-5	R/W	Reserved	000	**Internal use. Don't overwrite this bit.**	
4	R/W	Charge current bit 6	0	0: 0 mA 1: 4096 mA	
3	R/W	Charge current bit 5	0	0: 0 mA 1: 2048 mA	
2	R/W	Charge current bit 4	0	0: 0mA 1: 1024 mA	
1	R/W	Charge current bit 3	0	0: 0 mA 1: 512 mA	
0	R/W	Charge current bit 2	0	0: 0 mA 1: 256 mA	

Table 4 0x02H Charge Current() Register_0 (Default value=0x00)

Bit	Mode	Bit Name	Default value @POR	Description	Notes
7	R/W	Charge current bit 1	0	0: 0 mA 1: 128 mA	
6	R/W	Charge current bit 0	0	0: 0 mA 1: 64 mA	
5-0	/	Reserved	00 0000	**Internal use. Don't overwrite this bit.**	

Charge current ranges from 64mA to 8128mA, with 64mA resolution. If charge current is set to 0mA, charging is disabled.

The precharge current is clamp to maximum 384mA. If 1-cell configuration is applied, the fast charge current is clamped to maximum 2A when battery voltage is between 3V and minimum system voltage.

The charge current is reset to 0 when adapter removal or cell removal is detected.

DATASHEET DRAFT , SOUTHCHIP CONFIDENTIAL

Copyright © 2022, Southchip Semiconductor Technology (Shanghai) Co., Ltd.

Table 5 0x05H Charge Voltage() Register_1 (Default value set by CELL_PRES configuration)

Bit	Mode	Bit Name	Default value @POR	Description	Notes
7	R/W	Reserved	00	**Internal use. Don't overwrite this bit.**	
6	R/W	Charge voltage bit 11	0	0: 0 mV 1: 16384 mV	
5	R/W	Charge voltage bit 10	0	0: 0 mV 1: 8192 mV	
4	R/W	Charge voltage bit 9	0	0: 0 mV 1: 4096 mV	
3	R/W	Charge voltage bit 8	0	0: 0 mV 1: 2048 mV	
2	R/W	Charge voltage bit 7	0	0: 0 mV 1: 1024 mV	
1	R/W	Charge voltage bit 6	0	0: 0 mV 1: 512 mV	
0	R/W	Charge voltage bit 6	0	0: 0 mV 1: 256 mV	

Table 6 0x04H Charge Voltage() Register_0 (Default value set by CELL_PRES configuration)

Bit	Mode	Bit Name	Default value @POR	Description	Notes
7	R/W	Charge voltage bit 4	0	0: 0 mV 1: 128 mV	
6	R/W	Charge voltage bit 3	0	0: 0 mV 1: 64 mV	
5	R/W	Charge voltage bit 2	0	0: 0 mV 1: 32 mV	
4	R/W	Charge voltage bit 1	0	0: 0 mV 1: 16 mV	
3	R/W	Charge voltage bit 0	0	0: 0 mV 1: 8 mV	
2-0	/	Reserved	00	**Internal use. Don't overwrite this bit.**	

Charge voltage ranges from 1024mV to 19200mV, with 8mV resolution. Any charge voltage command which is not among 3000mV to 19200mV is ignored. If host writes 0x0000 to charge voltage register, the charge current is reset to 0mA and charge voltage is reset to default value based on CELL_PRES pin configuration.

DATASHEET DRAFT, SOUTHCHIP CONFIDENTIAL

Table 7 0x07H OTG Voltage() Register_1 (Default value=0x00)

Bit	Mode	Bit Name	Default value @POR	Description	Notes
7-6	R/W	Reserved	00	**Internal use. Don't overwrite this bit.**	
5	R/W	OTG voltage bit 11	0	0: 0 mV 1: 16384 mV	
4	R/W	OTG voltage bit 10	0	0: 0 mV 1: 8192 mV	
3	R/W	OTG voltage bit 9	0	0: 0 mV 1: 4096 mV	
2	R/W	OTG voltage bit 8	0	0: 0 mV 1: 2048 mV	
1	R/W	OTG voltage bit 7	0	0: 0 mV 1: 1024 mV	
0	R/W	OTG voltage bit 6	0	0: 0 mV 1: 512 mV	

Table 8 0x06H OTG Voltage() Register_0 (Default value=0x00)

Bit	Mode	Bit Name	Default value @POR	Description	Notes
7	R/W	OTG voltage bit 5	0	0: 0 mV 1: 256 mV	
6	R/W	OTG voltage bit 4	0	0: 0 mV 1: 128 mV	
5	R/W	OTG voltage bit 3	0	0: 0 mV 1: 64 mV	
4	R/W	OTG voltage bit 2	0	0: 0 mV 1: 32 mV	
3	R/W	OTG voltage bit 1	0	0: 0 mV 1: 16 mV	
2	R/W	OTG voltage bit 0	0	0: 0 mV 1: 8 mV	
1-0	/	Reserved	00	**Internal use. Don't overwrite this bit.**	

OTG voltage ranges from 3000mV to 24000mV, with 8mV resolution. Any OTG voltage command which is not among 3000mV to 24000mV is ignored.

OTG DAC offset is decided by Reg0x34<2> bit.

If low OTG voltage range bit Reg0x34<2>=1, the offset is 0V, the OTG voltage ranges from 3V to 22.72V.

If low OTG voltage range bit Reg0x34<2>=0, the offset is 1.28V, the OTG voltage ranges from 4.28V to 24V.

DATASHEET DRAFT, SOUTHCHIP CONFIDENTIAL

Table 9 0x09H OTG Current() Register_1 (Default value=0x00)

Bit	Mode	Bit Name	Default value @POR	Description	Notes
7	R/W	Reserved	0	**Internal use. Don't overwrite this bit.**	
6	R/W	OTG current bit 6	0	0: 0 mA 1: 3200 mA	
5	R/W	OTG current bit 5	0	0: 0 mA 1: 1600 mA	
4	R/W	OTG current bit 4	0	0: 0 mA 1: 800 mA	
3	R/W	OTG current bit 3	0	0: 0 mA 1: 400 mA	
2	R/W	OTG current bit 2	0	0: 0 mA 1: 200 mA	
1	R/W	OTG current bit 1	0	0: 0 mA 1: 100 mA	
0	R/W	OTG current bit 0	0	0: 0 mA 1: 50 mA	

Table 10 0x08H OTG Current() Register_0 (Default value=0x00)

Bit	Mode	Bit Name	Default value @POR	Description	Notes
7-0	R/W	Reserved	0000 0000	**Internal use. Don't overwrite this bit.**	

OTG current ranges from 50mA to 6400mA, with 50mA resolution.

DATASHEET DRAFT, SOUTHCHIP CONFIDENTIAL

Table 11 0x0BH VINREG Voltage() Register_1 (Default value=0x00)

Bit	Mode	Bit Name	Default value @POR	Description	Notes
7-6	R/W	Reserved	00	**Internal use. Don't overwrite this bit.**	
5	R/W	VINREG voltage bit 7	0	0: 0 mV 1: 8192 mV	
4	R/W	VINREG voltage bit 6	0	0: 0 mV 1: 4096 mV	
3	R/W	VINREG voltage bit 5	0	0: 0 mV 1: 2048 mV	
2	R/W	VINREG voltage bit 4	0	0: 0 mV 1: 1024 mV	
1	R/W	VINREG voltage bit 3	0	0: 0 mV 1: 512 mV	
0	R/W	VINREG voltage bit 2	0	0: 0 mV 1: 256 mV	

Table 12 0x0AH VINREG Voltage() Register_0 (Default value=0x00)

Bit	Mode	Bit Name	Default value @POR	Description	Notes
7	R/W	VINREG voltage bit 1	0	0: 0 mV 1: 128 mV	
6	R/W	VINREG voltage bit 0	0	0: 0 mV 1: 64 mV	
5-0	R/W	Reserved	00 0000	**Internal use. Don't overwrite this bit.**	

VINREG voltage ranges from 3200mV to 19520mV, with 64mV resolution. There is 3.2V DC offset for VINREG Register(0x0B/0A=0x0000).

Any VINREG voltage command which is not among 3200mV to 19520mV is ignored.

DATASHEET DRAFT, SOUTHCHIP CONFIDENTIAL

Table 13 0x0DH VSYSMIN Voltage() Register_1 (Default value=0x00)

Bit	Mode	Bit Name	Default value @POR	Description	Notes
7-6	R/W	Reserved	00	**Internal use. Don't overwrite this bit.**	
5	R/W	VSYSMIN voltage bit 5	0	0: 0 mV 1: 8192 mV	
4	R/W	VSYSMIN voltage bit 4	0	0: 0 mV 1: 4096 mV	
3	R/W	VSYSMIN voltage bit 3	0	0: 0 mV 1: 2048 mV	
2	R/W	VSYSMIN voltage bit 2	0	0: 0 mV 1: 1024 mV	
1	R/W	VSYSMIN voltage bit 1	0	0: 0 mV 1: 512 mV	
0	R/W	VSYSMIN voltage bit 0	0	0: 0 mV 1: 256 mV	

Table 14 0x0CH VSYSMIN Voltage() Register_0 (Default value=0x00)

Bit	Mode	Bit Name	Default value @POR	Description	Notes
7-0	R/W	Reserved	0000 0000	**Internal use. Don't overwrite this bit.**	

VSYSMIN voltage ranges from 1024mV to 16128mV, with 256mV resolution. There is 160mV DC offset for Vsysmin register, the actual minimum system voltage is 160mV higher than Vsysmin setting value. Any vsysmin command which is not among 1024mV to 16128mV is ignored. VSYSMIN voltage is reset to default value based on CELL_PRES pin configuration.

DATASHEET DRAFT, SOUTHCHIP CONFIDENTIAL

Table 15 0x0FH Input Current() Register_1 (Default value=0x41)

Bit	Mode	Bit Name	Default value @POR	Description	Notes
7	R/W	Reserved	0	**Internal use. Don't overwrite this bit.**	
6	R/W	Input current bit 6	1	0: 0 mA 1: 3200 mA	
5	R/W	Input current bit 5	0	0: 0 mA 1: 1600 mA	
4	R/W	Input current bit 4	0	0: 0 mA 1: 800 mA	
3	R/W	Input current bit 3	0	0: 0 mA 1: 400 mA	
2	R/W	Input current bit 2	0	0: 0 mA 1: 200 mA	
1	R/W	Input current bit 1	0	0: 0 mA 1: 100 mA	
0	R/W	Input current bit 0	1	0: 0 mA 1: 50 mA	

Table 16 0x0EH Input Current () Register_0 (Default value=0x00)

Bit	Mode	Bit Name	Default value @POR	Description	Notes
7-0	R/W	Reserved	0000 0000	**Internal use. Don't overwrite this bit.**	

Input current ranges from 50mA to 6400mA, with 50mA resolution. There is 50mA DC offset for Input Current register (0x0F/0E=0x0000).

DATASHEET DRAFT, SOUTHCHIP CONFIDENTIAL

Table 17 0x20H Charge Status() Register_0 (Default value=0x00)

Bit	Mode	Bit Name	Default value @POR	Description	Notes
7	R	Fault_ACOV	0	0: no ACOV fault 1: ACOV fault occurs If fault is disappeared, this bit is reset to 0 after it is read.	
6	R	Fault_BATOC	0	0: no BATOC fault 1: BATOC fault occurs If fault is disappeared, this bit is reset to 0 after it is read.	
5	R	Fault_ACOC	0	0: no ACOC fault 1: ACOC fault occurs If fault is disappeared, this bit is reset to 0 after it is read.	
4	R/W	SYSOVP_STAT	0	0: no SYSOVP fault 1: SYSOVP fault occurs This bit is cleared by writing this bit to 0.	
3	R/W	SYSSHORT_STAT	0	0: no SYSSHORT fault 1: SYSSHORT fault occurs This bit is cleared by writing this bit to 0.	
2	R	Fault_LATCHOFF	0	0: no force-latchoff fault 1: force-latchoff fault occurs When this bit is set to 1, it only can be cleared to 0 by disable force latch-off function (Reg0x30<3>=0).	
1	R	Fault_OTG_OVP	0	0: no OTG_OVP fault 1: OTG_OVP fault occurs If fault is disappeared, this bit is reset to 0 after it is read.	
0	R	Fault_OTG_UVP	0	0: no OTG_UVP fault 1: OTG_UVP fault occurs If fault is disappeared, this bit is reset to 0 after it is read.	

DATASHEET DRAFT, SOUTHCHIP CONFIDENTIAL

Copyright © 2022, Southchip Semiconductor Technology (Shanghai) Co., Ltd.

Table 18 0x21H Charge status() Register_1 (Default value=0x00)

Bit	Mode	Bit Name	Default value @POR	Description	Notes
7	R	AC_STAT	0	Input source status bit 0: input is not present, VBUS voltage is below V_{BUS_CONV} 1: input is present, VBUS voltage is above V_{BUS_CONV}	
6	R	ICO_DONE	0	ICO status bit 0: ICO is not finished 1: ICO is finished	
5	R	IN_VAP	0	VAP status bit 0: IC does not work in VAP status. 1: IC works in VAP status.	
4	R	IN_VINDPM	0	VINDPM status bit 0: Charger is not in VINDPM status during forward mode, and not in OTG voltage regulation loop in OTG mode. 1: Charger is in VINDPM status during forward mode, or in OTG voltage regulation loop in OTG mode.	
3	R	IN_IINDPM	0	IINDPM status bit 0: Charger is not in IINDPM status during forward mode, and not in IDCHG regulation loop in OTG mode. 1: Charger is in IINDPM status during forward mode, or in IDCHG regulation loop in OTG mode.	
2	R	IN_FCHRG	0	Charger fast charge status bit 0: Charger is not in fast charge status 1: Charger is in fast charge status	
1	R	IN_PCHRG	0	Charger precharge status bit 0: Charger is not in precharge status 1: Charger is in precharge status	
0	R	IN_OTG	0	OTG status bit 0: IC is not in OTG status 1: IC is in OTG status	

DATASHEET DRAFT , SOUTHCHIP CONFIDENTIAL

Table 19 0x22H Prochot Status() Register_0 (Default value=0x00)

Bit	Mode	Bit Name	Default value @POR	Description	Notes
7	R	STAT_VDPM	0	0: VDPM /PROCHOT is not triggered 1: VDPM /PROCHOT is triggered	
6	R	STAT_COMP	0	0: Independent comparator /PROCHOT is not triggered 1: Independent comparator /PROCHOT is triggered	
5	R	STAT_ICRIT	0	0: ICRIT /PROCHOT is not triggered 1: ICRIT /PROCHOT is triggered	
4	R	STAT_INORM	0	0: INORM /PROCHOT is not triggered 1: INORM /PROCHOT is triggered	
3	R	STAT_IDCHG	0	0: IDCHG /PROCHOT is not triggered 1: IDCHG /PROCHOT is triggered	
2	R	STAT_VSYS	0	0: VSYS /PROCHOT is not triggered 1: VSYS /PROCHOT is triggered	
1	R	STAT_Battery_Removal	0	0: Battery_Removal /PROCHOT is not triggered 1: Battery_Removal /PROCHOT is triggered When CELL_PRES is below VCELL_REMOVAL, battery removal is detected, one-shot /PROCHOT is asserted.	
0	R	STAT_Adapter_Removal	0	0: Adapter removal /PROCHOT is not triggered 1: Adapter removal /PROCHOT is triggered When VBUS is below VBUS_CONV, adapter removal is detected, one-shot /PROCHOT is asserted.	

DATASHEET DRAFT, SOUTHCHIP CONFIDENTIAL

Table 20 0x23H Prochot Status() Register_1 (Default value=0xA8)

Bit	Mode	Bit Name	Default value @POR	Description	Notes
7	/	Reserved	1	**Internal use. Don't overwrite this bit.**	
6	R/W	EN_PROCHOT_EXT	0	/PROCHOT extension mode bit 0: disable (default) 1: enable	
5-4	R/W	PROCHOT_WIDTH	10	/PROCHOT pulse width selection bit 00: 100μs 01: 1ms 10: 10ms (default) 11: 5ms	
3	R/W	PROCHOT_CLEAR	1	/PROCHOT clear bit 0: clear /PROCHOT and drive /PROCHOT to high 1: idle (default) When extension mode is selected(Reg23<6>=1), /PROCHOT is kept pull-down until host to write this bit to 0. When /PROCHOT is cleared, this bit is reset to 1.	
2	/	Reserved	0	**Internal use. Don't overwrite this bit.**	
1	R	STAT_VAP_FAIL	0	VAP fail status bit 0: VAP is not failed 1: VAP failed status When reversed VAP mode is initialed, if VBUS is not loaded to the setting voltage successfully, the number of failures is counted. If conservative failure number exceeds 7 times, this bit is set to 1 and VAP mode is latched off until host write 0 to clear latchoff.	
0	R/W	STAT_EXIT_VAP	0	VAP exit status bit 0: IC is not in VAP exit status 1: IC is in VAP exit status Once IN_VAP bit toggles from 1 to 0 by disable VAP or charger fault. This bit is set to 1. Host need to write 0 to clear it.	

DATASHEET DRAFT, SOUTHCHIP CONFIDENTIAL

Copyright © 2022, Southchip Semiconductor Technology (Shanghai) Co., Ltd.

Table 21 0x25H IN_DPM Current() Register_1 (Default value=0x41)

Bit	Mode	Bit Name	Default value @POR	Description	Notes
7	R/W	Reserved	0	**Internal use. Don't overwrite this bit.**	
6	R/W	IINDPM current bit 6	1	0: 0 mA 1: 3200 mA	
5	R/W	IINDPM current bit 5	0	0: 0 mA 1: 1600 mA	
4	R/W	IINDPM current bit 4	0	0: 0 mA 1: 800 mA	
3	R/W	IINDPM current bit 3	0	0: 0 mA 1: 400 mA	
2	R/W	IINDPM current bit 2	0	0: 0 mA 1: 200 mA	
1	R/W	IINDPM current bit 1	0	0: 0 mA 1: 100 mA	
0	R/W	IINDPM current bit 0	1	0: 0 mA 1: 50 mA	

Table 22 0x24H IN_DPM Current() Register_0 (Default value=0x00)

Bit	Mode	Bit Name	Default value @POR	Description	Notes
7-0	R/W	Reserved	0000 0000	**Internal use. Don't overwrite this bit.**	

If ICO is finished, the actual input current limit programmed in the register is updated to the IIN_DPM register. There is 50mA DC offset for Input Current register (0x25/24=0x0000).

DATASHEET DRAFT, SOUTHCHIP CONFIDENTIAL

Table 23 0x26H ADC_PSYS() Register

Bit	Mode	Bit Name	Default value @POR	Description	Notes
7-0	R	ADC_PSYS	0000 0000	8-bit Digital output of PSYS voltage LSB: 12mV Offset: 0mV Full Range: 3.06V	

Table 24 0x27H ADC_VBUS() Register

Bit	Mode	Bit Name	Default value @POR	Description	Notes
7-0	R	ADC_VBUS	0000 0000	8-bit Digital output of VBUS voltage LSB: 64mV Offset: 3.2V Full Range: 19.52V	

DATASHEET DRAFT, SOUTHCHIP CONFIDENTIAL

Table 25 0x28H ADC_IDCHG() Register

Bit	Mode	Bit Name	Default value @POR	Description	Notes
7-0	R	ADC_IDCHG	0000 0000	8-bit Digital output of battery discharge current IDCHG LSB: 256mA Offset: 0mA Full Range: 32.512A	

Table 26 0x29H ADC_ICHG() Register

Bit	Mode	Bit Name	Default value @POR	Description	Notes
7-0	R	ADC_ICHG	0000 0000	8-bit Digital output of battery charge current ICHG LSB: 64mA Offset: 0mA Full Range: 8.128A	

DATASHEET DRAFT, SOUTHCHIP CONFIDENTIAL

Copyright © 2022, Southchip Semiconductor Technology (Shanghai) Co., Ltd.

Table 27 0x2AH ADC_CMPIN() Register

Bit	Mode	Bit Name	Default value @POR	Description	Notes
7-0	R	ADC_CMPIN	0000 0000	8-bit Digital output of CMPIN voltage LSB: 12mV Offset: 0mV Full Range: 3.06V	

Table 28 0x2BH ADC_IIN() Register

Bit	Mode	Bit Name	Default value @POR	Description	Notes
7-0	R	ADC_IN	0000 0000	8-bit Digital output of input current IBUS LSB: 50mA Offset: 0mA Full Range: 6.35A	

DATASHEET DRAFT, SOUTHCHIP CONFIDENTIAL

Copyright © 2022, Southchip Semiconductor Technology (Shanghai) Co., Ltd.

Table 29 0x2CH ADC_VBAT() Register

Bit	Mode	Bit Name	Default value @POR	Description	Notes
7-0	R	ADC_VBAT	0000 0000	8-bit Digital output of battery voltage VBAT LSB: 64mV Offset: 2.88V Full Range: 19.2V	

Table 30 0x2DH ADC_VSYS() Register

Bit	Mode	Bit Name	Default value @POR	Description	Notes
7-0	R	ADC_VSYS	0000 0000	8-bit Digital output of system voltage VSYS LSB: 64mV Offset: 2.88V Full Range: 19.2V	

DATASHEET DRAFT, SOUTHCHIP CONFIDENTIAL

Copyright © 2022, Southchip Semiconductor Technology (Shanghai) Co., Ltd.

Table 31 0x2EH Manufacture ID() Register

Bit	Mode	Bit Name	Default value @POR	Description	Notes
7-0	R	Manufacture ID	0000 0011	**SC8886S: 0x03H. Internal use. Don't overwrite this bit.**	

Table 32 0x2FH Device ID() Register

Bit	Mode	Bit Name	Default value @POR	Description	Notes
7-0	R	Device ID	0110 0110	SC8886S: 0x66H	

DATASHEET DRAFT, SOUTHCHIP CONFIDENTIAL

Table 33 0x30H Charge Option1() Register_0 (Default value=0x11)

Bit	Mode	Bit Name	Default value @POR	Description	Notes
7	R/W	CMP_REF	0	Independent comparator reference 0: 2.3V (default) 1: 1.2V	
6	R/W	CMP_POL	0	Independent comparator polarity 0: CMPOUT outputs low when CMPIN is above threshold (default), 100mV hysteresis 1: CMPOUT outputs low when CMPIN is below threshold (default), no hysteresis	
5-4	R/W	CMP_deg	01	Independent comparator deglitch time 00: disable 01: 1μs (default) 10: 2ms 11: 5s	
3	R/W	EN_Force_latchoff	0	Force_latchoff enable bit 0: disable (default) 1: enable When this bit is set to 1, when CMPOUT outputs low, the converter is latchoff.	
2	R/W	EN_PTM	0	Pass through mode enable bit 0: disable (default) 1: enable	
1	R/W	EN_SHIP_DCHG	0	Shipping mode mode enable bit 0: disable (default) 1: enable When this bit is set to 1, a 30mA discharging current is pulled down from SRN pin, after 120ms, the discharging current is stopped and this bit is reset to 0.	
0	R/W	EN_AUTO_WAKEUP	1	Auto wakeup mode enable bit 0: disable 1: enable (default) When this bit is set to 1, if a battery which is below VSYSMIN voltage, the charger will charge the battery with 128mA for 30min, when battery is above VSYSMIN voltage or 30-min timer expired, the auto-wakeup is finished.	

DATASHEET DRAFT, SOUTHCHIP CONFIDENTIAL

Copyright © 2022, Southchip Semiconductor Technology (Shanghai) Co., Ltd.

Table 34 0x31H Charge Option1() Register_1 (Default value=0x02)

Bit	Mode	Bit Name	Default value @POR	Description	Notes
7	R/W	EN_IBAT	0	Battery charge and discharge current monitor IBAT output enable 0: disable (default) 1: enable	
6-5	R/W	EN_PROCHOT_LPWR	0	Independent comparator enable bit in low power mode 00: disable (default) 01: Reserved 10: enable CMPOUT trigger /PROCHOT (default) 11: Reserved	
4	R/W	EN_PSYS	0	System power monitor PSYS output enable 0: disable (default) 1: enable	
3	R/W	RSNS_RS1	0	Input current sense resistor 0: 10mΩ (default) 1: 5mΩ	
2	R/W	RSNS_RS2	0	Battery current sense resistor 0: 10mΩ (default) 1: 5mΩ	
1	R/W	PSYS_RATIO	1	PSYS current ratio selection 0: 0.25μA/W 1: 1μA/W (default)	
0	R/W	PTM_PINSEL	0	ILIM_HIZ pin function selection bit 0: charger enters HIZ mode when ILIM_HIZ is pulled down 1: charger enters PTM mode when ILIM_HIZ is pulled down	

DATASHEET DRAFT, SOUTHCHIP CONFIDENTIAL

Table 35 0x32H Charge Option2() Register_0 (Default value=0xB7)

Bit	Mode	Bit Name	Default value @POR	Description	Notes
7	R/W	EN_EXTLIM	1	ILIM_HIZ pin enable function 0: disable ILIM_HIZ, the input current limit is set by internal register 1: enable ILIM_HIZ, the input current limit is set by the lower value of internal register and ILIM_HIZ setting(default)	
6	R/W	EN_ICHG_IDCHG	0	IBAT pin direction selection 0: IBAT pin outputs discharging current (default) 1: IBAT pin outputs charging current	
5	R/W	Q2_OCP_VTH	1	Q2_OCP threshold 0: 210mV 1: 150mV (default)	
4	/	Reserved	1	**Internal use. Don't overwrite this bit.**	
3	R/W	EN_ACOC	0	0: disable ACOC(default) 1: enable ACOC	
2	R/W	ACOC_VTH	1	ACOC threshold 0: 133%*ILIM2 1: 200%*ILIM2 (default)	
1	R/W	EN_BATOC	1	0: disable BATOC 1: enable BATOC (default)	
0	R/W	BATOC_VTH	1	BATOC threshold 0: 133%*IDCHG_VTH 1: 200%* IDCHG_VTH (default)	

DATASHEET DRAFT, SOUTHCHIP CONFIDENTIAL

Table 36 0x33H Charge Option2() Register_1 (Default value=0x02)

Bit	Mode	Bit Name	Default value @POR	Description	Notes
7-6	R/W	PKPWR_TOVLD_DEG	00	Overload cycle time in peak power mode 00: 1ms (default) 01: 2ms 10: 10ms 11: 20ms	
5	R/W	EN_PKPWR_IDPM	0	Peak power mode enabled by IDPM 0: disable (default) 1: enable	
4	R/W	EN_PKPWR_VSYS	0	Peak power mode enabled by VSYS voltage 0: disable (default) 1: enable	
3	R/W	PKPWR_OVLD_STAT	0	Peak power mode overload cycle status 0: not in overload cycle 1: in overload cycle	
2	R/W	PKPWR_RELAX_STAT	0	Peak power mode relax cycle status 0: not in relax cycle 1: in relax cycle	
1-0	R/W	PKPWR_TMAX	10	Peak power cycle total time 00: 5ms 01: 10ms 10: 20ms (default) 11: 40ms	

DATASHEET DRAFT, SOUTHCHIP CONFIDENTIAL

Table 37 0x34H Charge Option3() Register_0 (Default value=0x30)

Bit	Mode	Bit Name	Default value @POR	Description	Notes
7	/	Reserved	0	**Internal use. Don't overwrite this bit.**	
6	R/W	EN_CON_VAP	0	0: disable (default) 1: enable When this bit is set to 1, another conservative way to trigger /PROCHOT is activated. Once VBUS is below 3.2V and VSYS<VSYS_TH1, /PROCHOT is also triggered.	
5	R/W	OTG_VAP_MODE	1	OTG pin function setting 0: OTG pin is used as VAP mode enable pin 1: OTG pin is used as OTG mode enable pin (default)	
4-3	R/W	IL_AVG	10	Inductor average current clamp setting: 00: 6A 01: 10A 10: 15A (default) 11: disable	
2	R/W	OTG_RANGE_LOW	0	OTG outputs offset setting 0: offset is 1.28V, OTG voltage ranges from 4.28V-20.8V(default) 1: offset is 0V, OTG voltage ranges from 3V-19.52V	
1	R/W	BATFETOFF_HIZ	0	BATFET control in HIZ mode 0: BATFET on during HIZ mode(default) 1: BATFET off during HIZ mode	
0	R/W	PSYS_OTG_IDCHG	0	PSYS function in OTG mode 0: PSYS indicates system power(default) 1: PSYS indicates total battery discharge power	

DATASHEET DRAFT, SOUTHCHIP CONFIDENTIAL

Table 38 0x35H Charge Option3() Register_1 (Default value=0x00)

Bit	Mode	Bit Name	Default value @POR	Description	Notes
7	R/W	EN_HIZ	0	HIZ mode enable control 0: disable (default) 1: enable	
6	R/W	RESET_REG	0	Reset register 0: idle (default) 1: reset all register When this bit is set to 1, all register is reset to default value except VINDPM. VSYSMIN is reset to 1S setting and charge voltage is reset to default value based on CELL_PRES. This bit goes back to 0 after register reset.	
5	R/W	RESET_VINDPM	0	Reset VINDPM 0: disable (default) 1: enable When this bit is set to 1, converter is stopped and charger detect the VBUS voltage and set a new value to VINDPM register. Then this bit goes back to 0 and converter resumes to switching.	
4	R/W	EN_OTG	0	OTG control bit 0: disable (default) 1: enable	
3	R/W	EN_ICO_MODE	0	ICO control bit 0: disable(default) 1: enable	
2-0	/	Reserved	000	**Internal use. Don't overwrite this bit.**	

DATASHEET DRAFT, SOUTHCHIP CONFIDENTIAL

Table 39 0x36H Prochot Option0() Register_0 (Default value=0x65)

Bit	Mode	Bit Name	Default value @POR	Description	Notes
7-4	R/W	VSYS_TH1	0110	VSYS threshold to trigger forward discharging VBUS in VAP mode 2-4s battery 0000-1111: 5.9V-7.4V with 0.1V step size. 1s battery 0000-0111: 3.1V-3.8V with 0.1V step size 1000-1111: 3.1V-3.8V with 0.1V step size	
3-2	R/W	VSYS_TH2	01	VSYS threshold to trigger /PROCHOT 2-4s battery 00: 5.9V 01: 6.2V (default) 10: 6.5V 11: 6.8V 1s battery 00: 3.1V 01: 3.3V (default) 10: 3.5V 11: 3.7V	
1	R/W	INORM_DEG	0	INROM trigger /PROCHOT deglitch time 0: 1ms (default) 1: 50ms	
0	R/W	LOWER_PROCHOT_VDPM	1	Enable lower VINDPM threshold to trigger /PROCHOT 0: 100%*VINDPM 1: lower threshold set by Reg0x37<0> (default)	

DATASHEET DRAFT, SOUTHCHIP CONFIDENTIAL

Table 40 0x37H Prochot Option1() Register_1 (Default value=0x4A)

Bit	Mode	Bit Name	Default value @POR	Description	Notes
7-3	R/W	ILIM2_VTH	0100 1	ILIM2 threshold 00001-11001: 110%-230%, step 5% 11010-11110: 250%-450%, step 50% 11111: ignored 01001: 150% (default) The ILIM2 is the percentage of IDPM setting by 0x0F/0x0E	
2-1	R/W	ICRIT_DEG	01	ICRIT trigger /PROCHOT deglitch time 00: 15μs 01: 100μs (default) 10: 400μs 11: 800μs	
0	R/W	PROCHOT_VDPM_80_90	0	Lower threshold of PROCHOT_VDPM comparator 0: 80%*VINDPM (default) 1: 90%*VINDPM	

DATASHEET DRAFT, SOUTHCHIP CONFIDENTIAL

Table 41 0x38H Prochot Option1() Register_0 (Default value=0XA0)

Bit	Mode	Bit Name	Default value @POR	Description	Notes
7	R/W	EN_PROCHOT_VDPM	0	VDPM triggers /PROCHOT 0: disable (default) 1: enable	
6	R/W	EN_PROCHOT_COMP	0	Comparator triggers /PROCHOT 0: disable (default) 1: enable	
5	R/W	EN_PROCHOT_ICRIT	1	ICRIT triggers /PROCHOT 0: disable 1: enable (default)	
4	R/W	EN_PROCHOT_INORM	0	INORM triggers /PROCHOT 0: disable (default) 1: enable	
3	R/W	EN_PROCHOT_IDCHG	0	IDCHG triggers /PROCHOT 0: disable (default) 1: enable	
2	R/W	EN_PROCHOT_VSYS	0	VSYS triggers /PROCHOT 0: disable (default) 1: enable	
1	R/W	EN_PROCHOT_Battery_removal	0	Battery removal triggers /PROCHOT 0: disable (default) 1: enable	
0	R/W	EN_PROCHOT_Adapter_removal	0	Adapter removal triggers /PROCHOT 0: disable (default) 1: enable	

DATASHEET DRAFT, SOUTHCHIP CONFIDENTIAL

Table 42 0x39H Prochot Option1() Register_1 (Default value=0x81)

Bit	Mode	Bit Name	Default value @POR	Description	Notes
7-2	R/W	IDCHG_VTH	1000 00	IDCHG threshold 000001-111111: 0-32256mA, step 512mA. 100000: 16384 (default) There is 128mA offset. If the register value is 000000b, the /PROCHOT is always triggered.	
1-0	R/W	IDCHG_DEG	01	IDCHG triggers /PROCHOT deglitch time 00: 1.6ms 01: 100µs (default) 10: 6ms 11: 12ms	

DATASHEET DRAFT, SOUTHCHIP CONFIDENTIAL

Copyright © 2022, Southchip Semiconductor Technology (Shanghai) Co., Ltd.

Table 43 0x3AH ADC Option () Register_0 (Default value=0x00)

Bit	Mode	Bit Name	Default value @POR	Description	Notes
7	R/W	EN_ADC_CMPIN	0	0: disable (default) 1: enable	
6	R/W	EN_ADC_VBUS	0	0: disable (default) 1: enable	
5	R/W	EN_ADC_PSYS	0	0: disable (default) 1: enable	
4	R/W	EN_ADC_IIN	0	0: disable (default) 1: enable	
3	R/W	EN_ADC_IDCHG	0	0: disable (default) 1: enable	
2	R/W	EN_ADC_ICHG	0	0: disable (default) 1: enable	
1	R/W	EN_ADC_VSYS	0	0: disable (default) 1: enable	
0	R/W	EN_ADC_VBAT	0	0: disable (default) 1: enable	

DATASHEET DRAFT, SOUTHCHIP CONFIDENTIAL

Copyright © 2022, Southchip Semiconductor Technology (Shanghai) Co., Ltd.

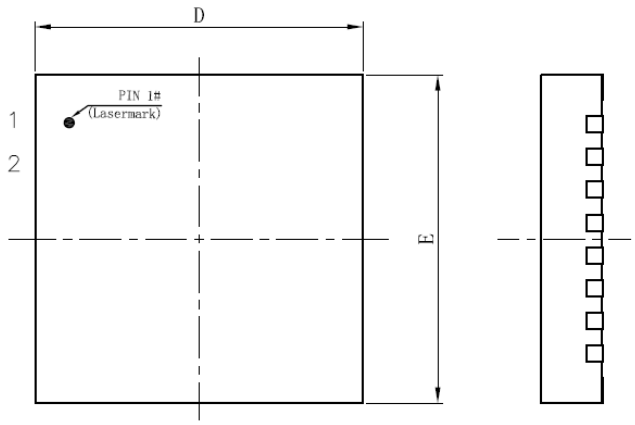
Table 44 0x3BH ADC Option1() Register_1 (Default value=0x20)

Bit	Mode	Bit Name	Default value @POR	Description	Notes
7	R/W	ADC_CONV	0	ADC conversion control 0: one shot mode 1: continuous mode every 1s	
6	R/W	ADC_START	0	ADC conversion start 0: no ADC conversion 1: Start ADC conversion and goes back to 0 after one-shot conversion is finished.	
5-0	/	Reserved	10 0000	**Internal use. Don't overwrite this bit.**	

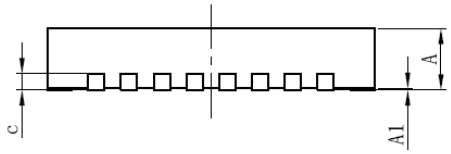
DATASHEET DRAFT, SOUTHCHIP CONFIDENTIAL

MECHANICAL DATA

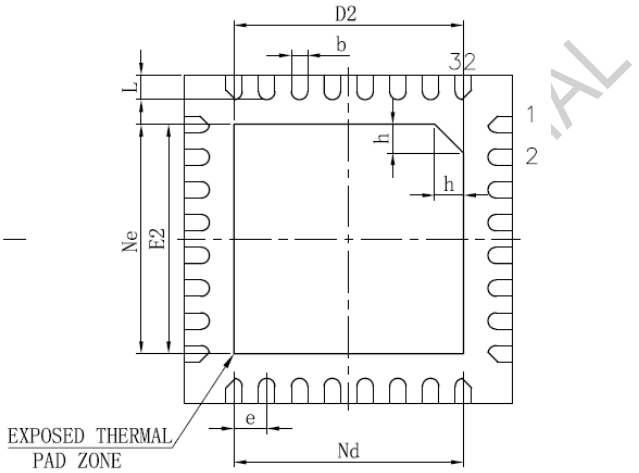
QFN32L (0404x0.75-0.4)



TOP VIEW



SIDE VIEW

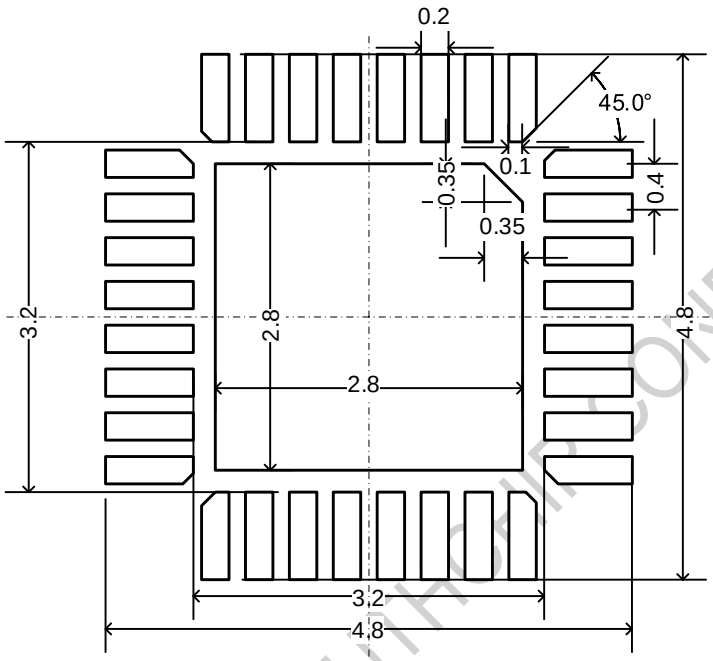


SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0	0.02	0.05
b	0.15	0.20	0.25
c	0.18	0.20	0.25
D	3.90	4.00	4.10
D2	2.70	2.80	2.90
e	0.40BSC		
Ne	2.80BSC		
Nd	2.80BSC		
E	3.90	4.00	4.10
E2	2.70	2.80	2.90
L	0.25	0.30	0.35
h	0.30	0.35	0.40
L/F载体尺寸	122X122		

DATASHEET DRAFT, S
AL

RECOMMEND FOOTPRINT

QFN32L (0404x0.75-0.4)



NOTES:

A. All linear dimensions are in millimeters

B. Publication IPC-7351 is recommended for alternate designs

C. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad

DATASHEET DRAFT, SOUTHCHIP CONFIDENTIAL