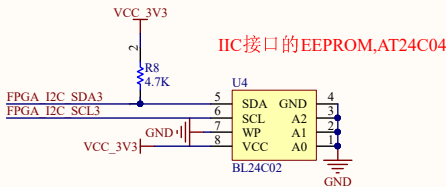
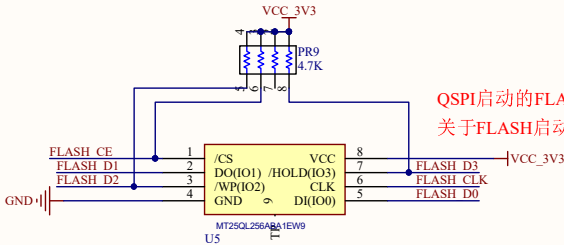
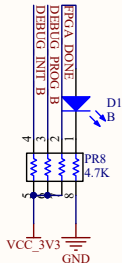
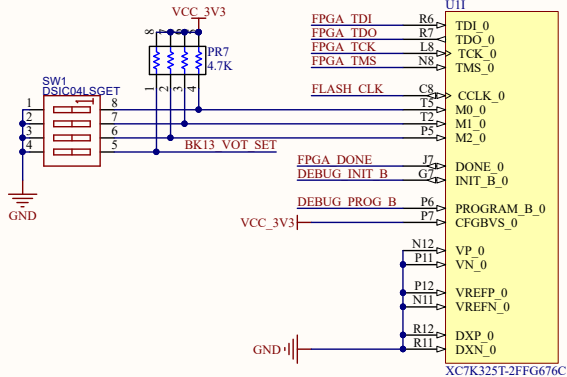


KINTEX-7芯片的调试接口部分

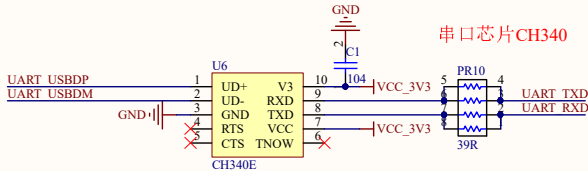


IIC接口的EEPROM,AT24C04

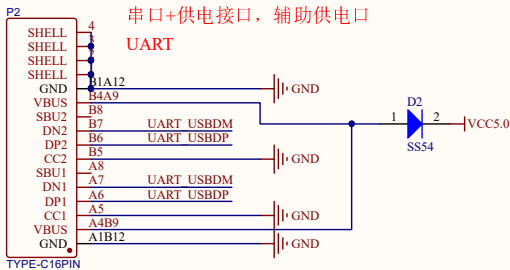


QSPI启动的FLASH存储器

关于FLASH启动请查看板子背面丝印说明



串口芯片CH340

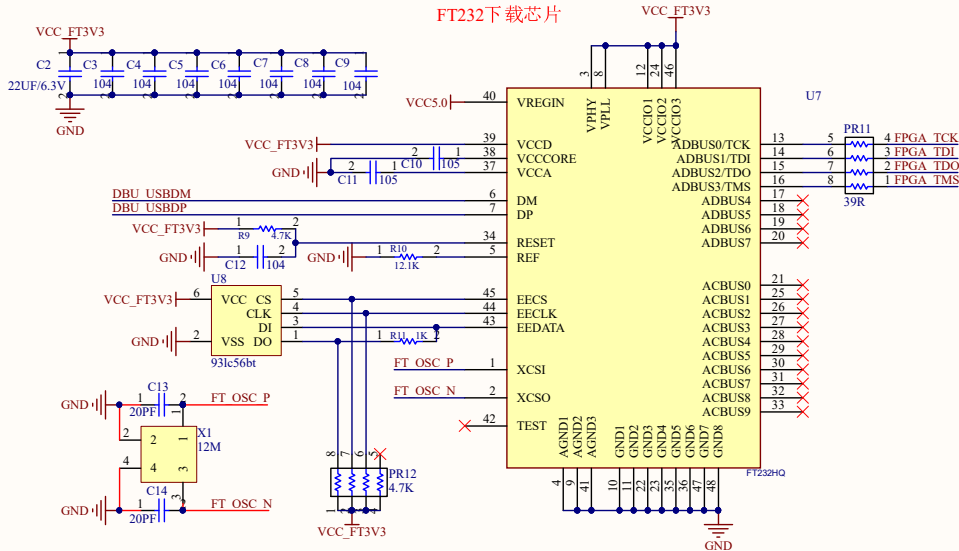
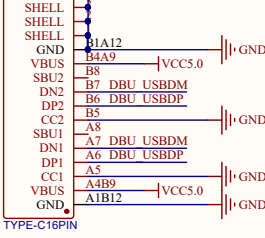


串口+供电接口, 辅助供电口

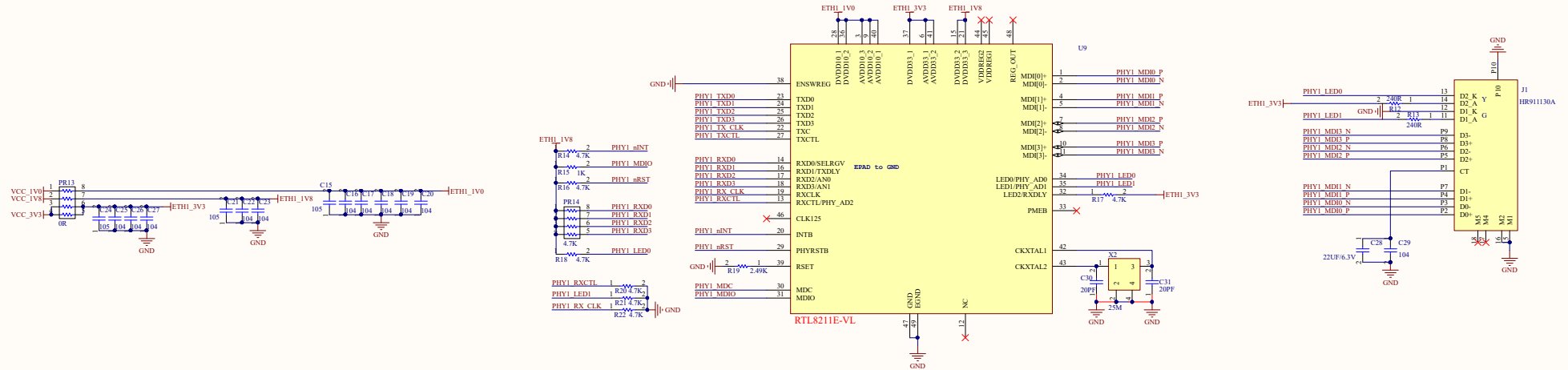
UART

调试+供电接口, 主供电口

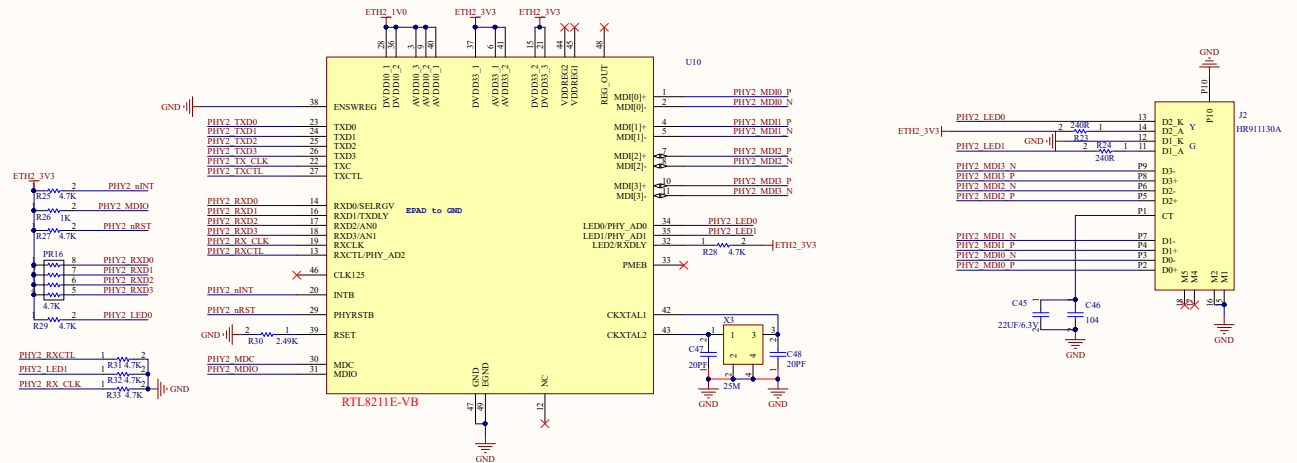
DEBUG



1.8V电平标准IO的千兆网PHY芯片

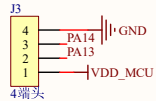


3.3V电平标准的千兆网PHY芯片

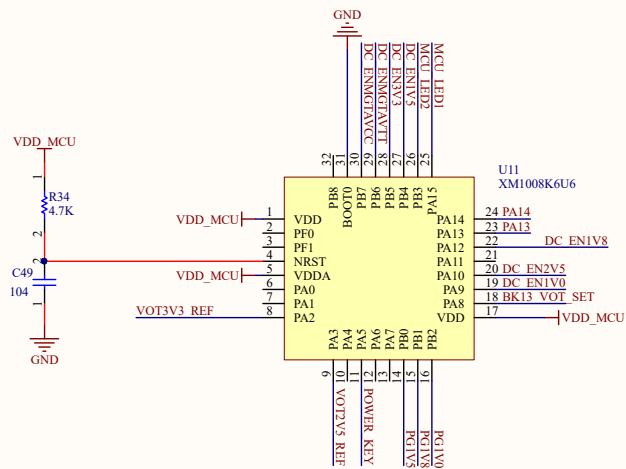


3.3V供电IO实际也可以使用VL后缀，实际需要调RGMII的IO Delay

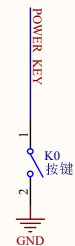
MCU的SWD调试口



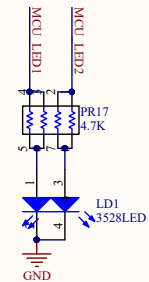
用于控制电源芯片上电顺序的ARM芯片



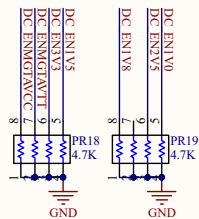
长按给FPGA各路电源上电按钮



MCU状态输出指示灯



所有控制电源使能信号必须下拉保证稳定



最大1080P@30HZ，60HZ时超范围但可以使用，不推荐VCC_3V3

The diagram illustrates the HDMI connection between the SHIELD M03 and the SHIELD M02. The SHIELD M03 is on the left, and the SHIELD M02 is on the right. The connection includes a 4.7k pull-up resistor on the VCC_HDMI1_OUT line and a 1k pull-down resistor on the VCC_3V3 line. The data lines are connected to the PR22 30R and PR23 30R components on the SHIELD M02.

SHIELD M03 Pin	SHIELD M03 Label	SHIELD M02 Pin	SHIELD M02 Label
23	SHELL4	23	GND
21	SHELL2	21	GND
19	HP DET	19	GND
18	+5V	18	VCC_HDMI1_OUT
17	GND	17	GND
16	DDC DATA	16	GND
15	DDC CLK	15	GND
14	NC	14	GND
13	CE Remote	13	HDMI1 CEC
12	CK-	12	HDMI1 CLK N
11	CK+	11	HDMI1 CLK P
10	CK Shield	10	HDMI1 DATA0 N
9	D0-	9	HDMI1 DATA0 P
8	D0 Shield	8	HDMI1 DATA1 N
7	D1-	7	HDMI1 DATA1 P
6	D1 Shield	6	HDMI1 DATA2 N
5	D2-	5	HDMI1 DATA2 P
4	D2 Shield	4	GND
3	SHELL1	3	GND
2	SHELL3	2	GND

The SHIELD M02 also includes two 30R resistors (PR22 and PR23) connected to the VCC_3V3 line.

Pin connections for RCLAMP0524P_C293965:

Pin Header	Pin	Signal	Direction
D4	1	HDMI2 DCLK N	IN
	2	HDMI2 DCLK P	IN
	3	HDMI2 DATA0 N	IN
	5	HDMI2 DATA0 P	IN
D5	1	HDMI2 DATA1 N	IN
	2	HDMI2 DATA1 P	IN
	3	HDMI2 DATA2 N	IN
	5	HDMI2 DATA2 P	IN

Ground connections are shown on both sides of the pin headers.

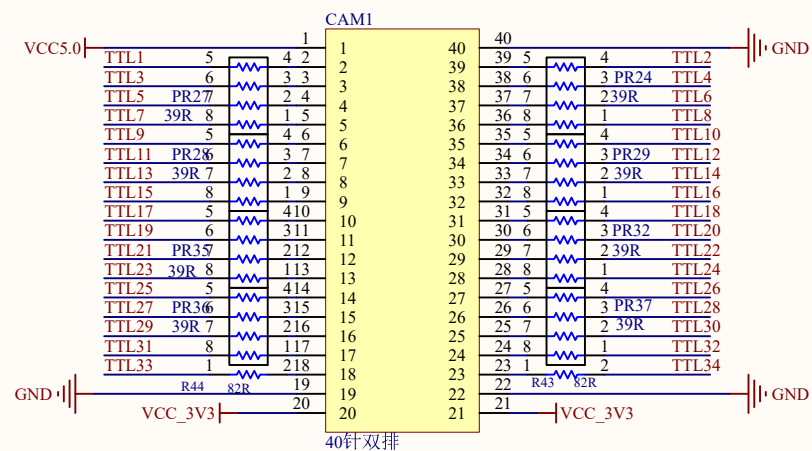
Pin 1: HDMI1_CLK N
Pin 2: HDMI1_CLK P
Pin 3: HDMI1_DATA0 N
Pin 4: HDMI1_DATA0 P
Pin 5: D7

Pin 10: HDMI1_CLK N
Pin 9: HDMI1_CLK P
Pin 8: HDMI1_DATA0 N
Pin 6: HDMI1_DATA0 P
Pin 7: RCLAMP0524P_C293965

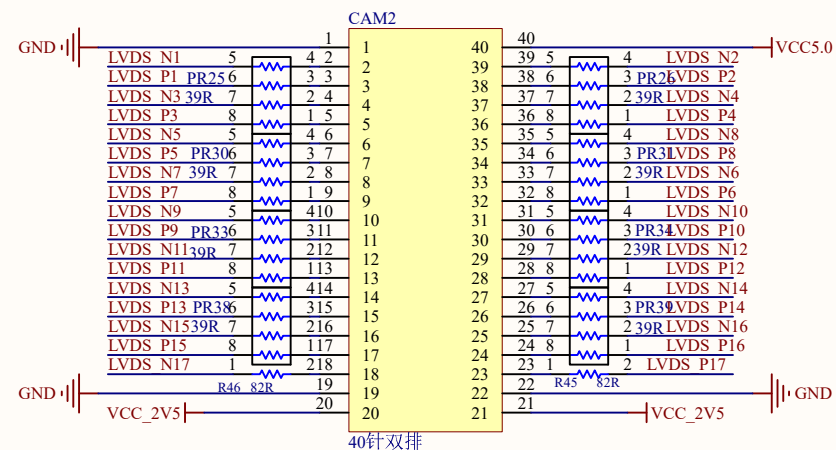
Pin 1: HDMI1_DATA1 N
Pin 2: HDMI1_DATA1 P
Pin 3: HDMI1_DATA2 N
Pin 4: HDMI1_DATA2 P
Pin 5: D8

Pin 10: HDMI1_DATA1 N
Pin 9: HDMI1_DATA1 P
Pin 8: HDMI1_DATA2 N
Pin 7: HDMI1_DATA2 P
Pin 6: HDMI1_DATA2 P
Pin 7: RCLAMP0524P_C293965

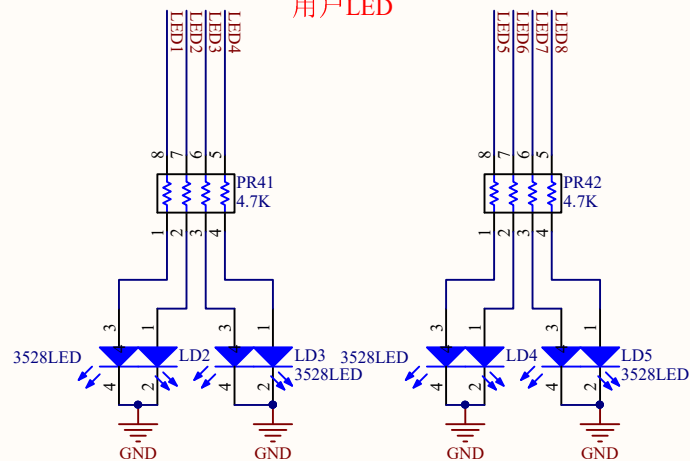
BANK16扩展出来的3.3V标准IO



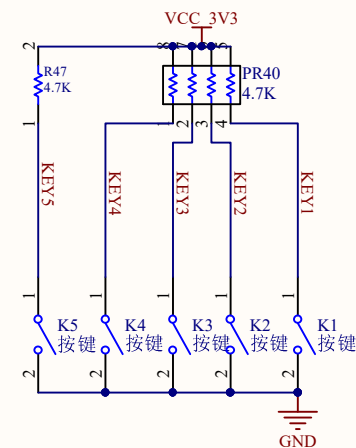
BANK13扩展出来的2.5/3.3V可调IO，支持LVDS（仅2.5V）



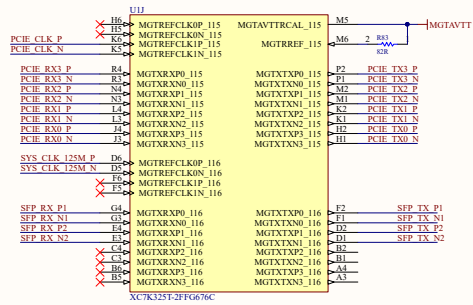
用户LED



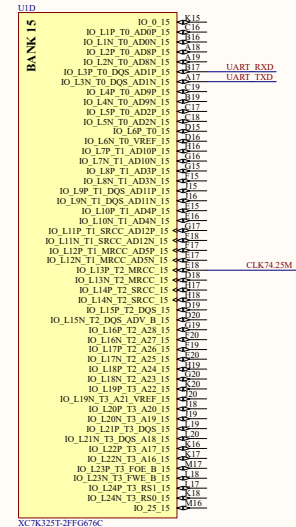
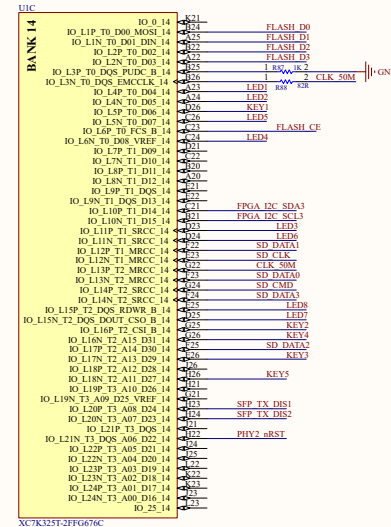
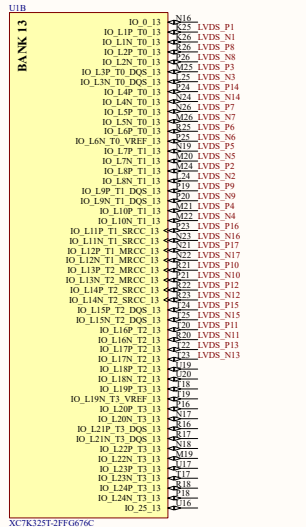
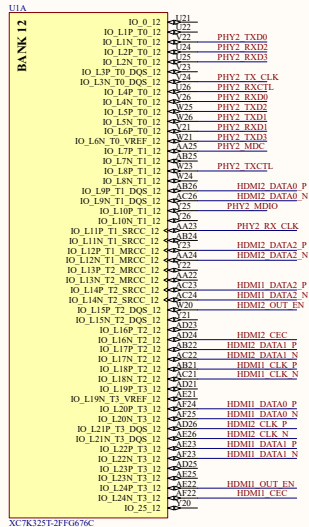
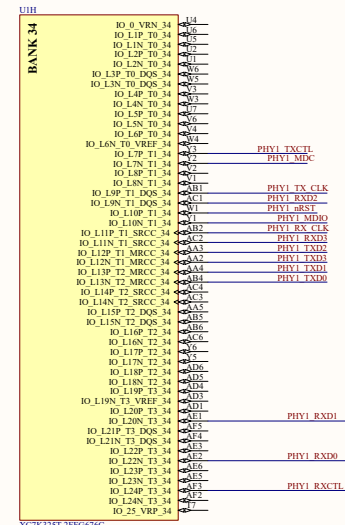
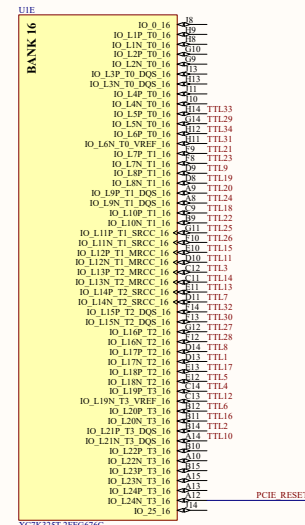
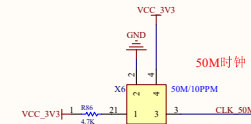
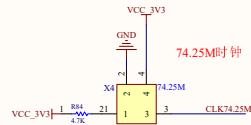
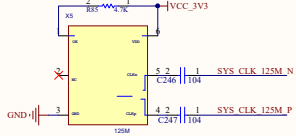
用户按钮

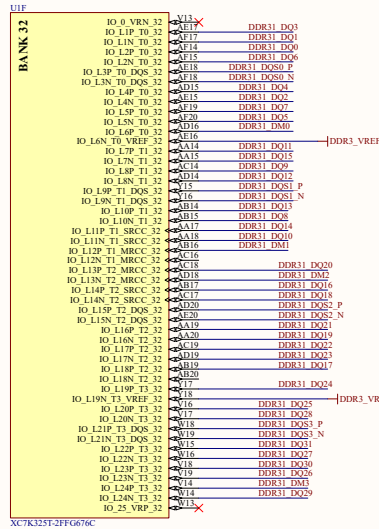
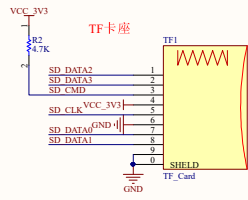


高速收发器BANK

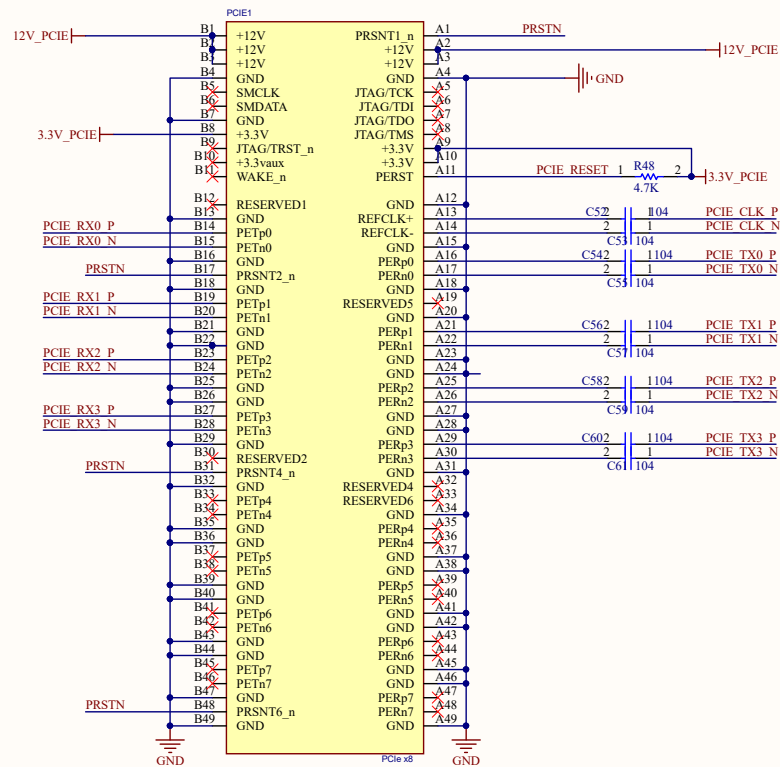


如果用户需要使用万兆以太网光通信功能，需将这个晶振更换为156.25Mhz 125M差分高速收发器参考时钟（默认出货125M）





PCIE金手指，使用X8宽度，实际是X4位宽



[illegible]

The schematic diagram illustrates the input stage of the 74VHC00, featuring a series of inverters (C150 to C170). A ground connection is established at C155. Power supply connections are provided at C150 (22uF/6.3V), C155 (22uF/6.3V), and C169 (VCC_3V3).

丁调

PCIE插槽12V转5V电源

[illegible]

