|  |  |
| --- | --- |
|  | **Karlsruhe Institute of Technology**  Institut für Technik der Informationsverarbeitung (ITIV)  Head of Institute  Prof. Dr.-Ing. Dr. h. c. Jürgen Becker  Prof. Dr.-Ing. Eric Sax  Prof. Dr. rer. nat. Wilhelm Stork |

**Digital Hardware Design Laboratory**

**Exercise: 1**

**Group: 11**

**Names: Weikang Wu**

Task 1 Synthesis of a Multiplexer

**1.1 introduction**

**1.2 What other possibility to parametrize a VHDL design do you know?**

A:

There are two ways to declare parameters inside one "Entity" Block, which are GENERIC and PORT declaration.

Furthermore inside the "Architecture" block the SIGNAL parameter can also be declared.

At the end part of "Architecture" the GENERIC and PORT parameters will be mapped with real channels.

**1.3 What is the difference between the schematics after the Synthesis compared to the one of the RTL Analysis?**

A:

The schematics after RTL Analysis is more general and independent from FPGA Structure, while schematics after Synthesis use all the units available on the specific FPGA.

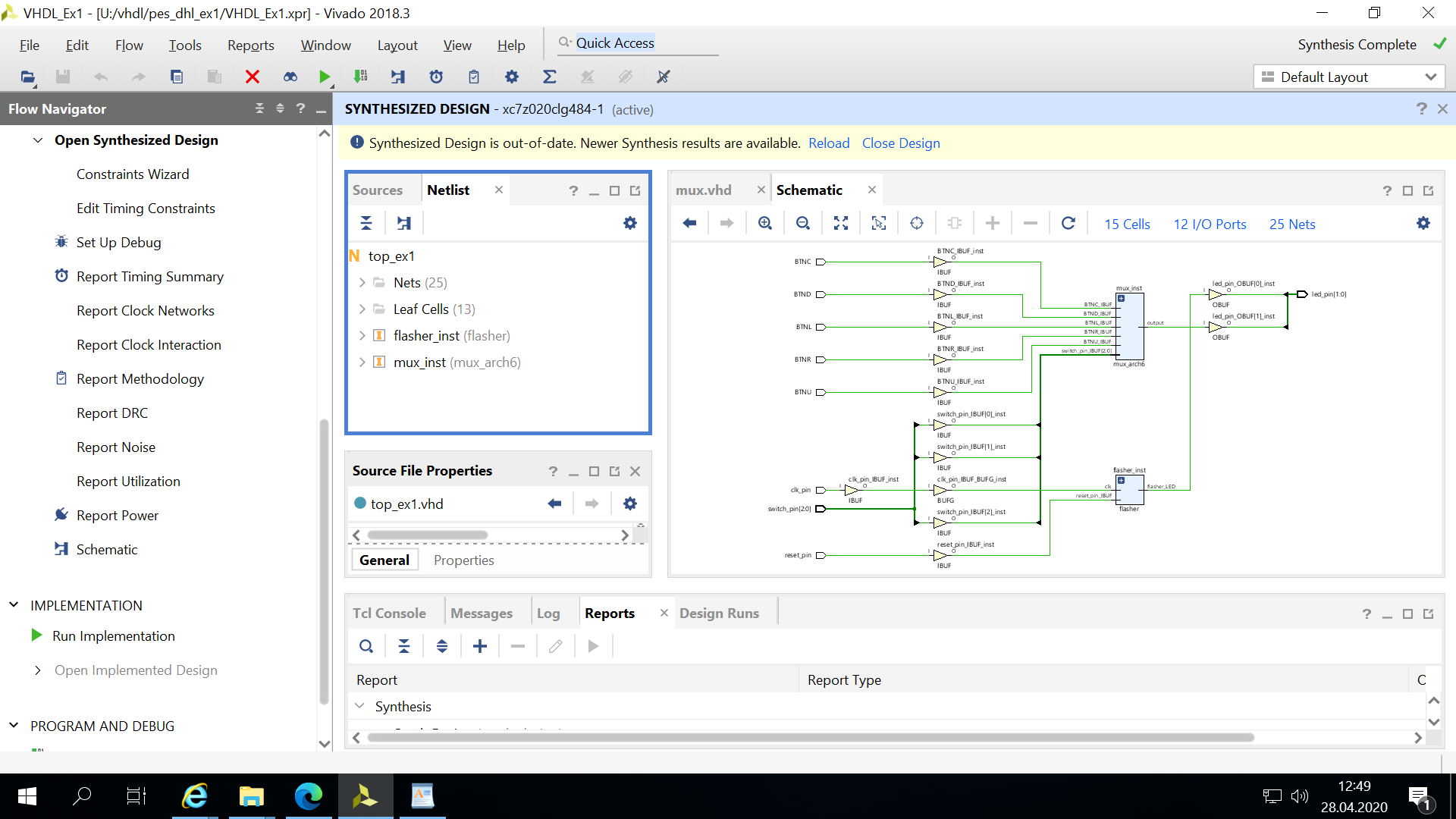
**1.4 Does the synthesized netlist look like you expected? Look at**

**the synthesis report, in order to get a hint what happened during synthesis.**

A:

------Following is decrepated because i misunderstand what the question is aimed at-----

Due to the fact that i dont know what the purpose of the multiplexer is, i will assume it´s a normal 5x1 multiplexer. According to the schematics from below:



i suppose it seems good to me. As the tasks suggest that there will be errors during the synthesis. Here are parts of critical warnings (instead of error) aroused inside the report:

*WARNING: [Vivado 12-584] No ports matched 'led\_shift\_pin[0]'. [U:/vhdl/pes\_dhl\_ex1/VHDL\_Ex1.data/constrs\_1/top.xdc:24]*

*CRITICAL WARNING: [Common 17-55] 'set\_property' expects at least one object. [U:/vhdl/pes\_dhl\_ex1/VHDL\_Ex1.data/constrs\_1/top.xdc:24]*

*Resolution: If [get\_<value>] was used to populate the object, check to make sure this command returns at least one valid object.*

*WARNING: [Vivado 12-584] No ports matched 'led\_shift\_pin[0]'. [U:/vhdl/pes\_dhl\_ex1/VHDL\_Ex1.data/constrs\_1/top.xdc:25]*

*CRITICAL WARNING: [Common 17-55] 'set\_property' expects at least one object. [U:/vhdl/pes\_dhl\_ex1/VHDL\_Ex1.data/constrs\_1/top.xdc:25]*

*Resolution: If [get\_<value>] was used to populate the object, check to make sure this command returns at least one valid object.*

*WARNING: [Vivado 12-584] No ports matched 'led\_shift\_pin[1]'. [U:/vhdl/pes\_dhl\_ex1/VHDL\_Ex1.data/constrs\_1/top.xdc:27]*

*CRITICAL WARNING: [Common 17-55] 'set\_property' expects at least one object. [U:/vhdl/pes\_dhl\_ex1/VHDL\_Ex1.data/constrs\_1/top.xdc:27]*

*Resolution: If [get\_<value>] was used to populate the object, check to make sure this command returns at least one valid object.*

*WARNING: [Vivado 12-584] No ports matched 'led\_shift\_pin[1]'. [U:/vhdl/pes\_dhl\_ex1/VHDL\_Ex1.data/constrs\_1/top.xdc:28]*

*CRITICAL WARNING: [Common 17-55] 'set\_property' expects at least one object. [U:/vhdl/pes\_dhl\_ex1/VHDL\_Ex1.data/constrs\_1/top.xdc:28]*

*Resolution: If [get\_<value>] was used to populate the object, check to make sure this command returns at least one valid object.*

After analysing the error codes above, i suggest they refer to the "Constraint files", where certain ports are not matched. Following are corresponding rows which cause the warnings.

*### LEDs for example 3*

*set\_property PACKAGE\_PIN V22 [get\_ports {led\_shift\_pin[0]}]*

*set\_property IOSTANDARD LVCMOS33 [get\_ports led\_shift\_pin[0]]*

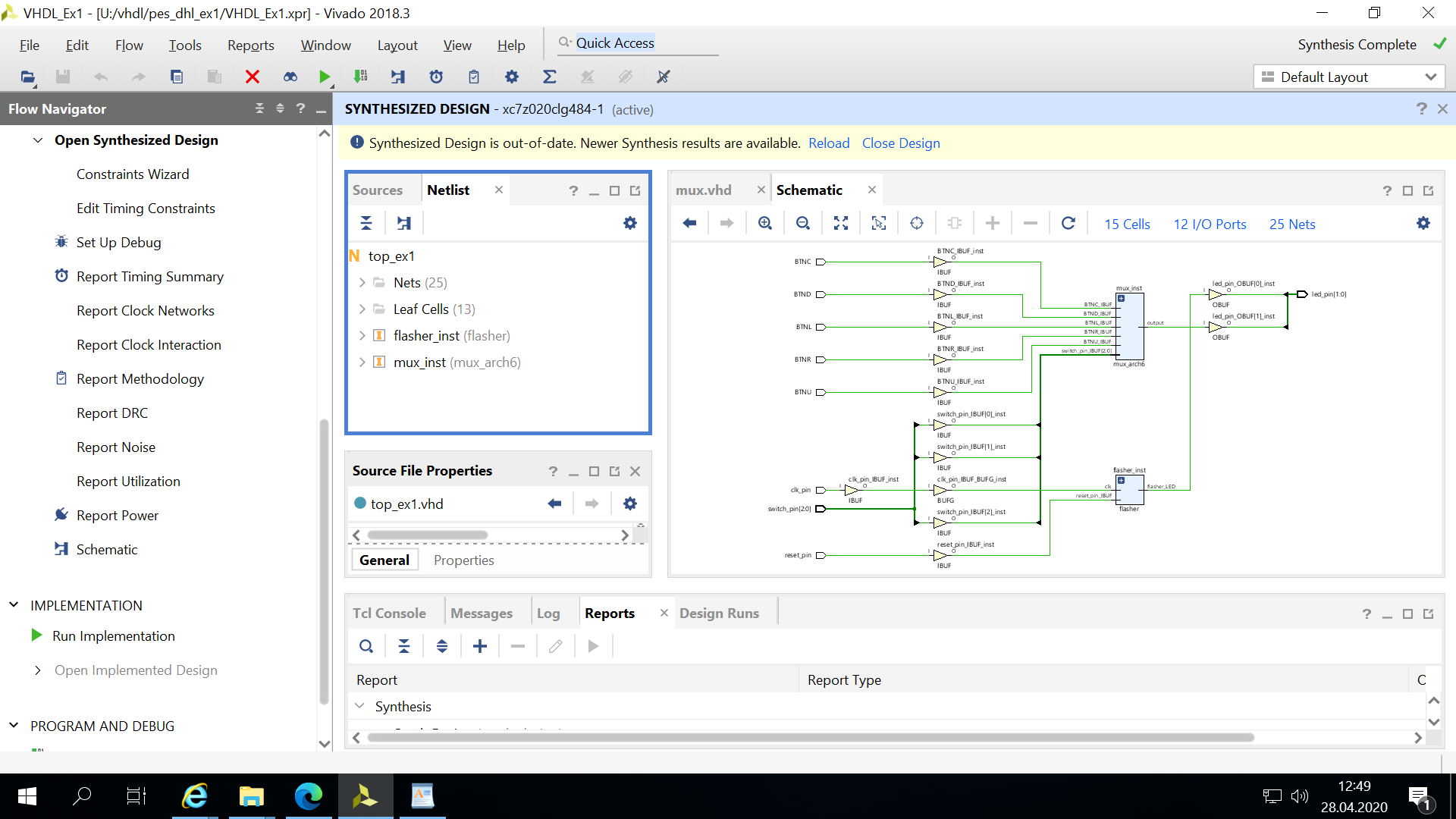
*set\_property PACKAGE\_PIN W22 [get\_ports {led\_shift\_pin[1]}]*

*set\_property IOSTANDARD LVCMOS33 [get\_ports led\_shift\_pin[1]]*

Now i´m confused about the comment said "LEDs for example 3", which may suggest these codes are prepared for example 3 and thus not relevant to our "multiplexer" problem? Or is it suggesting from the literal meaning, that we are going to build a multiplexer controlled by switches which will eventually result in some LEDs lighting and darkening.

----------New Version---------

so the schematics looks perfect fine as this picture depicts:



and from the log view, no fatal error was made, just some irrelevant warnings, which doesn´t cause the crash of synthesis.

**1.5 If not try to figure out which modeling mistake was made.Correct**

**the mistake, restart the synthesis and analyze the result.**

two areas where students should write their codes in:

-top\_ex1.vhd:

*-- STUDENT CODE HERE*

*for all : mux use entity work.mux (arch1) ;*

*-- STUDENT CODE until HERE*

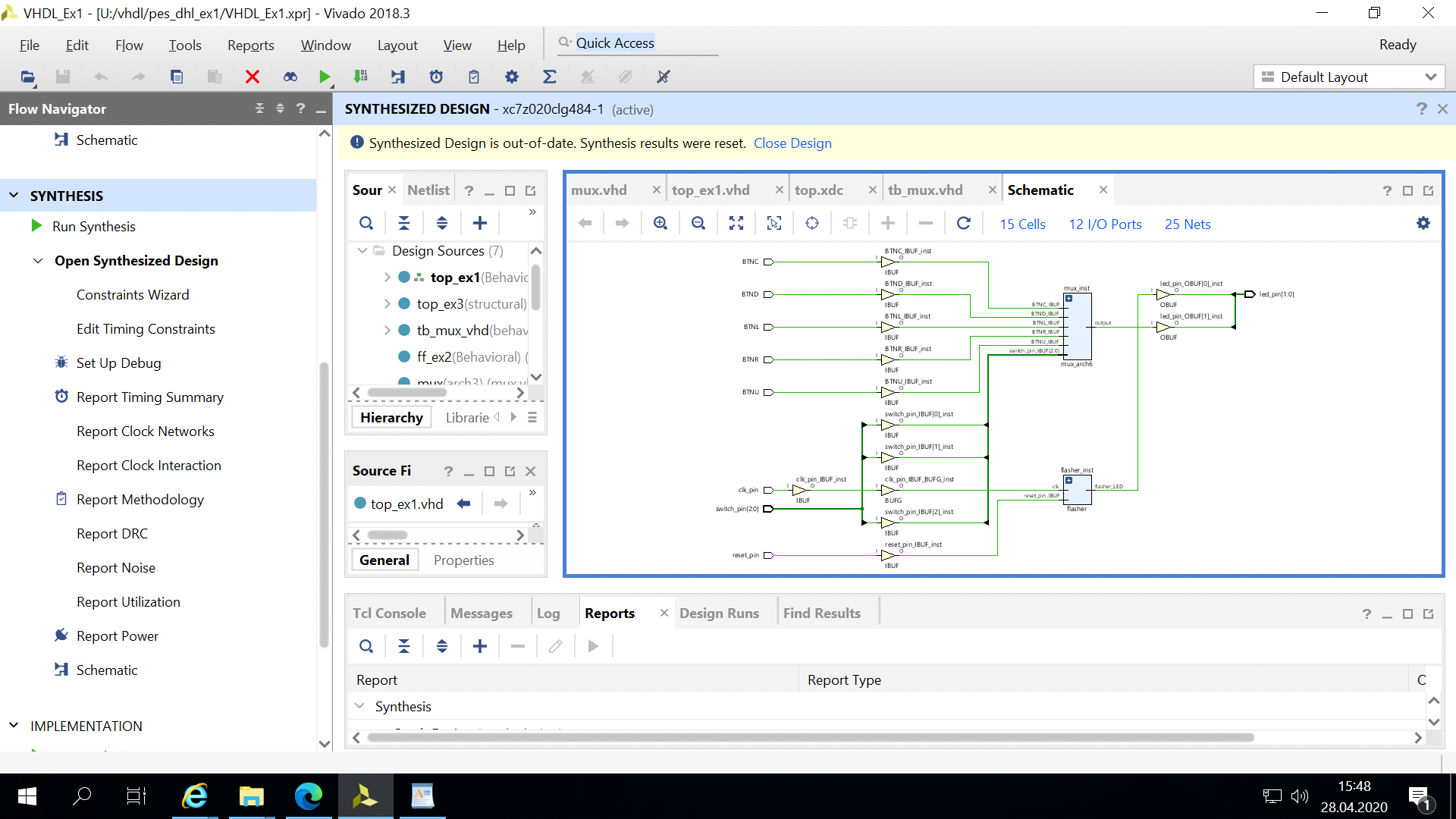
-mux.vhd:

*-- STUDENT CODE HERE*

*else input(0)*

*-- STUDENT CODE until HERE*

new result:



**1.6 Now change the configuration in order to select the architecture**

**arch2 and start the synthesis. Which modeling mistake was made here and**

**why does the synthesis tool nevertheless produce the correct netlist? Use the synthesis report to get a hint.**

A:

some error codes are listed here:

*-- when "101" => output <= input(5);*

*-- when others => output <= input(0);*

*when others => output <= '0';*

the second commented line maybe the solution to the problem, which returns input(0) when input switch gives number bigger than "101".

Corresponding log files:

*INFO: [Synth 8-638] synthesizing module 'top\_ex1' [U:/vhdl/pes\_dhl\_ex1/VHDL\_Ex1.srcs/sources\_1/imports/example1/top\_ex1.vhd:44]*

*INFO: [Synth 8-3491] module 'mux' declared at 'U:/vhdl/pes\_dhl\_ex1/VHDL\_Ex1.srcs/sources\_1/imports/example1/mux.vhd:33' bound to instance 'mux\_inst' of component 'mux' [U:/vhdl/pes\_dhl\_ex1/VHDL\_Ex1.srcs/sources\_1/imports/example1/top\_ex1.vhd:75]*

*INFO: [Synth 8-638] synthesizing module 'mux\_arch2' [U:/vhdl/pes\_dhl\_ex1/VHDL\_Ex1.srcs/sources\_1/imports/example1/mux.vhd:59]*

*WARNING: [Synth 8-614] signal 'input' is read in the process but is not in the sensitivity list [U:/vhdl/pes\_dhl\_ex1/VHDL\_Ex1.srcs/sources\_1/imports/example1/mux.vhd:62]*

*INFO: [Synth 8-256] done synthesizing module 'mux\_arch2' (1#1) [U:/vhdl/pes\_dhl\_ex1/VHDL\_Ex1.srcs/sources\_1/imports/example1/mux.vhd:59]*

*INFO: [Synth 8-3491] module 'flasher' declared at 'U:/vhdl/pes\_dhl\_ex1/VHDL\_Ex1.srcs/sources\_1/imports/example1/flasher.vhd:8' bound to instance 'flasher\_inst' of component 'flasher' [U:/vhdl/pes\_dhl\_ex1/VHDL\_Ex1.srcs/sources\_1/imports/example1/top\_ex1.vhd:82]*

*INFO: [Synth 8-638] synthesizing module 'flasher' [U:/vhdl/pes\_dhl\_ex1/VHDL\_Ex1.srcs/sources\_1/imports/example1/flasher.vhd:15]*

*INFO: [Synth 8-256] done synthesizing module 'flasher' (2#1) [U:/vhdl/pes\_dhl\_ex1/VHDL\_Ex1.srcs/sources\_1/imports/example1/flasher.vhd:15]*

*INFO: [Synth 8-256] done synthesizing module 'top\_ex1' (3#1) [U:/vhdl/pes\_dhl\_ex1/VHDL\_Ex1.srcs/sources\_1/imports/example1/top\_ex1.vhd:44]*

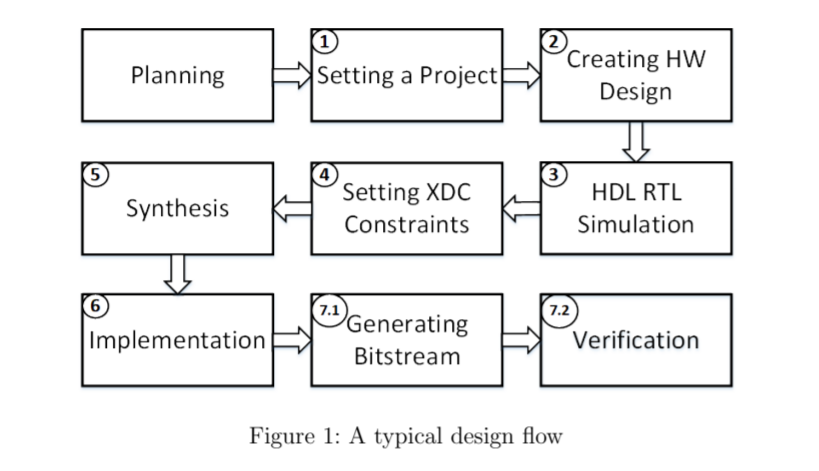
explanation:

Since we can see the exact same display of schematics after synthesis, we can conclude that both netlists are the same too. One possible explanation may be the changed behavior of one multiplexer can not be represented by its schematics, which represents for its structure.

**1.7 Before you continue, check if all steps of the tool chain completed successfully. In which step of the tool chain are the LOC constraints**

**merged into the design?**

tool chain illustrated:



I cant find any information related to LOC Constraints and therefore i would guess, LOC Constraints maybe merged together with XDC Constraints at step 4 in picture above.

Task 2 Synthesis of Flip-Flops

**2.1 Look at the architecture of the entity ff. How many Flip-Flops**

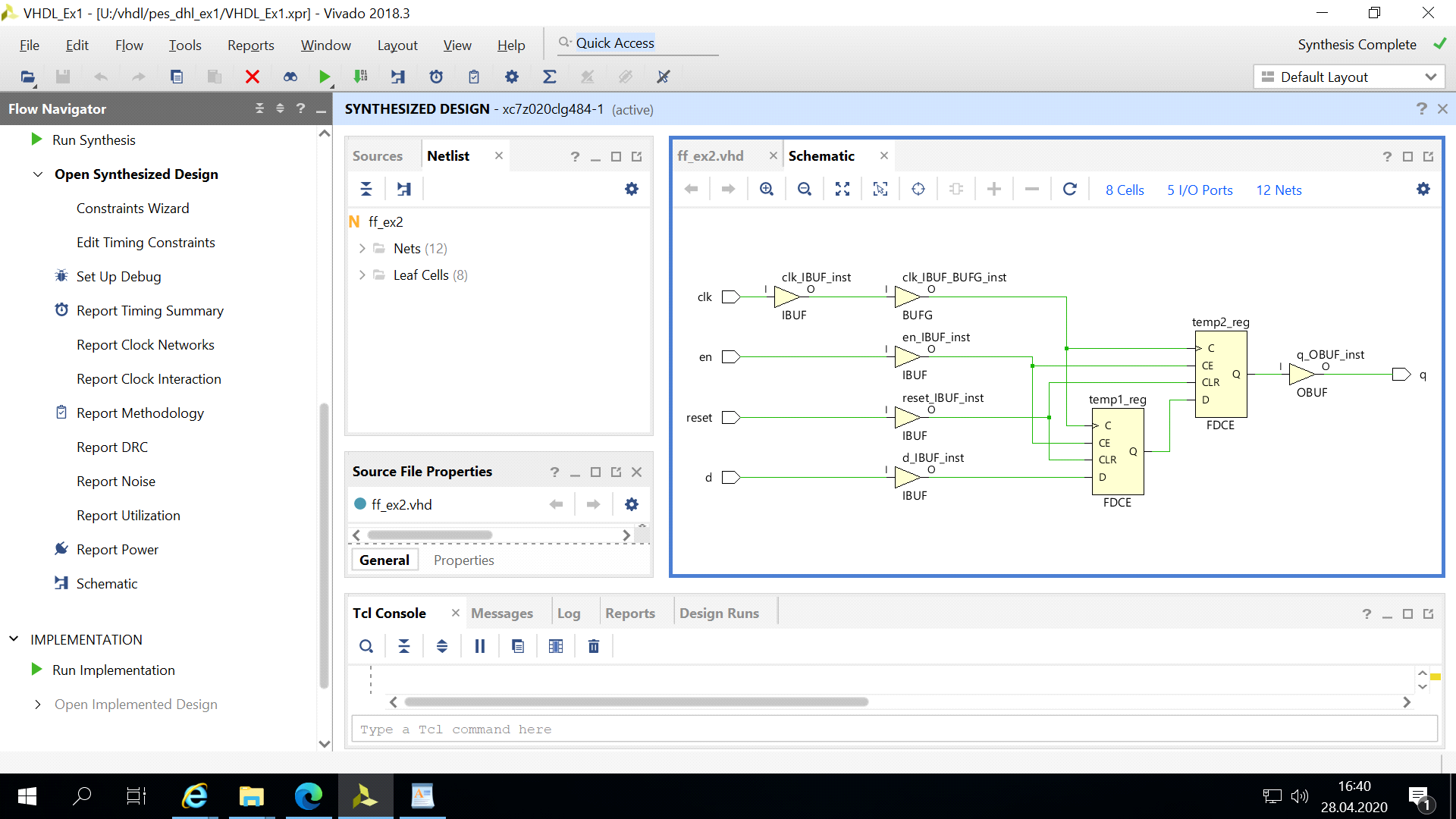
**will be synthesized by this description?**

Code:

*temp1 <= d;*

*temp2 <= temp1;*

imply that there will be 2 Flipflops.



**2.2 Is it also possible to create a flip-flop that is triggered on both**

**the positive and negative clock edges?**

yes, by modifying the if condition from:

*elsif clk'event and clk = '1' then*

to:

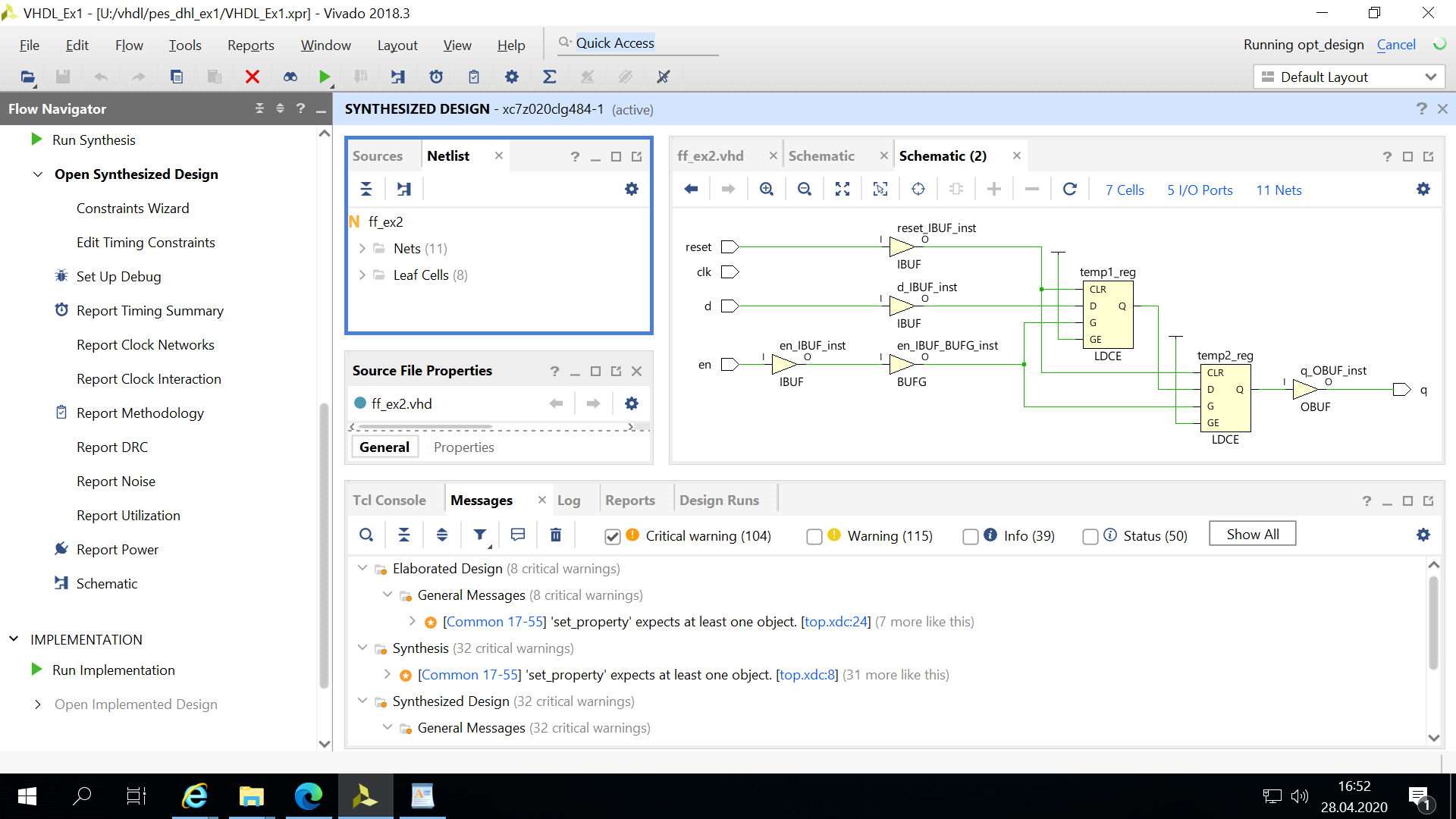
*elsif clk'event then* ----report event not implemented ERROR

*elsif rising\_edge(clk) or falling\_edge(clk) then* ----reported another ERROR

*else* ---successful, because clk is already in sensitivity list

**2.3 How would it still be possible to realize such a behavior in**

**hardware?**



Task 3 Comparison Behavioral Modeling - Structural Modeling

**3.1 introduction**

**properties:**

**y\_int: depth-1::0 (left::right)**

**d\_in: new input bit**

**load\_in: behavior, put input bit first and move all others right 1 step**

**l\_in: behavior, put first to the end and all others left 1 step**

**r\_in: behavior, put last to the first and all others right 1 step**

**reg\_depth: array length**

*//signal declaration*

*signal y\_int : std\_logic\_vector(reg\_depth-1 downto 0);*

*begin*

*// initalize output*

*y\_out <= y\_int;*

*//process of behavior sensitive to clk and reset*

*reg\_proc: process(clk,reset)*

*begin*

*// if reset, then all cleared*

*if (reset = '1') then*

*y\_int<= (others => '0');*

*//if rising edge*

*elsif ( clk'event and clk = '1') then*

*//if behavior as "load in"*

*if load\_in = '1' then*

*//first bit to first*

*y\_int(reg\_depth-1) <= d\_in;*

*// bits from depth-1 to 1 moves forward 1 step (move right 1 step)*

*y\_int(reg\_depth-2 downto 0) <= y\_int(reg\_depth-1 downto 1);*

*//if behavior as "right in", then output switch the last bit to the frontend bit*

*//The concatenation operator (&) operates on one-dimensional arrays to form a*

*new array with the contents of the right operand following the contents of*

*the left operand*

*elsif r\_in = '1' then*

*y\_int <= y\_int(0) & y\_int(reg\_depth-1 downto 1);*

*//if behavior as "left in", then move the first bit to the end*

*elsif l\_in = '1' then*

*Y\_int <= y\_int(reg\_depth-2 downto 0) & y\_int(reg\_depth-1);*

*//if behavior is not defined, pass*

*else*

*y\_int <= y\_int ;*

*end if;*

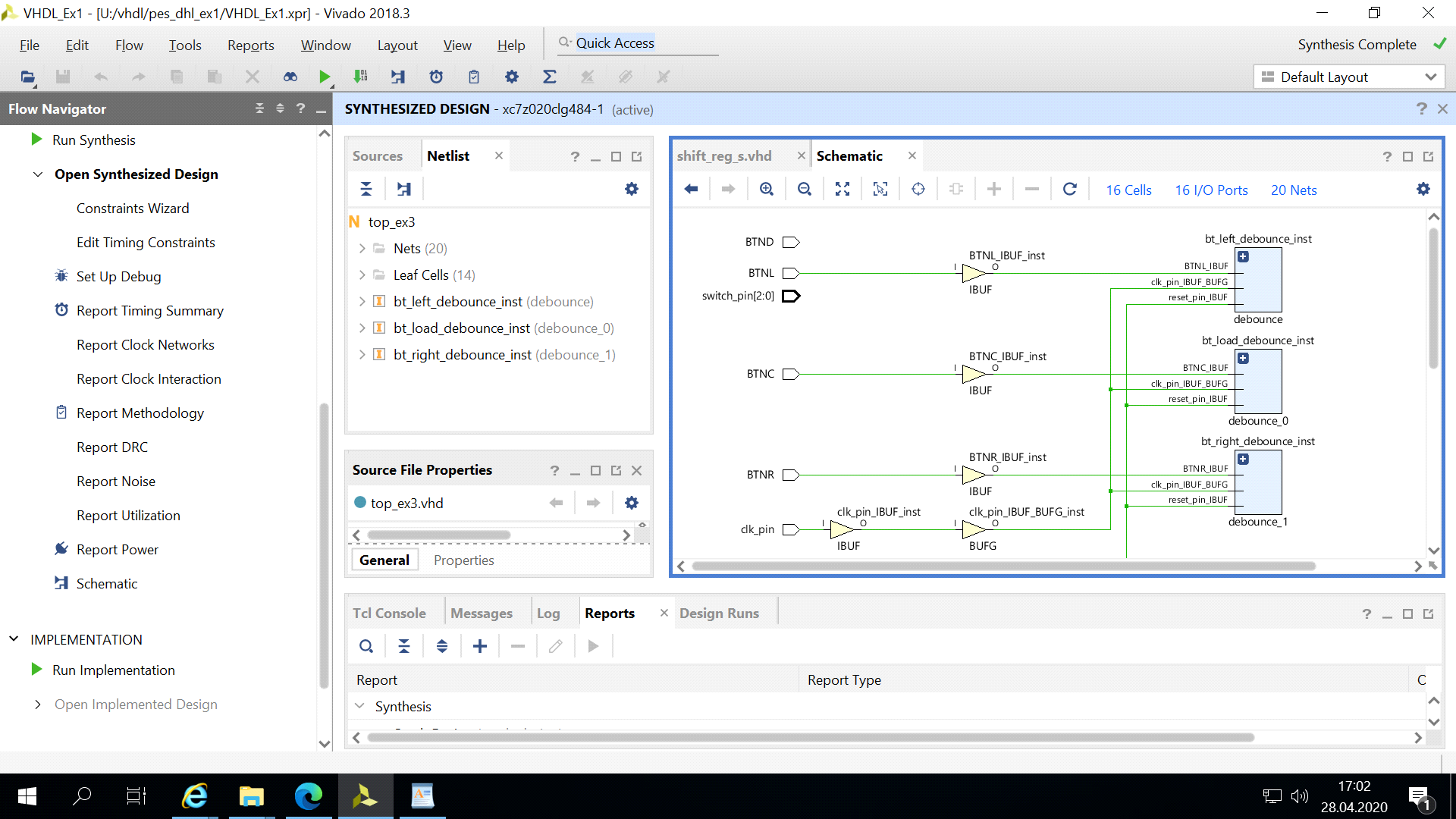
*end if;*

*end process;*

**3.2 Next start the synthesis and examine the generated netlist.**

**Which components are used to construct the ring-shift-register? Also give**

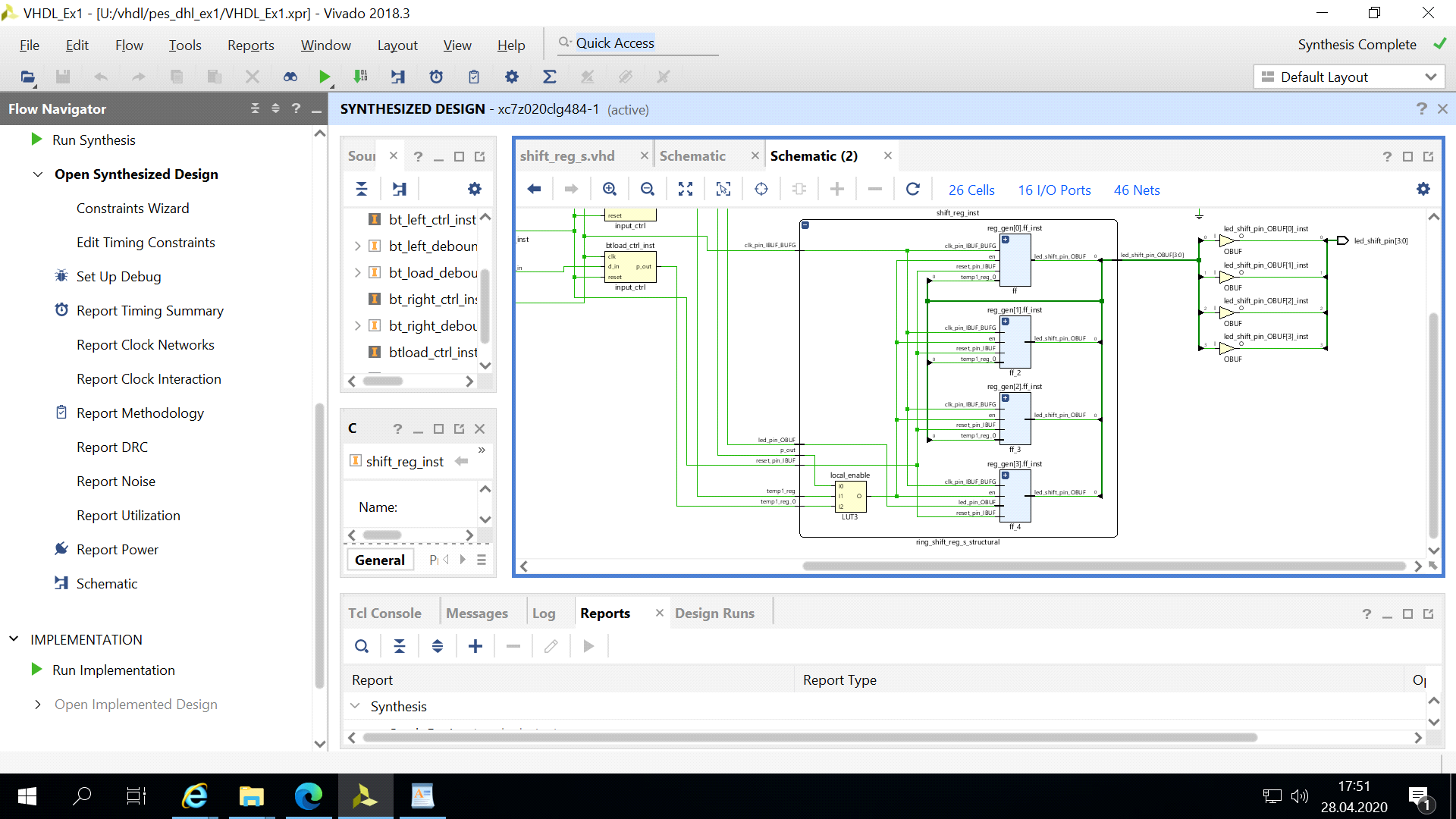
**their instance names.**

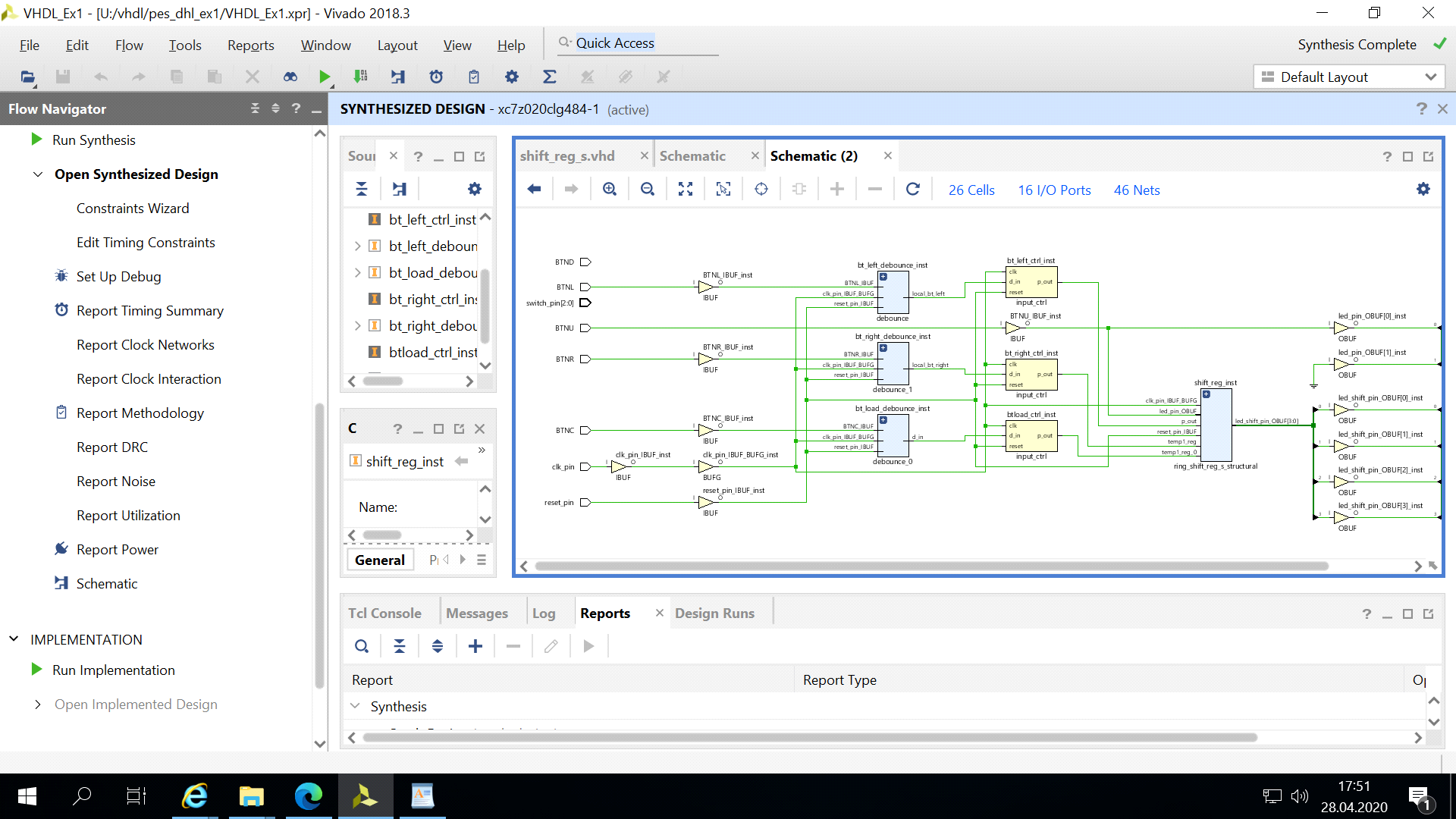


instance name: debounce

**3.3 Add the missing control logic for the multiplexer and the register**

**inputs/outputs. Extend the structural architecture in the VHDL code to implement this logic**





*--reg\_enable logic*

*-- STUDENT CODE HERE*

*local\_enable <= l\_in and r\_in and load\_in;*

*-- STUDENT CODE until HERE*

*--mux select logic*

*-- STUDENT CODE HERE*

*local\_sel(0) <= (not r\_in) and (not load\_in);*

*local\_sel(1) <= (not l\_in) and (not load\_in);*

*-- STUDENT CODE until HERE*

Task 4 Design and Synthesis of FSMs

4.1 Now it is your task to realize the missing unit input\_ctrl (input\_ctrl.vhd). Its purpose is to solve the second issue to allow selective

control of the ring-shift-register

*architecture ip\_ctrl\_be of input\_ctrl is*

*type state\_type is (zero,one);*

*signal current\_state:state\_type;*

*begin*

*curr\_proc:process(clk,reset)*

*begin*

*if reset = '1' then*

*current\_state <= zero;*

*elsif (clk'event and clk = '1') then*

*case current\_state is*

*when zero =>*

*if d\_in = '1'then*

*current\_state <= one;*

*end if;*

*when one =>*

*current\_state <= zero;*

*end case;*

*end if;*

*end process;*

*out\_proc: process(current\_state)*

*begin*

*case current\_state is*

*when zero =>*

*p\_out <= '0';*

*when one =>*

*p\_out <= '1';*

*end case;*

*end process;*

*end ip\_ctrl\_be;*

4.2 Start the synthesis and look at the resulting netlist. How

was the desciption of the FSM transferred into a netlist? Does the number

of registers match the expected numbers? Can you reconstruct the logic for

the state transitions and the output logic?

