Project 3 Report

ECE 2500

Xiaoyu Hou

12/8/2020

Abstract

The project is about cache simulate and find the relationship between miss rate, cache size, and associativity. As the result, it is easy to find that the increasing cache size will reduce the miss rate.

Introduction

In this project, we will find how do the cache size and cache associativity affect cache effectiveness, especially focus on load miss, load hit, store miss, the store hit, average memory access time, and miss rate. Following terms are used in the rest of the paper:

Cache size: How many words can cache hold (in KB)

Cache associativity: Divide the cache into sets, so each block can hold n items

Load miss/Store miss: Can't find needed data in the cache

Load hit/Store hit: Find the needed date in the cache

Average memory access time: Average time to access memory (in cycles)

Miss rate: Overall miss rate

Simulation software

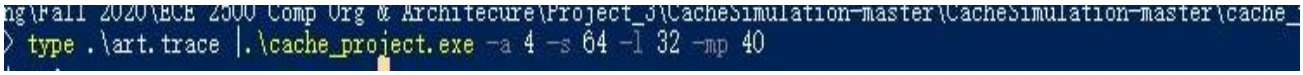
✧ *Introduction of simulation software and data used*

The simulation software simulates the read and load data from the cache. The input data are memory trace file, associativity of the cache, the block size (in bytes) of the cache, the size (in KB) of the cache, the miss penalty (in cycles) of a miss.

To run the simulate software, I create the console application which is called cache_project.exe. After I have the executable file, I can do the simulation using the command line in the power shell.

✧ *Input data format in command line*

For example, this is the command line in the power shell:



.\art.trace: memory trace file

.\cache_project.exe: the executable file of the cache simulation

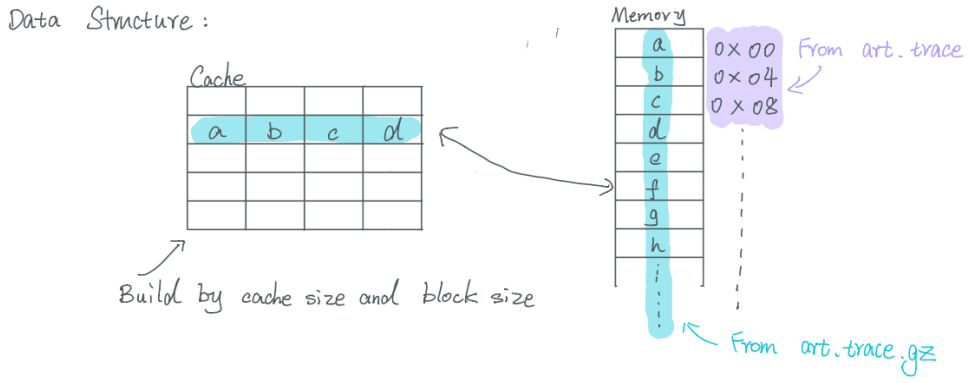
-a 4: The associativity of the cache, which is 4 in the example

-s 64: The size of the cache, which is 64KB in the example

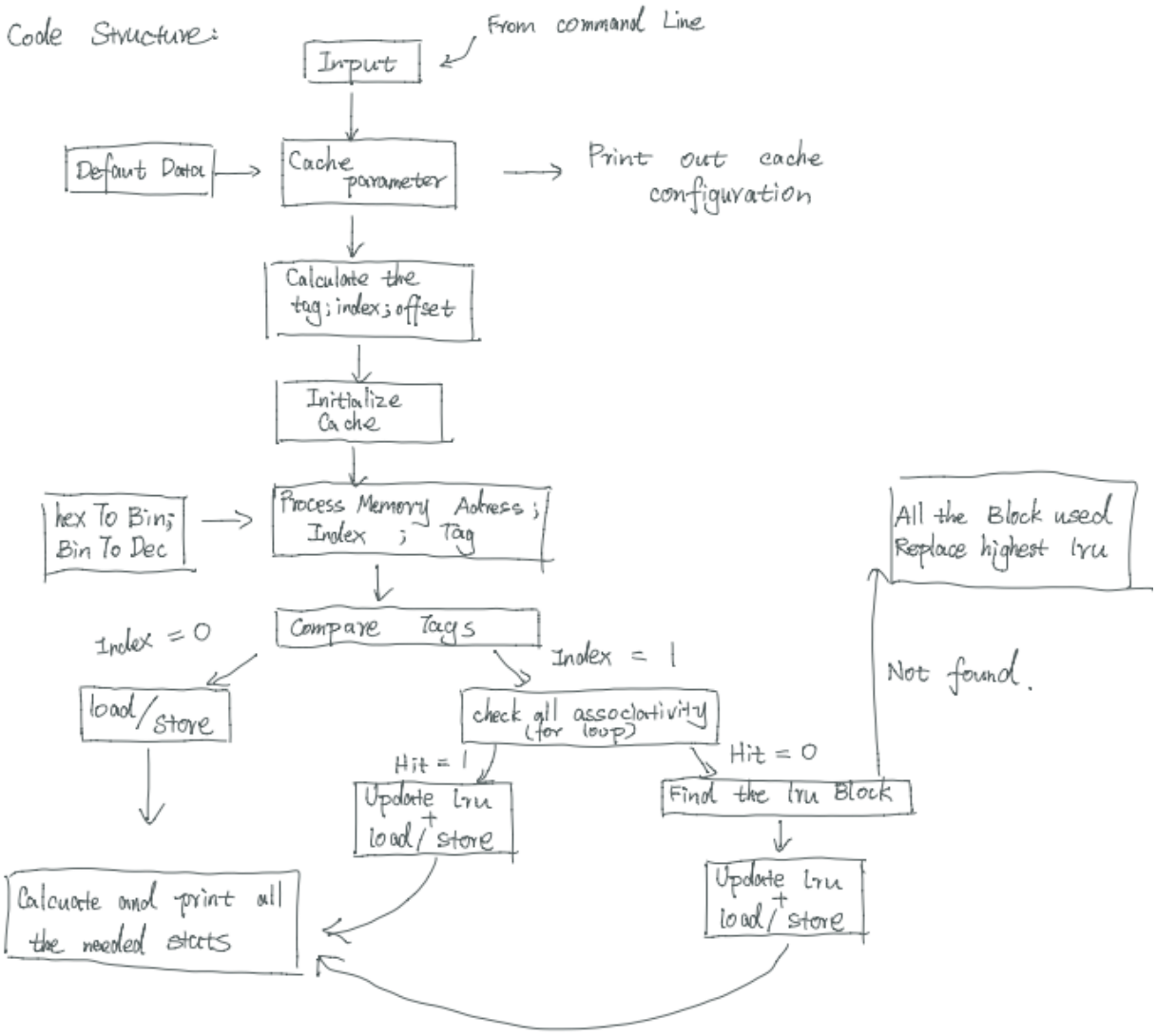
-l 32: The block size of the cache, which is 32bytes in the example

-mp 40: The miss penalty of a miss, which is 40 cycles in the example

✧ *Data Structures*



✧ *Code Structures*



Experiment & Result

Following is the data from "Part 2 – Trading off the cache size and associativity while keeping the block size constant":

	Average memory access time	Miss rate
256KB, 1	9.92	0.25
64KB,1	10.20	0.25
32KB, 1	10.20	0.25
16KB, 1	8.48	0.30
128KB, 2	10.00	0.25
64KB, 4	10.12	0.25
32KB, 8	10.13	0.25
16KB, 16	10.13	0.25
8KB, 32	10.13	0.25

According to the chart above, the increasing cache size will make the miss rate reduce. But the miss rate will stay constant after the cache size which is 32KB. Furthermore, the miss rate could be reduced by increase the associativity. However, the average memory access time could be increased when increasing cache size at the beginning and increasing cache size will decrease the average access time.

Summarize

In this project, we use C language to simulate the cache work for the memory and focus on the relationship between cache size, access time, and miss rate. After simulate and analyze, I find the increasing cache size could make the miss rate decrease and make the access time increase at the beginning, keep increase cache size will make the miss rate stable and make the access time decrease.