MPQ5613T

Automotive TFT LCD Bias Driver with Gate Voltage Shaping and VCOM Buffer

PRELIMINARY SPECIFICATIONS SUBJECT TO CHANGE

DESCRIPTION

The MPQ5613T is an integrated power supply for automotive LCD TFT Bias. It integrates a boost converter, a synchronous buck-boost inverter, an adjustable positive charge pump output and an adjustable negative charge pump output for the gate voltages. It also includes a VCOM Buffer and gate voltage shaping function for minimizing the external components. It is designed to power TFT LCD panels from a regulated 3.3V or 5V supply, or the battery directly, 12V.

The VDDP can output a maximum 21.8V voltage, the VDDN could output a minimum -16.6V negative voltage, the VGH could output a maximum 43.2V voltage and the VGL could output a minimum -15.9V negative voltage.

The I²C interface and programmable power on sequence for VDDP, VDDN, VGL and VGH make the IC suitable for different applications. An internal soft-start function prevents input overload at startup. Cycle-by-cycle current limiting reduces component stress.

Robust protections are included to guarantee safe operation of the device. Protections modes include input under-voltage lockout (UVLO), cycle-by-cycle current limit protection for SWP and SWN, over-temperature protection (OTP), under-voltage protection (UVP) for VDDP, VDDN, VGH and VGL, output over-current protection (OCP) for VCOM and output current limit protection for VDDP.

The MPQ5613T is available in a tiny 4mmx5mm, 28-pin QFN package.

FEATURES

- 2.7 to 12V Operating Input Range
- 2A Current Limit for Boost
- 2.5A Current Limit for Buck-Boost
- 250mΩ MOSFET for Boost
- 200mΩ/250mΩ Power MOSFET for Sync-Buck-Boost
- I²C Interface with Customized IC address, 1 Time OTP (One Time Program) for Registers.
- Programmable Fsw, up to 3MHz, Spread Spectrum for Better EMI
- Frequency Synchronization and Interleave (180°) Buck-Boost and Boost control for Better EMI
- Input and Output Disconnection.
- 4 Outputs with Gate Voltage Shaping and VCOM Buffer In a Single Package
  - Boost up to 21.8V
  - Buck-Boost Inverter low to -16.6V
  - Adjustable Positive Charge Pump, up to 43.2V, 50mA
  - Adjustable Negative Charge Pump, -15.9V, 50mA
  - Gate Voltage Shaping with Programmable Falling Time
  - VCOM Buffer, 25mA
- High Efficiency
- Programmable Power-On/off Sequence
- VIN Under Voltage Lockout (UVLO)
- UVP for VDDP, VDDN, VGH and VGL
- Cycle-by-Cycle Current Limit Protection for SWP and SWN
- OCP for VCOM
- Output current limit protection for VDDP
- Fault Flag
- Available in AEC-Q100 Qualified Grade 1
- QFN-28 (4mmx5mm) Package

APPLICATIONS

- Car Navigation Displays
- TFT LCD Displays
- Tablet PCs

TYPICAL APPLICATION

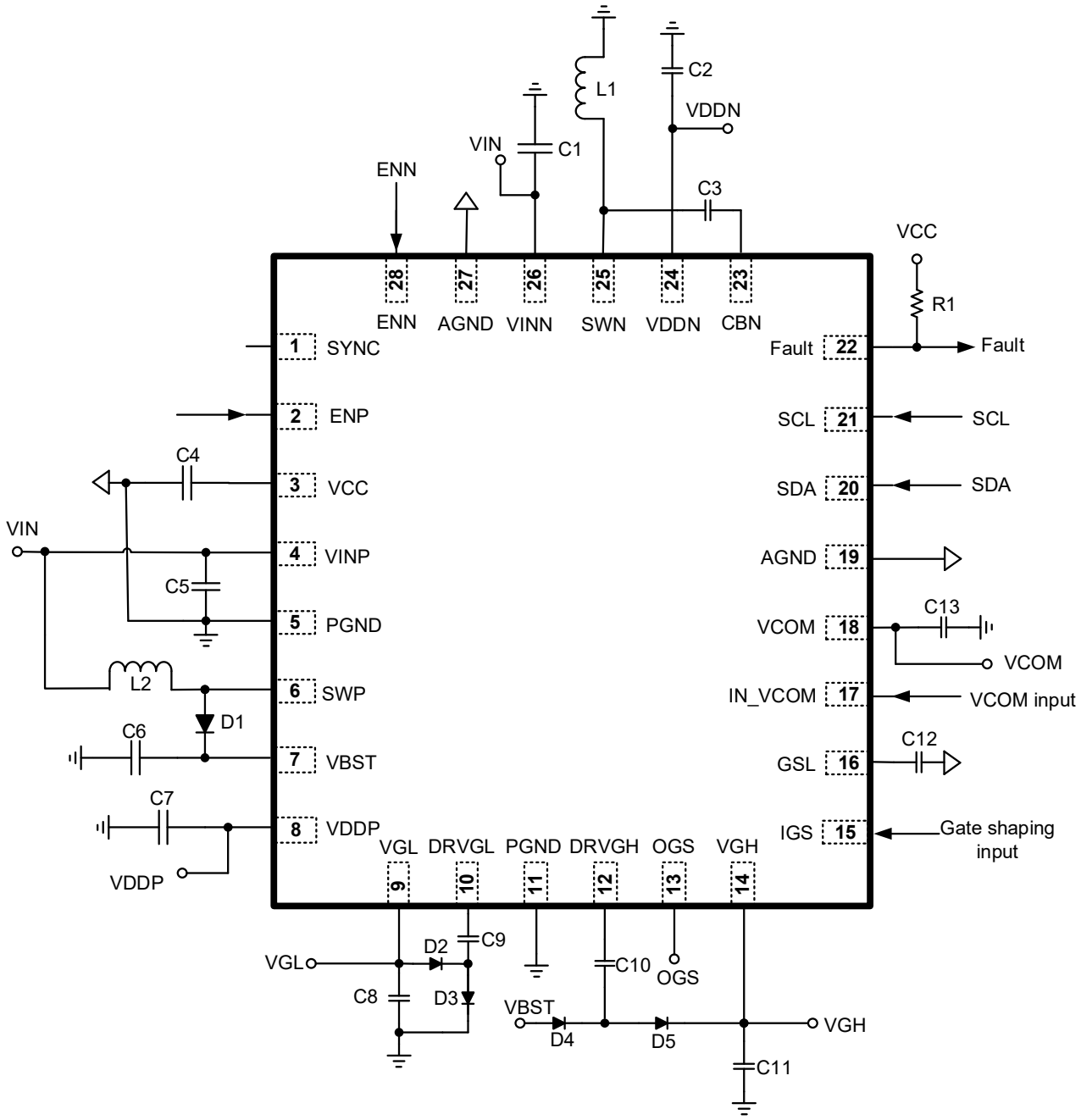


Figure 1: Typical Application Circuit

ORDERING INFORMATION

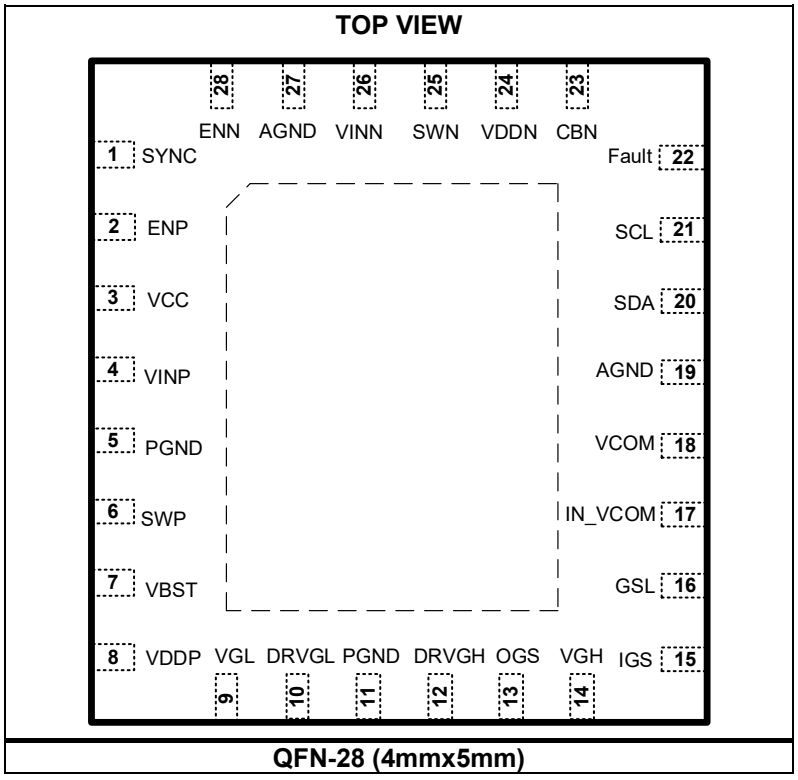
Part Number*	Package	Top Marking	MSL Rating
MPQ5613TGVE-xxxx-AEC1**	QFN-28 (4mmx5mm)	*See Below*	2

* For Tape & Reel, add suffix -Z (e.g. MPQ5613TGVE-xxxx-AEC1-Z)
** "xxxx" is the register setting option. The factory default is "0000." For custom options, please contact an MPS FAE to obtain a "xxxx" value.

TOP MARKING

(TBD)

PACKAGE REFERENCE



QFN-28 (4mmx5mm)

PIN FUNCTIONS

Pin #	Name	Description
1	SYNC	**Frequency synchronization input.** Set FSYNC_EN = 0b and connect a pulse signal on this pin to synchronize the operating frequency. If FSYNC_edge = 0b (default), the rising edge of the synchronizing signal synchronizes the turn on of Boost MOSFET.
2	ENP	**Enable signal for the boost converter.**
3	VCC	**IC Internal power supply.** VCC provides power for the internal MOSFET switch gate driver and the internal control circuitry. Bypass VCC to AGND with a 1μF or greater capacitor.
4	VINP	**IC Supply Power Input.** VINP supplies the power to the MPQ5613T. Bypass VINP to AGND with a 4.7μF or greater capacitor.
5	PGND	**Power Ground for boost stage.** Connect PGND to AGND as close to the MPQ5613T as possible.
6	SWP	**Boost Converter Power Switch Node.** Connect an inductor between the input source and SWP, and connect a rectifier diode from SWP to the main output VBST to complete the step-up converter. SWP is the drain of the internal 250mΩ N-Channel MOSFET switch.
7	VBST	**The output of the boost converter.** Connect a large enough output capacitor from this pin to the power ground. Layout the output capacitor, the rectifier diode, the SWP pin and PGND pin as small loop as possible. VBST is the supply for the positive and negative charge pump driver.
8	VDDP	**The output positive voltage for TFT Bias driver.** VDDP and VBST are connected together through an internal MOSFET. At fault condition, VDDP and VBST are disconnected.
9	VGL	**Negative charge pump output voltage.** Bypass this pin to PGND with capacitor larger than 1uF.
10	DRVGL	**Negative charge pump driver.** Please refer to the typical application for external components connection.
11	PGND	**Power ground.**
12	DRVGH	**Positive charge pump driver.** Please refer to the typical application for the external components connection.
13	OGS	**The gate signal output to drive the TFT gate with programmable falling time.** OGS is internally connected to VGH through a MOSFET.
14	VGH	**High voltage input for the gate driver.** It is usually the output of the positive charge pump. Bypass this pin to GND with a capacitor larger than 1uF.
15	IGS	**Gate shaping input control signal.**
16	GSL	**Gate output signal slew rate set pin.** Connect a typical 68pF cap on this pin.
17	IN_VCOM	**VCOM buffer input voltage.**
18	VCOM	**VCOM buffer output pin.** Please refer to the typical application for the external components connection.
19, 27	AGND	**IC analog ground.** Connect the AGND to exposed pad.
20	SDA	**I²C data signal input.** Connect this pin to GND if not use.
21	SCL	**I²C clk signal input.** Connect this pin to GND if not use.
22	Fault	**Fault signal.** Open drain during normal operation, pulled to low at fault condition. After all regulators are turned-on, Fault pin is pulled to low if any regulators output voltage value are fall below 60% of its threshold, and then the entire chip will shut down.
23	CBN	**Bootstrap driver supply for the buck-boost high-side MOS.** Connect a capacitor between this pin and SWN.
24	VDDN	**The buck-boost inverter output.** Connect a large enough output capacitor from this pin to the power ground PGND. The VDDN also supplies the VCOM buffer for a negative VCOM output.
25	SWN	**Buck-boost inverter Power Switch Node.** Connect an inductor between SWN and PGND.
26	VINN	**Power supply for buck-boost.** Bypass this pin to PGND with a 2.2uF or greater capacitor. Layout capacitors of VINN and VDDN very close to VINN and VDDN pin, place the VINN capacitor, VINN pin, the VDDN capacitor and the VDDN pin as small loop as possible.
28	ENN	**Enable signal for the buck-boost converter.**
Pad	Exposed pad	**No internal electrical connections.** Solder it to PGND plane to reduce thermal resistance.

ABSOLUTE MAXIMUM RATINGS (1)

VIN Supply Voltage…….....-0.3V to +14V
SWP, VBST, VDDP…….....-0.3V to +25V
DRVGH, DRVGL…….....-0.3V to +25V
OGS, VGH, GSL……-0.3V to +45V
VDDN, VGL…….-18V to +0.6V
SWN…….....-18V to +14V
CBN-SWN……...-0.3V to +6V
VIN-VDDN……....0V to +32V
IN_VCOM, VCOM……VDDN to VDDP
VCC……... .....-0.3V to +6.5V
All Other Pins……...-0.3V to +5.3V
Junction Temperature……..……+150°C
Lead Temperature……+260°C
Storage Temperature ……...-65°C to +150°C
Continuous Power Dissipation (T_A = +25°C) (2)
QFN-28 (4mmx5mm)…… 3.66W

ESD Ratings

Human body model (HBM)……±2kV
Charged-device model (CDM)……...±750V

Recommended Operating Conditions (3)

Input Voltage…….....……2.7V to 12V
VDDP Output Voltage……V_{IN} to 21.8V
VDDN Output Voltage……...-16.6V to 0V
OGS, VGH Voltage……...VDDP to 43.2V
VGL Voltage……..…-15.9V to 0V
Maximum Junction Temp. (T_J)..... +150°C

Thermal Resistance (4)….. θ_{JA} θ_{JC}

QFN-28 (4mmx5mm) ……	34.1	2.4	°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on approximately 1” square of 1 oz copper.

ELECTRICAL CHARACTERISTICS

V_{IN} = 5V, T_J = -40°C to +150°C, typical value is at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Input Voltage Range	V_{IN}		2.7		12	V
VINP Under-Voltage Lockout (UVLO) Threshold	V_{IN_UVLO}	Rising edge	2.25		2.65	V
VINP UVLO Hysteresis				150		mV
VINP Stand-by current	I_{STB}	V_{ENP} = V_{ENN} = 0V, I²C is active			250	µA
VINP Quiescent Current	I_Q	V_{ENP} = V_{ENN} = 3.3V, No switching		2.4	3.2	mA
LDO output voltage	V_{CC}	VINP > 5.5V	4.75	5	5.25	V
Oscillator						
Switching Frequency	f_{SW}	FSET[2:0] = 011b	1.2	1.4	1.6	MHz
		FSET[2:0] = 100b	1.9	2.2	2.5	MHz
Maximum Duty Cycle	D_{MAX}	f_{SW} = 1.4MHz	82	85		%
		f_{SW} = 2.2MHz	72	78		%
Synchronization high threshold	V_{SYNC_HI}		1.4			V
Synchronization low threshold	V_{SYNC_LO}				0.6	V
Control Input (ENP, ENN)						
ENP turn on threshold	V_{ENP_ON}		1.4			V
ENP turn off threshold	V_{ENP_OFF}				0.6	V
ENN turn on threshold	V_{ENN_ON}		1.4			V
ENN turn off threshold	V_{ENN_OFF}				0.6	V
Power Switch (SWP, SWN)						
SWP On Resistance	R_{SWP_ON}	V_{IN} = 5V		250		mΩ
		V_{IN} = 3V		300		mΩ
SWP Current Limit	I_{SWP_LIM}	Duty = 80%	2	2.5		A
SWP Leakage Current	I_{SWP_LK}	V_{SWP} = 25V		0.5	1	µA
VDDP	V_{DDP}	VDDP[7:0] = 7Eh, T_J = 25°C	-0.89%	9	+0.89%	V
		-40°C < T_J < +150°C	-1.33%	9	+2.11%	V
SWN high side On Resistance	R_{SWNH_ON}	CBN-SWN = 5V		200		mΩ
		CBN-SWN = 3V		250		mΩ
SWN low side On Resistance	R_{SWNL_ON}	Gate Driver = 5V		250		mΩ
		Gate Driver = 3V		300		mΩ
SWN Cycle-by-Cycle Current Limit	I_{SWN_LIM}		2.5	3		A
SWN Leakage Current	I_{SWN_LK}	V_{SWN} = -18V, 14V			1.5	µA
VDDN	V_{DDN}	VDDN[7:0] = 56h, T_J = 25°C	-4.95 (-1%)	-5	-5.05 (+1%)	V
		-40°C < T_J < +150°C	-4.94 (-1.2%)	-5	-5.1 (+2%)	V
Thermal Shutdown Threshold (5)	T_{ST}	Rising edge		170		°C
		Hysteresis		20		°C

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 5V, T_J = -40°C to +150°C, typical value is at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Disconnection MOS (Between VBST and VDDP)						
R_{DS_ON} of disconnection MOS		VBST = 9V		250		mΩ
Fault signal (Fault)						
Fault pull low resister	R_{FF}			100		Ω
Positive charge pump						
VGH output voltage	V_{GH}	VGH[7:0] = 7Bh,T_J = 25°C	-1.39%	17.3	+2.37%	V
		-40°C < T_J < +150°C	-1.97%	17.3	+3.87%	V
High side driver on resistance		output 50mA		4		Ω
Gate shaping						
IGS high level threshold	V_{IGS_HI}		1.4			V
IGS low level threshold	V_{IGS_LO}				0.6	V
OGS minimum output voltage	V_{OGS_MIN}	OGS_min[7:0] = 00h	1.75	2	2.33	V
Negative charge pump						
VGL output voltage	V_{GL}	VGL[7:0] = A0h, T_J = 25°C	-7.87 (-1.63%)	-8	-8.17 (+2.13%)	V
		-40°C < T_J < +150°C	-7.85 (-1.88%)	-8	-8.25 (+3.13%)	V
High side driver on resistance		output 50mA		4		Ω
VCOM Buffer						
VCOM voltage range	V_{COM_RANGE}		VDDN+2		VDDP-2	V
			-13.19		+19.8	V
VCOM voltage	V_{COM}	VCOM[7:0] = 7Bh, T_J = 25°C	-1.2%	4.413	+1.2%	V
Input bias current	$I_{IN\_VCOM\_BIAS}$		-300	10	300	nA
VCOM output current capability	I_{VCOM}	VDDN+2V, VDDP-2V		25		mA
Delay Time(power on/off sequence)						
VGL delay time	T_{DLYGL}	DLYGL[3:0] = 0001b		2		ms
VGH delay time	T_{DLYGH}	DLYGH[3:0] = 0001b		2		ms
VDDP delay time	T_{DLYDP}	DLYDP[3:0] = 0001b		2		ms
I²C INTERFACE						
Input Logic Low	V_{IL}				0.99	V
Input Logic High	V_{IH}		2.31			V
Output logic low(5)	V_{OL}	I_{LOAD} = 3mA			0.4	V
SCL clock frequency(5)	f_{SCL}		10		1000	kHz
Bus free Time(5)	t_{BUF}	Between stop and start condition	0.5			µs
Holding time after (repeated) start condition(5)	t_{HD_STA}	After this period, the first clock is generated	0.26			µs
Repeated start condition set-up time(5)	t_{SU_STA}		0.26			µs
Stop condition set-up time(5)	t_{SU_STO}		0.26			µs

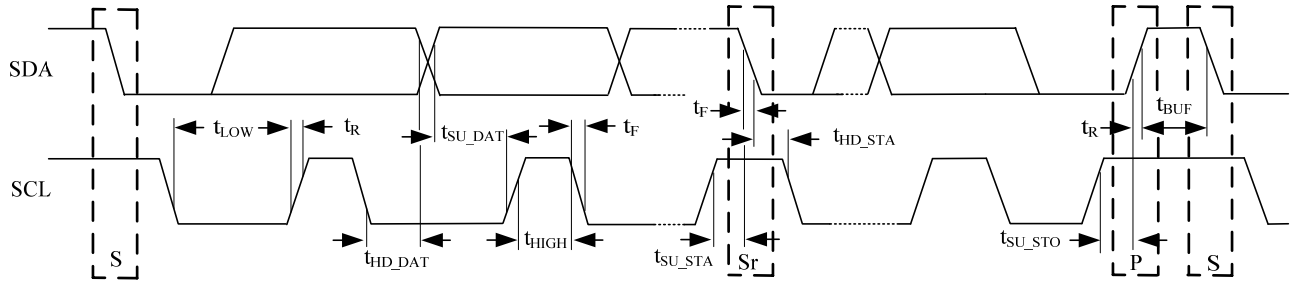
ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 5V, T_J = -40°C to +150°C, typical value is at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
I²C INTERFACE (*Continued*)						
Data hold time(5)	t_{HD_DAT}		0			ns
Data set-up time(5)	t_{SU_DAT}		50			ns
Clock low timeout(5)	$t_{TIMEOUT}$		25		35	ms
Clock low time(5)	t_{LOW}		0.5			µs
Clock high time(5)	t_{HIGH}		0.26			µs
Clock/data fall time(5)	t_F				120	ns
Clock/data rise time(5)	t_R				120	ns

Notes:

5) Typical values are guaranteed by design, not production tested.



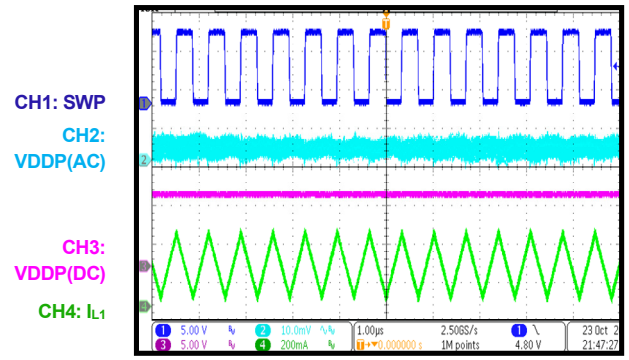
S = Start Condition
Sr = Repeated Start Condition
P = Stop Condition

Figure 2: I²C Compatible Interface Timing Diagram

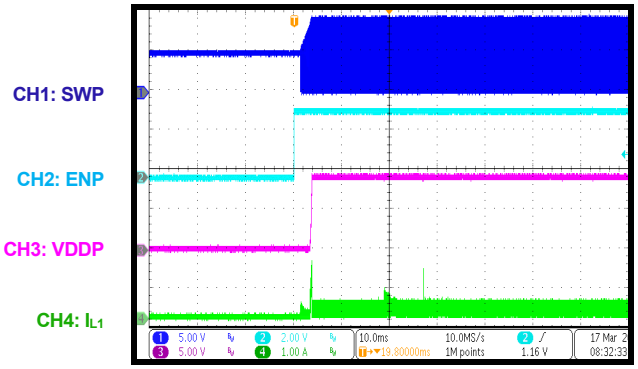
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 5V, V_{DDP} = 9V, V_{GH} = 17.3V, V_{GL} = -8V, V_{DDN} = -5V, L1 = L2 = 4.7µH, f_{SW} = 1.4MHz, T_A = 25°C, unless otherwise noted.

VDDP: Steady State
VDDP load = 100mA



VDDP: ENP Power On
VDDP load = 100mA



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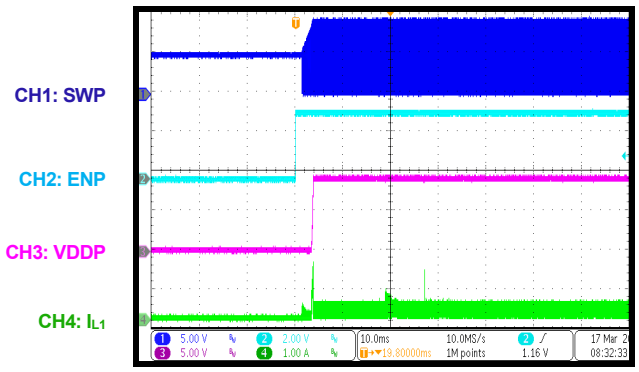
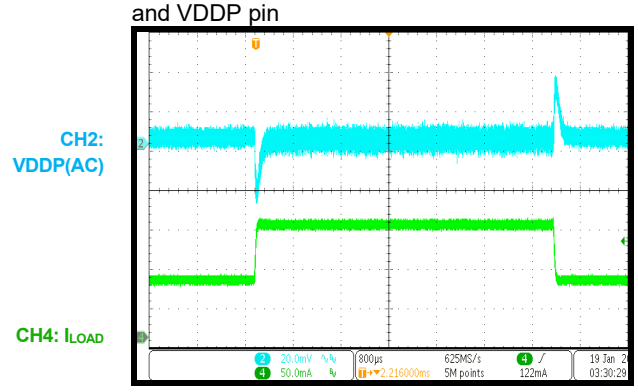
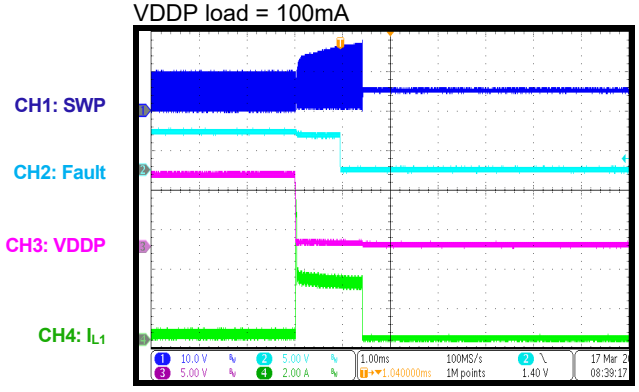


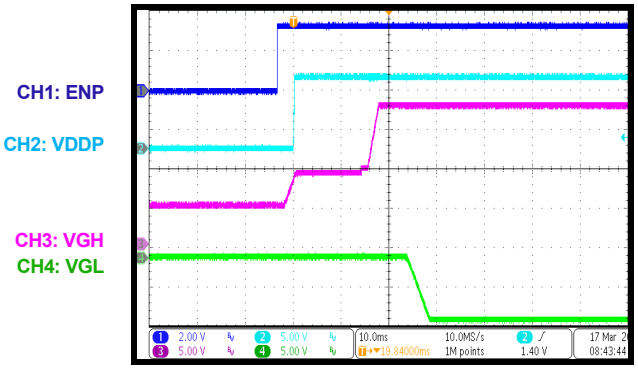
VDDP: Load Transient Response
VDDP load = 70mA to 140mA, 10µF for VBST and VDDP pin



VDDP: VDDP Short to GND Protection
VDDP load = 100mA



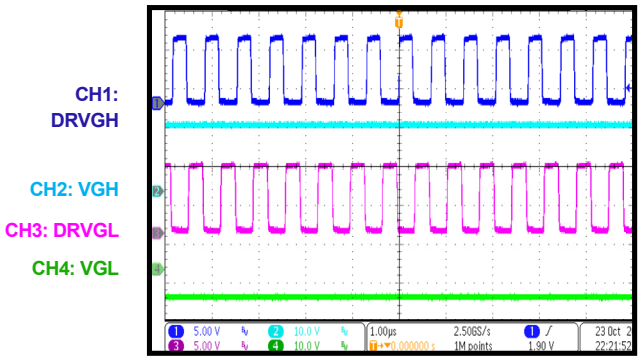
VGH/VGL: ENP Power On
DLYGH = 15ms, DLYGL = 25ms, DLYDP = 0ms, no Load



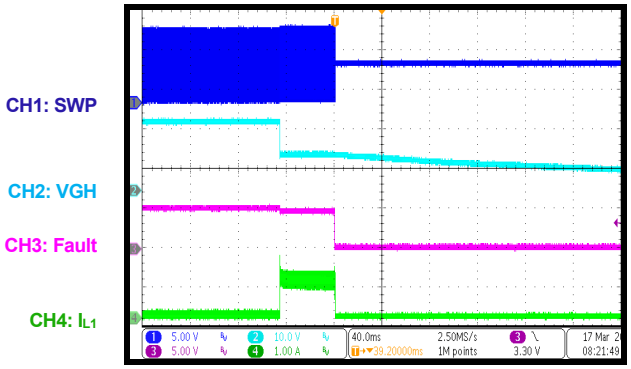
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{DDP} = 9V, V_{GH} = 17.3V, V_{GL} = -8V, V_{DDN} = -5V, L1 = L2 = 4.7µH, f_{SW} = 1.4MHz, T_A = 25°C, unless otherwise noted.

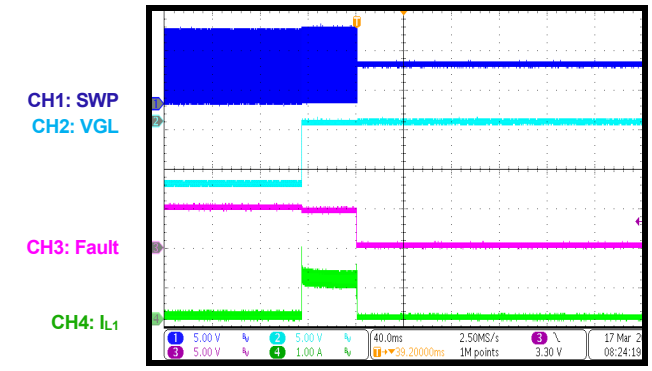
VGH/VGL: Steady State
VGH and VGL load = 50mA



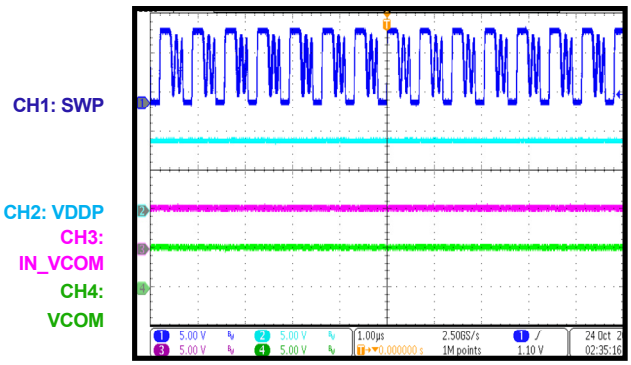
VGH/VGL: VGH Short to VBST
No load



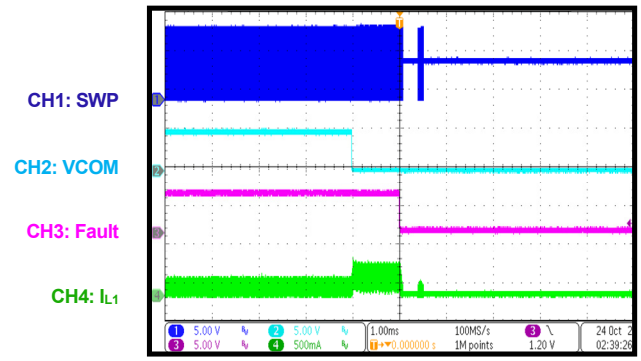
VGH/VGL: VGL Short to GND
No load



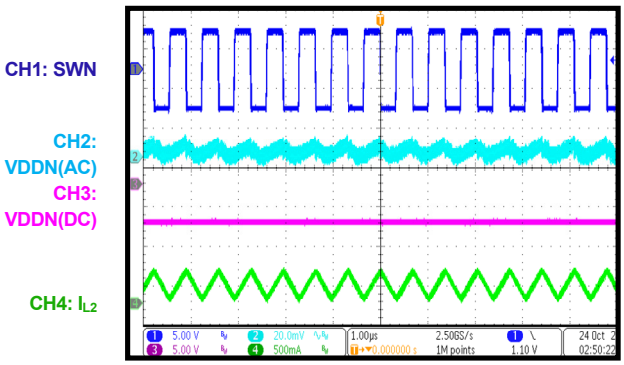
VCOM: Steady State
IN_VCOM = 5V, VCOM load = 25mA



VCOM: VCOM Short to GND
IN_VCOM = 5V, VCOM load = 25mA



VDDN: Steady State
VDDN load = 100mA



TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

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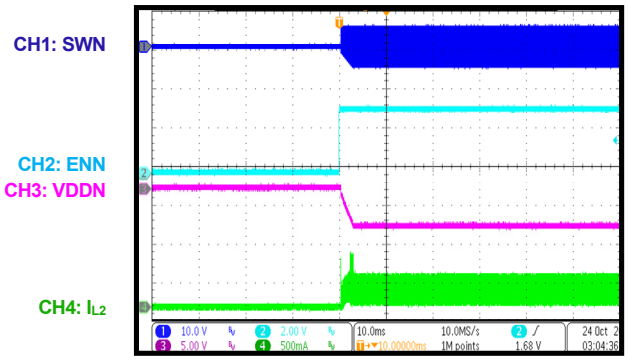
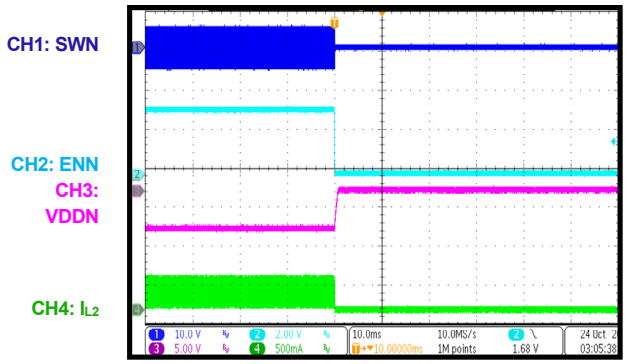
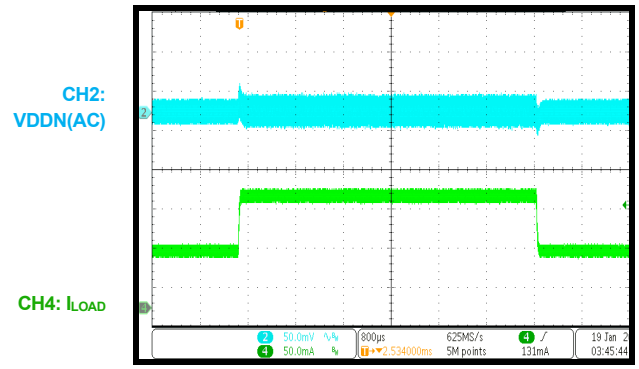
VDDN: ENN Power On
VDDN load = 100mA



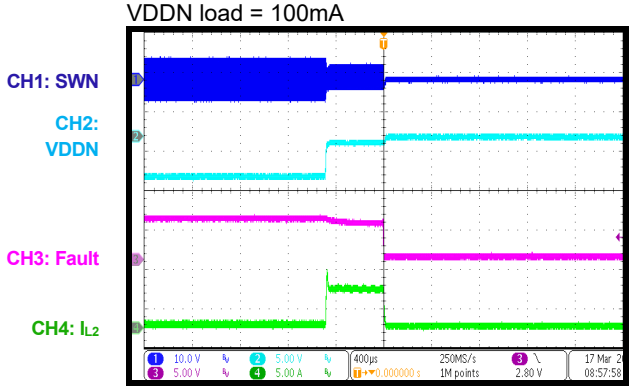
VDDN: ENN Power Off
VDDN load = 100mA



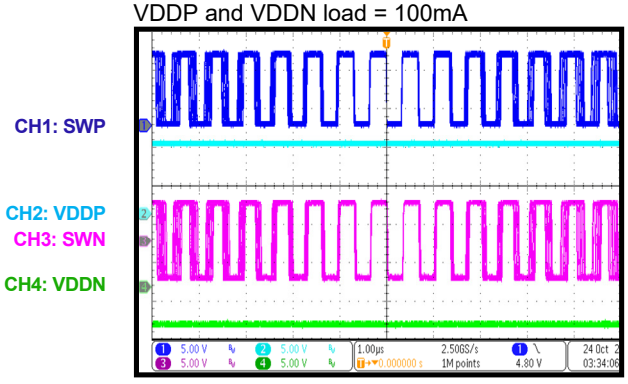
VDDN: Load Transient Response
VDDN load = 70mA to 140mA, 10µF for VDDN pin



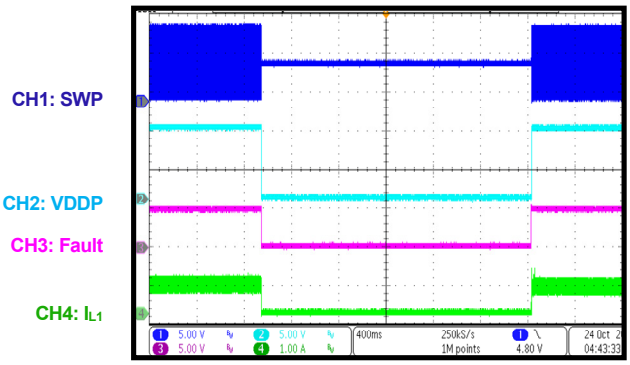
VDDN: VDDN Short to GND Protection
VDDN load = 100mA



Frequency Spread Spectrum
Modulation frequency = 1/100 of f_{SW},
Jitter range = 5% of f_{SW},
VDDP and VDDN load = 100mA



Over-Temperature Protection
VDDP load = 300mA, Heat the IC then recover



FUNCTIONAL BLOCK DIAGRAM

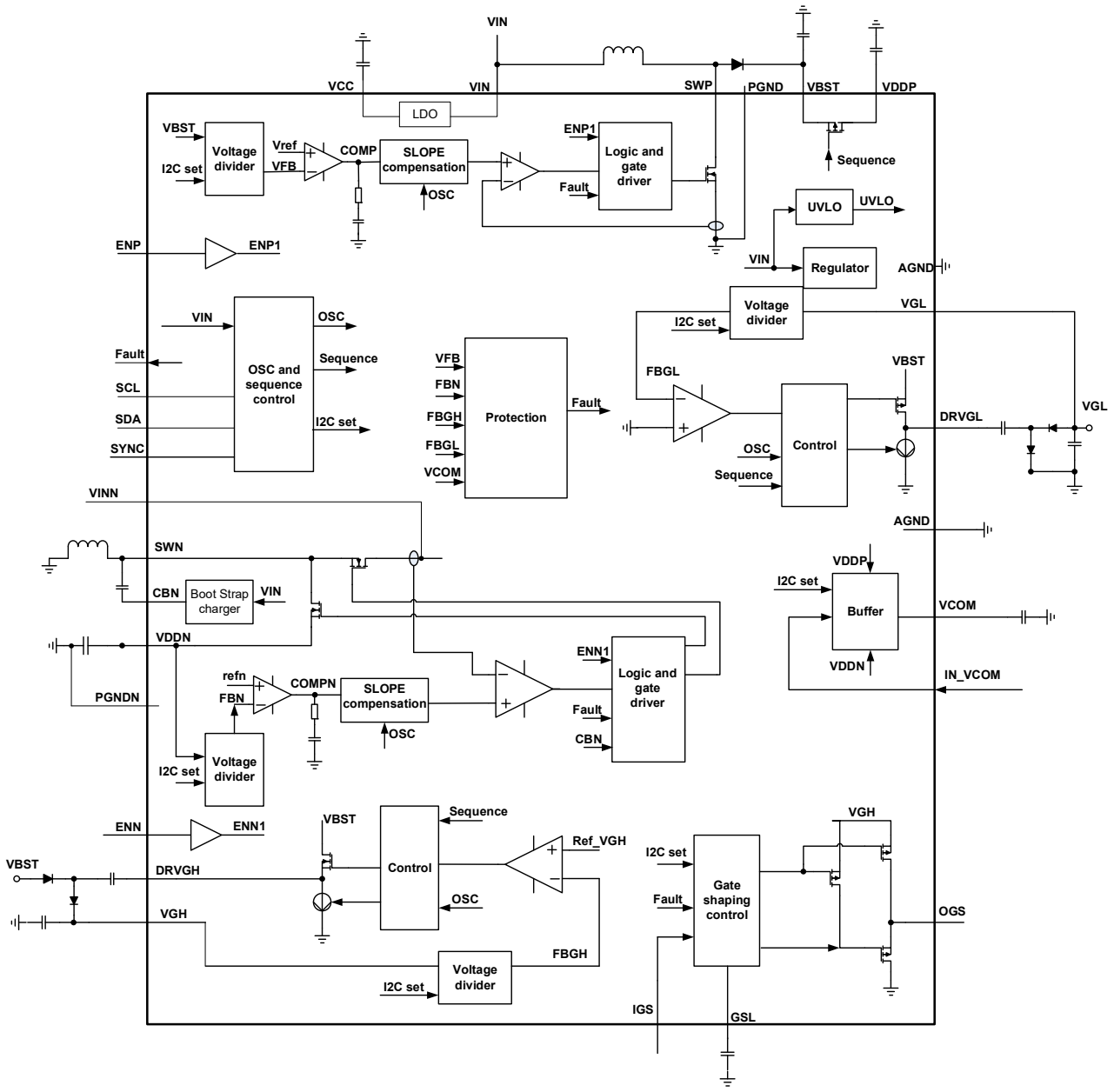


Figure 3: Functional Block Diagram

OPERATION

The MPQ5613T is an integrated power supply for automotive LCD TFT Bias. It integrates a boost converter, a synchronous buck-boost inverter, an adjustable positive charge pump output and an adjustable negative charge pump output for the gate voltages. It also includes a VCOM Buffer and a gate voltage shaping function for minimizing the external components. It is designed to power TFT LCD panels from a regulated 3.3V or 5V supply, or the 12V battery directly.

The boost converter and the buck-boost inverter are controlled independently and they could be set by I²C. The positive and negative charge pump could be set to a proper value by I²C.

Internal 5V Regulator

The MPQ5613T includes an internal linear regulator (VCC). When VIN is greater than 5.5V, this regulator outputs a typical 5V power supply to the internal MOSFET switch gate driver and the internal control circuitry.

When VINP is smaller than 5V and bigger than its UVLO, IC could work normally and the VCC will be almost equal to VINP. However, low VINP maybe will cause bigger $R_{DS(ON)}$, especially VIN≤2.7V.

Boost Converter

The fixed-frequency (set by FSET[2:0]) boost converter employs a current-mode control architecture that maximizes loop bandwidth to provide fast-transient responses needed for TFT LCD driver. High switching frequency allowing for smaller inductors and capacitors minimizes board space and thickness.

ENP pin and ENP bit

The boost converter is controlled by ENP pin and ENP bit. Both of them is high, the boost converter starts working; any one of them is low, the boost converter stops working.

VDDP

The VDDP voltage can be set from 2.7V to 9.1V with 50mV/step and from 9.2V to 21.8V with 100mV/step by register VDDP[7:0]. The default VDDP voltage is 9V.

Note: To keep the normal operation of Boost converter, the VDDP voltage should be greater than input voltage.

The VDDP delay time when power on can be set from 0ms to 65ms by register DLYDP[3:0]. The starting point of delay time is when VBST voltage reaches 90% of set VDDP voltage. Once the delay time ends, the disconnect MOS between VBST and VDDP turns on, and VDDP voltage starts establishing.

Boost Disconnect MOS

The output of the boost converter (VBST) could be disconnected from the real output VDDP for the TFT driver, through an internal MOSFET.

If the VIN is low and the input power line from previous DC/DC to the MPQ5613T is long, the VINP pin maybe will be pulled to lower than its UVLO because of a big inrush current when the disconnect MOS turns on moment, then IC will work abnormally. To avoid this, below two methods are recommended as Figure 4 shows.

1. Providing a separate routing (as the red line shows in Figure 4) to VINP pin from the previous DC/DC output to eliminate the voltage drop with long power routing.
2. Adding a RC filter on the VINP pin (Rf and Cf in Figure 4), 24Ω+10μF are recommended.

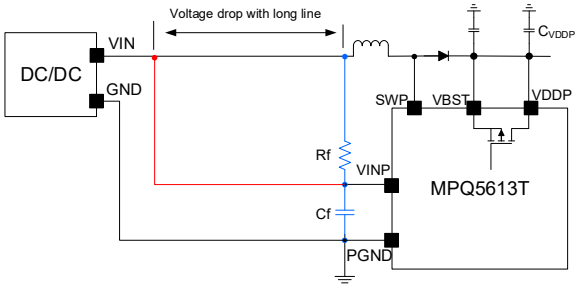


Figure 4: Recommended VINP pin circuit

Buck-boost Inverter for VDDN

The buck-boost inverter also employs a current-mode control architecture and its switching frequency is same as the boost converter. The IC employs a interleave(180º) buck-boost and boost control for better EMI. There is an internal switching clock with 50% duty cycle. The rising

edge of clock controls the low-side MOSFET of boost converter turns on, and the falling edge of clock controls the high-side MOSFET of buck-boost inverter turns on.

ENN Pin and ENN Bit

The buck-boost inverter is controlled by ENN pin and ENN bit. Both of them is high, the buck-boost inverter starts working; any one of them is low, the buck-boost inverter stops working.

The VDDN voltage can be set from -0.7V to -10.3V with 50mV/step and from -10.4V to -16.6V with 100mV/step by register VDDN[7:0]. The default VDDN voltage is -5V.

Frequency Synchronization function

If the FSYNC_EN bit is set to 0, the switching frequency is synchronized by an external signal on Sync pin.

Note: FSYNC_edge bit sets the synchronization edge: rising edge or falling edge. If FSYNC_edge=0b, the rising edge of the synchronizing signal synchronizes the turning on of boost MOSFET. If FSYNC_edge=1b, the falling edge of the synchronizing signal synchronizes the turning on of boost MOSFET.

Frequency Spread Spectrum

The MPQ5613T uses switching frequency jitter to spread the switching frequency spectrum to improve EMI performance. This reduces the spectrum spike around the switching frequency and its harmonic frequencies.

The frequency jitter range is selected by the SPR[1:0].

- SPR[1:0]=00b, no spread spectrum
- SPR[1:0]=01b(default), the jitter range is 5% of the switching frequency (±2.5%)
- SPR[1:0]=10b, the jitter range is 10% of the switching frequency (±5%)
- SPR[1:0]=11b, the jitter range is 20% of the switching frequency (±10%)

The modulation frequency is selected by SPF bit.

- SPF=0b (default), the modulation frequency is 1/100 of the switching frequency
- SPF=1b, the modulation frequency is 1/200 of the switching frequency

Figure 5 shows the frequency spread spectrum function when setting f_{SW} = 1.4MHz, SPR[1:0] = 01b and SPF = 0b.

The jitter range is 5% of f_{SW}. The maximum f_{SW} is about 1.435MHz, and the minimum f_{SW} is about 1.365MHz. The modulation frequency is 1/100 of the switching frequency, which is about 14kHz.

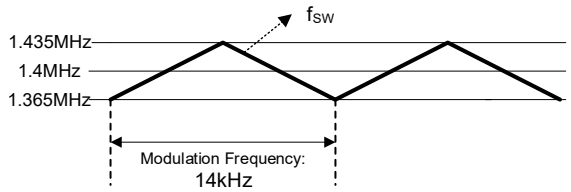


Figure 5: Frequency Spread Spectrum

Positive Charge Pump for VGH

MPQ5613T integrates a positive charge pump converter for VGH. Figure 6 shows the external circuit of positive charge pump.

The VGH voltage can be set from 5V to 17.8V with 100mV/step and from 18V to 43.2V with 200mV/step by register VGH[7:0]. The default VGH voltage is 17.3V.

The VGH delay time when power on can be set from 0ms to 65ms by register DLYGH[3:0]. The starting point of the delay time is when the VBST voltage reaches 90% of the set VDDP voltage. After the delay time ends, the VGH voltage starts establishing with soft-start.

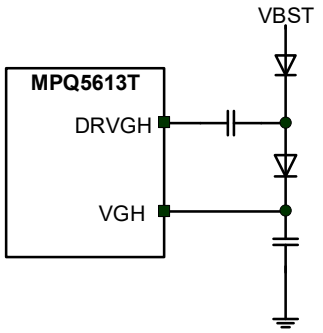


Figure 6: External Circuit of Positive Charge Pump

Negative Charge Pumps for VGL

MPQ5613T integrates a negative charge pump converter for VGL. Figure 7 shows the external circuit of negative charge pump.

The VGL voltage can be set from 0V to -9.6V with 50mV/step and from -9.7V to -15.9V with 100mV/step by register VGL[7:0]. The default VGH voltage is -8V.

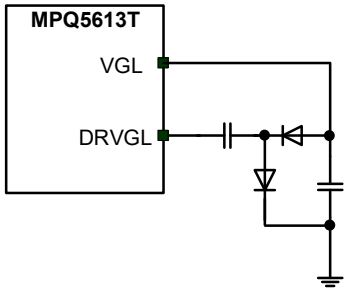


Figure 7: External Circuit of Negative Charge Pump

The VGL delay time when power on can be set from 0ms to 65ms by register DLYGL[3:0]. The starting point of the delay time is when the VBST voltage reaches 90% of the set VDDP voltage. After the delay time ends, the VGL voltage starts establishing with soft-start.

VCOM Buffer

The VCOM buffer is supplied from VDDN and VDDP, therefore VCOM could output a positive or a negative voltage between VDDN+2V and VDDP-2V.

The VCOM buffer is active after VDDP and VDDN are established and Fault pin is high.

Two methods set the VCOM Buffer voltage:

1. Set the VCOM_EN bit to 0, the VCOM buffer output voltage follows the IN_VCOM pin voltage.
2. Set the VCOM_EN bit to 1, VCOM buffer output voltage follows the VCOM_RANGE[1:0] and VCOM[7:0].

Gate Voltage Shaping

The gate voltage shaping circuit output OGS is used to drive the TFT. The gate voltage shaping circuit is supplied from VGH, which is typically the output of the positive charge pump. The gate voltage shaping output OGS is controlled by the input signal IGS. When IGS is high, OGS outputs a high level voltage VGH, and when IGS is low, OGS outputs a low level. The GSLR[2:0] could set the OGS falling time. The OGS minimum level is set by OGS_min[7:0]. Figure 8 shows the control sequence of OGS pin.

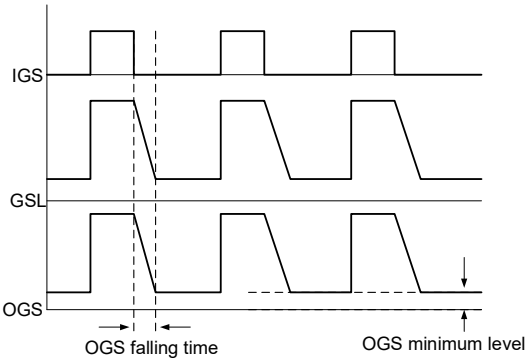


Figure 8: The Control Sequence of OGS Pin

The gate shaping function is active when the positive charge pump output has achieved 90% of its target voltage. The gate shaping output OGS is then controlled by its input IGS.

Note: it is recommended to add a 1nF between OGS and GND for holding the low level of OSG well.

Power-On/off Sequencing

The MPQ5613T sequences its outputs at startup through the time sequence programmable by I²C.

When the input voltage VIN rises above the under-voltage lockout (UVLO) threshold, IC is enabled. The boost converter and buck-boost inverter are controlled independently by their enable signal ENP and ENN. When ENP is high, the boost converter starts to work and when ENN is high, the buck-boost inverter starts to work.

After ENP is high, the Boost start working with Soft Start. When the VBST up to 90% of VDDP, it is the origin to count the delay time of DLYDP, DLYGH and DLYGL.

Figure 9 shows the delay time sequence among VDDP, VGH and VGL when setting the delay time DLYDP < DLYGH < DLYGL by the register 0x00 and 0x01. The following are detailed explanations of time duration in Figure 9.

T_{S_VB}: Soft-start time of VBST.

T_{D_P}: Delay time of VDDP when power on, it can be set by DLYDP[3:0].

T_{S_N}: Soft-start time of VDDN.

T_{D_H}: Delay time of VGH when power on, it can be set by DLYGH[3:0].

T_{S_H}: Soft-start time of VGH.

T_{D_L}: Delay time of VGL when power on, it can be set by DLYGL[3:0].

T_{S_L}: Soft-start time of VGL.

The VDDN is controlled by ENN pin and ENN bit independently.

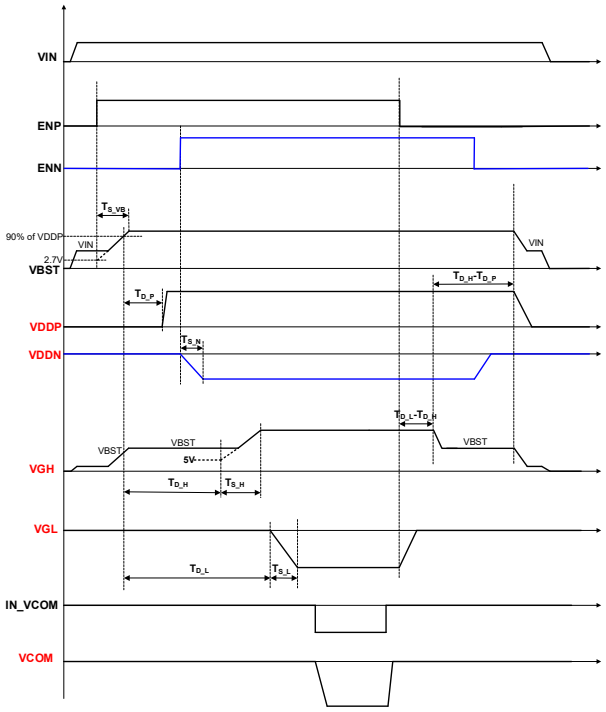


Figure 9: Power on/off Sequence when VGL Established after VDDP

The VDDN, VGH and VGL could be established before or after VDDP.

The power off control is reverse from the power on sequence. The outputs which are established lastly would be powered off firstly. If VIN drops lower than its UVLO threshold, the IC shuts down immediately. Figure 10 shows the power on/off sequence when VGL established before VDDP.

Note: During the power on and power off process of VDDP, VGH and VGL, don't change the registers DLYDP[3:0], DLYGH[3:0] and DLYGL[3:0] by I²C, otherwise the power on/off sequence may be incorrect.

Note: It is recommended to pull the ENN pin to low for above 1ms when turning off the VDDN, and pull the ENP pin to low until the power off sequence of VDDP, VGH and VGL ends.

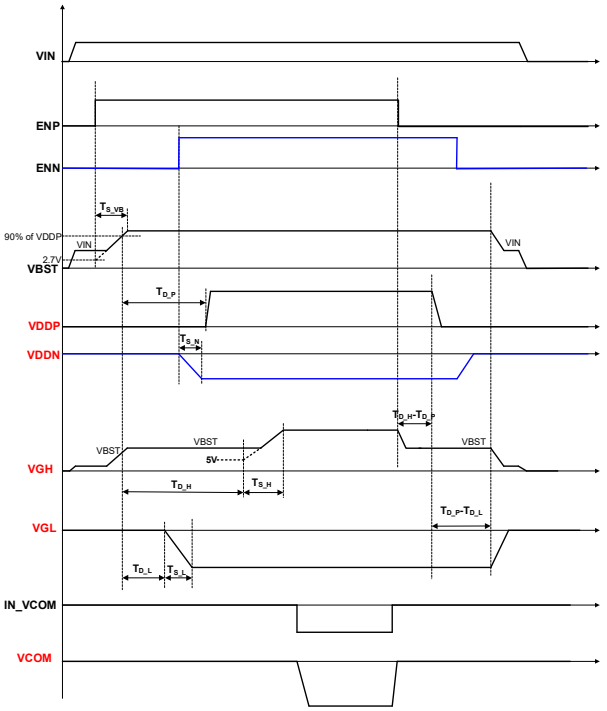


Figure 10: Power on/off Sequence when VGL Established before VDDP

When VGH is powered by VBST externally (In Figure 9 and 10), the VGH voltage is precharged to VBST voltage firstly, and the VGH voltage will follow VIN voltage before Boost converter is enabled. To eliminate this VIN platform voltage, the VGH can also be powered by VDDP externally as the following Figure 11 shows.

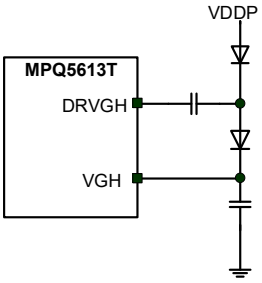


Figure 11: External Circuit of Positive Charge Pump when VGH is Powered by VDDP

The Figure 12 shows the power on/off sequence when VGH is powered by VDDP externally. Before the delay time of VGH ends, the VGH voltage is precharged to VDDP voltage from 0V, and VIN platform voltage is eliminated.

Note: If the Figure 11 circuit is used to eliminate the VIN platform voltage of VGH, the VDDP voltage must establish before VGH and turn off after VGH, otherwise VGH under-voltage protection (UVP) may be triggered.

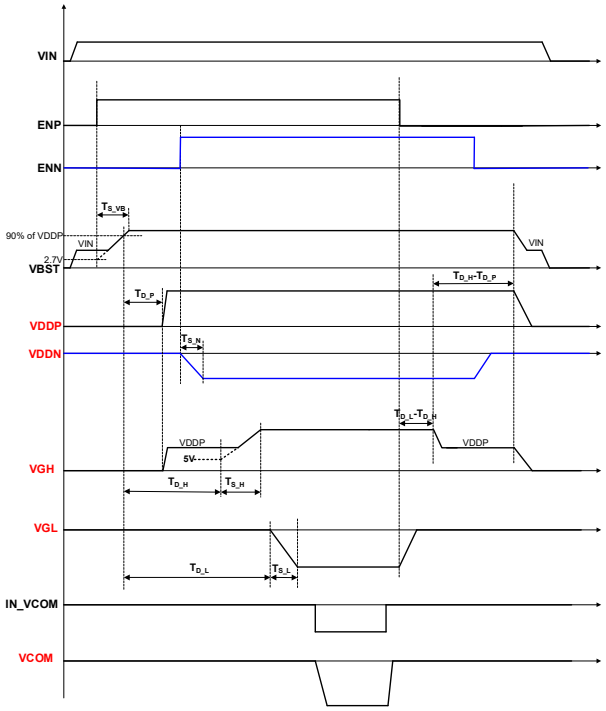


Figure 12: Power on/off Sequence when VGH is powered by VDDP

The VCOM buffer is active after VDDP and VDDN are established and Fault pin is high.

Soft-Start

The MPQ5613T integrates soft-start function for VBST, VDDN, VGH and VGL. Table 1 shows the soft-start time of 4 outputs, and each step is 32μs. For example, the soft-stat time of VGL can be evaluated by the following methods:

1. When VGL voltage (V_{GL}) ≥ -9.6V, the soft-start time of VGL is about (-V_{GL})/0.05*32μs.
2. When -15.9V ≤ V_{GL} ≤ -9.7V, the soft-start time of VGL is about 6144us+(-9.6V-V_{GL})/0.1*32μs.

Note: During the soft-start time of VDDN, VGH and VGL, their under-voltage protections (UVP) are disabled. After the soft start time end, the UVP detection time of VDDN is 0.5ms, VGH and VGL are 48ms. The UVP of VDDP is disabled during the T_{S_VB} and T_{D_P}.

Table 1: Soft-Start Time

Name	Range1	/step	Range2	/step
VBST	2.7V~9.1V	50mV	9.2V~21.8V	100mV
VDDN	-0.7V~-10.3V	50mV	-10.4V~-16.6V	100mV
VGH	5V~17.8V	100mV	18V~43.2V	200mV
VGL	0V~-9.6V	50mV	-9.7V~-15.9V	100mV

Protection

The MPQ5613T includes robust protections to guarantee safe operation of the device. The following are the major protection modes:

- Outputs under-voltage protection (UVP)
- Output over-current protection for VCOM
- Cycle-by-cycle current limit protection for SWP and SWN.
- Output current limit protection for VDDP
- VIN under-voltage lockout (UVLO)
- Over-temperature protection (OTP)

Output Under-Voltage Protection (UVP)

Each of the 4 outputs (VDDP, VDDN, VGH, and VGL) has an internal comparator that monitors its respective output voltage. When anyone of the 4 output voltages is below approximately 60% of the set regulation voltage, an internal counter starts. If the fault condition lasts for UVP detection time (T_{UVP}), all outputs are disabled. The Fault pin is pulled to low and the corresponding fault bit is set to 1.

The T_{UVP} of VDDP is 1ms, the T_{UVP} of VDDN is 0.5ms, the T_{UVP} of VGH and VGL is 48ms.

Note: The UVP is disabled during the soft-start process of corresponding output.

There are two protection modes for UVP by setting PMODE bit:

- PMODE = 0b (latch off mode), once the UVP of anyone output is triggered, all outputs are disabled and the IC latches off. The Fault pin is pulled to low and the corresponding fault bit is set to 1. Only when Vin resets, the IC can restart, the Fault pin can recover to high and fault bit can be cleared.

- PMODE=1b (hiccup mode), once the UVP of anyone output is triggered, all outputs are disabled. The MPQ5613T will detect if the fault is removed every 10ms. Once the fault is removed, the MPQ5613T recovers working and the Fault pin is released to high again. The fault bit can be cleared by writing 1 to corresponding bit after fault condition removed.

Output Over-Current Protection (OCP) for VCOM

The VCOM buffer has output over-current protection (OCP). When the VCOM's output sourcing current above about 36mA or sinking current above about 46mA and lasts for 1ms, the protection is triggered. All outputs are disabled and the Fault pin is pulled low. The protection mode can also be set by PMODE bit.

Cycle-by-Cycle Current Limit Protection for SWP and SWN

To prevent the external components from exceeding current stress rating in some cases, the MPQ5613T has cycle-by-cycle current limit protection for SWP current of boost converter and SWN current of buck-boost inverter. If the switching current reaches the current limit threshold, the IC stops switching until the next clock cycle. The Fault pin is not pulled to low under this fault condition.

Output Current Limit Protection for VDDP

The MPQ5613T integrates the output current limit protection for VDDP. The maximum output current is clamped to the current limit threshold about 600mA. When the output current limit condition occurs, The Fault pin is not pulled to low under this fault condition.

VIN under-voltage lockout (UVLO)

The MPQ5613T integrates VIN under-voltage lockout (UVLO) protection. The internal circuit does not work until VINP reaches the UVLO rising threshold.

Over-temperature protection (OTP)

When the die's junction temperature (T_J) exceeds the upper threshold (T_{ST}), the IC shuts down. And IC recovers to normal operation when temperature drops below the lower threshold. Typically, the hysteresis value is about 20°C.

I²C Interface Register Description

I²C Chip Address:

The 7 bits MSB device address can be configured via one-time programmable memory (OTP). MPS can provide the customized IC address for the user, the default IC address is 0x57. If user wants other IC addresses, please contact an MPS FAE to obtain a customized suffix "xxxx" value for MPQ5613TGRE-xxxx-AEC1-Z.

After the START condition, the I²C-compatible master sends a 7-bit address followed by an eighth read (Read: 1) or write (Write: 0) bit.

Figure 13 shows the I²C-compatible device address of MPQ5613TGVE-0000-AEC1-Z.

1	0	1	0	1	1	1	R/W

Figure 13: I²C- Compatible Device Address of MPQ5613TGVE-0000-AEC1-Z

I²C REGISTER MAP

Register Short Name	R/W	Add	Default	D7	D6	D5	D4	D3	D2	D1	D0
DELAY1	**R/W**	**00H**	75H	DLYGL[3:0]				DLYGH[3:0]			
DELAY2	**R/W**	**01H**	00H	Reserved				DLYDP[3:0]			
VDDP	**R/W**	**02H**	7EH	VDDP[7:0]							
VDDN	**R/W**	**03H**	56H	VDDN[7:0]							
VGH	**R/W**	**04H**	7BH	VGH[7:0]							
VGL	**R/W**	**05H**	A0H	VGL[7:0]							
CON1	**R/W**	**06H**	00H	Reserved		FSYNC_ EN	FSYNC_ edge	PMODE	GSLR[2:0]		
OGS_ min	**R/W**	**07H**	00H	OGSL[7:0]							
CON2	**R/W**	**08H**	DAH	ENP	ENN	FSET2	FSET1	FSET0	SPR1	SPR0	SPF
VCOMS	**R/W**	**09H**	04H	Reserved					VCOM_RANGE[1:0]		VCOM_ EN
VCOM	**R/W**	**0AH**	7BH	VCOM[7:0]							
Fault	**R/W**	**0BH**	00H	Reserved		FLT_ VDDP	FLT_ VDDN	FLT_ VGH	FLT_ VGL	FLT_OTP	FLT_ VCOM
DEV_ID	**R**	**0CH**	38H	ID[7:0]							

Notes:

6) The default values are for the MPQ5613TGVE-0000-AEC1-Z registers. The default value of 0x00~0x0A can be redefined if the one-time programmable function is available.
7) Leave corresponding pins float if internal registers are used.
8) Please don't change the default value of reserved registers.

REGISTER DESCRIPTION

DELAY1 (0x00)

The DELAY1 command sets the delay time of VGL and VGH.

Bits	Access	Bit Name	Default	Description
7:4	R/W	DLYGL[3:0]	0111b	Delay time for VGL output set (refer to VBST up to 90% of VDDP). 0000 to 1111 sets the delay time at 0ms, 2ms, 5ms, 8ms, 10ms, 15ms, 20ms, 25ms(default), 30ms, 35ms, 40ms, 45ms, 50ms, 55ms, 60ms, 65ms.
3:0	R/W	DLYGH[3:0]	0101b	Delay time for VGH output set (refer to VBST up to 90% of VDDP) 0000 to 1111 sets the delay time at 0ms, 2ms, 5ms, 8ms, 10ms, 15ms (default), 20ms, 25ms, 30ms, 35ms, 40ms, 45ms, 50ms, 55ms, 60ms, 65ms.

DELAY2 (0x01)

The DELAY2 command sets the delay time of VDDP.

Bits	Access	Bit Name	Default	Description
7:4	R	RESERVED	0000b	Reserved
3:0	R/W	DLYDP[3:0]	0000b	Delay time for VDDP output set (refer to VBST up to 90% of VDDP). 0000 to 1111 sets the delay time at 0ms(default), 2ms, 5ms, 8ms, 10ms, 15ms, 20ms, 25ms, 30ms, 35ms,40ms, 45ms, 50ms, 55ms, 60ms, 65ms.

VDDP (0x02)

The VDDP command sets the voltage of VDDP.

Bits	Access	Bit Name	Default	Description
7:0	R/W	VDDP[7:0]	7Eh	VDDP output voltage from 2.7V to 21.8V. 0 to 128 sets the VDDP voltage from 2.7V to 9.1V, 0.05V/step; 129 to 255 sets the VDDP voltage from 9.2V to 21.8V, 0.1V/step. The default VDDP voltage is 9V.

VDDN (0x03)

The VDDN command sets the voltage of VDDN.

Bits	Access	Bit Name	Default	Description
7:0	R/W	VDDN[7:0]	56h	The VDDN output voltage from -0.7V to -16.6V. 0 to 192 sets the VDDN voltage from -0.7V to -10.3V, 0.05V/step; 193 to 255 sets the VDDN voltage from -10.4V to -16.6V, 0.1V/step. The default VDDN voltage is -5V.

VGH (0x04)

The VGH command sets the voltage of VGH.

Bits	Access	Bit Name	Default	Description
7:0	R/W	VGH[7:0]	7Bh	The VGH output voltage from 5V to 43.2V. 0 to 128 sets the VGH voltage from 5V to 17.8V, 0.1V/step; 129 to 255 sets the VGH voltage from 18V to 43.2V, 0.2V/step. The default VGH voltage is 17.3V.

VGL (0x05)

The VGL command sets the voltage of VGL.

Bits	Access	Bit Name	Default	Description
7:0	R/W	VGL[7:0]	A0h	The VGL output voltage from 0V to -15.9V. 0 to 192 sets the VGL voltage from 0V to -9.6V, 0.05V/step; 193 to 255 sets the VGL voltage from -9.7V to -15.9V, 0.1V/step. The default VGL voltage is -8V.

CON1 (0x06)

The CON1 command sets the switching synchronization function and the slew rate of OGS.

Bits	Access	Bit Name	Default	Description
7:6	R	RESERVED	00b	Reserved
5	R/W	FSYNC_EN	0b	Frequency synchronization enable: 0: Enable 1: Disable
4	R/W	FSYNC_ edge	0b	Frequency synchronization edge selection: 0: rising edge 1: falling edge
3	R/W	PMODE	0b	Protection Mode set: 0: latch off mode 1: hiccup mode, 10ms period.
2:0	R/W	GSLR[2:0]	000b	OGS gate shaping falling slew rate set 000 to 101 sets the slew rate (C_{GSL} = 68pF): 000:1 V/μs (default), 001:2 V/μs, …, 101:6V/μs (110/111 reserved)

OGS_min (0x07)

The OGS_min command sets the minimum voltage of OGS.

Bits	Access	Bit Name	Default	Description
7:0	R/W	OGS_min [7:0]	00h	Gate output voltage minimum level set. 2V~24V, 0.2V/step 00h: 2V (default) 6Eh: 24V 6Fh~FFh: reserved

CON2 (0x08)

The CON2 command sets the enable bits of VDDP and VDDN, switching frequency and spread spectrum.

Bits	Access	Bit Name	Default	Description
7	R/W	ENP	1b	Boost converter internal enable bit: (Boost converter is controlled by external ENP pin and internal ENP bit, pull ENP pin to high if use this bit.) 0: disable 1: enable
6	R/W	ENN	1b	Buck-boost inverter enable: (Buck-boost inverter is controlled by external ENN pin and internal ENN bit, pull ENN pin to high if use this bit) 0: disable 1: enable

5:3	R/W	FSET[2:0]	011b	Operating switching frequency set: 000: 350kHz 001: 650kHz 010: 950kHz 011: 1.4MHz 100: 2.2MHz 101: 3MHz (low accuracy) 110 and 111 are reserved.
2:1	R/W	SPR[1:0]	01b	Spread spectrum range set: 00: no spread spectrum 01: 5% of operating frequency 10: 10% of operating frequency 11: 20% of operating frequency
0	R/W	SPF	0b	Spread spectrum modulation frequency set: 0: 1/100 of operating frequency 1: 1/200 of operating frequency

VCOMS (0x09)

The VCOMS command sets the VCOM range and VCOM enable bit.

Bits	Access	Bit Name	Default	Description
7:3	R	RESERVED	00000b	Reserved
2:1	R/W	VCOM_ RANGE[1:0]	10b	If VCOM_RANGE=00, -13.19V to -2.99V If VCOM_RANGE=01, -3.05V to -0.5V If VCOM_RANGE=10, -0.507V to +9.693V If VCOM_RANGE=11, +9.6V to +19.8V
0	R/W	VCOM_EN	0b	I²C to set VCOM voltage Enable: 0: disabled, VCOM follows VCOM_IN pin 1: enabled, VCOM follows I²C set value

VCOM (0x0A)

The VCOM command sets the voltage of VCOM.

Bits	Access	Bit Name	Default	Description
7:0	R/W	VCOM[7:0]	7Bh	VCOM voltage set: If VCOM_RANGE=00, 00h to FFh sets the VCOM output voltage from -13.19V to -2.99V, 40mV/step. If VCOM_RANGE=01, 00h to FFh sets the VCOM output voltage from -3.05V to -0.5V, 10mV/step. If VCOM_RANGE=10, 00h to FFh sets the VCOM output voltage from -0.507V to +9.693V, 40mV/step. (default 4.413V) If VCOM_RANGE=11, 00h to FFh sets the VCOM output voltage from +9.6V to +19.8V, 40mV/step.

FAULT (0x0B)

The FAULT command reads the fault bits. In hiccup mode, once one fault is removed, write 1 to clear the corresponding fault bit.

Bits	Access	Bit Name	Default	Description
7:6	R	RESERVED	00b	Reserved
5	R/W	FLT_VDDP	0b	VDDP fault status output 0: no fault 1: fault
4	R/W	FLT_VDDN	0b	VDDN fault status output 0: no fault 1: fault
3	R/W	FLT_VGH	0b	VGH status output 0: no fault 1: fault
2	R/W	FLT_VGL	0b	VGL fault status output 0: no fault 1: fault
1	R/W	FLT_OTP	0b	Over Temperature fault status output 0: no fault 1: fault
0	R/W	FLT_VCOM	0b	VCOM fault status output 0: no fault 1: fault

DEV_ID (0x0C)

The DEV_ID reads the device ID.

Bits	Access	Bit Name	Default	Description
7:0	R/W	ID[7:0]	38h	Device ID.

APPLICATION INFORMATION

Selecting the Input Capacitor

The input capacitor reduces the surge current drawn from the input supply as well as the switching noise from the device. The input capacitor impedance at f_{SW} should be below the input source impedance to prevent the high-frequency switching current from passing through to the input. Use ceramic capacitors with X5R or X7R dielectrics for their low ESR and small temperature coefficients. It is recommended to use >10μF ceramic capacitor for Boost and Buck-Boost input respectively.

Selecting the Inductor

The MPQ5613T requires two inductors for Boost converter and Buck-Boost inverter. A larger-value inductor results in less ripple current, lower peak inductor current, and less stress on the internal MOSFET. However, the larger-value inductor has a larger physical size, higher series resistance, and lower saturation current. Choose an inductor that does not saturate under the worst-case load conditions.

It is recommended to use 4.7μH inductors for Boost and Buck-Boost for most applications.

With the given inductor value, the inductor DC current rating should be at least 40% higher than maximum peak inductor current for most applications. Inductor's DC resistance should be as small as possible for higher efficiency.

Selecting the Output Capacitor

The output capacitor keeps the output voltage (V_{OUT}) ripple small and ensures feedback loop stability. The output capacitor impedance must be low at f_{SW}. Lower capacitance may lead to increased voltage ripple. Generally, the lower I_{OUT}, the lower the required output capacitance. Ceramic capacitors with X7R dielectrics are recommended for their low-ESR characteristics. Figure 15 shows the recommended output capacitors for all outputs.

Selecting the Charge Pump Flying Capacitor

The flying capacitors are needed for positive and negative charge pump. It is recommended to use 100nF ceramic capacitors for most applications.

PCB Layout Guidelines

Careful attention must be given to the PCB layout and component placement. Efficient placement of the high-frequency switching path is critical to prevent noise and electromagnetic interference. For the best results, refer to Figure 14 and follow the guidelines below:

1. Recommend to connect the GND of VCC capacitor (C6) and VINP capacitor (C7) to the AGND (Pin 27) directly, and place these capacitors as close to the IC as possible.
2. The Boost switching key loop SWP Pin → Diode (D1) →VBST capacitor (C8 and C9) →PGND (Pin 5) should be as small as possible.
3. For the VGH and VGL part, the schottky diodes and flying capacitors should be as close as possible to the VGH, VGL, DRVGL, DRVGH and PGND (Pin 11).
4. The Buck-Boost key loop VINN Pin → VINN capacitor (C1 and C2) → VDDN capacitor (C3 and C4) → VDDN Pin should be as small as possible.
5. Connect AGND pins and PGND pins together on the thermal pad, and refer all logic signals (including SYNC, ENP, ENN, Fault, SCL and SDA) to AGND.

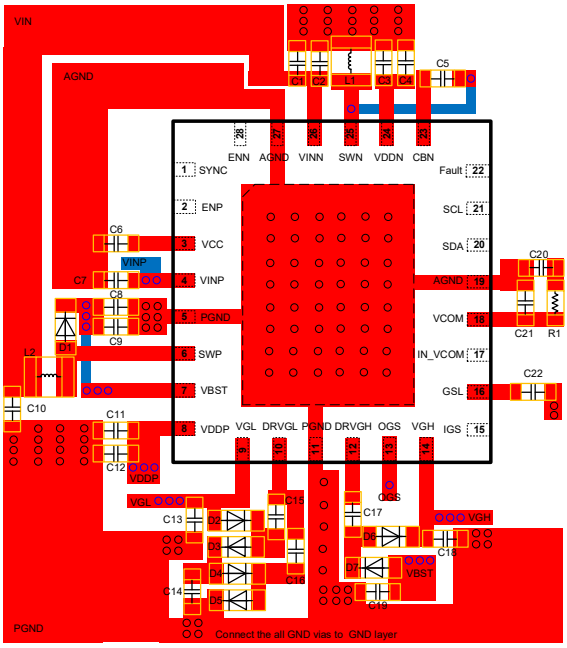


Figure 14: Recommended PCB Layout

TYPICAL APPLICATION CIRCUIT

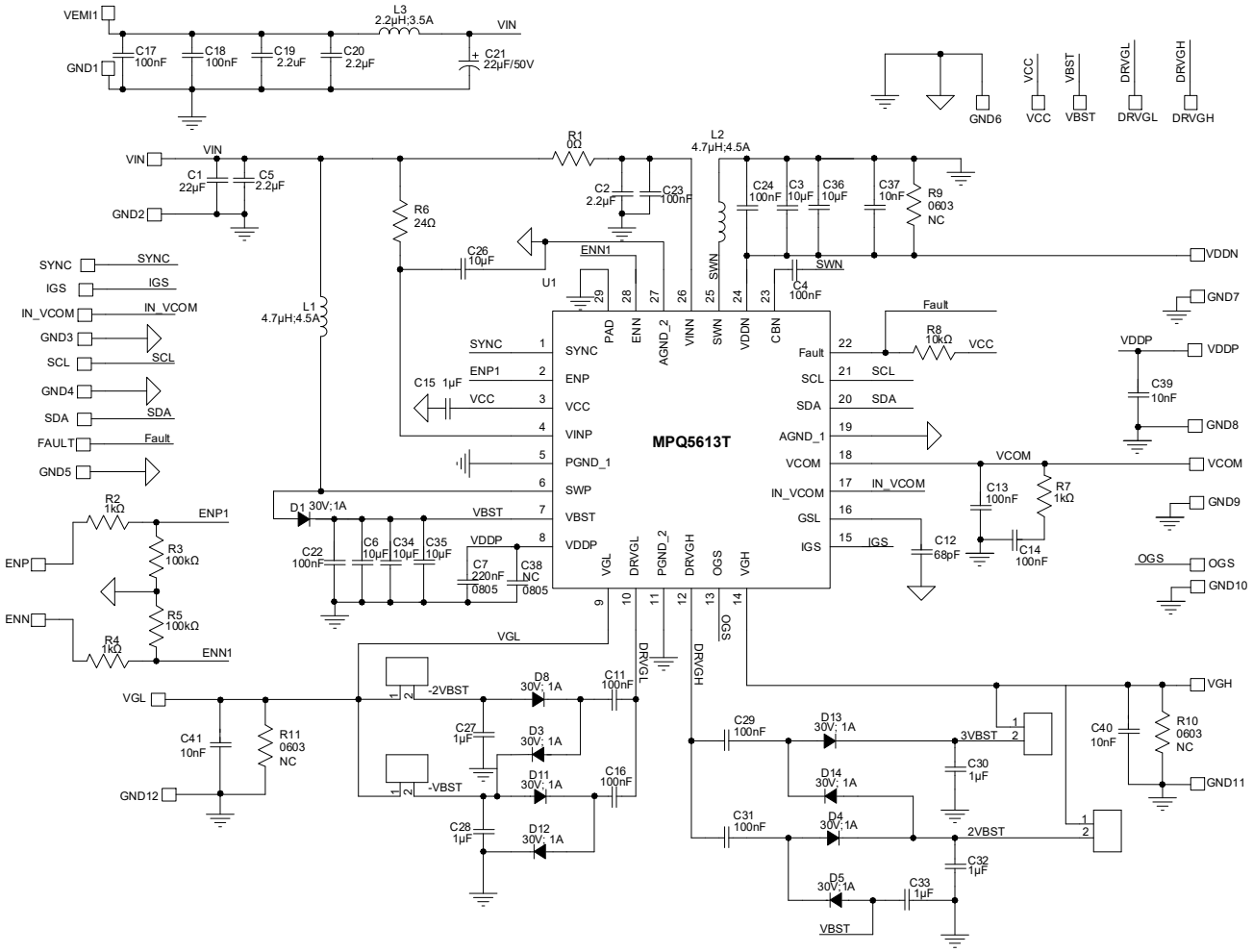
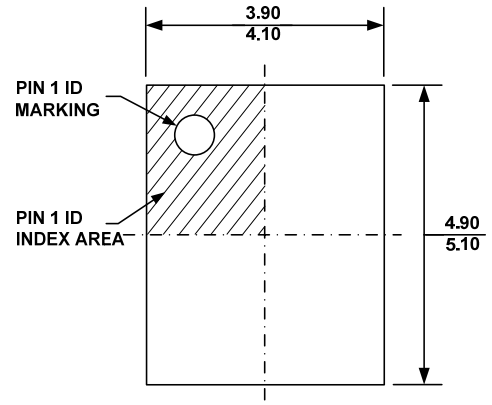


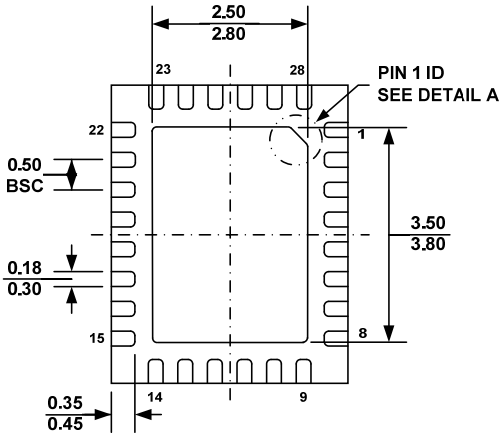
Figure 15: Typical Application Circuit

PACKAGE INFORMATION

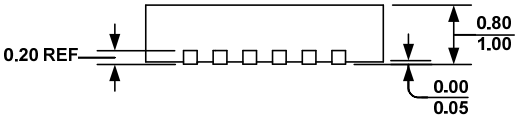
QFN-28 (4mmx5mm)
Wettable Flank



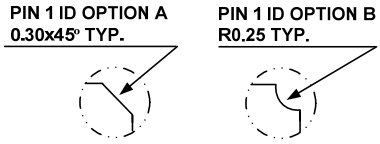
TOP VIEW



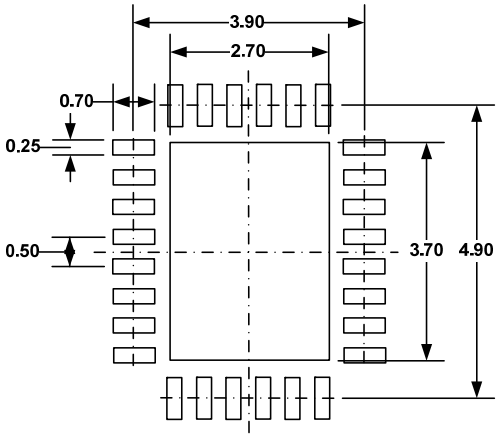
BOTTOM VIEW



SIDE VIEW



DETAIL A

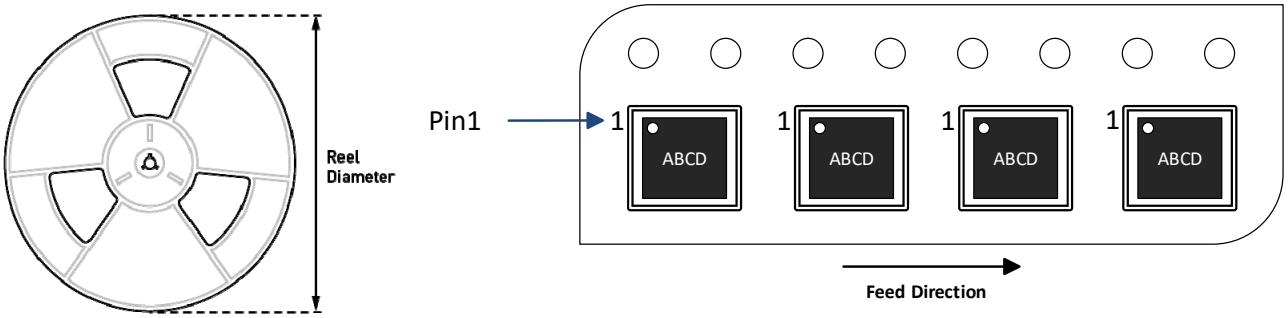


RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETER MAX.
4) DRAWING CONFORMS TO JEDEC MO-220, VARIATION VGHD-3.
5) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MPQ5613TGVE-xxxx-AEC1-Z	QFN-28 (4mmx5mm)	5000	N/A	N/A	13 in	12 mm	8 mm