VE270 RC Week 5 2020.6.10

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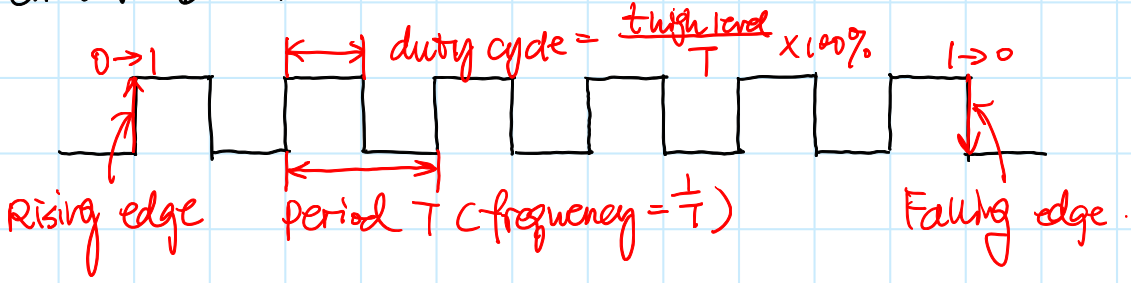
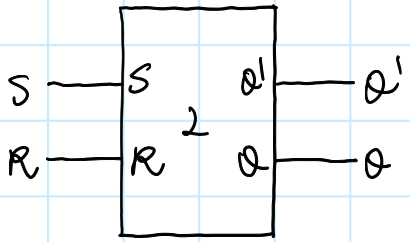
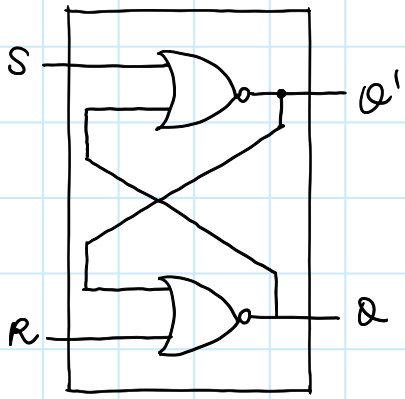
- **Clock Signal**
  - Periodic pulse train used in sequential circuit to synchronize circuit behavids.



- **Control Inputs**
  - Asynchronous:
    Control signal do not depend on the clock signal.
  - Synchronous:
    Control signal depend on the clock signal
    Output changes only when the clock signal changes, i.e. Rising / Falling edges.
  - Active low:
    It controls when it's low
  - Active high:
    It controls when it's high.

• SR Latch





S	R	Q	Q^+
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	x
1	1	1	x

$\Rightarrow Q^+ = S + R'Q$

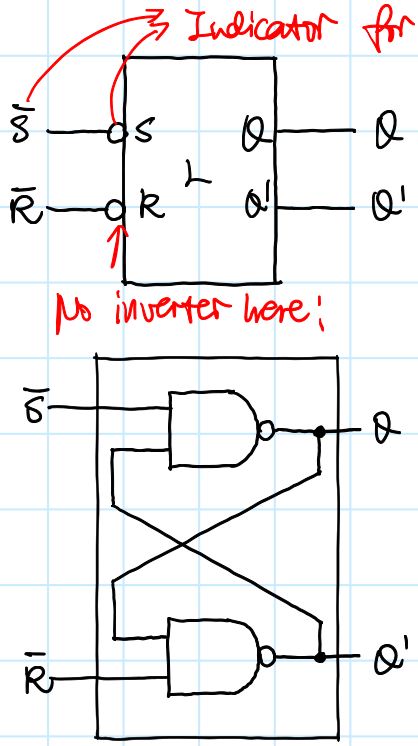
No action ⇒ Hold value

R(Reset) = 1 ⇒ Q = 0

S(Set) = 1 ⇒ Q = 1

Set and Reset at the same time ⇒ Not allowed

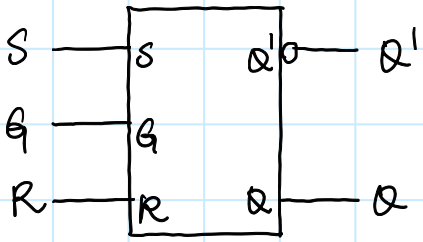
• Alternative Implementation of SR Latch

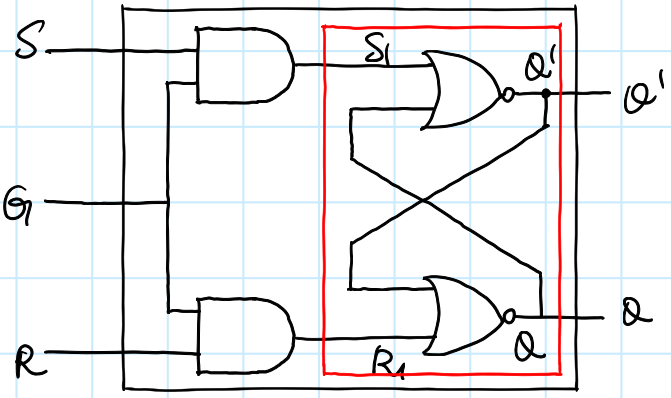


S	R	Q	Q^+
0	0	0	x
0	0	1	x
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

The way S, R are controlling the output is completely opposite to the SR Latch above

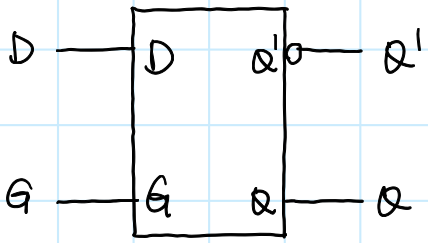
- **Gated SR Latch**

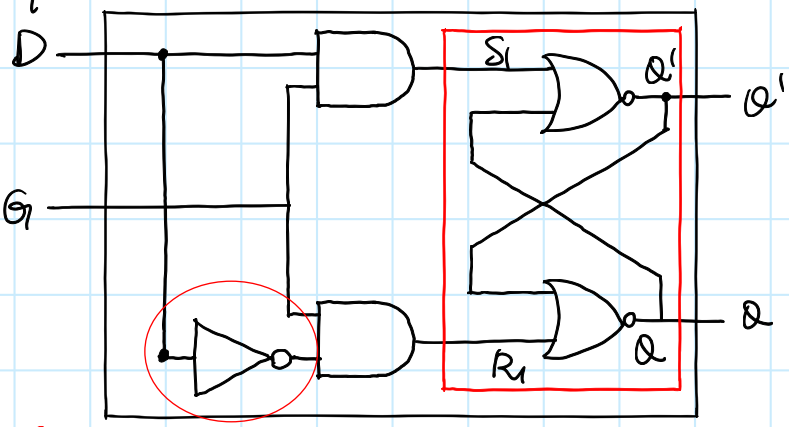




G	S	R	Q^+	
0	x	x	Q; Latch locked	G=0 : Unable the latch
1	0	0	Q; Hold state	G=1 : Enable the latch. Work as an SR Latch.
1	0	1	0; Reset state	
1	1	0	1; Set state	
1	1	1	Not allowed	

- **Gated D Latch (Transparent Latch)**



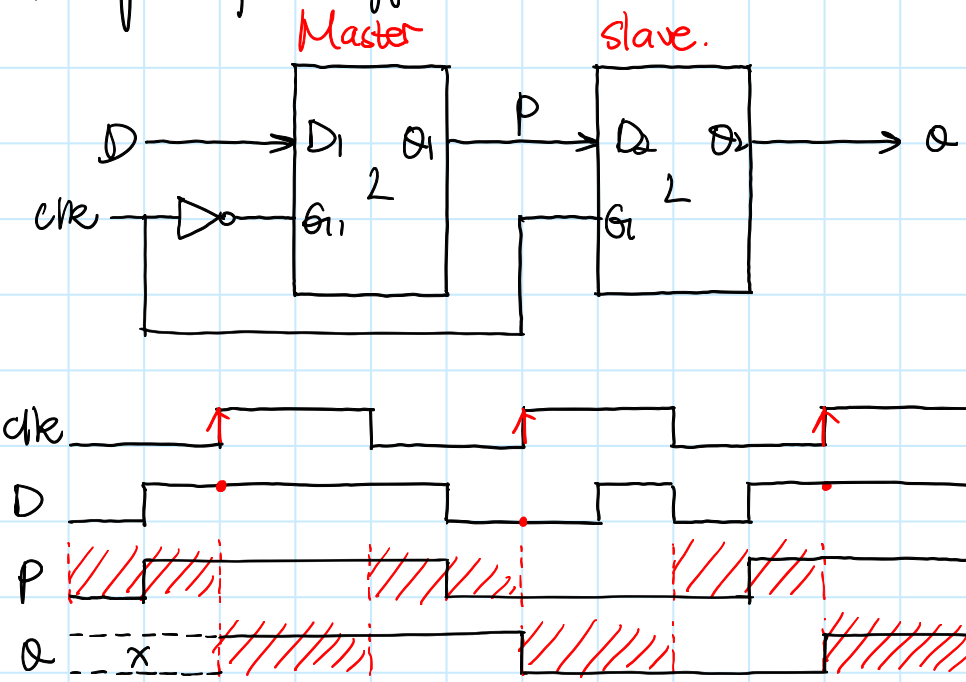


Solution to the unstable problem caused by S=R=1 in SR Latch!

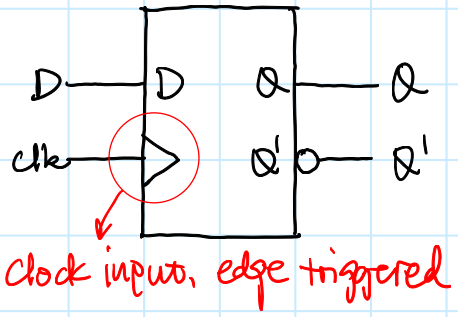
G	D	Q^+	
1	0	0	Q copy the input D.
1	1	1	Q is stored in the D Latch and reflect on the output
0	x	Q	Q doesn't change

- **Level Sensitive:** The input value is stored into the latch only when G has high level

- **D Flip Flop**
  - Rising-edge triggered Master-Slave D flip flop.

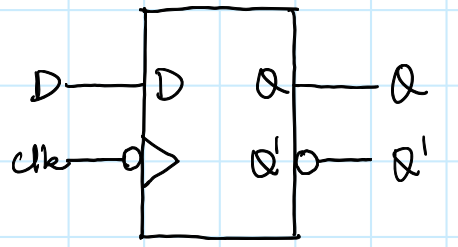


  - Rising Edge Triggered D Flip Flop.



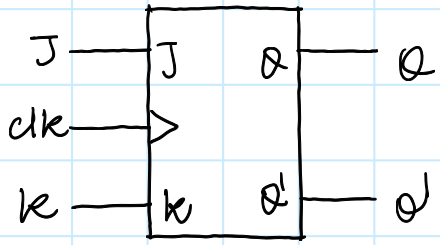
clk	D	Q^t	
↑	0	0	Q gets the value of D at the time point of rising edge
↑	1	1	
0	x	Q	Q doesn't change
1	x	Q	

  - Falling Edge Triggered D Flip Flop.



  - Edge Sensitive: The output changes only at the rising/falling edges of the clock signal.

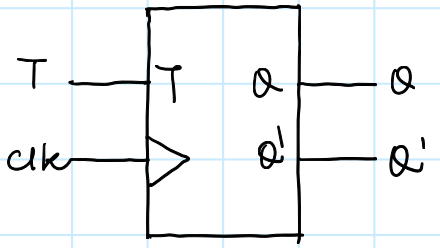
• Rising Edge Triggered J-K Flip Flop



J	K	Q^+	
0	0	Q	
0	1	0	Consider K as "Reset"
1	0	1	Consider J as "Set"
1	1	Q'	

$Q^+ = JQ' + K'Q$ * Memorize it together with SR Latch.

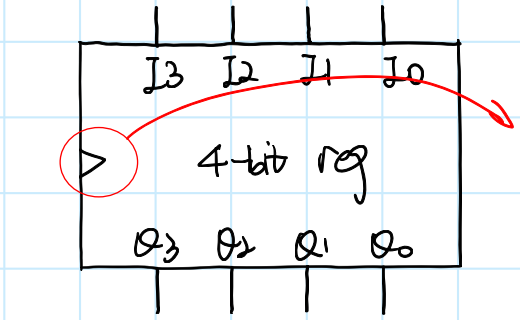
• Rising Edge Triggered T Flip Flop



clk	T	Q^+
↑	0	Q
↑	1	Q'

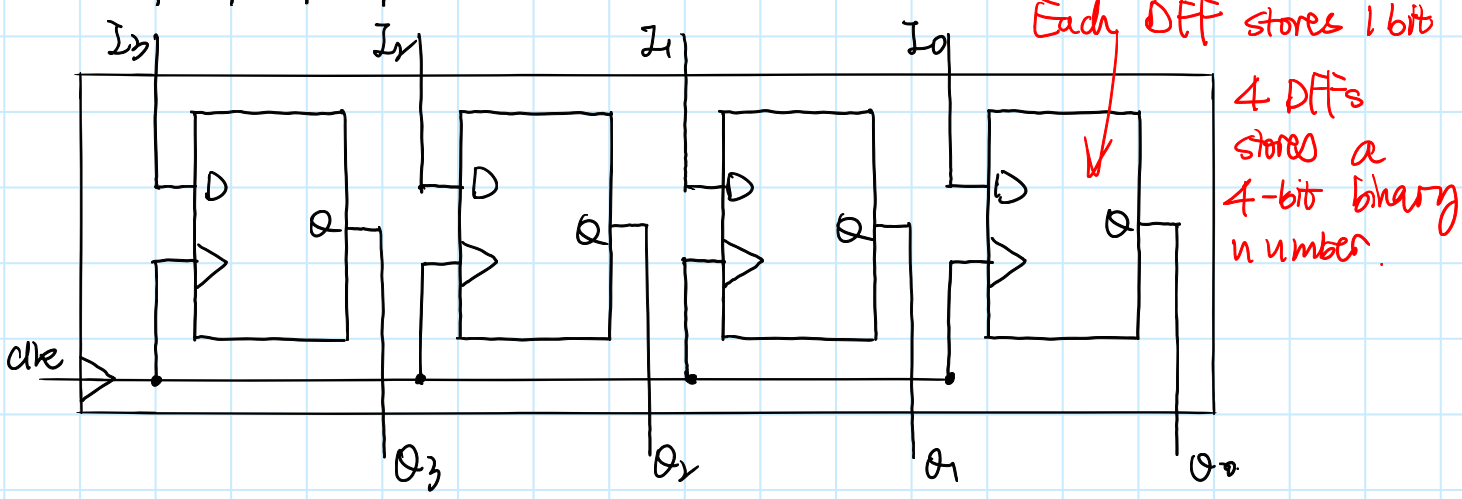
$\Rightarrow Q^+ = T'Q + TQ' = T \oplus Q$

- **Register**
  - Store multiple bits. (multiple flip flops sharing clock signal)



Edge sensitive

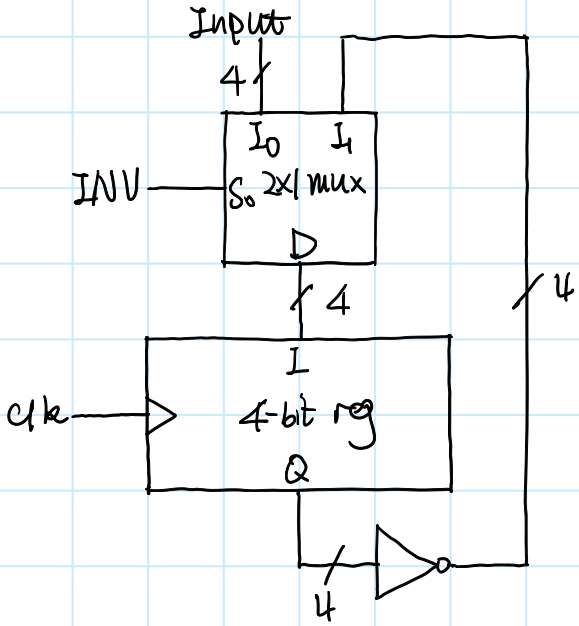
↑ : Load the input into the register and reflect on the outputs.



Each DFF stores 1 bit

4 DFFs stores a 4-bit binary number.

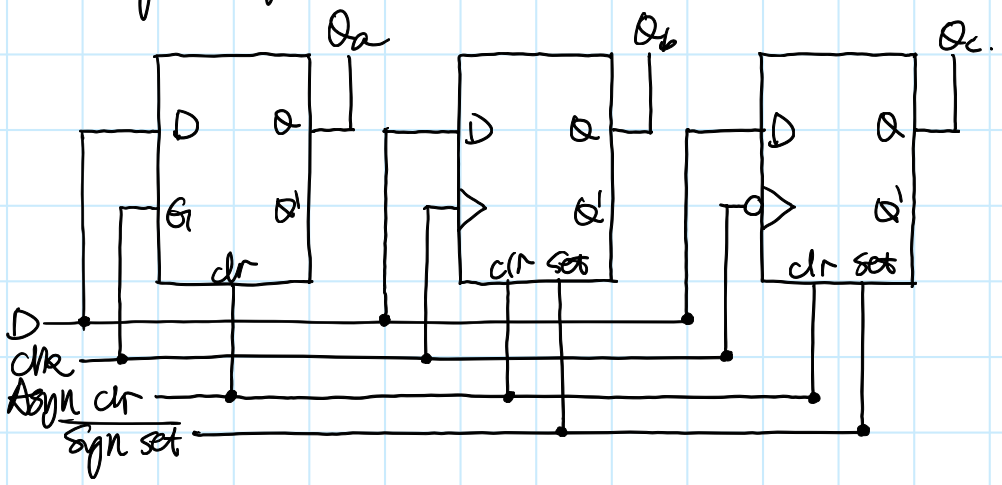
  - Design a 4 bit register with an enable signal "INV", such that when INV = 1, content of the 4 bit register is inversed (e.g. 1011 becomes 0100), and when INV = 0, the register works as normal.

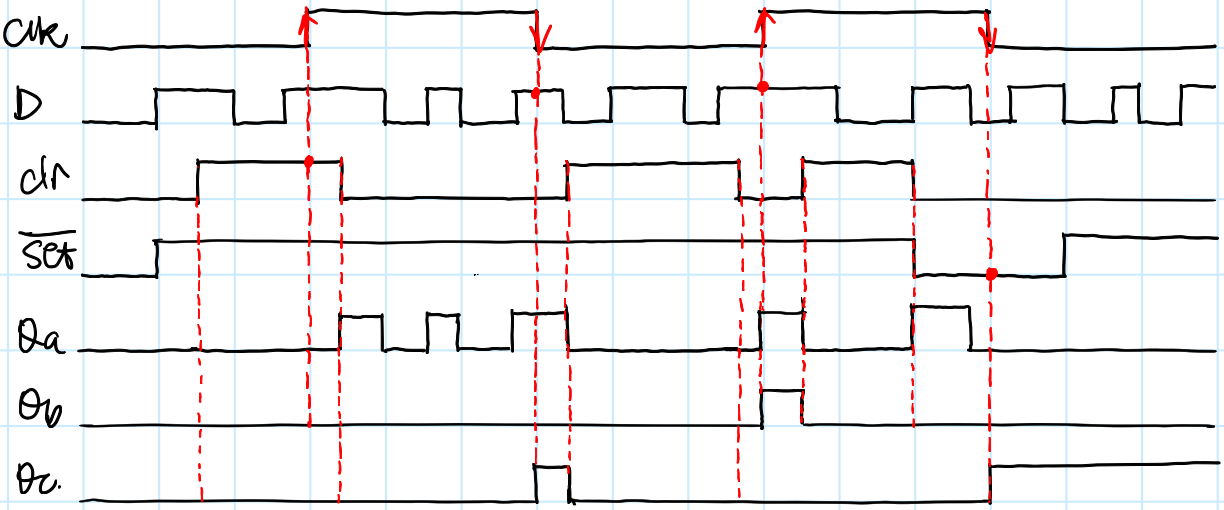


- Latch v.s. Flip Flop
  - Same: storage elements in sequential circuits.
  - Difference:

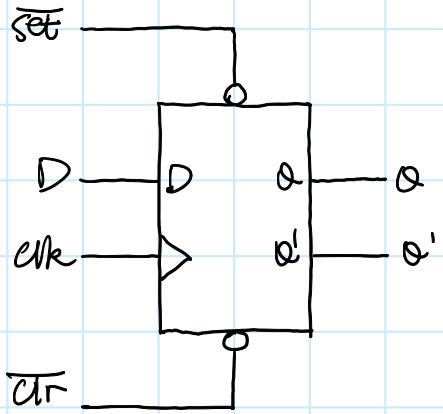
Latch	Flip Flop
Level Sensitive: The input matters whenever the control signal is high	Edge Sensitive: The input matters only at active edges (rising or falling)
Asynchronous to clock signal	Synchronous to clock signal.

  - Timing diagram.





- Implementation of Asynchronous Control Input



- Implementation of Synchronous Control Input.