Plan this week: Timing & Logic Timing analysis for gates, clks, etc.

Part 1: Gates - Review (Using Jerry Yang's Lecture 11)

- Combinational (Gates)
- Sequential - Sequencing

Pick-Delay-Primal: (Know this that one is a lesson)

- Step 1: Generate a high-level block diagram.
- Step 2: Create a sequencing
- Step 3: Create a delay model for a cell
- Step 4: Create the timing diagram

Example 1: Two Gate Pipeline:

Suppose you want to run this "two gate" function in 1 clocking. Let each gate take 1 ns long gates, you need to drive it in the clock of the machine, and let the input signal [illegible] — [illegible] machine. Then the question goes to [illegible] [illegible] [illegible]. And now you draw a [illegible] of gates, you need the input [illegible] to the combinational [illegible]. Make [illegible] sure [illegible] on "and" function in this machine, we use [illegible] all kinds of other [illegible] the same [illegible]. Looking [illegible] is not [illegible] and. You can [illegible] [illegible] [illegible] [illegible]. But suppose you say [illegible] [illegible] [illegible]