VE270 Quiz 3 6.4 Candy Candies.

Question 15 分

Design a combinational circuit that has 3 single bit input signals. The circuit counts the number of "0"s in the input bits and outputs the number in binary format.

1) Capture the function with truth table

2) Give logic equation(s) of the output(s)

3) Implement the circuit with a 3x8 decoder and logic gate(s)

1)

x	y	z	F_1	F_0
0	0	0	1	1
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	0	0

2).

F_1

x \ yz	00	01	11	10
0	1	1	0	1
1	1	0	0	0

$F_1 = x'y'z' + x'y'z + x'yz' + xy'z'$ ✓

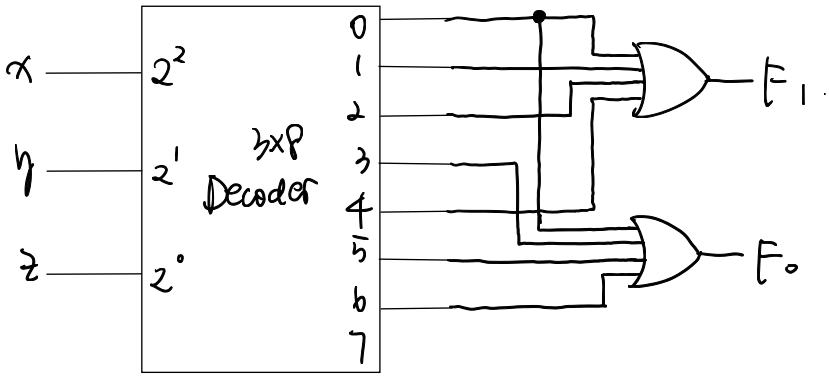
$= y'z' + x'y' + x'z'$

F_0

x \ yz	00	01	11	10
0	1	0	1	0
1	0	1	0	1

$F_2 = x'y'z' + x'yz + xy'z + xyz'$

3) $F_1 = \Sigma m(0, 1, 2, 4)$ $F_2 = \Sigma m(0, 3, 5, 6)$.



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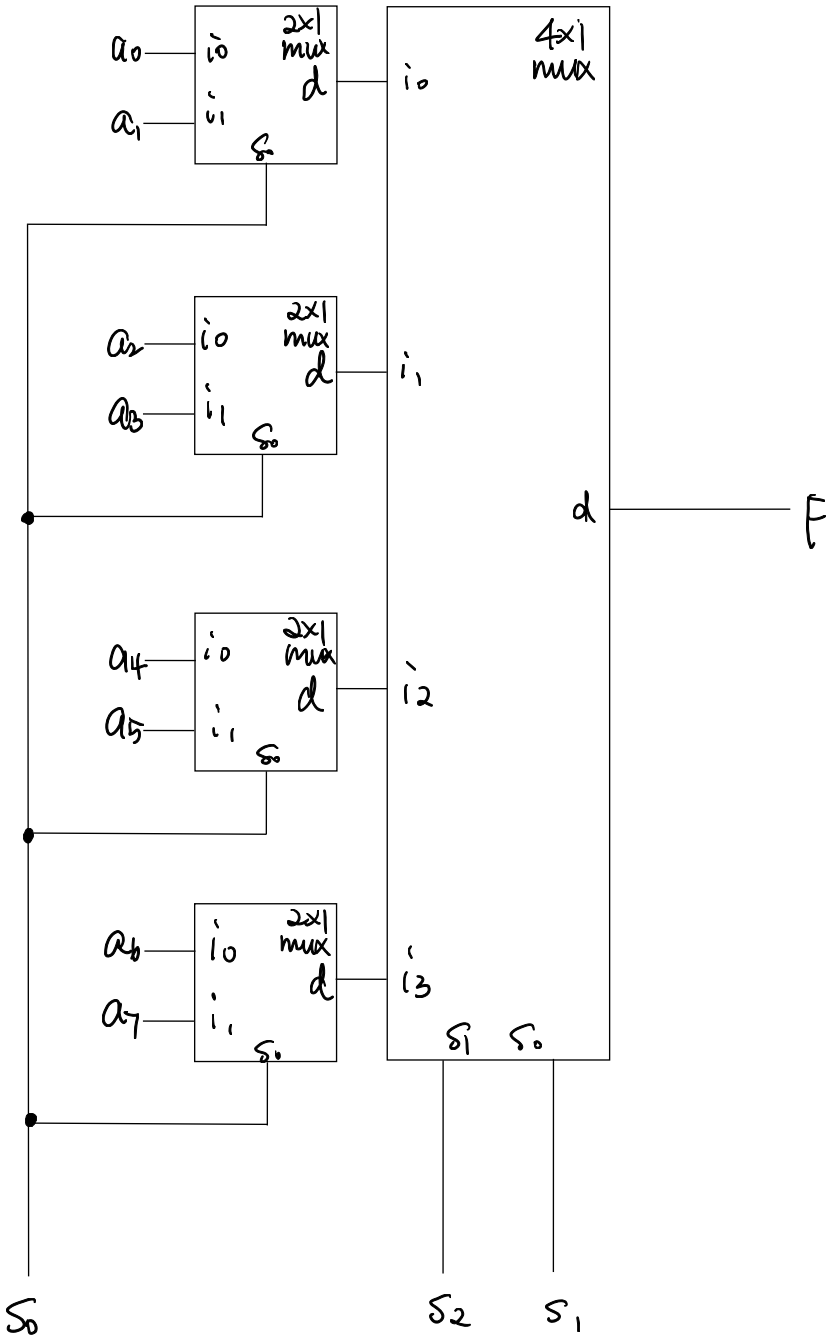
Question 10 分

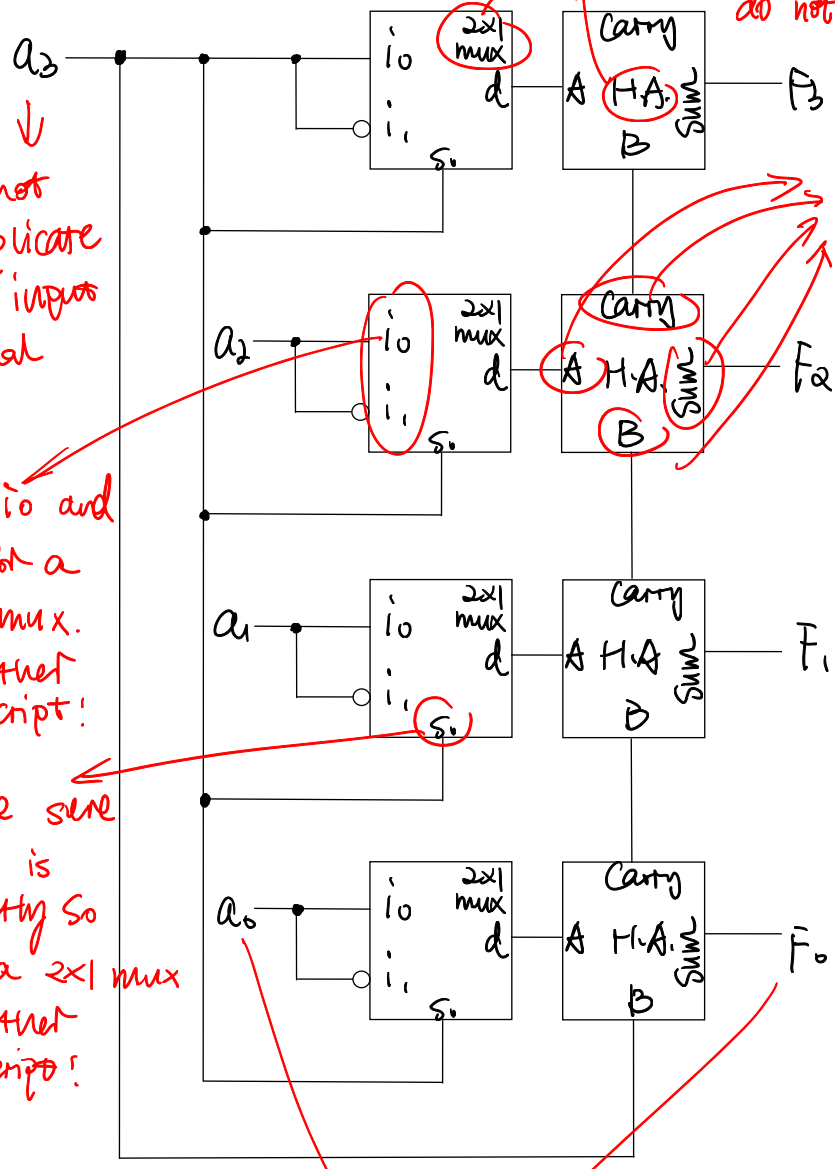
Show how four 2-to-1 and one 4-to-1 MUXs could be connected to form an 8-to-1 MUX. Make sure the select signals are clearly connected and labeled.



VE270 Quiz 3 bit Candy Candies.

Question DO NOT use truth table! 25 分

Design a circuit that calculates the absolute value (magnitude) of a 4-bit 2's complement number. For example, magnitude of "1101" is "0011", magnitude of "0011" is also "0011". Use building blocks.



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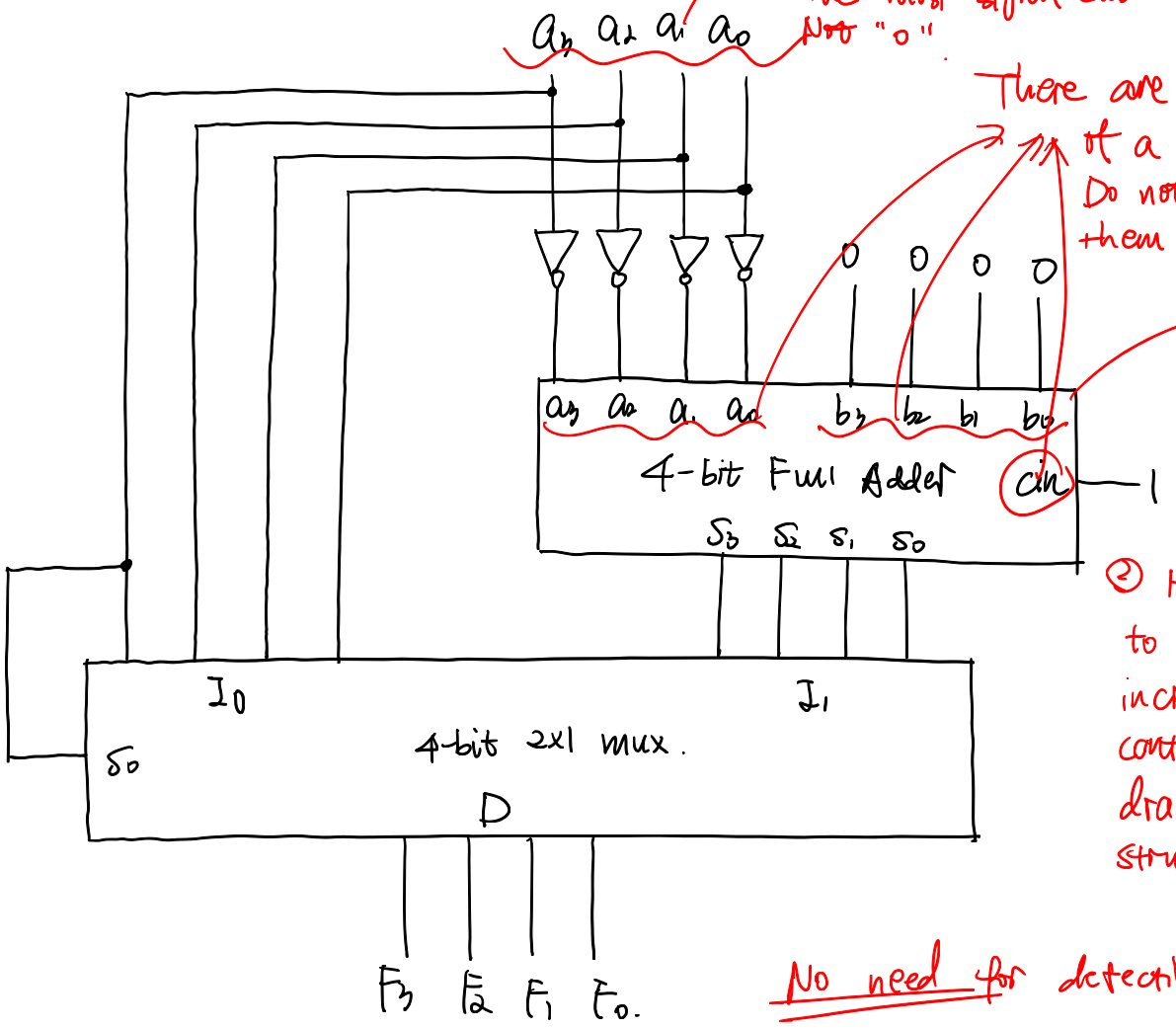
Another solution for problem 3:



a_3, a_2, a_1, a_0 all of the 4 bits are needed. Do not omit a_3. Consider the case 1000 ⇒ 1000 the most significant bit is still "1" Not "0".

There are three inputs of a Full Adder. Do not forget any of them.

① There is no building block called 4-bit Half Adder.

② If you want to use one-bit incrementor which contains 4 H.A.'s. draw the internal structure.

No need for detecting overflow!