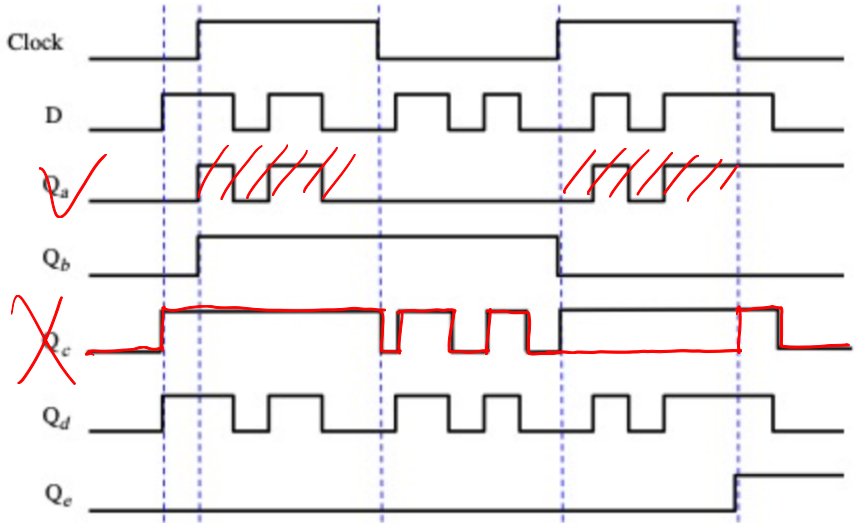
VE270 Quiz 4 2020.6.11. Candy Candies.

Question 10 分

Which of the following timing diagram(s) may be produced with a D Latch?

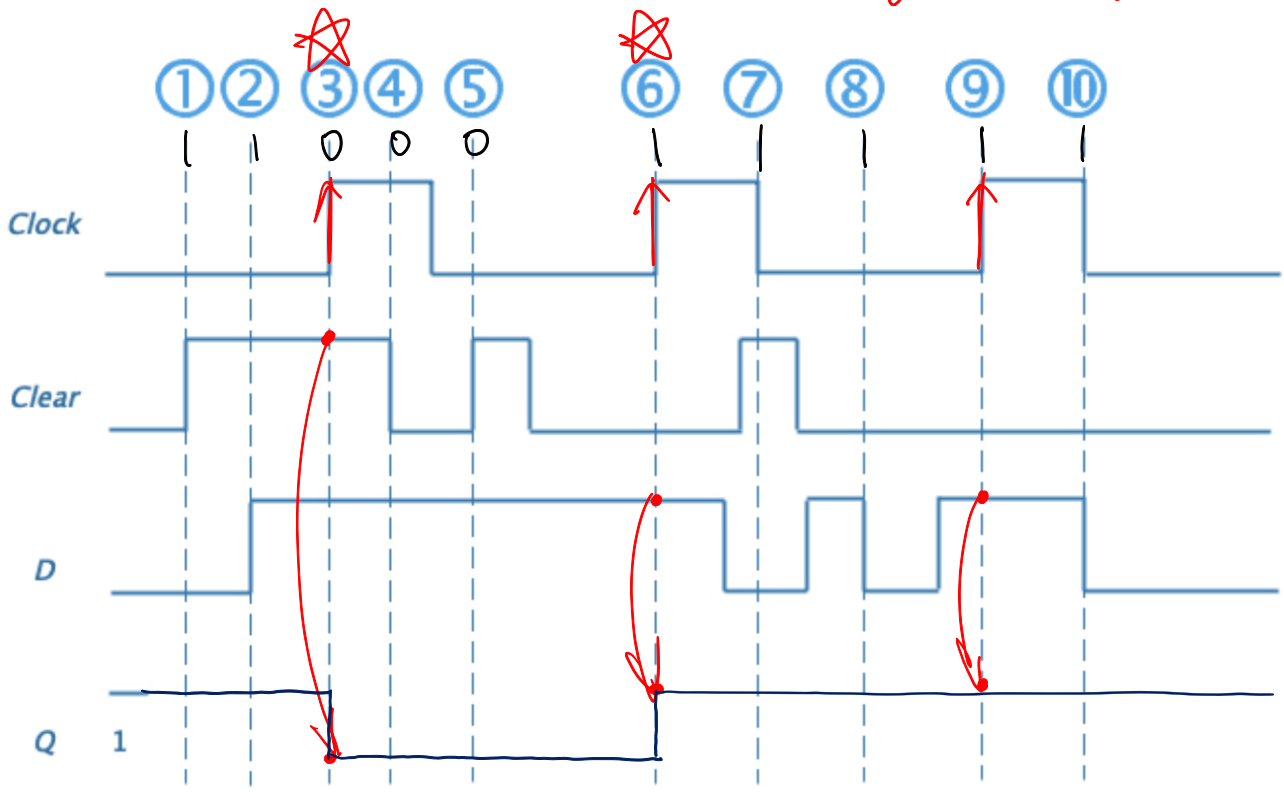


Sensitive to high level

The correct output of a gated D-Latch sensitive to low level.

Question 15 分

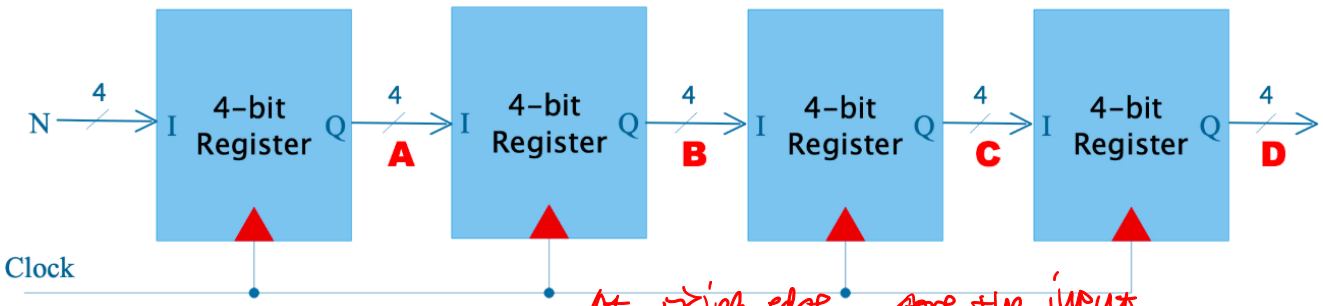
Given a D flip-flop with synchronous active high Clear signal, as well as Clock and D inputs, shown in the following timing diagram, what are the values of output Q (0 or 1) at the moments labelled with the circled numbers? Assume initial value of Q is 1. Consider ideal situations (No delay at ⑤ ⑥)

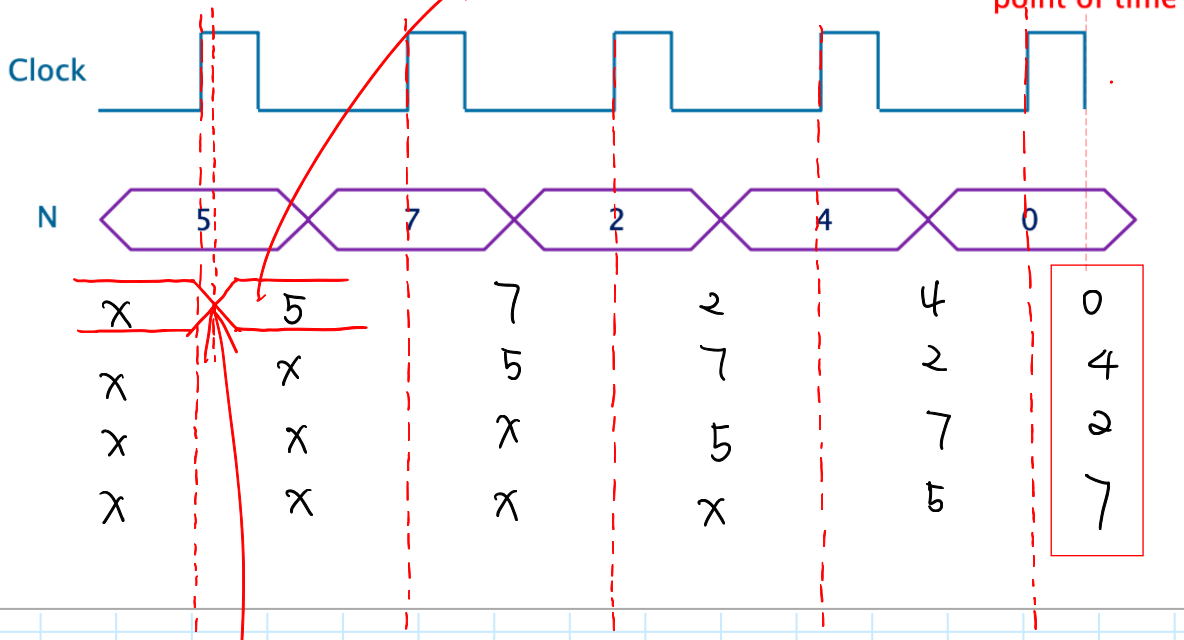


VE270 Quiz 4 2020.6.11. Candy Candies.

Question 10 分

Given following circuit and timing diagram of its inputs, what are the values of signals A, B, C, and D at the Examine Point of Time?





At rising edge, store the input and reflect on the output (A). Examine point of time

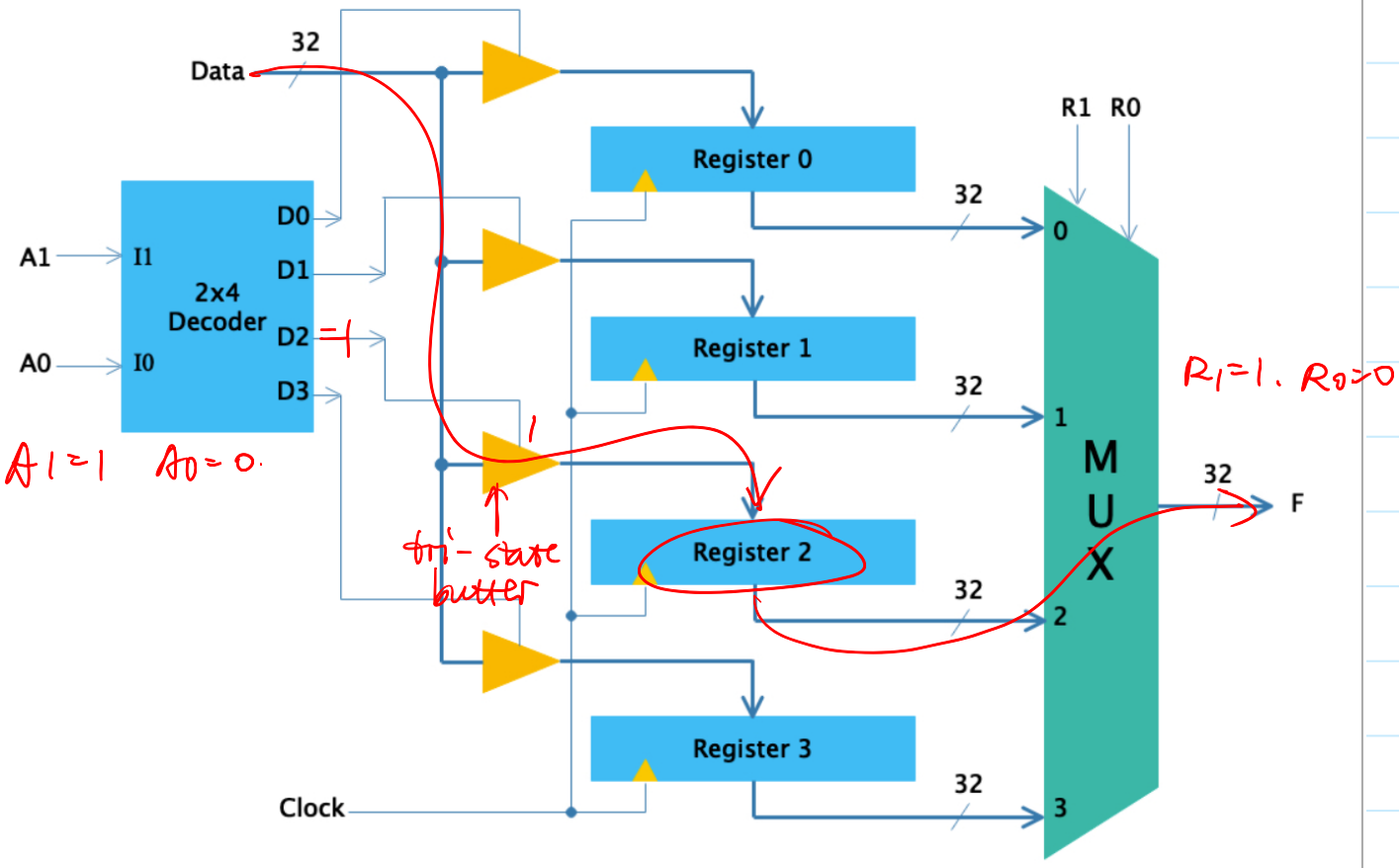
A = [A]	X → 5	7	2	4	0
B = [B]	X	X	5	7	2	4
C = [C]	X	X	X	5	7	2
D = [D]	X	X	X	X	5	7

A small delay before the output of "5"
That is, there is no output value of A at exactly the first rising edge.
So for the second register at the first rising edge
it remains to be "X"

VE270 Quiz 4 2020.6.11. Candy Candies.

Question 15 分

Given the following circuit, describe in text how to store the "Data" input in "Register 2", and then how to put the stored "Data" on the output "F".



① To store the data input in "Register 2":
Set A1=1. A0=0 to make the output D2 of the 2x4 Decoder to be 1 which enables the tri-state buffer connected to Register 2. So that Data can pass through this buffer and stored in Register 2 after the rising edge of the clock.

② Put the stored "Data" on the output "F".
Set R1=1. R0=0 to let the mux to choose the signal from the port labeled "2" and then outputs the data (a point).

pay attention to rising edge / (a period) high level. They are different