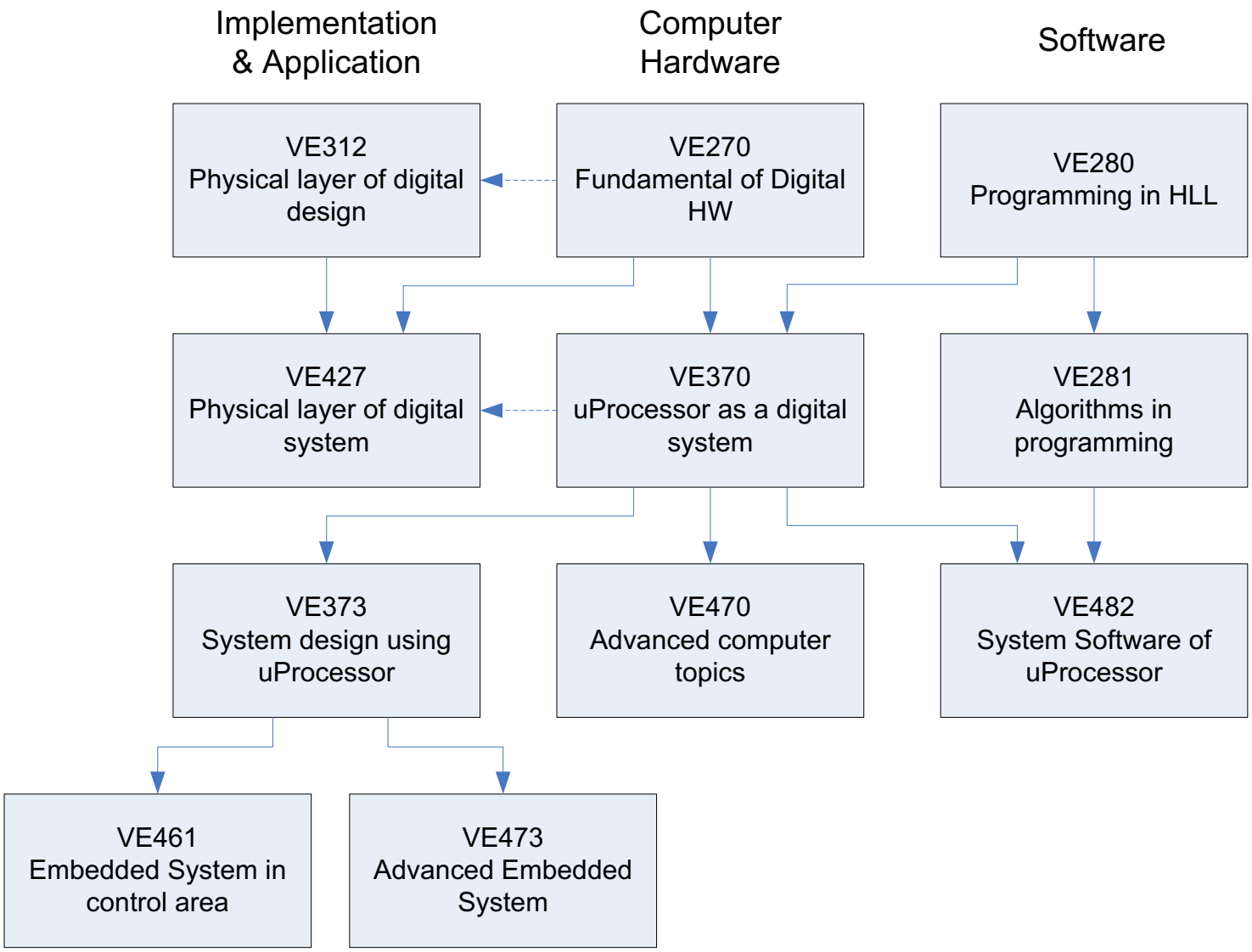
VE270 Intro to Logic Design
Course Overview

Instructional Support

- **My Office:** JI New Building 400E
- **Contact:** gzheng@sjtu.edu.cn
- **Office Hours:** W 4:00-6:00pm / Th 8:00-10:00am on Piazza
- **TA:** Mr. ZHAO Wenbo, zhaowenbo@sjtu.edu.cn
  Mr. CHEN Yuchi, citrate@sjtu.edu.cn
  Ms. TANG Mingyi, tmy19991006@sjtu.edu.cn
  Ms. ZHAO Yiqing, zhaoyq@umich.edu
  TAs' office hours to be announced
- **Recitation class:** one session per week on zoom (recorded)

Courses in CE Curriculum



Purpose of the Course

- Understand the fundamental principles in design and implementation of digital logic circuits including combinational circuits, sequential circuits, and finite state machines.
- Develop skills for top-down design and bottom-up verification for digital components and systems.
- Develop skills in using contemporary computer aided tools and programmable logic devices in digital logic design.
- Improve communication skills to effectively function on a team.

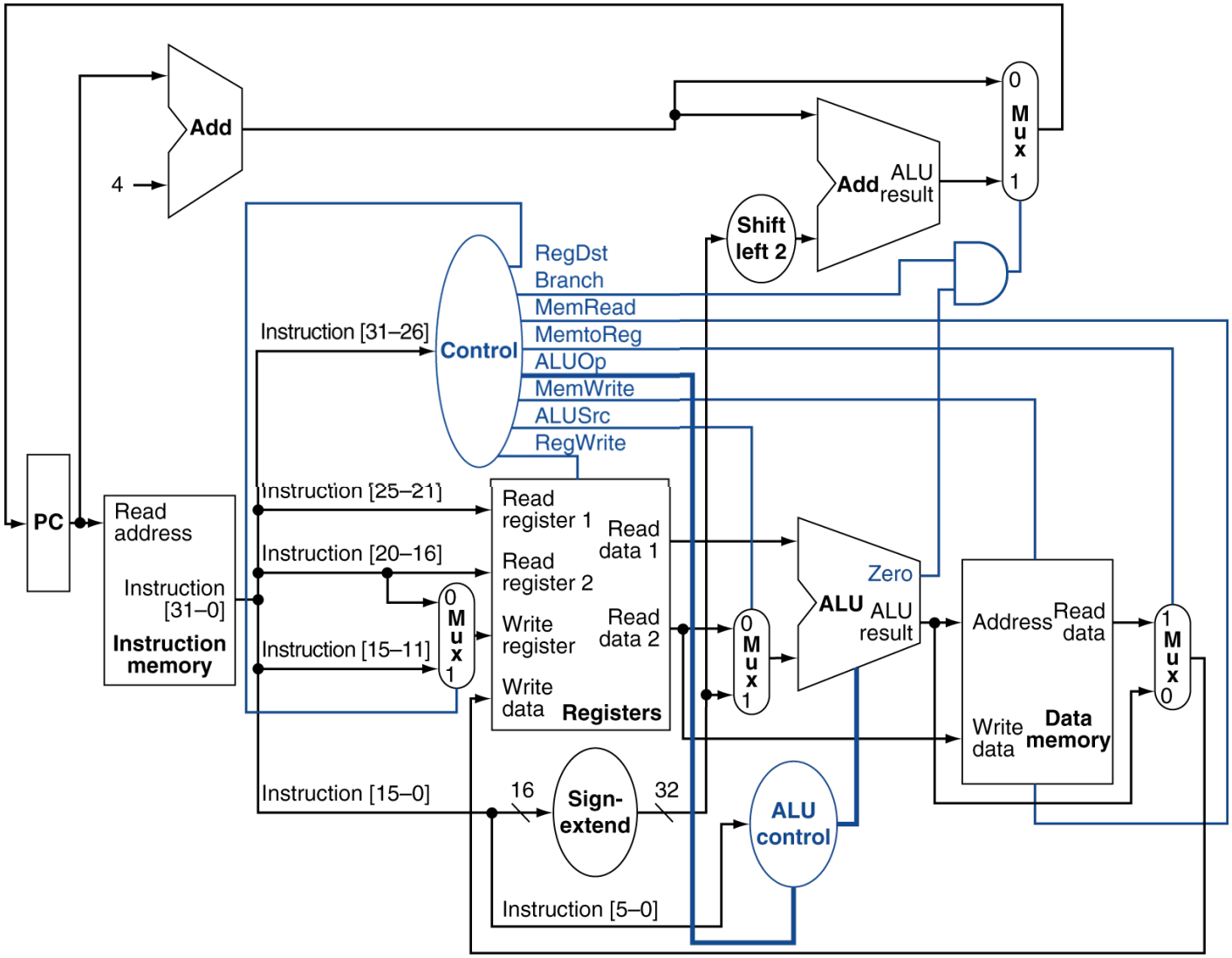
Minimum Expectation

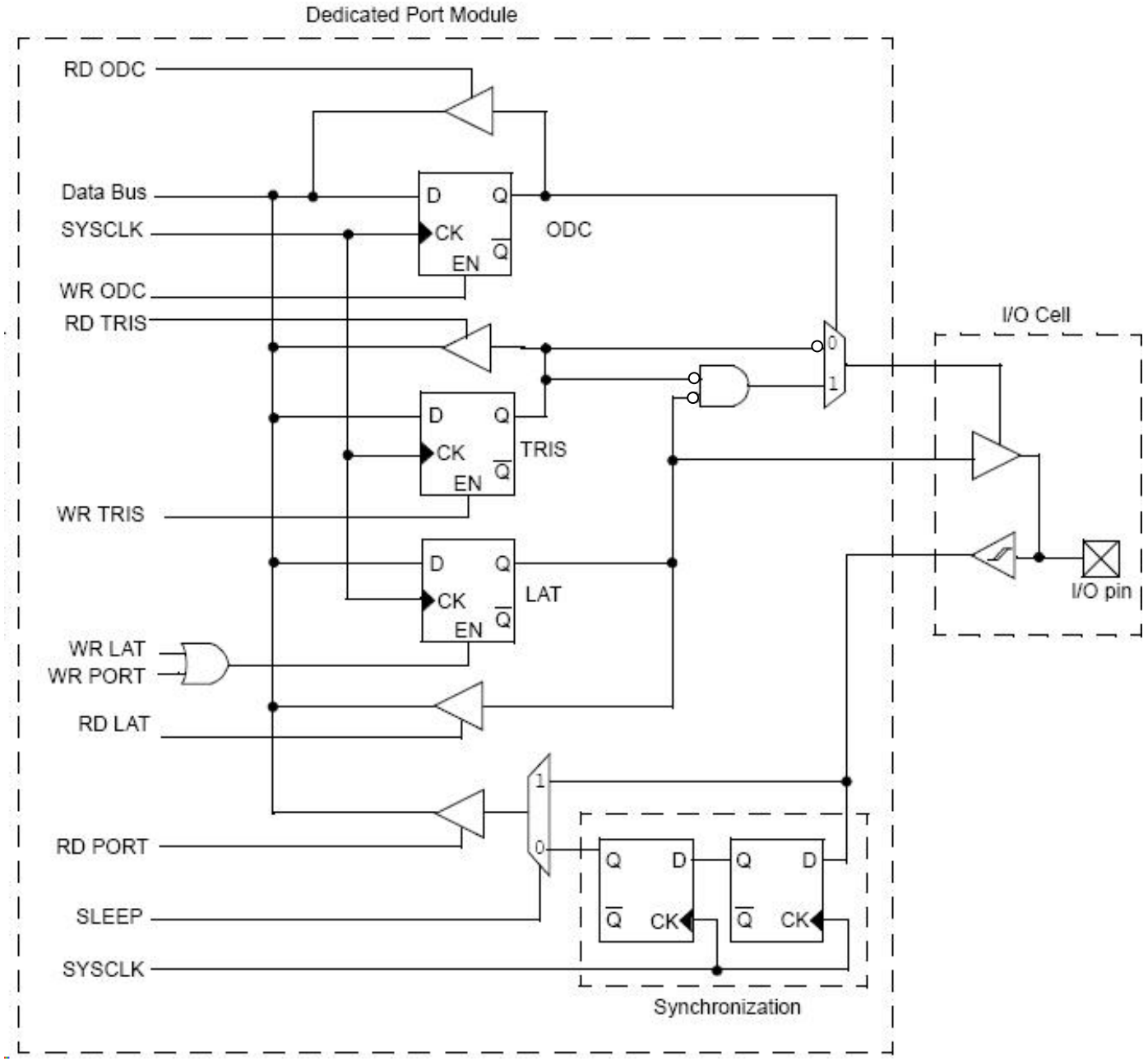
- Ability to perform simple arithmetic in binary, octal, hexadecimal, BCD number systems
- Ability to manipulate logic expressions using binary Boolean algebra.
- Ability to generate the prime implicants of logic functions of 5 or fewer variables using graphical (Karnaugh map) method, and to obtain their minimal two-level implementations with and without don't cares.
- Ability to analyze and synthesize small multi-level combinational logic circuits containing AND, OR, NOT, NAND, NOR, and XOR gates based on simple delay models.
- Ability to use basic functional & timing (clocking) properties of latches & flip-flops.
- Ability to analyze synchronous sequential circuits to extract next-state/output functions

Minimum Expectation (Continue)

- Ability to translate a word statement specifying the desired behavior of a simple sequential system into a finite state machine (FSM), to simplify and build the architecture that consists of state register and next state/output logic.
- An ability to implement simple digital systems using controller and basic datapath components such as registers, memories, counters, multiplexers, ALUs, etc.
- Basic knowledge of possible issues and restrictions in digital system.
- Ability to design and test simple digital systems using a hardware description language and CAD tools
- Knowledge of programmable logic devices and ability of implementing a logic circuit in FPGA.
- Experience and communication skills to function on a team.

Seriously, what are we going to learn?




Dedicated Port Module
RD ODC
Data Bus
SYSCLK
WR ODC
RD TRIS
WR TRIS
WR LAT
WR PORT
RD LAT
RD PORT
SLEEP
SYSCLK
D
Q
CK
EN
ODC
TRIS
LAT
I/O Cell
I/O pin
Synchronization

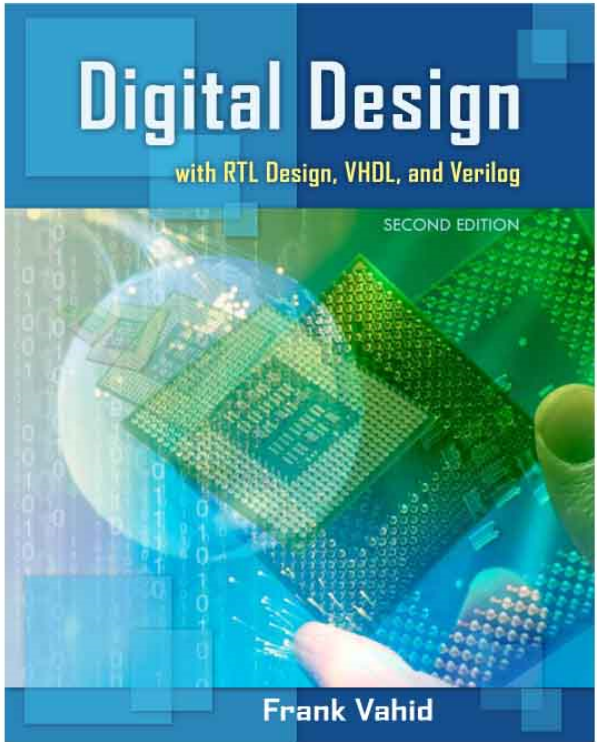
Topics to Cover and Tentative Schedule

- Boolean algebra
- Logic gates
- Combinational circuits
- Flip-flops
- Hardware Description Language (HDL)
- Sequential circuits
- Finite state machine (FSM)
- Circuit optimization
- Arithmetic circuits
- Design skills for digital components
- Computer-aided design
- Memory
- Programmable logic devices

Textbook

- **Textbook:**

  Frank Vahid, *Digital Design 2/e*, John Wiley & Sons, 2010. ISBN 9780470531082



Tentative Schedule

- **On Syllabus**

Course Policies

- **Honor Code:** All students in the class are bound by the Honor Code of the Joint Institute (http://umji.sjtu.edu.cn/academics/academic-integrity/honor-code/) as well as the *Addendum to the Honor Code for Online Teaching*. You may not seek to gain an unfair advantage over your fellow students; you may not consult, look at, or possess the unpublished work of another without their permission; and you must appropriately acknowledge your use of another's work.
- **Test:** Test procedure will be announced prior to the tests. Anyone violating the test procedure will be given an 'F' for the test.

Course Policies

- **Attendance:** Attendance to the lectures is strongly encouraged, not only because difficult concepts are discussed during the lectures, but also because it is an effective way to get engaged in class activities. Attendance to the designated lab sessions is required.
- **Participation:** Active participation is highly expected for all students. This involves participation in interactive activities during the lecture time, proper assistance to other students in group studying, contributions to the Q&A on Piazza, etc.

Course Policies

- **Individual Assignments:** Due to the online teaching format, most of the assignments are individual efforts. All submissions must represent your own work. Duplicated submission is not allowed and will trigger an honor code violation investigation. However, students are encouraged to discuss course topics and help each other to understand the problems.
- **Group Assignments:** Some assignments may be team efforts. The work submitted must reflect the work of the entire team.
- **Submission:** All assignments should be submitted electronically on Canvas before the specific deadline.

Assessment Methods

- **Homework & Quiz:**
  - Typically, one homework set is assigned each week, 9-10 homeworks.
  - Submission of homework is NOT required.
  - Instead, students will be given a pop quiz on the due date for each homework assignment.

- **Examination:**
  - The examinations are to measure the level of achievement of the minimum expectations.
  - Requirements of the examinations will be announced prior to the exams.
  - The typical types of exam problems include conceptual understanding, computation, procedural development, short answer, analysis, design, etc.
  - The exams may be given on paper or online.

Assessment Methods

- **Lab Experiment:**
  - 7 lab experiments, starts from wk#2
  - Due to COVID-19, take-home individual work until further notice.
  - Demonstration is required for each lab.
  - Every student will be orally examined about implementation problems in a lab during the demonstration.
  - Labs will be graded on completeness, correctness, effectiveness in analyzing and presenting lab outcomes, oral exam performance, source files, and other required submissions. No lab grade will be given until all the files are submitted.
  - Students should successfully demonstrate a working circuit to the TAs before your lab session ends.
  - Late demonstration is acceptable with 20% deduction from the lab grade for each day extended until all the points are deducted.

Assessment Methods

- **Participation and Etiquette:**
  - Students are encouraged to actively participate in all kinds of classroom activities including, but not limited to,
    - classroom interaction with the instructor and other students on zoom,
    - effective contribution on Piazza,
    - active participation in group study.
  - Inappropriate behavior will result in deduction of points in this part of course evaluation.

Lab Equipment and Software

- **Xilinx Vivado HLx (WebPACK)**

Download for free at:
https://www.xilinx.com/member/forms/download/xef.html?filename=Xilinx_Vivado_SDK_2017.2_0616_1_Win64.exe&akdm=0

(registration needed)

- **NI Multisim**

Download the Education Edition evaluation version for free at:
http://www.ni.com/gate/gb/GB_ACADEMICEVALMULTISIM/US

- **Digilent Basys 3 Xilinx Artix-7 FPGA Training board** (partially sponsored by Digilent Inc.)

Grading Policy

• Participation & Etiquette	10%
• Weekly Quiz	15%
• Lab	40%
• Midterm Exam	15%
• Final Exam	20%
Total	**100%**

- **Note: final letter grades will be curved**

Lab Grading Policy

- Lab grade components:
  - Demonstration (sw and hw): 60% of a lab grade
  - Source File: 20% of a lab grade
  - Oral Examination: 20% of a lab grade
- Late demonstration is acceptable with 20% deduction from the lab grade for each day extended until all the 60% are deducted.
- Late submission of source files and peer evaluation report will result in a 0% for those two parts of the lab. A grade for a lab will not be given until source files and peer evaluation reports are submitted.

Some Advices

- This course looks simple, but not necessarily true for everyone
- Attend lectures, I might talk about something useful occasionally
- Having doubts? Interrupt me and ask
- Seek help from the instructor and TAs, make good use of class time and our office hours
- Labs are very important and helpful with learning this subject, start before the lab, lab time might not be enough
- Respect the software, the software will do what's asked to do
- I reward hard working students, I don't mind giving more As; but I cannot give all As; I do fail students if I have to
- We check honor code violations seriously, you don't want to test your luck
- Check Canvas frequently for important announcements