



JOINT INSTITUTE

交大密西根学院

99

Ve270 Introduction to Logic Design

Homework 4

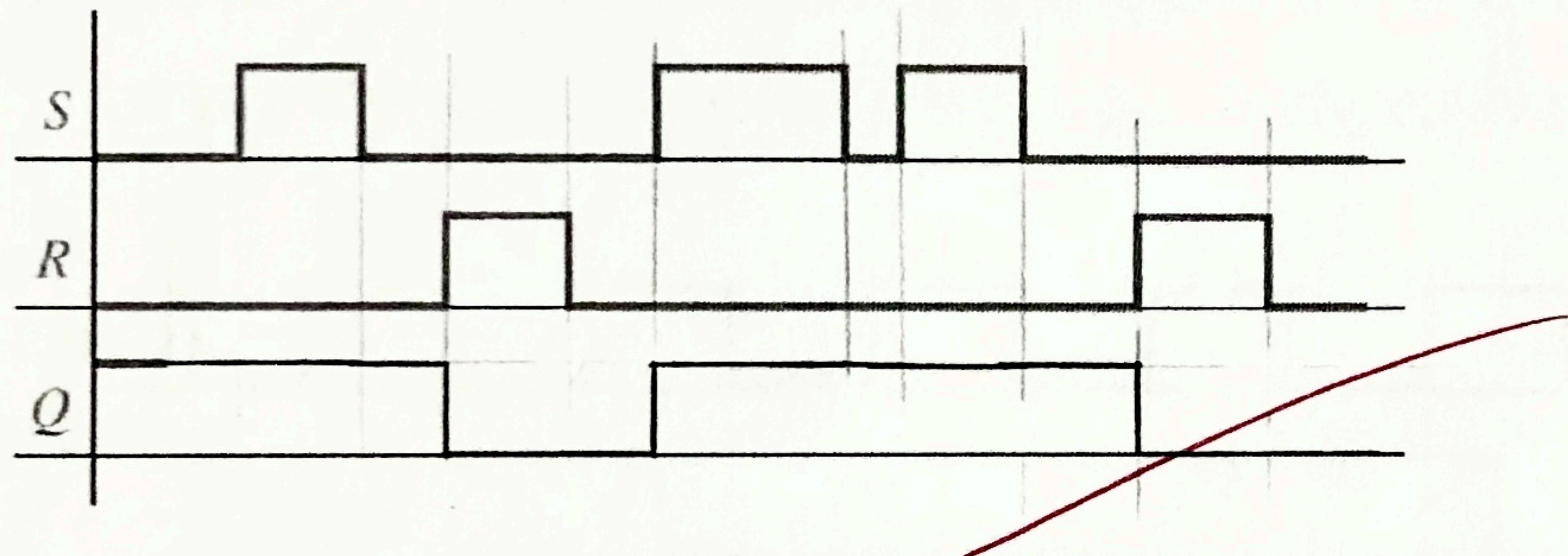
Assigned: October 15, 2019

Due: October 22, 2019, 4:00pm.

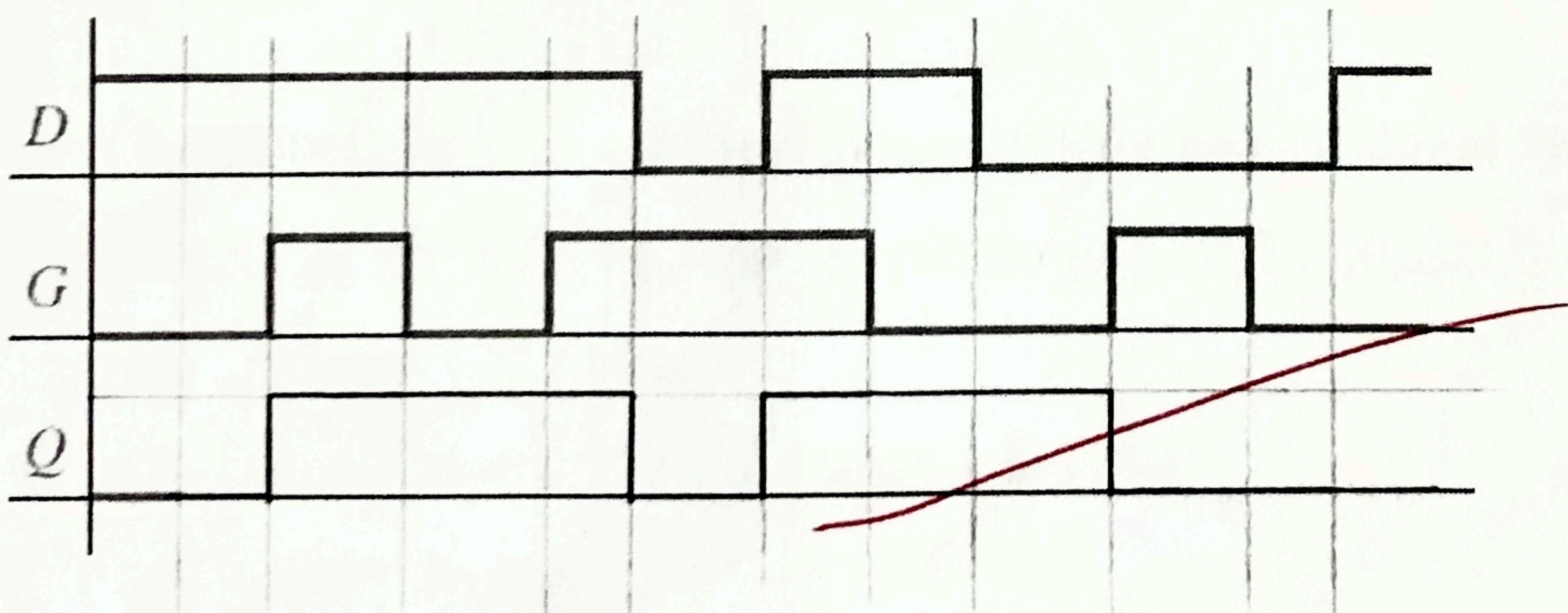
The homework should be submitted in hard copies.

Note: you may ignore the gate delay when drawing a timing diagram unless required differently.

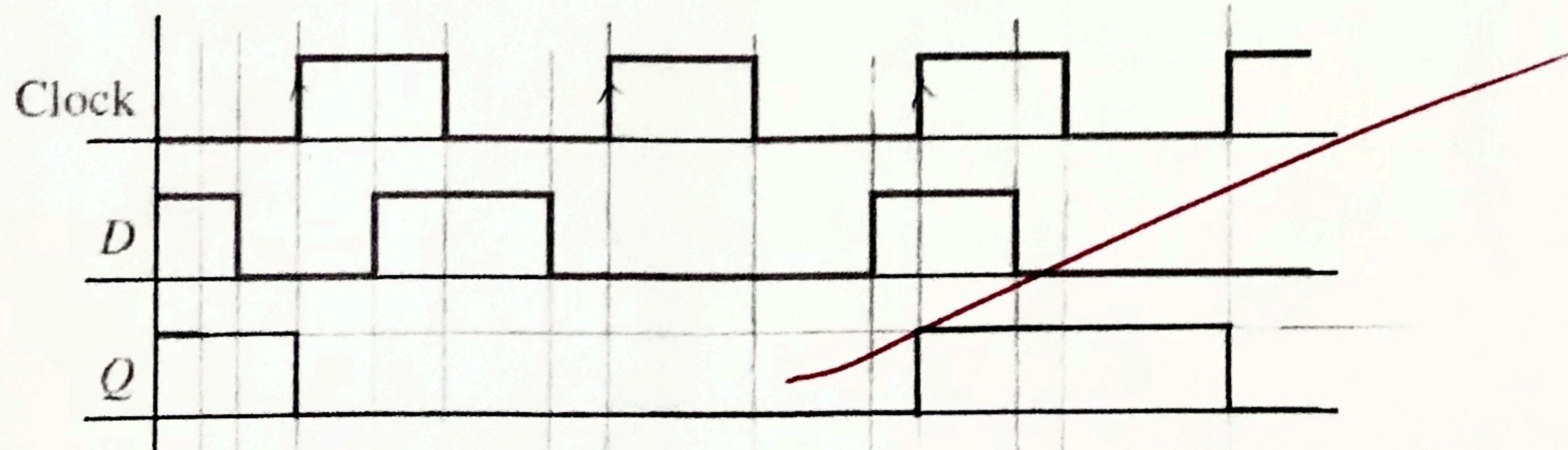
- (10 points) Complete the following timing diagram for an SR latch. Assume Q begins at 1.



- (10 points) Complete the following timing diagrams for a gated D latch. Assume Q begins at 0.



- (10 points) Complete the following diagrams for the rising-edge triggered D flip-flop. Assume Q begins at 1.

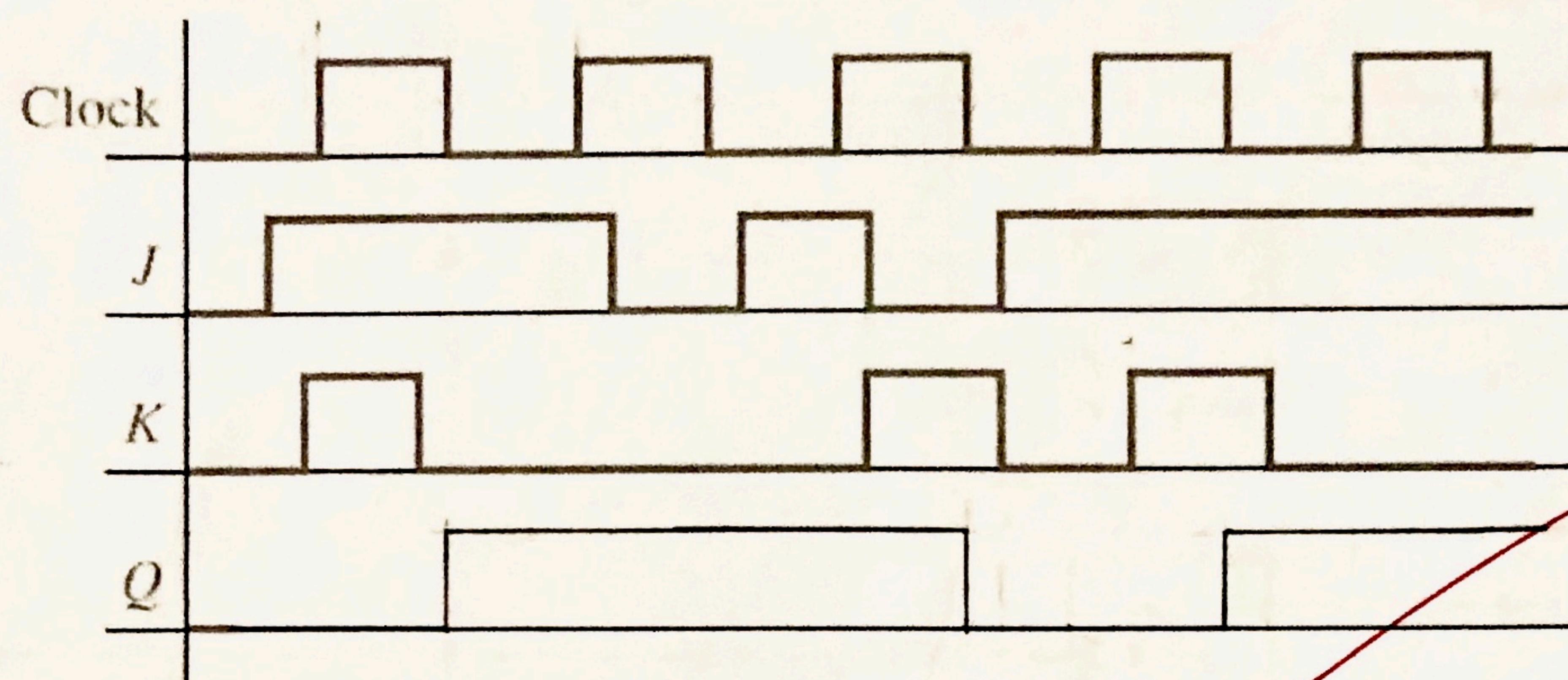




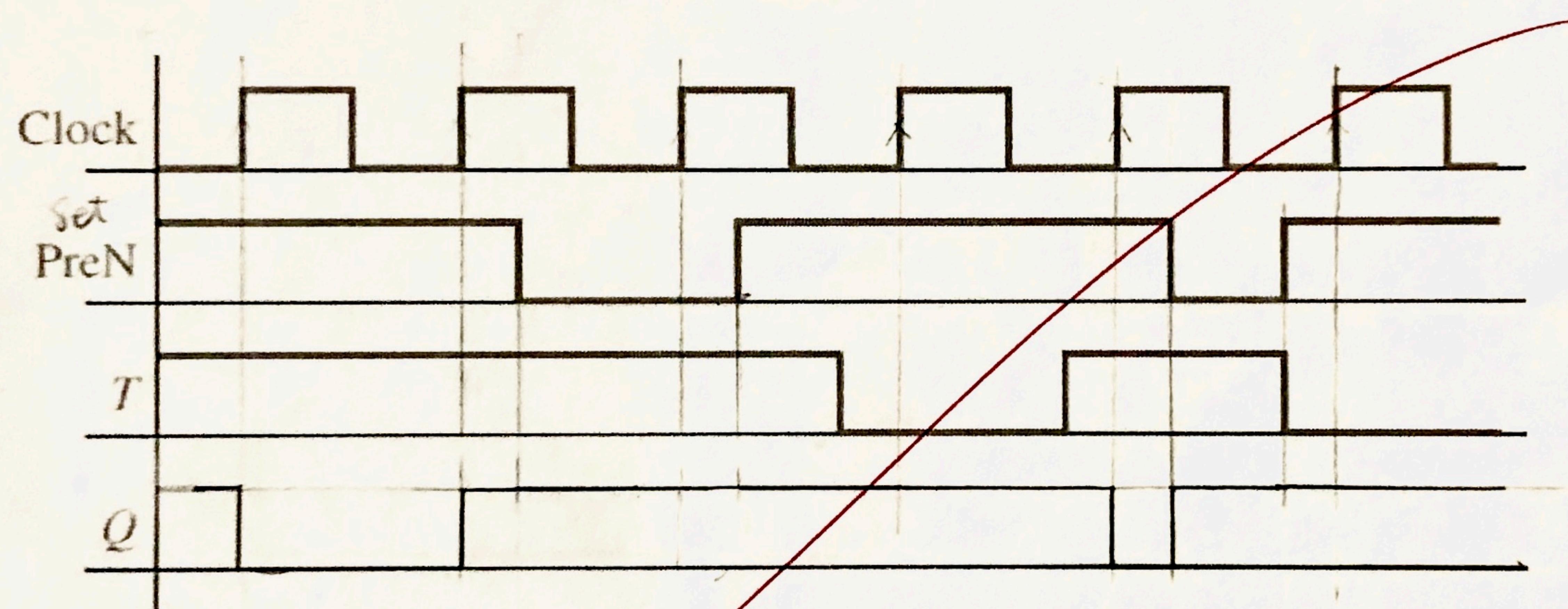
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4. (10 points) Fill in the timing diagram below for a falling-edge triggered J-K flip-flop.
Assume Q begins at 0.



5. (15 points) Fill in the following timing diagram for a rising-edge triggered T flip-flop with an asynchronous active-low preset input (PreN, equivalent to set). Assume Q begins at 1.



6. (15 points) Design a 4-bit register with an enable signal “REV”, such that when REV = 1, content of the 4-bit register is reverse (e.g. 1011 becomes 1101), and when REV = 0, the register works as normal.
7. (15 points) Problem 3.19. Draw schematic.
8. (15 points) Problem 3.20.

