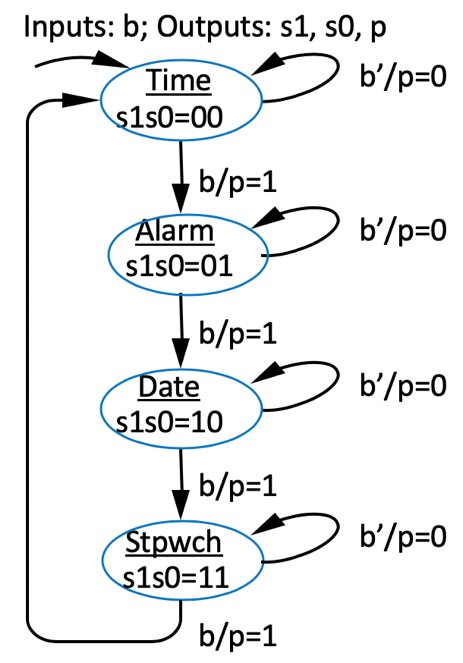
**Ve270 Introduction to Logic Design Homework 8**

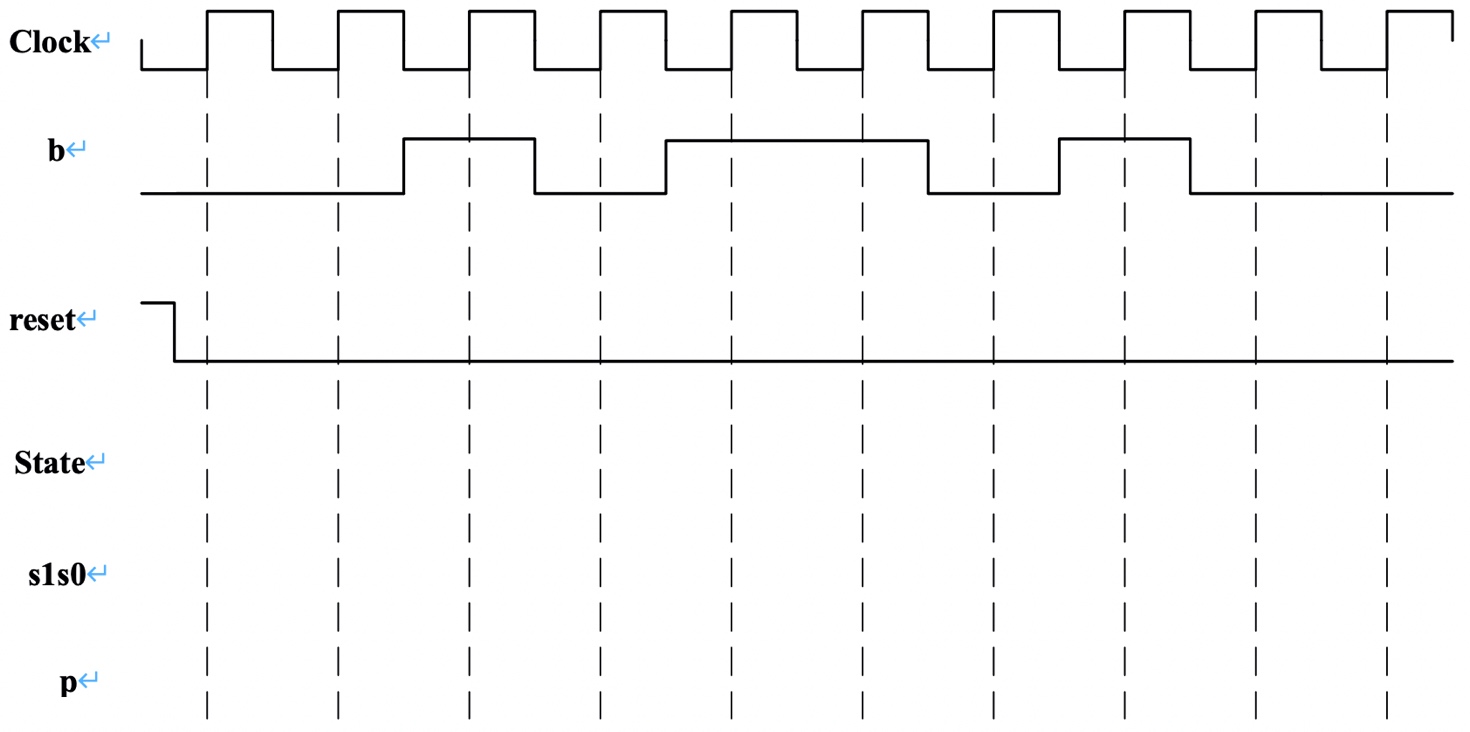
**Assigned: July 14, 2020**

**Due: July 21, 2020, 2:00pm.**

**A pop quiz will be given on July 23.**

1. Given a finite state machine described as the following state diagram, complete the timing diagrams of states and outputs s1s0 and p according to the given inputs b and reset. Ignore delays. (20 Points)





1. Problem 5.3 (15 points)
2. Problem 5.4 (20 points)
3. Problem 5.14. (25 points)
4. (20 points) Create an FSM that interfaces with the datapath in following figure. The FSM should use the datapath to compute the average value of the 16 32-bit elements of an array A. Array A is stored in a memory, with the first element at address 26, then second at address 27, and so on. Assume that putting a new value onto the address lines *M\_addr* causes the memory to almost immediately output the read data on the *M\_data* lines. Ignore overflow issues.

