中国科学技术大学

硕士学位论文

准延迟不敏感异步标准单元库的设计与实现

作者姓名：　Shahzad Haider

学科专业：　电子科学技术

导师姓名：　陈松副教授

完成时间：　二〇一九年五月三十日

University of Science and Technology of China

A dissertation for master's degree

Design of Quasi-Delay-Insensitive Asynchronous Cell Library at 40nm CMOS Technology

Author: Shahzad Haider

Speciality: Electronics Science and Technology

Supervisor: Associate Prof. Song Chen

Finished time: May 30, 2019

中国科学技术大学学位论文原创性声明

本人声明所呈交的学位论文，是本人在导师指导下进行研究工作所取得的成果。除已特别加以标注和致谢的地方外，论文中不包含任何他人已经发表或撰写过的研究成果。与我一同工作的同志对本研究所做的贡献均已在论文中作了明确的说明。

作者签名：_____ 签字日期：_____

中国科学技术大学学位论文授权使用声明

作为申请学位的条件之一，学位论文著作权拥有者授权中国科学技术大学拥有学位论文的部分使用权，即：学校有权按有关规定向国家有关部门或机构送交论文的复印件和电子版，允许论文被查阅和借阅，可以将学位论文编入《中国学位论文全文数据库》等有关数据库进行检索，可以采用影印、缩印或扫描等复制手段保存、汇编学位论文。本人提交的电子文档的内容和纸质论文的内容相一致。

保密的学位论文在解密后也遵守此规定。

☑ 公开 ☐ 保密（____ 年）

作者签名：_____ 导师签名：_____

签字日期：_____ 签字日期：_____

摘　要

在工业上，由于缺乏异步电路设计的工具、技术和相关逻辑单元库，使得设计人员难以在 SoC 设计中应用异步电路，因此，异步电路很少应用于工业设计领域。此外，深亚微米工艺也增加了漏电流功耗。基于准延迟不敏感的读出放大器半缓冲逻辑单元库是一种强大的异步电路设计库，它能够在深亚微米工艺下平衡延迟和功耗的影响。

为了减少这种差距，本文提出了一种有效的异步准延迟不敏感逻辑单元库的设计，该库采用了适合深亚微米 CMOS 实现的设计流程，着重于减少传播延迟和功耗。该方法通过闩锁效应来平衡逻辑单元中晶体管的尺寸和性能，通过多电压阈值技术进一步减少了功率约束下的传播延时。该方法在实现晶体管网络中整体性能的平衡非常有用，同时能够对功率约束下关键路径和非关键路径上的晶体管进行加速或减速。

该基于先进的准延迟不敏感的读出放大器半缓冲逻辑单元库的设计方法已通过 SMIC 40nm 工艺的验证。具有 Muller C 元件的基本单元被设计并以 1.1V 标称电压进行测试，亚阈值电压设为 400mV，并在不同的温度下以 1GHz 的频率进行采样验证。该设计的原理图、版图设计和仿真在 Cadence ICFB 完成，并使用 Cadence 模拟设计环境中的 Spectre 模型进行验证。当以先前的库为基准进行测试时，生成的逻辑单元库显示出传播延时和功耗均有所改善。

关键词：异步; 准延迟不敏感; 低功耗；高性能；设计流程；逻辑努力；多电压阈值

ABSTRACT

Asynchronous circuits are not being adopted in industry due to the lack of asynchronous circuit design tools, techniques, and logic cell libraries. The lack of tools, techniques, and logic cell libraries makes it challenging for designers to pursue asynchronous circuits in SoC design. Furthermore, implementation at deep submicron substantial increase in leakage power consumption. Quasi-Delay-Insensitive based Sense Amplifier Half-Buffer logic cell library is a robust class of asynchronous circuit design approach which pose overhead of delay and power consumption at deep submicron.

To contribute in reducing the gap, this work present design of efficient asynchronous Quasi-delay-insensitive logic cell library using proposed design flow suitable for deep submicron CMOS implementation with emphasis on reduction of propagation delay and power consumption. The proposed design flow size/balance transistors in the logic cell via Logical Effort technique. The flow further reduce propagation delay under power constraint via Multi-Voltage Threshold technique. Such an approach is useful in deep submicron design to achieve the most balanced configuration in a transistor network while speeding/slowing the transistor for critical and non-critical paths under power constraint.

The design flow is tested by developing improved Quasi-Delay-Insensitive based Sense Amplifier Half-Buffer logic cell library on 40nm CMOS technology. The basic library cells along a Muller C element were developed and tested using 1.1V nominal voltage. The subthreshold voltage was set to 400mV with 1GHz frequency sampling under different temperatures for validation. Cadence ICFB was used in designing the schematic, symbol, layout and test circuits. The verification was performed with Spectre models using Cadence Analog Design Environment. The resulting logic cell library when benchmarked with predecessor libraries show improvement in propagation delay and power consumption.

Key Words: asynchronous; Quasi-Delay-Insensitive; low-power; high-performance; design flow; logical effort; multi-voltage threshold;

Contents

List of Figures

List of Tables

Notation

τ	Technology specific time constant
d_{abs}	Absolute delay without technology parameters

Chapter 1 Introduction

The widespread use of electronics in our society have dominated manual operations. In fact, electronics have dominated every sector of humans. Consumer electronics gained preference in modern life especially in communication sector by improving the way of life. Almost everything of mechanical nature has been replaced with electronic alternatives and continues to do so. Such evolution of electronics pave ways of efficient transition in to a modern world where computation is faster, storage is bigger, devices are smaller, and power efficient than ever.

The exponential decrease in feature size of gate length is predicted to go as far as 3 nanometers by year 2021 as shown in 1.1. It is important for designers and industry to keep up with the ever-increasing requirements of high speed, low performance, densely packed transistors on a shrinking die[1-2]. The increasing density of integrating transistors and decreasing feature size demands evolution in design techniques and repetitive tasks of circuit design for SoC[3]. On other hand, the increasing gap between system specification and manufacturing leads to exploitation of different techniques of circuit design[4]. To efficiently fill this gap a set of standard cell library and algorithms are used according to defined set of instructions known as design flow to reduce the design time to market.

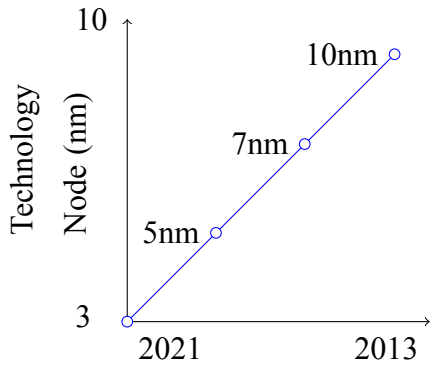


Fig. 1.1 Transistor scaling timeline[5]

The most dominated philosophy of digital Integrated Circuits (IC) design today is synchronous. Synchronous circuits are dependent on clock signals in discrete time to operate at precise time for correctness. This approach substantially reduces design time by modeling in Hardware Description Language (HDL) to translate and map design in to gates[6]. Such approach employs limitations on Very Large-Scale Integration (VLSI) like System-on-Chip (SoC) designs since clock accumulates to ∼45% of total power

consumption and in some high-performance processors ~70%. International Roadmap for Semiconductors predict ~22% to ~54% of asynchronous adoption by year 2026[5].

Alternatively, asynchronous circuits does not use discrete time to synchronize operations across a chip. The synchronization of processing elements and sequencing is performed with handshaking protocols. Such a mechanism leads to arrangement of modules in a way where storage elements are activated on demand which results in less switching of transistors and faster outputs[7]. This capability of circuits can be molded into benefits of low power consumption, high operating speed, less emission of electromagnetic noise and robustness towards variations in PVT. Furthermore, the resulting chip is free from clock distribution and skew problems.

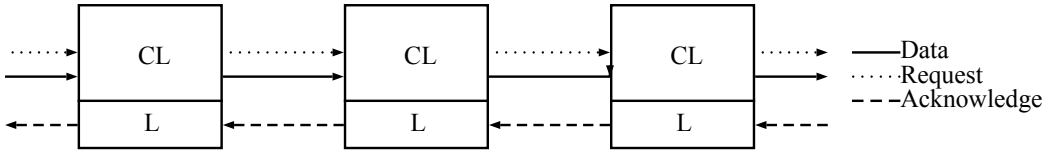


Fig. 1.2 Asynchronous Pipeline

The aim of this work is to evaluate the latest quasi-delay-insensitive based asynchronous logic cell library Sense Amplifier Half-Buffer (SAHB) for penalty of propagation delay and power consumption due to deep submicron challenges in 40nm CMOS technology. This aim is further extended in devising a design flow suitable in developing logic cell library with improved architecture. The simulation results of logic cell library designed with this design flow when benchmarked with predecessor logic cell library at 65nm show improvements in propagation delay and power consumption. The proposed design flow can be used in developing logic cell library for any technology. The techniques used in the design flow make it technology independent by striping the technology parameters for improving logic cell performance.

The authors in[8] implemented sequential decoder for low-power high-performance applications with design flow of quasi-delay-insensitive pre-charged half buffer (PCHB) logic cell library. The flow was used to develop all the required views as per specification. The logic library cell was developed for TSMC 25nm CMOS technology, the resulting performance was satisfactory compared to work in[9]. The logic cell library in this work was developed using 65nm CMOS technology. The resulting logic cell library achieve low-performance and high-performance with resistance against known and unknown PVT variations. However, when similar logic cell library is developed using 40nm CMOS technology result in poor performance.

The main focus of this work was the design of an efficient quasi-delay-insensitive

based logic cell library using a proposed design flow at 40nm CMOS technology. The logic cell library developed is limited to post-layout simulations only. The proposed design flow was used in developing QDI SAHB logic cell library and verified using functional simulation and post-layout simulations with technology specific parameters. The design flow is limited to logic cell design only and does not cover system level design process. There are various techniques of system level designs, which can be used after exporting the library contents. The system level designs are mostly performed using Cadence Encounter or Synopsys DC which are not covered in this work. The following research questions are addressed in this work:

1. Designing quasi-delay-insensitive based SAHB logic cell library in deep submicron can impose penalty on propagation delay and power consumption?
2. How the design of quasi-delay-insensitive based SAHB logic cell library can be improved at deep submicron to consume less power and delay?

It has been reported in various studies that designs at DSM have increased leakage hence resulting in more power consumption and propagation delay. According to International Technology Roadmap for Semiconductors (ITRS)[10], the design at 65nm or lower CMOS technology require significant modifications in communication architectures and protocols. This work proposes a design flow which use logical effort and multi-voltage threshold transistor techniques to counter DSM effects reported by ITRS. Finally, designing at deep submicron for quasi-delay-insensitive SAHB logic cell must follow deep submicron guidelines to reduce leakage for optimizing propagation delay and power consumption.

1.1 Contributions

This work show that key to efficient implementation of quasi-delay-insensitive SAHB logic cells in deep submicron relies on balancing/sizing transistors via logical effort and multi-voltage threshold technique to optimize the overall performance. This approach is consolidated in proposed design flow and the SAHB logic cell library was developed at 40nm CMOS technology using the proposed design flow with efficient performance results in comparison to its predecessor design approaches[9].

To balance/size the transistors in the logic cell, method of logical effort (LE) technique[11] is used. This technique is relatively easy and therefore widely used in VLSI designs. Performance improvement has been presented in various works and some of them can be seen in[12-16]. Furthremore, the logic cells can be improved via MVT tech-

nique, another similar technique Dual Voltage Threshold (DVT) which is widely used in reducing power consumption only. However, this work use MVT technique[17] to optimize both propagation delay and power consumption simultaneously.

The resulting logic cell development of quasi-delay-insensitive logic cell library using proposed design flow show ∼4% reduction in propagation delay and ∼33% reduction in power consumption. Finally, the design flow is technology independent which makes it useful in developing and optimizing the logic cell library not limiting at 40nm CMOS technology.

1.2 Thesis organization

The remainder of this work is organized as follows. Chapter 2 provides literature review of asynchronous circuits focusing on QDI class SAHB design approach and techniques used in this work. Chapter 3 presents the proposed design flow and improved QDI SAHB cell architecture. Chapter 4 presents the improved logic cell library developed in this work. Chapter 5 presents the simulation and results of QDI SAHB buffer cell. Chapter 8 discuss conclusions and future work. Complete library cell layouts can be consulted in Appendix A.

Chapter 2 Preliminaries

2.1 Design Flow

A typical fully-custom back-end design flow is shown in 3.1, which is widely used in analog circuit design. However, for digital circuit design a pre-designed standard cell library is provided by foundries which is extensively tested before releasing. Using a front-end design flow the logic cell libraries are used via Hardware Description Language (HDL) to model a design. Such standard libraries serve as building blocks for synchronous circuits which is not commercially available for asynchronous circuits. In a nutshell, there is a huge gap of design flow and standard logic cell libraries for asynchronous circuit design. However, there has been few design flows and logic cell library proposed by academia for asynchronous circuits and discussed in subsequent paragraphs.

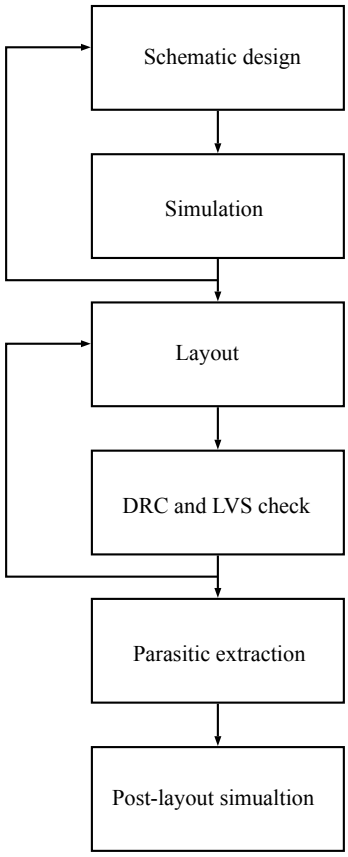


Fig. 2.1 Typical full-custom design flow

The Figure 2.1 show that fully-custom design flow which provide very high design density, performance, and flexibility for circuit design. However, the design time is very long which makes it difficult for the designers and industry to opt. To close the

design gap for asynchronous circuit, availability of design flows and standard logic cell libraries are crucial.

Table 2.1 Trade-off in design styles

	Fully-custom	**Cell-based**	**Pre-diffused**	**Pre-wired**
Density	Very high	High	High	Medium low
Performance	Very high	High	High	Medium low
Flexibility	Very high	High	Medium	Low
Design time	Very long	Short	Short	Very short
Manufacturing time	Medium	Medium	Short	Very short
Cost (low volume)	Very high	High	High	Low
Cost (high volume)	Low	Low	Low	High

STFB based standard logic cells for asynchronous circuit design and flow is presented in[18] which achieved high-performance by controlling top-block sizes and/or wire length in the place and route flow. However, this flow is concentrated on high performance only. This makes it not suitable for low-power applications.

ASCEND design flow[19] provides faster development and characterization of asynchronous logic cell library with a separate tool for layout design. The design flow is tested with a 65nm CMOS technology. However, this flow does not optimize the logic cell library and layout automated tool is not suitable for complex asynchronous logic cells.

2.2 Asynchronous Logic Cell Libraries

An area efficient high-speed of upto 1.4GHz non-linear pipeline was developed using STFB logic cell library in[18]. The development and verification was performed for TSMC 25nm CMOS technology. Local handshaking embedded in the logic cell employs asynchronous communication channel. The logic cell library is only available through MOSIS education program. Synopsys and Cadence can be used in developing the logic cells using the specified design flow. However, this flow is limited to development of STFB logic cell library.

The work in[18] present asynchronous logic cell library with design of low-power and high-performance sequential decoder. The logic cell library is generated using the steps of specification, design, abstract, symbol and behavioral views which are characterized for electrical behavior. The STFB logic cell library is available free through

MOSIS educational program for TSMC 25nm CMOS technology. However, the library requires further improvement in performance with strength and load capacitance.

The authors in[9] propose a design of quasi-delay-insensitive SAHB logic cell library for asynchronous circuits. The cell design provide local handshaking embedded in the cell with various features of robustness against PVT variations, input completeness, and full-range dynamic voltage scaling (FDVS). A Kogge Stone 64bit adder was designed and verified with 1GHz sampling frequency of 1V as nominal, 350mV as subthreshold voltage.

2.3 Optimization Techniques

2.3.1 Logical Effort

The fastest way to estimate delay in a CMOS circuit can be obtained using Logical Effort[11]. Basically, the Logical Effort finds out the fastest functions for a given circuit, how big the transistors should be to achieve less propagation delay, and the number of stages to achieve desired delay in circuit. Logical effort can be used to improve delay in a circuit by modifying the transistor sizes or circuit topology.

Logical effort provides a simple model for delay for a logic gate to estimate propagation delay. According to this model, such delays are caused by the capacitive load of the gate and the circuit's topology[13-14]. Inverter gates are the best and simple examples of amplifications for large driving of capacitances. It is because of the simplicity of transistors connected in the inverter cell, which is not true in comparison for a NAND gate where the transistors are in parallel and series together. That is why the NAND has higher delay when compared with inverter with similar load and transistor sizing. The benefit of logical effort is to quantify these parameters in an easy delay model for best selection of topology and transistor sizing.

The logical effort, strips the technology dependent delay parameters in a specified unit of time constant τ. This is basically the delay from a functional verification of the Process Design Kit (PDK) process. Thus, τ is the delay of an inverter driving a similar inverter without any parasitic delay. In this 40nm CMOS technology, the τ is 40 ps and delay is characterized without parasitics in 2.1.

$$d_{abs} = d_{\tau} \tag{2.1}$$

$$d = f + p \tag{2.2}$$

$$f = gh \tag{2.3}$$

$$h = \frac{C_{out}}{C_{in}} \tag{2.4}$$

The delay in the gate is contributed contributed by two factors; parasitic (p)and effort delay (f). This total delay can be calculated using the Equation 2.2. Further simplifying the delay model, the effort delay is divided in to two sub parts as in 2.3. The product of g and h, shows the product of logic gate and load characterization. The g from Equation 2.3 provides the ability of producing output current with respect to the logic's topology which is independent of gate sizing. h is how the sizing of transistors can affect performance and load driving and calculated as per Equation 2.4. Furthermore, the electrical effort is the ratio of output capacitance to input capacitance. Combining the Equations 2.1, 2.2 and 2.3 a complete equation can be obtained for delay without effects of technology in 2.5.

$$d = \tau(gh + p) \tag{2.5}$$

In summary the parameters used in delay calculations are:

- τ: Characteristic delay
- h: Electrical effort
- g: Logical effort
- p: Parasitic delay

The operational speed and energy consumption is impacted by transistor topology and sizing in a circuit. Logical effort use effective current models to optimize critical paths. When transistor sizes are increased to improve speed, consequently result in delay and power consumption due to the charging and discharging of input and output large capacitances[11]. This proves that transistor sizing alone do not contribute in achieving speed. Hence, a trade-off or effective technique is required for optimized circuit performance and energy consumption. The transistor sizing should be done to balance the speed and load of successive logic gates.

Ivan Sutherland provided a fastest way to logical effort for synchronous[11] and asynchronous circuits[14] and provided example implementation in GasP asynchronous circuits[13]. The authors in[12] presented an approach for selecting transistor sizing to optimize energy consumption and speed of asynchronous circuits which uses discrete values from standard cell library and handling multi-stage CMOS cells.

2.3.2 Multi V_{th} Technique

As the density of transistors on die increases and the channel length of transistors decreases, introduces challenges to the designers. Among those challenges, the most important is the leakage produced in the circuit. To understand this, lets take a look at the transistor voltage which is applied for the operations. The transistor is considered ON when the supply voltage (V_{DD}) is higher than the threshold voltage (V_{th}) and considered OFF when its V_{DD} is lower than V_{th}. To reduce the leakage in circuit techniques are required to reduce leakage at the transistor level. While a transistor in sub-threshold region is not OFF completely which can be observed with leaking current flowing[20]. Moreover, the transistor can function properly with such leaking current. This provides the opportunity of low-power operations of transistor and there has been a substantial research contributions since 1960s. This feature attracts the applications of low-powered devices dependent on limited batteries. There are various kinds of V_{th} transistors provided by foundries. The most common types provided are RVT/SVT, HVT, LVT which are described below:

- RVT/SVT: Regular/Standard-V_{th} Transistors
- HVT: High-V_{th} Transistors
- LVT: Low-V_{th} Transistors

As the name suggest, the regular/standard voltage transistors are typical transistors without nominal voltage for operations. The HVT provides reduced leakage power with increase in delay and LVT provides decreased delay with increased leakage current. Trade-off is the most important aspect in IC design consideration. Similarly, in case of threshold voltage transistors it is important to trade-off between speed and power consumption. The most efficient technique is Multi-Voltage Threshold (MVT) Transistors. The slack based MVT techniques is considered most efficient for circuits with improvement in terms of speed and power consumption.

In short, all the transistors are replaced with one kind of transistors HVT or LVT depending on the requirements and under a constraint the transistors in critical and non-critical path are replaced to achieve required speed and power consumption.

MVT technique was used in[21] was applied to NoC swith with an enhanced $DualV_{th}/DualT_{ox}$ CMOS technique showed overall of μ83% reduction in power consumption with μ20% reduction against origianl $DualV_{th}/DualT_{ox}$ CMOS technique. In[22] the authors simulated 1-bit full adder at 0.7 voltage and results show 80-85% reduction in power consumption with no impact on chip area when bench marked with

typical CMOS design approach.

Another approach containing MVT was reported in[23] where standard cells were targeted for power reduction and was reduced to 80.51%. This approach is based on post-layout analysis of delay, leakage and parasitic capacitance and various techniques including MVT were applied. Application specific comparative study was reported in[24] finding suitable techniques for combinational and sequential circuits. The authors reported that triple phase technique proved best for combinational while MVT based dynamic forward body bias trimode technique best suit sequential circuits.

An SoC design was implemented in 90nm technology at 1 voltage called power consumption reduction strategy (PCRS)[25] using various techniques including MVT design approach resulted in 5.15% reduction in power consumption. The authors in[20] presented low-power optimization technique (LPOT) using MVT techniques by simulating 1 voltage 32-bit pipelined RISC microprocessor at 90nm CMOS technology showed reduction by 20% at the clock cycle of 1.35ns. In[26] a power consumption optimization methodology (PCOM) via MVT technique is presented and simulated for the design of 1 voltage 32-bit MIPS microprocessor at 90nm CMOS technology at 0.9ns period has reduced by 27.23% in static period and 12.53% in dynamic switching period.

The authors in[27] present a study on MVT technique by replacing SVT/RVT with only HVT may leads to drastic increase of power consumption due to required transistor sizing required to satisfy delay constraints. A low-power design technique (LPDT) was proposed in[28] using MVT technique for low-power micro-pipeline processor operating at 1 voltage using 90nm CMOS technology show 17.8% average total power consumption. In[29] an energy efficient and low-power 4-bit Binary Coded Decimal (BCD) adder was simulated at 45nm CMOS technology using MVT technique show 47.41% power consumption reduction. The adder consumes $1.384\mu W$ with supply voltage of 1V at 200 MHz frequency.

A technique based on MVT and Gate Diffusion Input (GDI) was reported in[30] for low-power, energy efficient and high-speed full adder. The technique reduced 51.18% of average power consumption in reported design operating at 0.9 voltage on 45nm CMOS technology. The authors in[31] propose an algorithm for small designs which opt for replacing HVT transistors on non-critical path and LVT transistors on critical path for an efficient trade-off of delay and power consumption. Using HVT transistor to reduce leakage power under delay constraint is an NP-hard problem and the proposed work approximate polynomial time algorithm to address this problem.

A critical-path aware power consumption optimization (CAPCOM) technique was

introduced in[32] via MVT technique is used in design of low-power SoC using 90nm CMOS technology at 1 voltage show 44.9% reduction in power consumption when compared to a typical MVT CMOS technique. A variable run-time for commercial project of IC using MVT technique was proposed in[33] show reduction of 23.52% power consumption.

The simulation in[30] show substantial reduction in power consumption when an XOR gate is designed using MVT technique and bench marked against its conventional CMOS, transmission gates, and Complementary Pass-Transistor Logic (CPL) simulations at 45nm CMOS technology with 0.9 supply voltage. Two cell libraries were designed in[17] for 130nm and 90nm CMOS technology using MVT technique by replacing LVT cells on critical paths and SVT/RVT cells on non-critical path shows 5% - 30% reduction in power consumption. The authors in[34] presents a comparison of conventional MVT and proposed approach via MVT technique with 14.186% savings in power consumption.

An iterative refinement model is presented in[35] based on classic dynamic programming (DP) which includes an enhanced timing optimization algorithm, multiplier selection method, delay/power splitting approaches resulting in 20% reduction in delay and 3% reduction in power consumption. An interesting study is presented in[36] comparing the results of DVT and MVT where MVT show reduction in power consumption of 65% and 25% reduction using Dual V_{th} designs.

The authors in[37] optimize proposed MVT library cell design with 27% shows advantage of MVT cells for low-power designs. A technique introduced in[38] with High Threshold Voltage (HTV) assignment priority factor show 25% reduction in total average power consumption. A technique using subcircuit extraction assign proper threshold voltrage to all signal paths in circuit shows 12% savings on leakage power.

A mixed technique in[39] combines Dual Threshold CMOS, Mixed-T_{ox} CMOS, and pin-reordering resulted in 65% reduction in leakage power consumption. Another technique in[40] use high voltage and standard voltage sleep transistors to reduce leakage with 3 order of magnitude when bench marked with MCNC'91 circuits. The authors in[16] presents a design methodology incorporating MVT in to quasi-delay-insensitive circuits NCL circuits which focus on solving the data loss during sleep mode.

2.4 Sense Amplifier Half-Buffer (SAHB)

It is important to understand the building blocks of an asynchronous circuit system which includes selecting the data encoding and handshaking style. QDI SAHB use dual-rail encoding which represent 2 wires per bit and 4 phase handshaking protocols which is sometimes known as Return-to-Zero (RTZ) protocol.

Table 2.2 Dual-rail codeword

Codeword	T	F
Empty	0	0
Valid ’0’	0	1
Valid ’1’	1	0
NULL	1	1

For a complete set of communication between elements of asynchronous circuits, a defined set of cycle is executed for delivery of data. As can be seen in Figure 2.2 the request signals are integrated into data wires.

For a 2-phase protocol circuits, the initiating element send data by passing valid information on data line, transitioning the request signal. The receiving element receives the data along with transition on request signal.

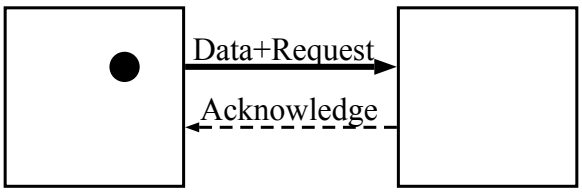


Fig. 2.2 Dual-rail 4-phase protocol

The sender confirms receiving data by transitioning the acknowledge signal, after which there is no guarantee of data validity. This marks the end of a complete 2-phase communication between processing elements in asynchronous circuits.

In 4-phase protocol circuits, the initiating element send data by passing valid information on data line, setting request signal to high. The receiving element receives the data and with request signal and respond by setting acknowledge signal high. The sender confirms receiving of acknowledge by setting the request low marking the end of data validity. In response, the receiving element sets the acknowledgement low. This marks the end of a complete 4-phase communication between processing elements in asynchronous circuits.

Figure 2.4 shows a block of SAHB cell template with inputs and outputs. A gen-

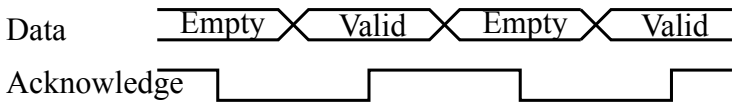


Fig. 2.3 Dual-rail 4-phase protocol waveform

eral SAHB cell template have complementary signals for all the provided signals. Lack, nLack, Rack, nRack are the handshaking signals known as left acknowledgment, complementary left acknowledgment, right acknowledgment, complementary right acknowledgment respectively. These handshaking signals are used for controlling the 4-phase protocol communication integrated inside and outside the cell. As discussed in previous sections the dual-rail circuits have request signal integrated into data wires, which is not visible to designers. For data wires, the inputs are Datan and its complementary signal nDatan while outputs are QT with complementary signal nQT and QF with complementary signal nQF.

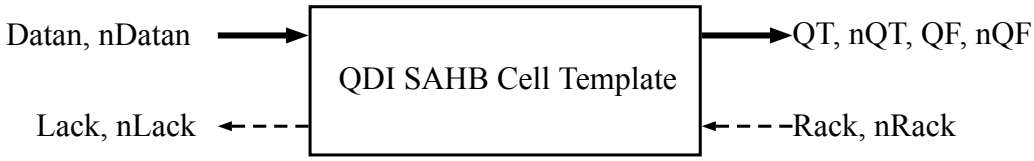


Fig. 2.4 QDI SAHB cell template

The QDI SAHB is a new cell design approach from[9] which provides intriguing features of high speed, low power consumption, and high operational robustness. The QDI SAHB cell is broken in three parts based on the kind of operations for understanding. These blocks include evaluation (EV) block, sense amplifier (SA) block, and complementary buffers (CB) block. In the rest of the text, the acronyms of EV, SA and CB will be used as shown in Figure 2.5.

The EV and SA blocks work together to guarantee asynchronous 4-phase protocol operations. Integrating the 4-phase QDI protocol where the switching of the gates is done according to the handshaking signals. This helps the SAHB cell to operate under known and unknown PVT variations. While the EV block works on subthreshold voltage, it is important to speed up the output as soon as the data is valid using the cross-coupled latch with a positive feedback technique.

With scaling down of technology in nanometer design, the parasitic capacitance is of growing concern. For low parasitic capacitance the EV block in completely designed using only NMOS transistors instead of PMOS and NMOS. By using only, the NMOS transistors, the resulting design has less parasitic capacitance and less power consumption. Due to its design in static logic design makes it appropriate for full-range dynamic

voltage scaling (FDVS).

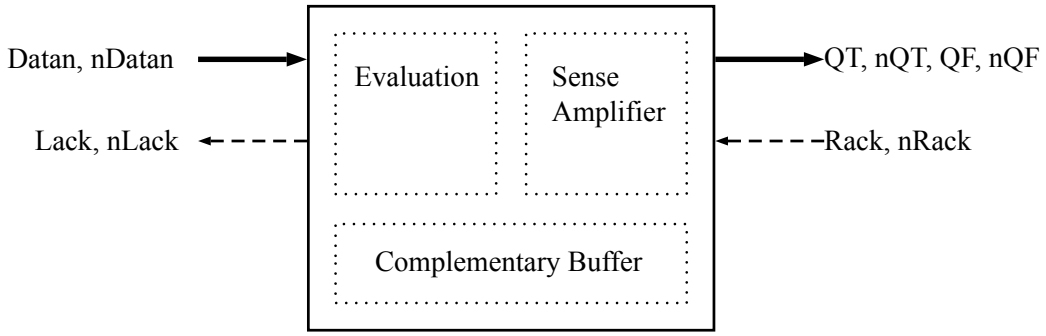


Fig. 2.5 QDI SAHB blocks

Thus, the supply voltage and deep subthreshold voltage can range from 1V to 0.3V respectively. The library contains basic cells which can be used for complementary operations as well. The two-input AND cell can also be used for NAND operations using its complementary signals. Similarly, two-input OR, XOR, MUX and three-input AND-OR (AO) can be used as NOR, XNOR, IMUX and AOI respectively using respective complementary signals. The authors performed experiment and presented results with parameters of 1V at 1GHz frequency sampling for PVT variations. The results show extensive improvements in performance and power consumption when compared with PCHB[18] which is another cell design approach in the QDI integrated latch family.

However, the original author work was targeted for 65nm technology while this work is performed on 40nm technology which present some challenges of nanometer designs. These challenges are addressed in coming chapters and techniques are also presented to counter these challenges. Furthermore, these techniques are tested at 40nm technology for the design of SAHB and an improved architecture based on these solutions are provided.

The figure 2.5 shows the inputs and outputs signals of a QDI SAHB cell template. The inputs are Rack and Datan; where the outputs are Lack, QT and QF. In addition to these signals, there are logical complementary signals of nRack, nDatan, nLack, nQT and nQF. Due to the 4-phase handshake protocol the operations usually alternate between evaluation and reset. Using the reset the Lack and Rack signals are set to low resulting in empty Datan, QT and QF signals. Alternatively, for complementary signals the nLack and nRack are set to high resulting in empty Datan, QT and QF signals. As per the codewords explained in table – for a valid codeword the bits are different and similar bits for empty and null codewords.

For evaluation, setting a valid codeword on Datan and setting Rack to low while nRack to high will set the evaluation block in motion. These signals with valid code-

words will trigger the logic realization and latch the result while setting to Lack to high (nLack to low) indicating the validity of output. For reset when empty codewords are provided to Datan and Rack is set to high (nRack is set to low) will result in empty codeword on output signals (and null codeword on complementary outputs). Furthermore, the Lack is set low to indicate the outputs are empty (nLack is set to high). This marks the end of communication cycle for evaluation and is ready for next operation.

The sense amplifier participates in 4-phase asynchronous operations by making sure all the inputs are available before amplifying outputs while the result is latched until the handshaking cycle is completed. Once the a full 4-phase handshaking cycle is completed, the outputs are set to empty and the complementary outputs are set to NULL which further generates the handshaking signals. The complementary buffer block generates all the required complementary signals for outputs and feedback signals used in the cell. These complementary signals are further used for completion detection also generating the Lack and nLack handshaking signals.

Chapter 3 Proposed Design Flow via Techniques

3.1 Introduction

This chapter present a detailed insight of the the proposed design flow and development of QDI SAHB cell library from[9] at 40nm CMOS technology. This chapter also explains in detail the techniques used in proposed design flow for improving the existing library design. The EDA tools used in design process are Cadence Virtuoso, Mentor Calibre and Spectre models.

3.2 Design Flow

As explained in Chapter 1, the design flow used in development of this standard cell library is fully-custom. The fully-custom design approach is a tedious and recursive process. A proposed design flow is presented in this chapter for improving development of QDI SAHB cells. Conventionally a pre-designed standard cell library is provided by foundries which are extensively tested before releasing. Such standard libraries serve as building blocks for a complete circuit which is not commercially available for asynchronous circuits. The proposed design flow is shown in Figure 3.1, the steps which are used in this work and discussed in subsequent subsections.

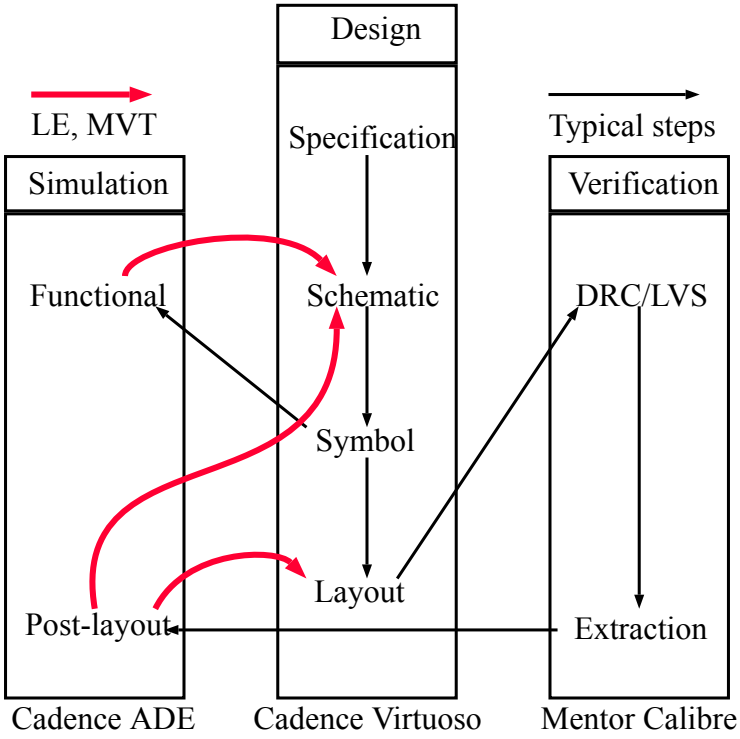


Fig. 3.1 Proposed design flow

3.2.1 Specification

The specification is the first step in design flow. The specification remains the same as per the original work of QDI SAHB from[9]. The cells in original work is designed at 65nm CMOS technology with 1 voltage at 1GHz frequency sampling. The transistor network is a complex combination with one block only containing NMOS transistors while the architecture remains same in this implementation. However, in this work the cell library is designed at 40nm CMOS technology. The cells operate at full-range dynamic voltage scaling (FDVS) for V_{DD} from 1V nominal voltage to sub-threshold voltage of 300mV; while in this work the nominal voltage starts from 1.1 voltage nominal to sub-threshold voltage of 400mV suitable for implementations according to available PDK. In terms of features, the designed QDI SAHB cell must adhere to following:

- 4-phase embedded handshaking protocol
- Speeding the output from evaluation block
- Reduced parasitic capacitance in evaluation block
- Reduced redundant internal switching
- FDVS operations

Since it is important for asynchronous circuits to have correct operations, the 4-phase handshaking protocol embedded in cell provides correct operations at different process, voltage and temperature parameters. The cross-coupled latch in sense amplifier speed up the output evaluation for faster operations. The parasitic capacitance can be substantially be reduced by opting both pull-up and pull-down network composed of NMOS transistors in evaluation block. Careful handcrafting of layout is important to couple the blocks of evaluation and sense amplifier for reduced switching. Finally, the FDVS results in lower power consumption consisting leakage and dynamic consumption.

3.2.2 Schematic

The schematics of QDI SAHB loigc cells were first designed in Cadence Virtuoso Schematic Editor using 40nm Process Design Kit (PDK). The schematic were designed with the sizing specified by authors in[9]. According to their implementation, transistors in critical path PMOS were sized 410/40nm and NMOS were sized 270/40nm, where X/Ynm specify X as the width of transistor and Y as the length. Similarly, for non-critical paths the PMOS transistors were sized 205/40nm and 135/40nm width and length respectively. This ratio of PMOS over NMOS is set as reference and considered as $1X$ transistor sizing for the rest of logic gates.

When porting a design to different technology requires accordingly transistor sizing the design was modified as per the ratios of PMOS over NMOS appropriate in available PDK. The critical path transistor ratio of PMOS over NMOS was set as 480/40nm for PMOS transistors and 240/40nm for NMOS transistors while in non-critical path the transistor ratio of PMOS over NMOS was set as 200/40nm for PMOS transistors and 120/40nm for NMOS transistors.

1. Improvement using transistor sizing

The transistor sizing to improve the performance of the logic cells are performed via Logical Effort (LE) technique. In this technique according to the Equation 2.5 the technology dependent characteristic and parasitic delay associated to the logic cell were stripped off. Using the logical effort and electrical effort values of each logic cell the transistors were balanced under delay and power constraints. Once the balanced transistor sizing was extracted using Equation 2.3, the parasitic delay was added to it post-layout along with the characteristic delay of how worse the logic cell is performing when referenced to an inverter from similar technology.

The logic cells were further simulated and analyzed for performance with characteristic and parasitic delays. Revisting the balancing of logic cell transistor network appropriately, if required improvement targets are not met.

Since the design was tested in multiple stages, the PMOS over NMOS ratio for third stage was set as 600/40nm for PMOS and 300/40nm for NMOS transistors in critical path. For non-critical path the ration was set as 240/40nm for PMOS transistors and 120/40nm for NMOS transistors. Furthermore, the ratio of PMOS transistors in completion detection was set as 300/40nm and 120/40nm for NMOS transistors.

Table 3.1 show summarized PMOS over NMOS ratio of transistor widths. The first row specify the parameters from original work, second row is the as it is implementation of design with specified transistor sizing in original work of QDI SAHB cell work. The design with as it as sizing resulted in incorrect operations. Third row specify the transistor sizing according to minimum sizing of 40nm CMOS technology PDK where the propagation delay and power consumption was substantially increased. Finally, through analysis and recursive processes of improvement an appropriate transistor sizing was assigned and resulted in reducing the propagation delay as per requirements in design specification.

2. Improvement using Multi V_{th} Technique

As explained in chapter 2 the MVT is an efficient technique for fruitful trade-off for reducing power consumption. Some authors use high voltage threshold transistors as

sleep transistor to reduce power consumption while others reduce power consumption by using high voltage threshold in non-critical path and low voltage threshold transistors in critical path to reduce power consumption and propagation delay, respectively.

This work take full advantage of the complex transistor network used in QDI SAHB logic cell and propose a three step approach of using three different types of transistors under delay and power constraints. In first step, the transistors on critical path were replace with low voltage threshold for high speed operations starting from the outputs all the way to the transistors connected to input signals.

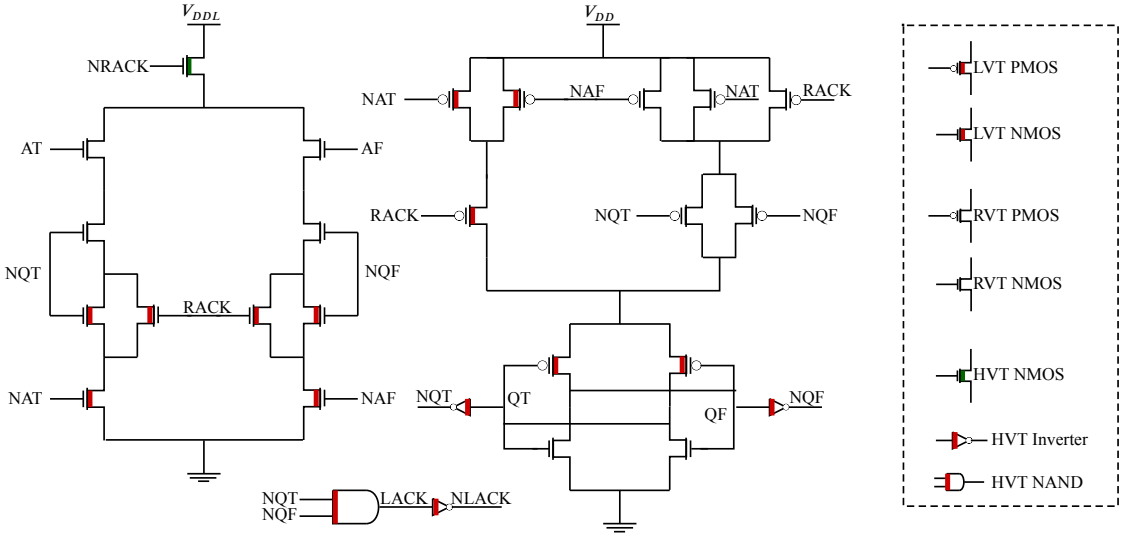


Fig. 3.2 Improved architecture of QDI SAHB buffer cell

This approach increased the switching speed of output signals with a little overhead in power consumption. Second step replace each transistor on non-critical path with high voltage threshold to reduce the power consumption under delay constraint. Third step is crucial for operation correctness where in sense amplifier block parallel transistors responsible for latching results until a full complete cycle is set as regular/standard

Table 3.1 Summarized transistor ratio of PMOS over NMOS

	Critical path		Non-critical path		
Ref/ Stage	**PMOS transistor width**	**NMOS transistor width**	**PMOS transistor width**	**NMOS transistor width**	**Remarks**
[28]	410	270	205	135	Original work
1st	410	270	205	135	Designed as it is
2nd	480	240	200	120	Base design
3rd	600/300	300/120	240	120	Improved design

voltage threshold transistors. The Figure 3.2 schematic of improved architecture for QDI SAHB buffer cell.

3.2.3 Symbols

The process of symbol creation is necessary and straight forward. The symbol is a required views in Cadence design flow which is used extensively in simulation process. Due to the design complexity of QDI SAHB cells and the increased number of inputs and outputs the symbol pins list must carefully be designed. As QDI SAHB asynchronous cells require data signals and handshaking signals with its complementary signals, the handshaking signals in pins list are in reverse order with respect to data signals. This helps in easier connections of logic gate level in test circuits and pipeline designs. The Figure 3.3 shows a buffer symbol as an example with pins list specified.

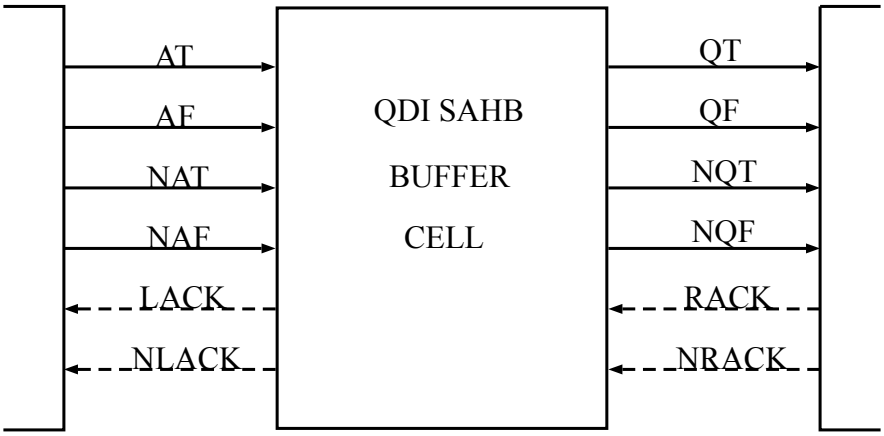


Fig. 3.3 Symbol and pins list of QDI SAHB buffer cell

By opting such pins list makes it easier for interconnection of symbols in simulation circuits. However, the V_{DD}, V_{DDL}, and GND signals are omitted from the figure for simplicity. There are no recursive tasks for symbol creation, unlike schematic and layout creation.

3.2.4 Functional Simulation

This design flow is recursive and requires revisiting functional simulation after each change in schematic until achieved required propagation delay and power consumption. The functions performed in the library cells are following:

$$\begin{aligned} QT &= AT \\ QF &= AF \end{aligned} \tag{3.1}$$

$$\begin{aligned} QT &= AT \cdot BT \\ QF &= AF \cdot BF \end{aligned} \tag{3.2}$$

$$\begin{aligned} QT &= AT \cdot BF + AF \cdot BT \\ QF &= AT \cdot BT + AF \cdot BF \end{aligned} \tag{3.3}$$

$$\begin{aligned} QT &= AT \cdot BT + CT \\ QF &= (AF \cdot BF) \cdot CF \end{aligned} \tag{3.4}$$

These equations specify the logic requirements of library cells. Equation 3.1 shows requirements for buffer operation, Equation 3.2 shows equation for AND/NAND logic gate. Furthermore, the Equation 3.3 and Equation 3.4 shows equations for XOR/XNOR and AO/AOI logic gates respectively.

The functional simulations were performed in Cadence Analog Design Environment (ADE) using Spectre models provided by 40nm CMOS technology. The instance of library cell was created in schematic view for validation. The instance was connected using wires to the nominal voltage and subthreshold voltage sources. A common ground instance was created to provide common ground to all the instances. For sampling inputs as test signals to the cell instance voltage pulses were used which is known as vpulse in Cadence environment. However, no voltage values were specified due to the nature of simulation with variant values a variable name was assigned to each of the source. Similarly, for fully-dynamic voltage scale simulations variables were applied to the nominal and subthreshold voltage sources of the logic cell. The output signals were set to output ports for probing purpose in simulation. Once the test bench circuit is carefully designed in Cadence Schematic Editor, Cadence ADE tool was launched for simulations.

To verify the functionality three kind of results; logic function, propagation delay and average power consumption. The propagation delay and power consumption can be extracted only when the logic function is verified with correct output.

$$T_P = 2 * t_F + 2 * t_B \tag{3.5}$$

To verify the function of logic cell, Figure 2.3 can be referenced to guarantee outputs based on 4-phase handshaking protocol.

$$Power_{average} = \frac{Power_{V0} * 1.1}{2n} + \frac{Power_{V1} * 0.4}{2n} \tag{3.6}$$

The simulation setup and results are explained in subsequent chapters.

3.2.5 Layout

Creating layout at deep submicron have strict and narrow design rules. The minimum spacing rules at deep submicron design must be carefully designed to avoid cross talk and parasitic capacitance. Cadence Layout XL was used in designing layout.

The automated tool from academia for asynchronous cell layout design ASCEND was used[41]. However, the ASCEND tool could not design the cell due to the complexity of feedback signals. The feedback signals were temporarily removed from design to bypass the complexity while using the ASCEND automated layout tool. With such approach the automated layout of the cell was designed using ASCEND resulting in a huge area of logic cell area which is not suitable for asynchronous logic cell layout design. There are no other tools in academia or industry which can automate design of QDI asynchronous logic cells.

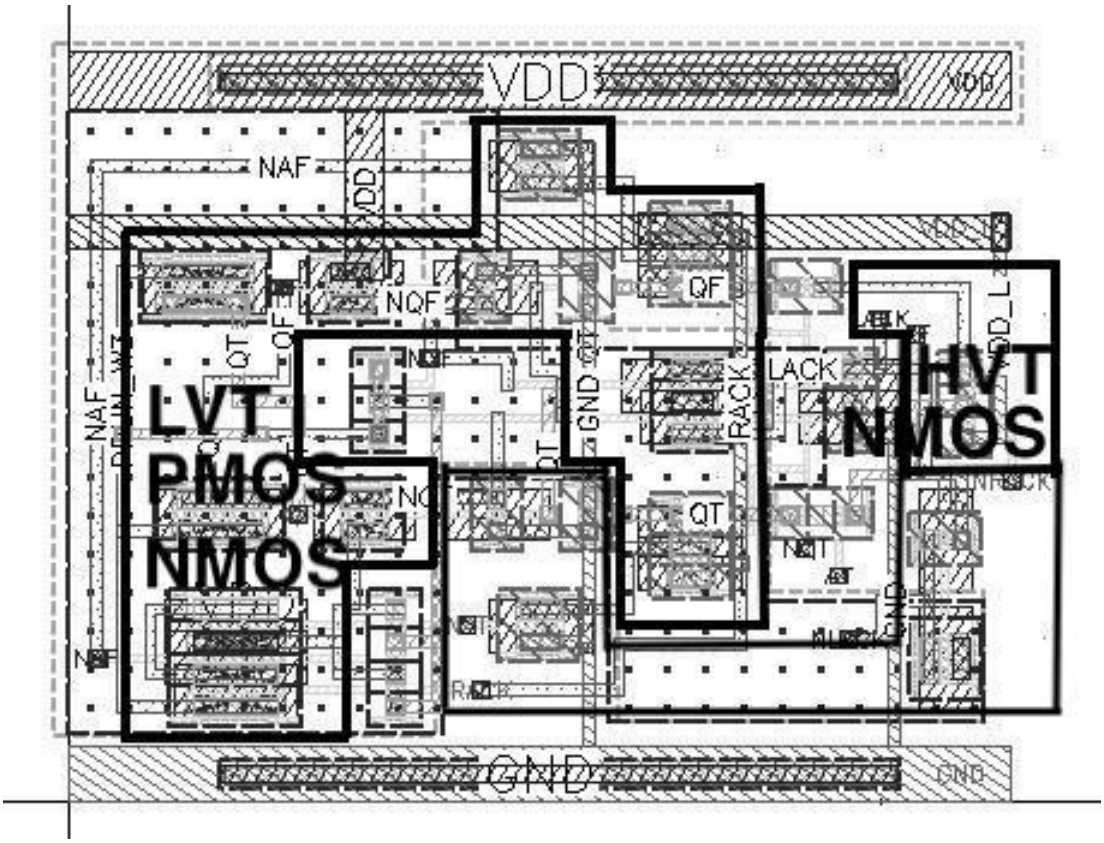


Fig. 3.4 QDI SAHB buffer layout

Finally, manual approach was used for layout design. The cells were handcrafted using Cadence Layout XL editor. The transistors instances were imported to layout view from schematic. The placement of transistors in critical path is done in such a way that the path is reduced as much as possible in layout design. This can reduce the parasitic capacitance produced due to narrow metal spacing rules in deep submicron.

Furthermore, the non-critical path transistors are placed and wrapped around critical path transistors. The placement is done in such a way that feedback signals distance can be kept minimum. The QDI SAHB logic cell height is set fixed as 4 microns with variable width for cells depending on the area requirement. Figure 3.4 show carefully handcrafted layout of QDI SAHB cell whose IC area is only 21.5 microns.

3.2.6 Design rules

Design Rule Check (DRC) was performed using Mentor Calibre tool for layout rules provided by foundry. It is important for layout to follow design for manufacturability (DFM) otherwise the layout won't be able to fabricate. This work is only limited to post-layout simulation at this point, following DRC is still important to pass without any errors and critical warnings to effectively perform extraction.

Furthermore, Layout versus Schematic (LVS) is an important step for correct operations of post-layout simulations and parasitic extraction.

3.2.7 Parasitic Extraction

Parasitic Extraction sometimes known as PEX was also performed using Mentor Calibre tool using the rule file provided by foundry. This process is tedious and require revisiting if proper guidelines are not followed designing layout. The parasitic capacitance on metal wires can be more which contributes to higher propagation delay and power consumption if wires are longer. The coupling capacitance was reduced by observing design rules and provide ample space between signal wires. This process was revised multiple times after modifying layout for decreasing parasitic capacitance and coupling capacitance.

The extraction mode in Calibre output was selected to use xACT 3D with Accuracy 600 for accurate estimation of parasitics. Transistor level with C + CC (Capacitance + Coupling Capacitance) was selected in extraction type with No Inductance. This mode and type of selection takes in to account all the important factors in estimating resistance and capacitance. The extraction process creates Calibre view with resistros and capacitors in a schematic view for post-layout simulation.

3.2.8 Post-layout simulation

The final step in proposed design flow is the post-layout simulation. Post-layout simulation is performed using Calibre view (in general called extracted view) using Cadence ADE tool. The similar simulation test bench from functional simulation can

be used by adding ”calibre” keyword to the Switch View List in Environment Options window. A separate configuration file can also be created to specify the module instance to use Calibre view for simulation.

Revisiting the schematic design recursively according to the design flow resulted in efficient design with improved propagation delay and power consumption. Parametric analysis simulations are performed for different temperature values with different nominal and subthreshold voltages. The characterization of asynchronous circuits can be performed in industry EDA tools[42] but this work perform it using Cadence ADE tool.

Chapter 4 Library Cells

4.1 Introduction

As discussed in Chapter 1, this work contributes by proposing a design flow for improving QDI SAHB library logic cells development. This library is different from original work of QDI SAHB with two main techniques. First, logical effort is used in balancing the transistors for efficient trade-off of propagation delay. Second, the static CMOS design approach is exploited by employing multi voltage threshold transistors to further improve the propagation delay under power constraint and vice versa. Third, it propose a design flow suitable and effective for designing asynchronous QDI SAHB integrated latch approach.

4.2 Process Development Kit

When using the proposed flow and techniques it is important to use a process development kit which provides access to standard/regular, high, and low voltage threshold transistors (RVT, HVT, LVT). The process development kit used in this work have channel length of 40 nanometer and provides multiple voltage threshold transistors. The different voltage threshold transistors available in this work are as following:

- RVT: This type of transistor have almost equal trade-off between propagation delay and power consumption
- HVT: HVT transistors provide low leakage resulting low power consumption at the cost of slow switching speed in transistors
- LVT: LVT transistors proved high speed transistor switching at the cost of increased leakage resulting in higher power consumption

4.3 Naming convention

It is equally important to use a naming convention in naming the library logic cells. The naming convention is later used in producing documentation with function, output load, power consumption and delay values extracted to a pdf format file by Cadence Liberate: an electrical characterization tool. However, electrical characterization using Cadence Liberate is not covered in this work and performed manually using Spectre simulations. The convention used in naming the library cells is

LIBRARY_CELL_STRENGTH where an X1 and X2 buffer can be named as SAHB-BUFFX1 and SAHBBUFFX2, respectively.

4.4 Library Gates

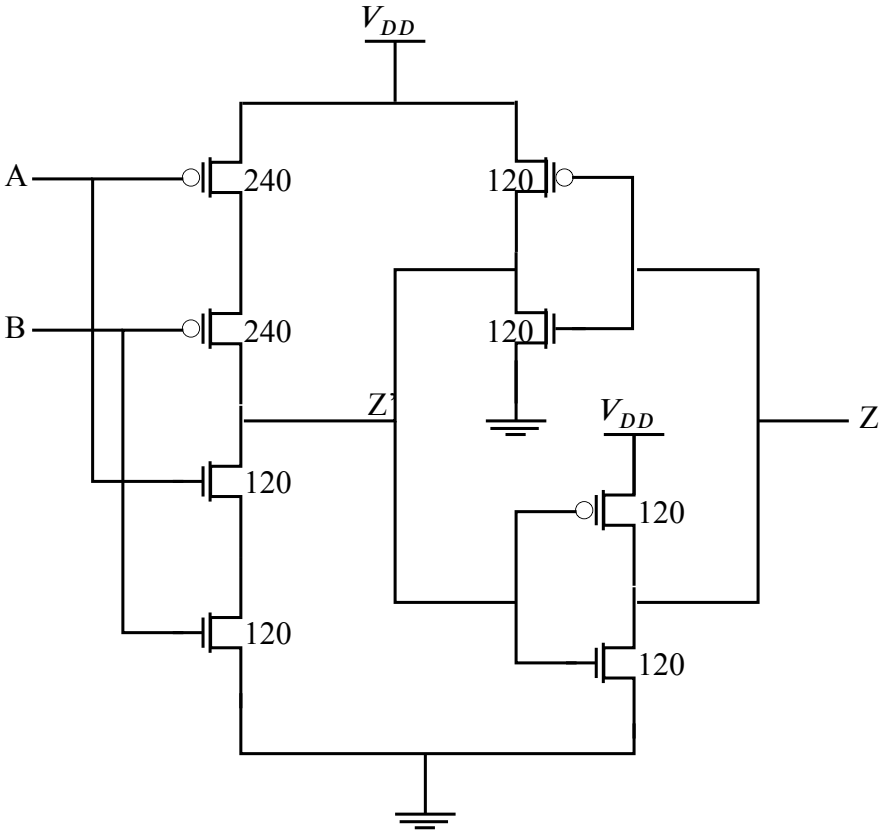
The library gates contains following logic gates:

- 1 input buffer logic cell
- 2 input NAND/AND logic cell
- 2 input XNOR/XOR logic cell
- 3 input AOI/AO logic cell
- 2 input MUX/IMUX logic cell
- 2 input Muller C element

The dual-rail improved QDI SAHB logic cell library contain above listed logic cells along with its complementary functions as the cell design approach is static CMOS. The Muller C element is based on weak feedback design approach which is much stable under various conditions. There is no mutual exclusion cell used in this library as it is not required since the logic cells provides input completeness feature. To join or split the connections of asynchronous logic cells, the Muller C element logic cell is used. In this work, only X1 strength of logic cells are available.

4.5 Schematics and layout

The schematics of improved library cells are listed below. The schematic figures 4.2, 4.5, 4.11, 4.8, 4.14 consists of transistor sizes which were determined via the method of logical effort. The sizing of transistors are mentioned next to them. Furthermore, the type of transistor used at each stage in transistor network was specified using different colors. The regular transistors are unchanged and show typical symbol of transistors in black color. The HVT transistors are mentioned in green color for reducing the leakage and overall power consumption of logic cells. The red color in transistor specify the LVT transistors to further speed up the outputs for faster operation. The sizing of standard NAND and inverter operations performed in logic cell are highlighted with color for HVT based transistor operations and sizing according to logical effort. Finally, the table in each schematic figure show the ports list logic cell which includes inputs, outputs, and power nets. The library layouts are listed in Appendix A section.



Ports list	
Inputs	A B
Outputs	Z Z'
Power	VDD GND

Fig. 4.1 Weak-feedback Muller C element schematic

4.6 2-input logic cells

The difference among these logic cells are the number of inputs while the number of outputs remains the same. Figures 4.5, 4.8 QDI SAHB NAND/AND/XNOR/XOR cell is 2-input cell where AF, AT, BF, and BT are the standard inputs with complementary signals NAF, NAT, NBF, and NBT. Furthermore, the handshaking control signals remains the same throughout the library design. The RACK and its complementary NRACK signals are the inputs and LACK with complementary NLACK signals are the output.

The design flow start constructing the cell design of NAND/AND/XNOR/XOR gate with original as it is porting using 40nm CMOS technology. The as it as implementation impose higher propagation delay and power consumption in this case. One of the distinctive features of the proposed design flow is Logical Effort which assign efficient sizing and balancing of transistors. To understand how the sizing and balancing is per-

formed, the cell design is virtually broken down into different section according to the input nodes. The logical effort for each section is calculated using the input nodes for critical and non-critical paths. Let's take an example of critical path where the output of the dual-rail is latched and amplified through the sense amplifier half buffer sub-module. Using the equations of LE from Chapter 2, the approximate delay value of the complete cell circuit is calculated by multiplying it with the electrical effort which is the output capacitance over input capacitance.

The resulting approximate delay is without parasitic capacitance delay at first stage. In case of improvement in propagation delay is required, the process is iterated to achieve desired and best-case value. Upon satisfactory result of achieving effort delay (f), the parasitic delay and added for actual approximate delay value and further computed with tau factor for absolute delay. At this point, the best possible sizing of transistors is assigned in the logic cell. This show how worse the NAND/AND/XNOR/XOR logic cell is performing against the reference inverter.

The logic cell may still lack performance in power consumption due to upsizing of transistors. The MVT technique utilizes different flavors of transistors provide by the process kit. If process kit provide access to LVT and HVT transistors, which are required by the proposed design flow in improving the power consumption under delay constraint and vice versa.

The process of MVT starts at the outputs of the NAND/AND/XNOR/XOR logic cell. The propagation delay under constraint using the transient simulation watches the performance while replacing transistors. The important thing to note here is that the logic cell is segregated in to two parts with critical and non-critical path circuits. The non-critical path circuits can utilize the benefits of the HVT transistors since those are efficient in controlling the leakage. In QDI SAHB, it was identified through simulations that most of the leakage power consumption was observed at the evaluation block. The first replacement is of regular transistor is performed in evaluation block for the transistor connecting the subthreshold voltage supply to the rest of the circuit. This transistor acts as sleep transistor in the circuit while contributing to the 4-phase handshaking protocol cycle, which makes it best candidate for HVT transistor replacement.

In critical path, where the handshaking output signal is the most critical for activating next component in circuit is replaced with LVT transistors. This critical path is scattered around the circuit since the handshaking output signals is generated from the data signals. This implies that the number of LVT transistors will be more than the HVT transistors in the circuit. The replacement can be started in sense amplifier

block by replacing transistors in critical path whose gate connections are either data or handshaking input signals.

This process does not include modifying the sizing of the transistors which could lead into misbalancing the transistor network. The PMOS transistors in the pull-up network of sense amplifier are replaced with LVT. Since the similar function is performed in pull-down network of evaluation block, the corresponding transistors should also be replaced with PMOS LVT flavors. This is important since, the function is generated and latched to output using the pull-up network of the sense amplifier and pull-down network of evaluation block.

Furthermore, for the handshaking output control signals of LACK and NLACK which are equally critical for operations, both PMOS and NMOS transistors from the cross coupled latch to the complementary NLACK signal are replaced with the LVT transistor flavor.

When these techniques are followed through the proposed design flow provides the best balancing of the forward propagation and backward propagation delays contributing to improvement in overall speed performance. Furthermore, the LVT and HVT controlling the current flow according to the handshake sequence provides lowest possible average power consumption substantially reducing the leakage power. The layouts of QDI SAHB BUFF/NAND/XNOR logic cells are shown in figures A.2, A.3, A.5, respectively. Alternatively, the propagation delay and power consumption for buffer cell are shown in figures 4.3, 4.4. Figures 4.6, 4.7 shows the propagation delay and power consumption of NAND cell. Similarly, the figures 4.9, 4.10 shows the propagation delay and power consumption of XNOR cell.

This process of sizing/balancing transistors via LE and improving the speed while controlling current via MVT technique can be used iteratively to satisfy the required performance parameters.

4.7 3-input logic cells

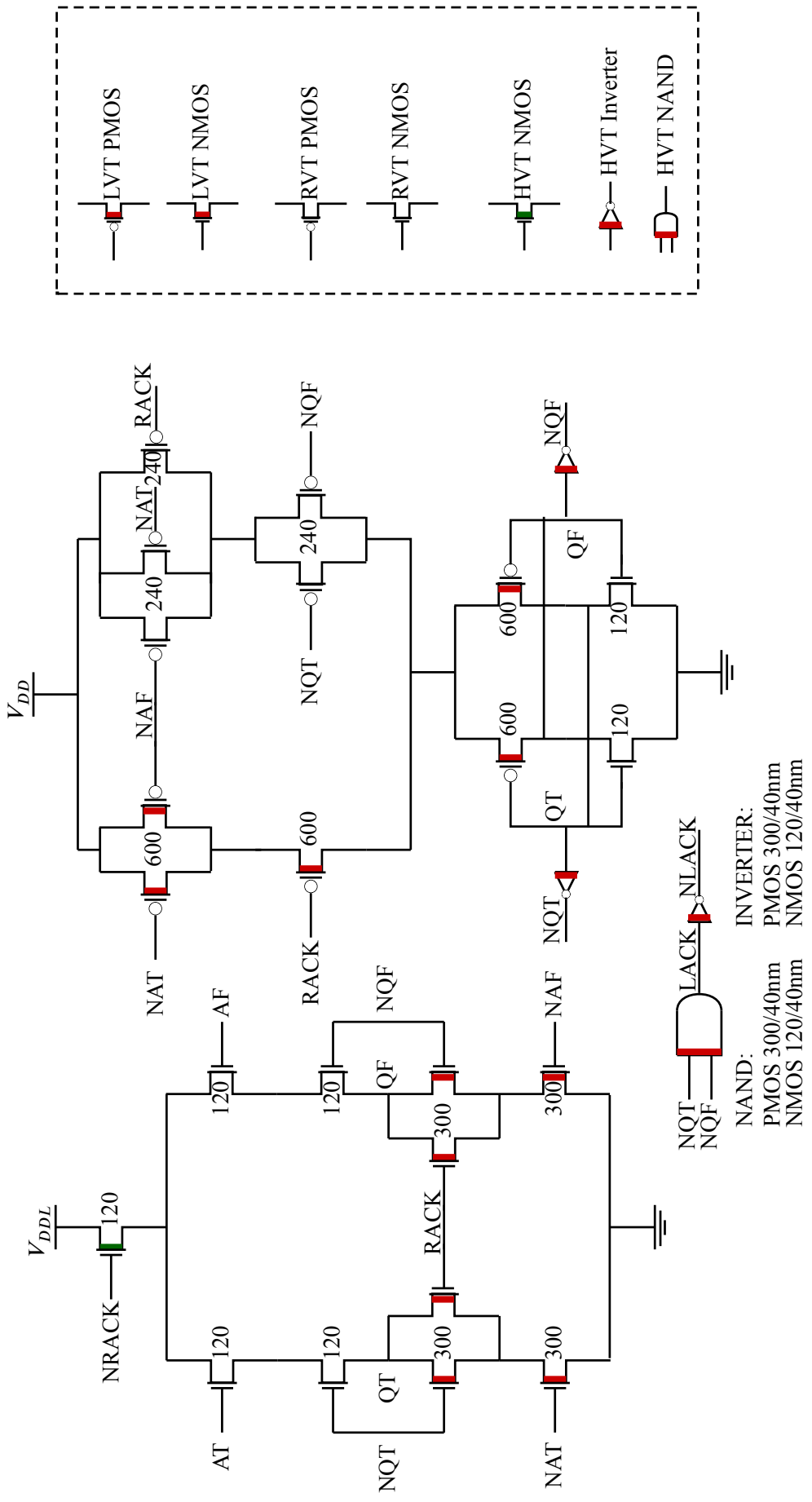
Advancing in the logic cell library contents, there are two logic cells which present 3-inputs as per required Boolean functions. Figure 4.11 AOI/AO logic cell is a straight forward 3-input And Or Invert cell, where the inputs A and B are inputs to function AND while its result and input C together are the inputs of to function OR. Furthermore, in figure 4.14 show 2-input IMUX/MUX cell which is technically a 3-input XNOR/XOR cell where inputs A and B are data inputs while input C is select signal. There is slight

difference between the XNOR/XOR function and IMUX/MUX in the pull-down network and base transistor base connections in the pull-up network of evaluation block due to similarity in Boolean function.

The efficient implementation of these two cells through the proposed design flow is only different due to the increased number of inputs. In which case a slightly more calculation of LE is performed for absolute delay of the logic cell and more transistors are replaced with different flavors while the rest of the process remains same.

The propagation delay and power consumption for these cells are shown in figures 4.12, 4.13 and figures 4.15, 4.16 for XNOR and IMUX cells, respectively.

The library cell layouts are presented in Appendix A, while performance parameter of these library cells is presented in Chapter 5.



Ports list	
Inputs	AF AT NAF NAT NRACK RACK
Outputs	LACK NLACK NQF NQT QF QT
Power	VDD VDDL GND

Fig. 4.2 Improved SAHB inverter/buffer logic cell schematic

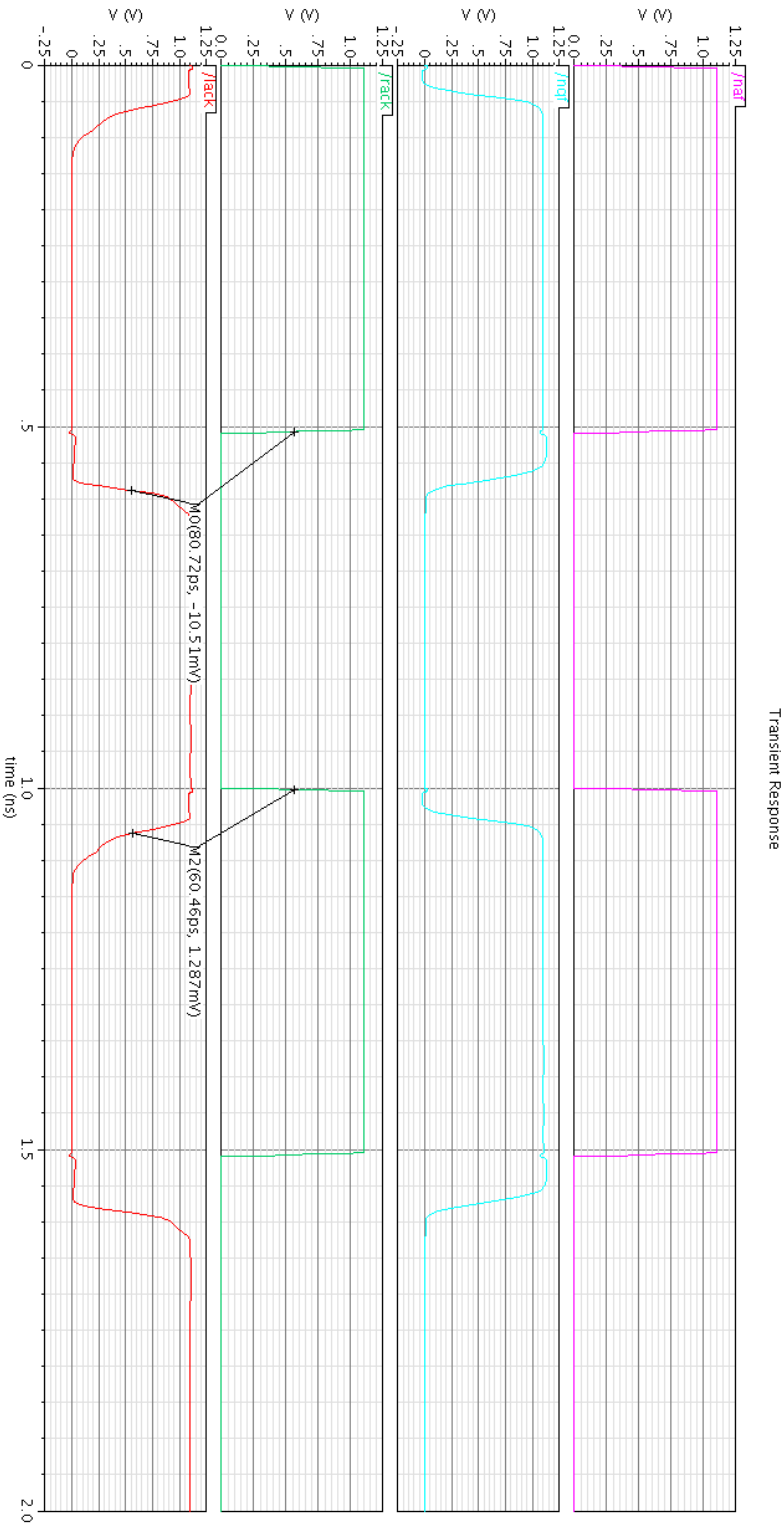


Fig. 4.3 Propagation delay of improved SAHB buffer logic cell

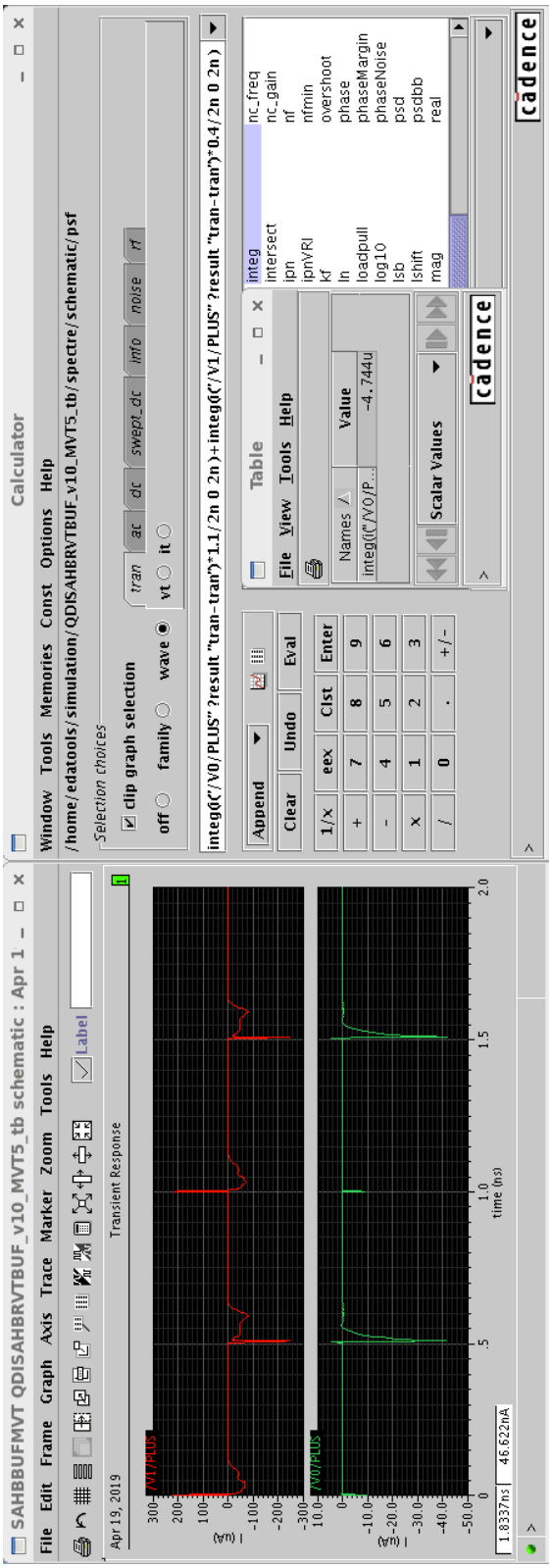
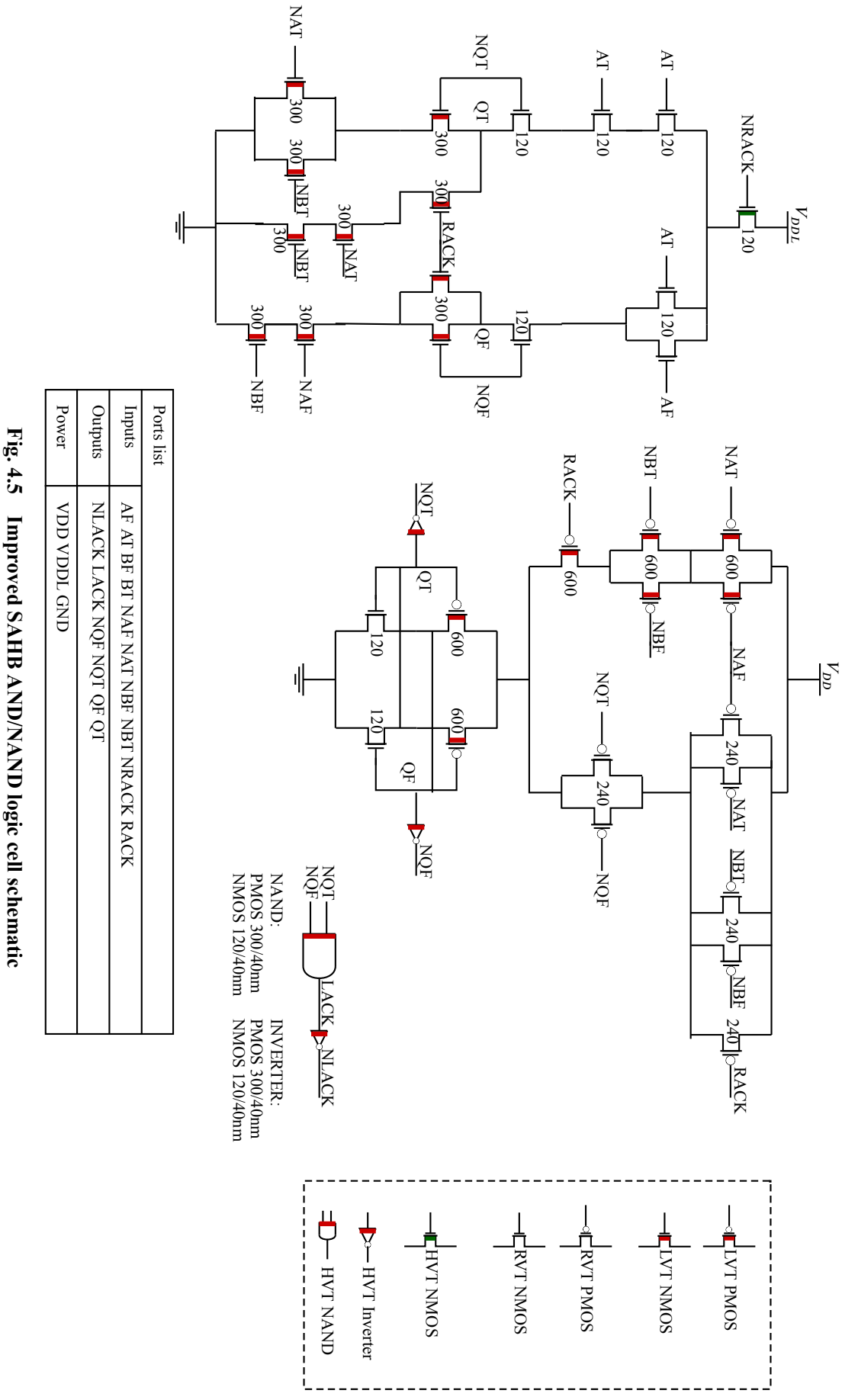


Fig. 4.4 Power consumption of improved SAHB buffer logic cell



Ports list	
Inputs	AF AT BF BT NAF NAT NBF NBT NRACK RACK
Outputs	NLACK LACK NQF NQT QF QT
Power	VDD VDDL GND

Fig. 4.5 Improved SAHB AND/NAND logic cell schematic

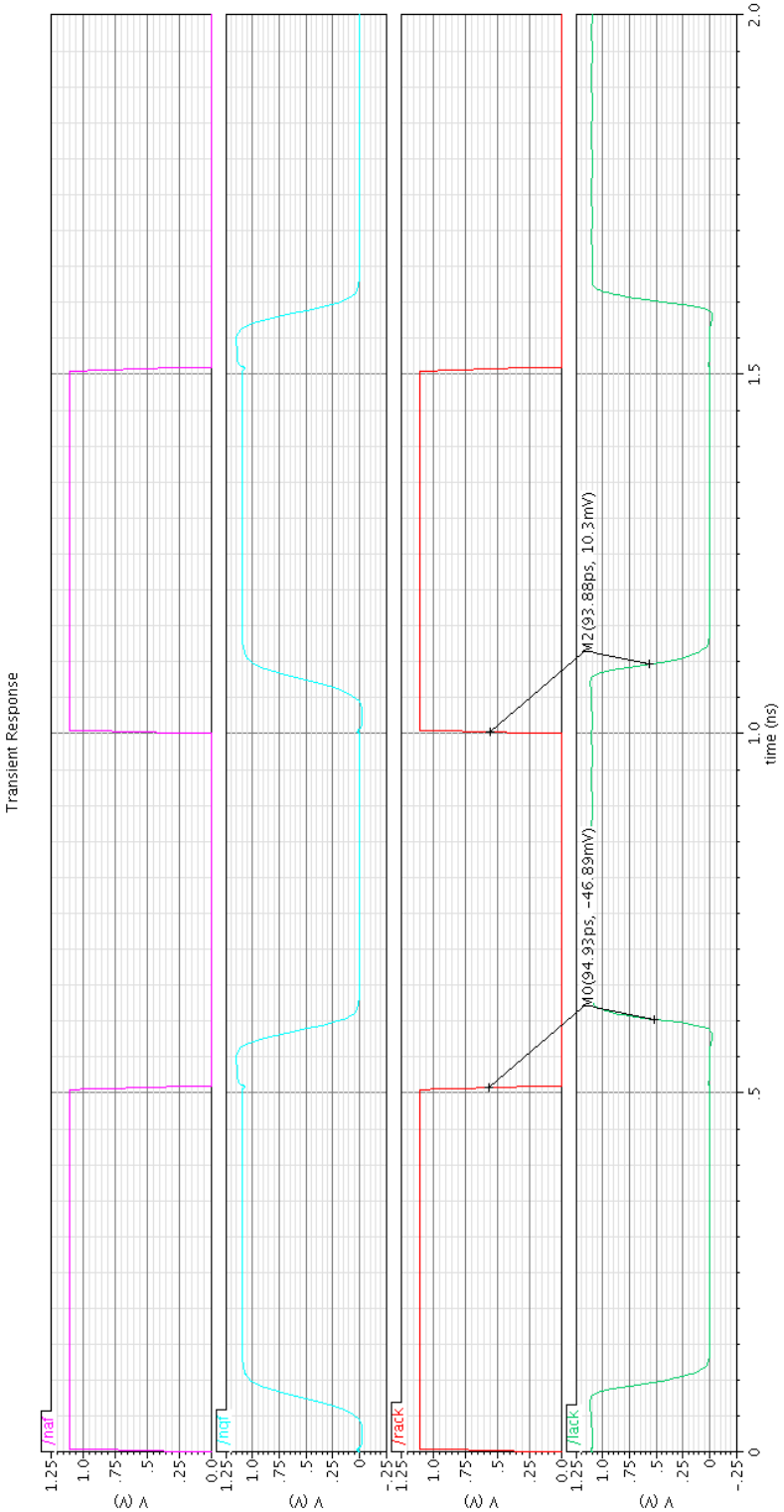


Fig. 4.6 Propagation delay of Improved SAHB AND/NAND logic cell

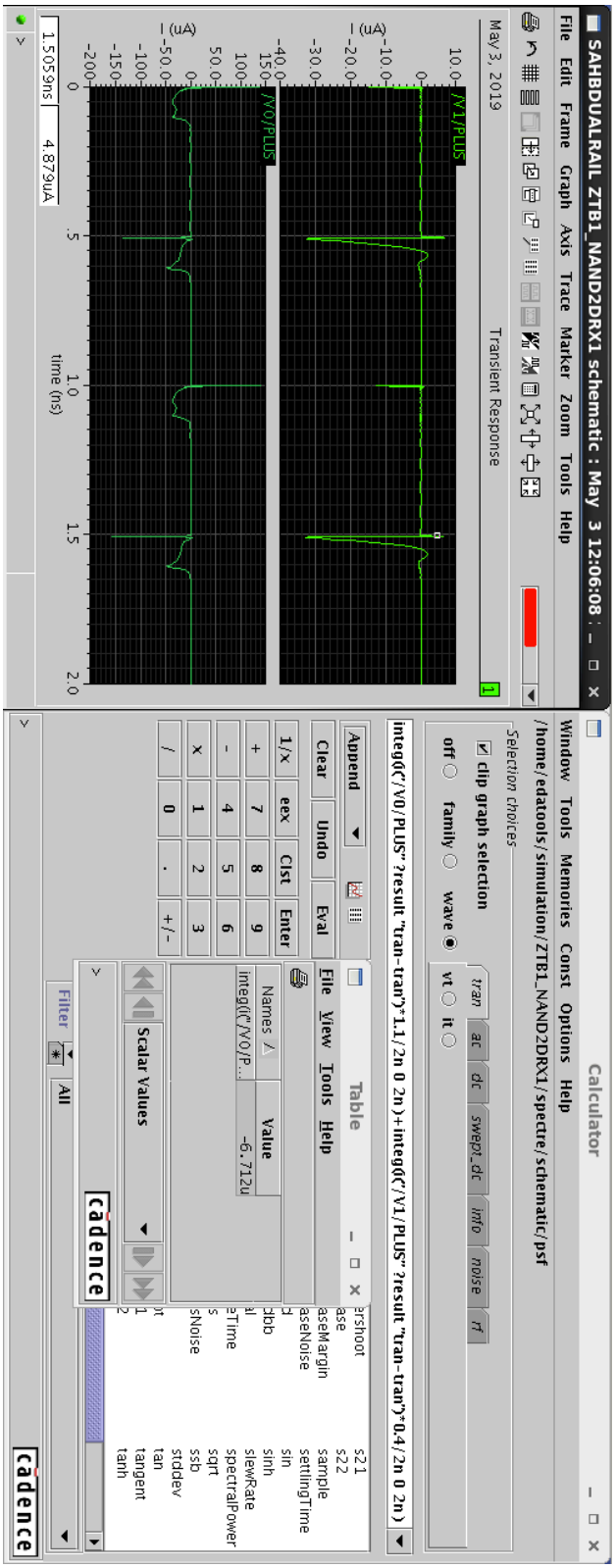


Fig. 4.7 Power consumption of Improved SAHB AND/NAND logic cell

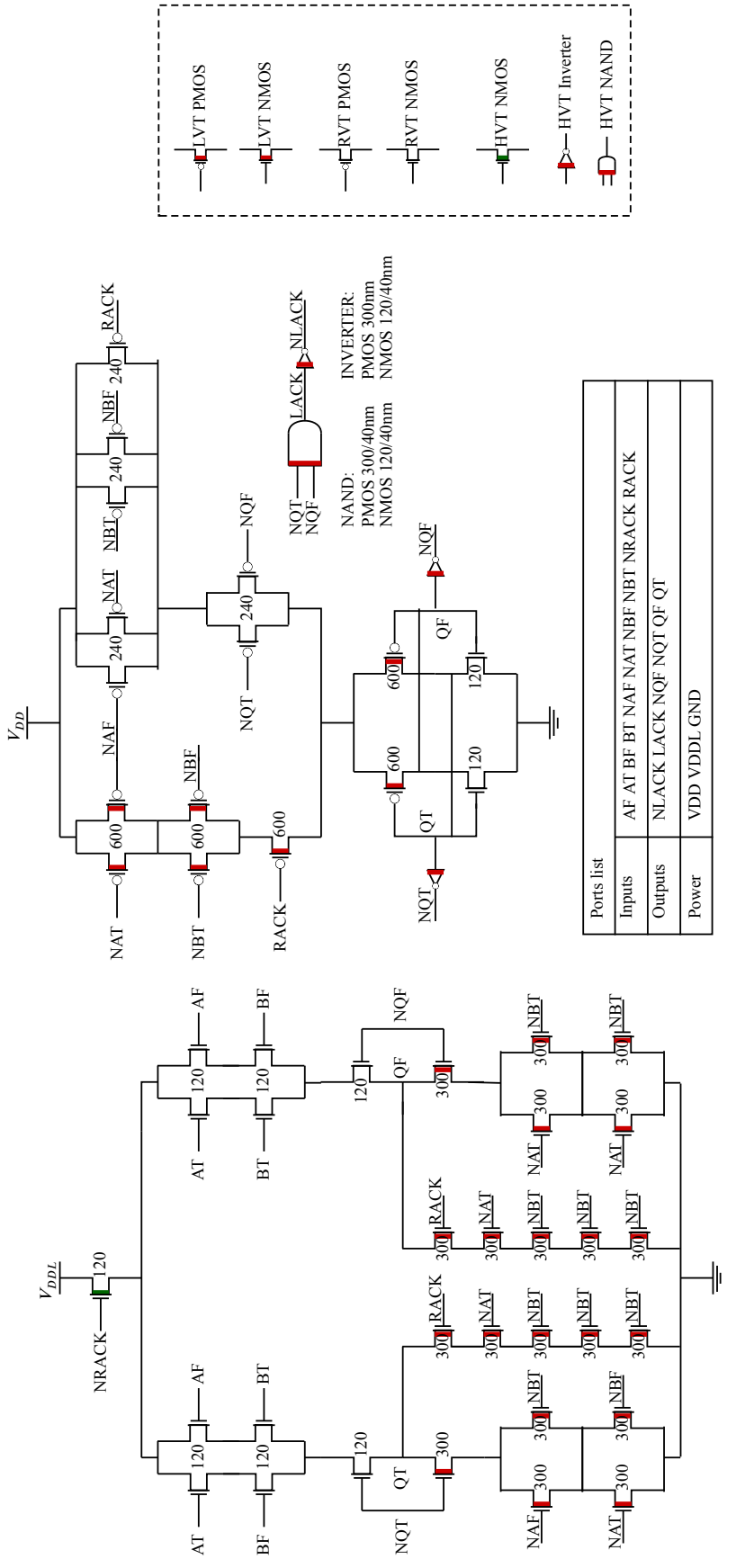


Fig. 4.8 Improved SAHB NOR/XNOR logic cell schematic

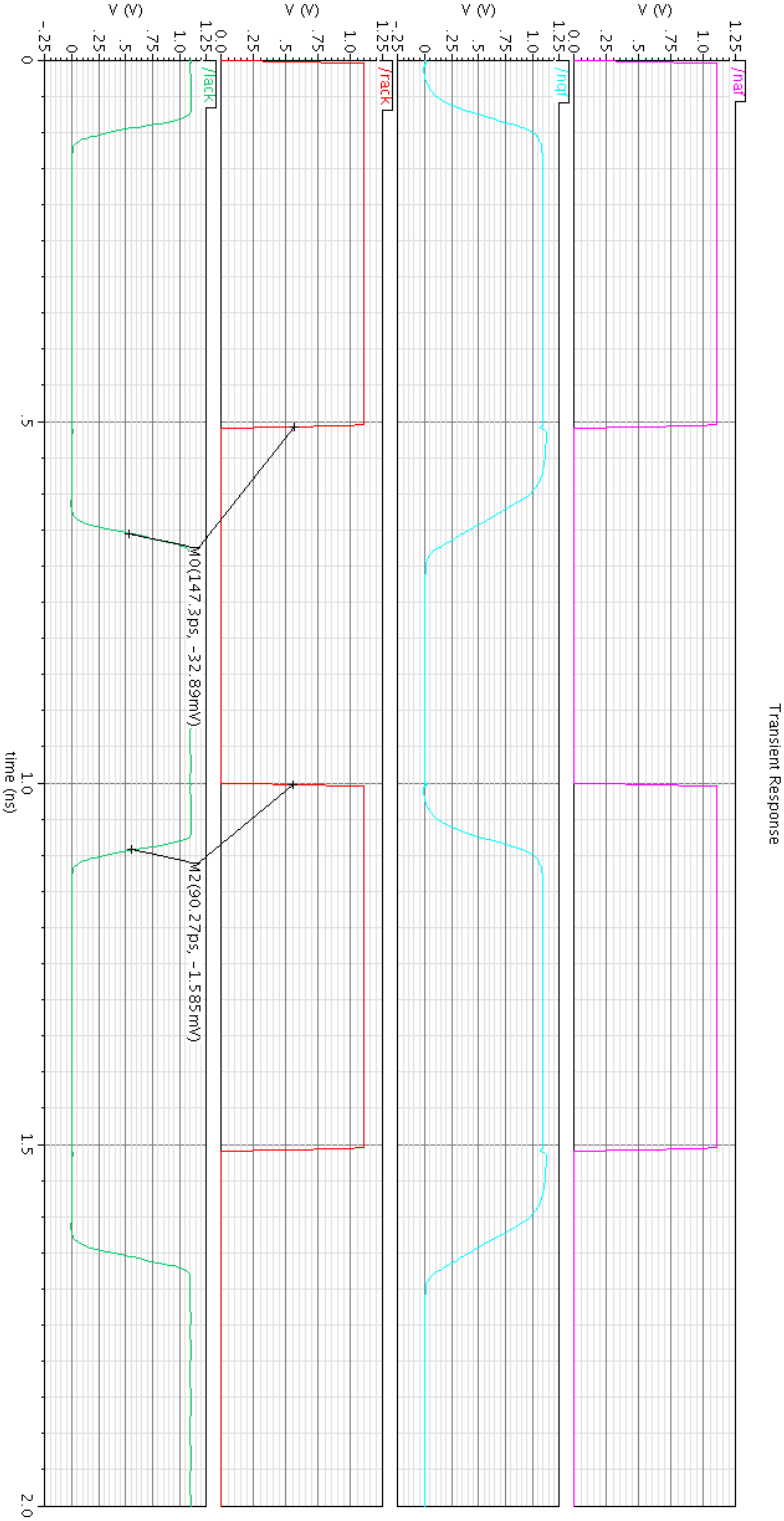


Fig. 4.9 Propagation delay of Improved SAHB XOR/XNOR logic cell

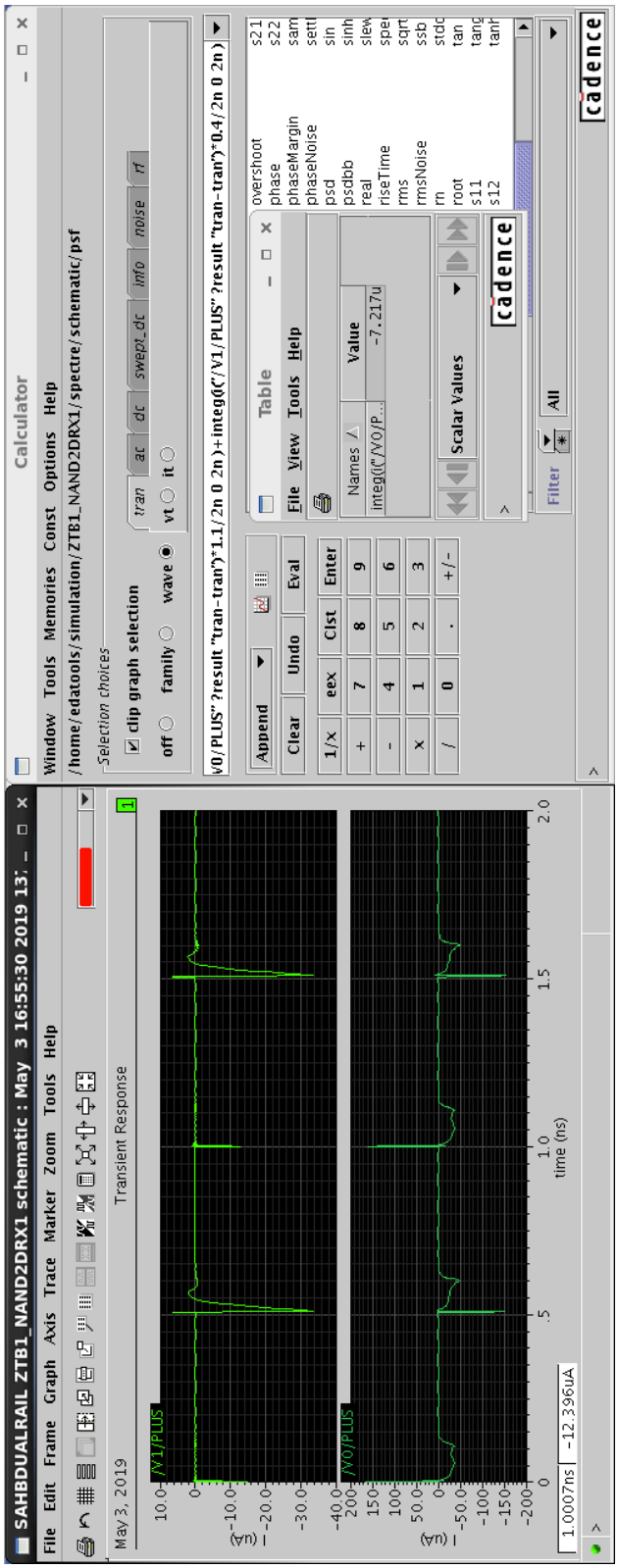


Fig. 4.10 Power consumption of Improved SAHB XOR/XNOR logic cell

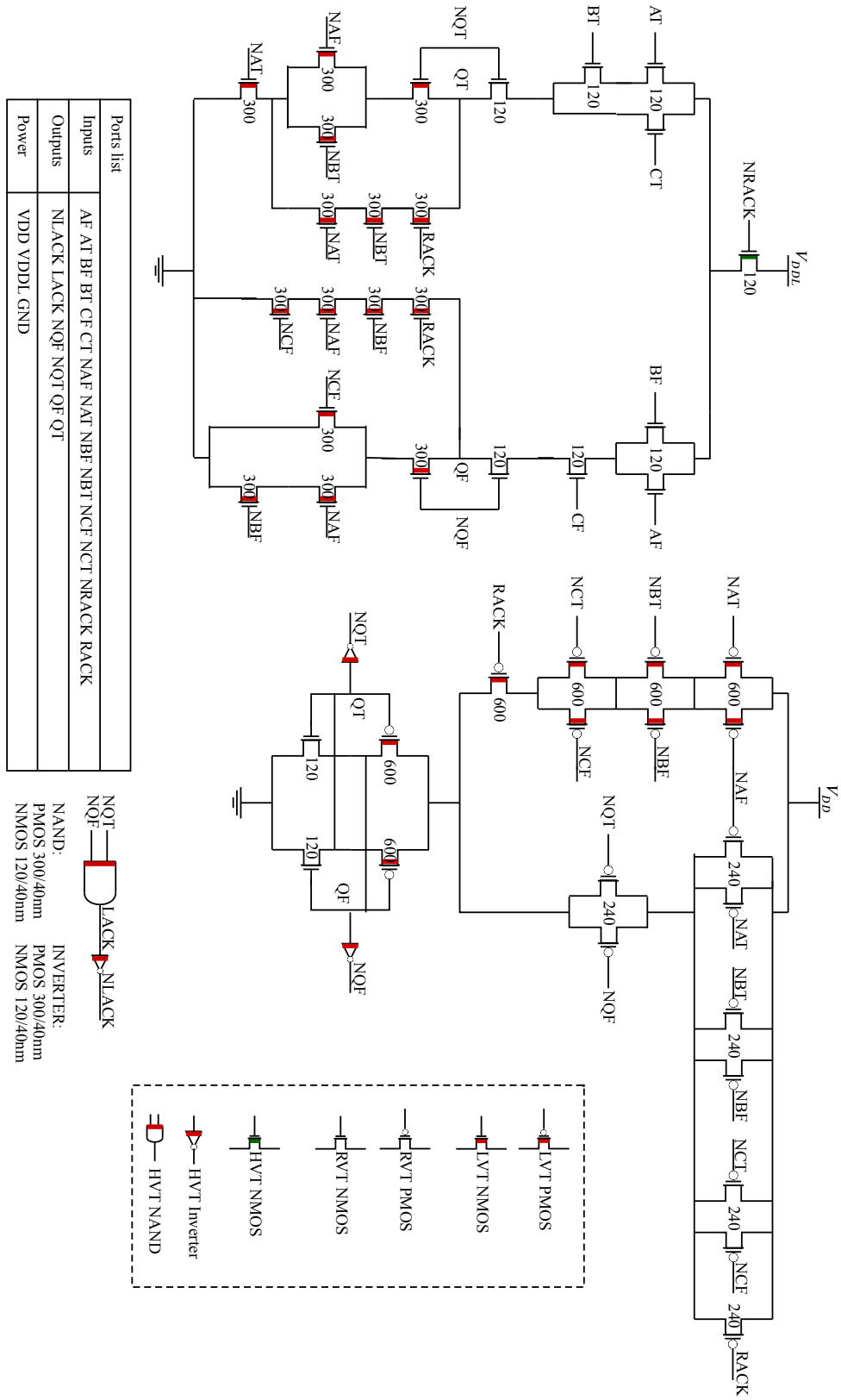


Fig. 4.11 Improved SAHB AO/AOI logic cell schematic

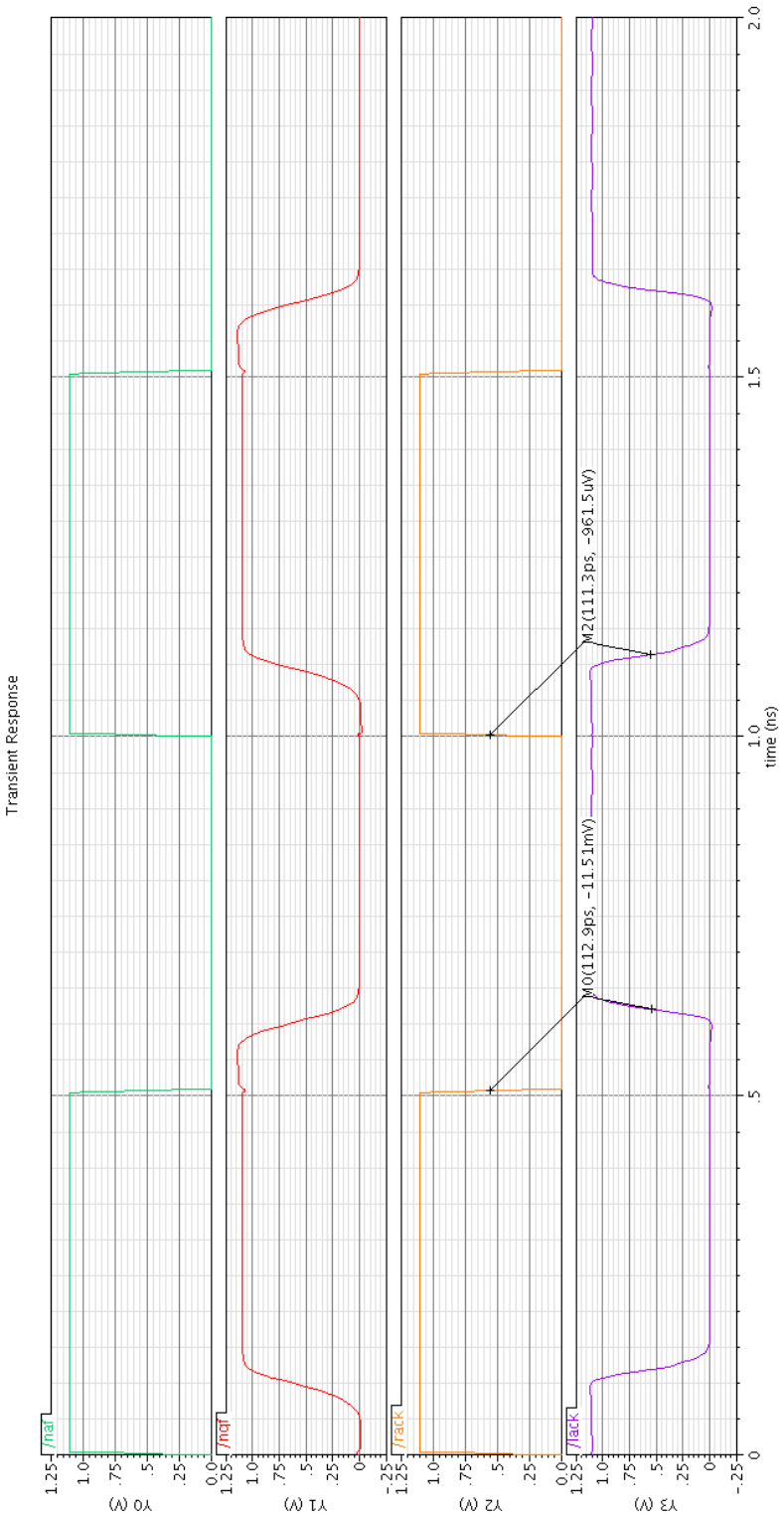


Fig. 4.12 Propagation delay of Improved SAHB AO/AOI logic cell

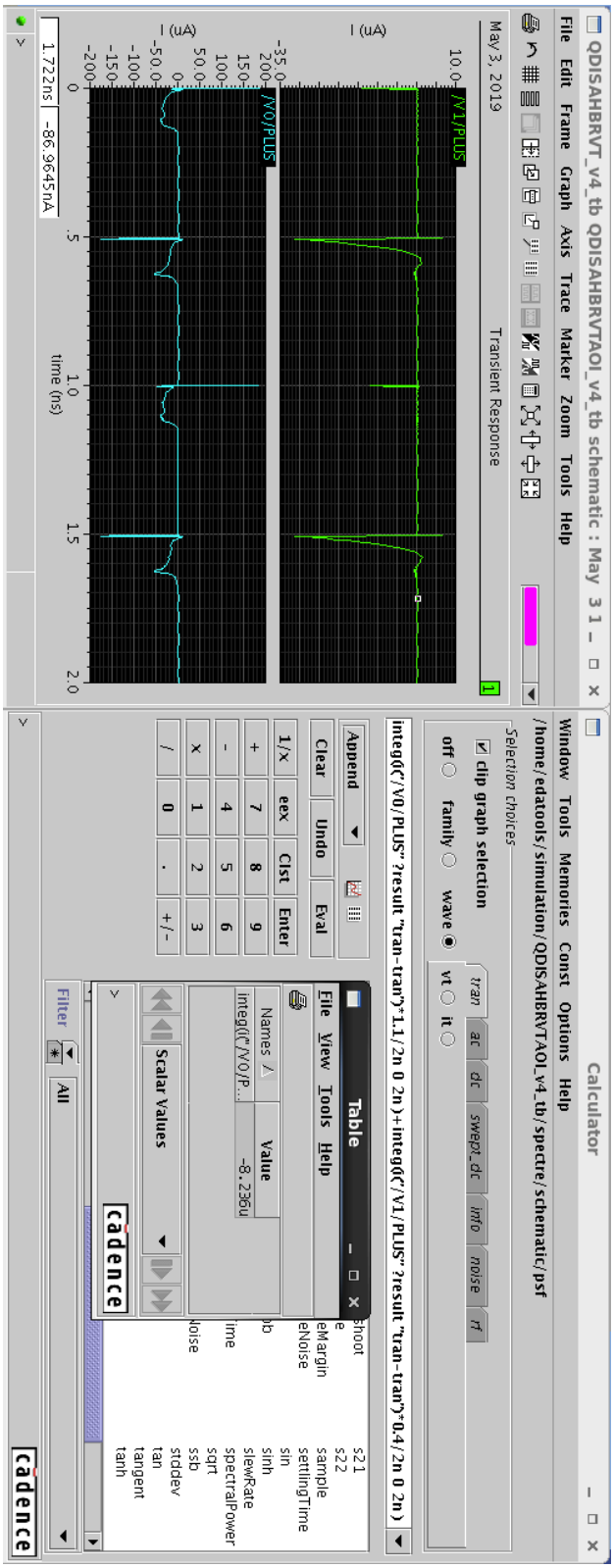


Fig. 4.13 Power consumption of Improved SAHB AO/AOI logic cell

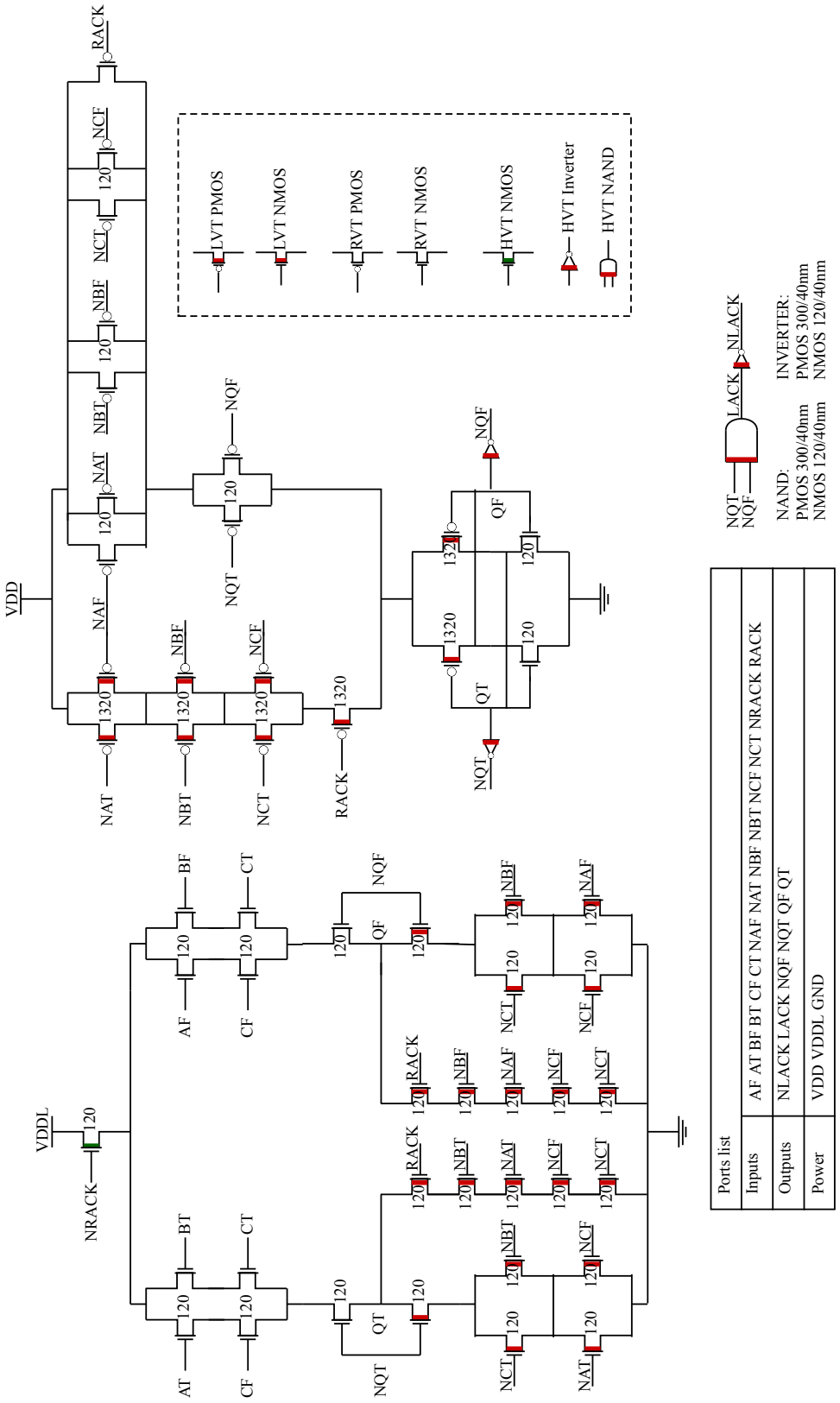


Fig. 4.14 Improved SAHB MUX/IMUX logic cell schematic

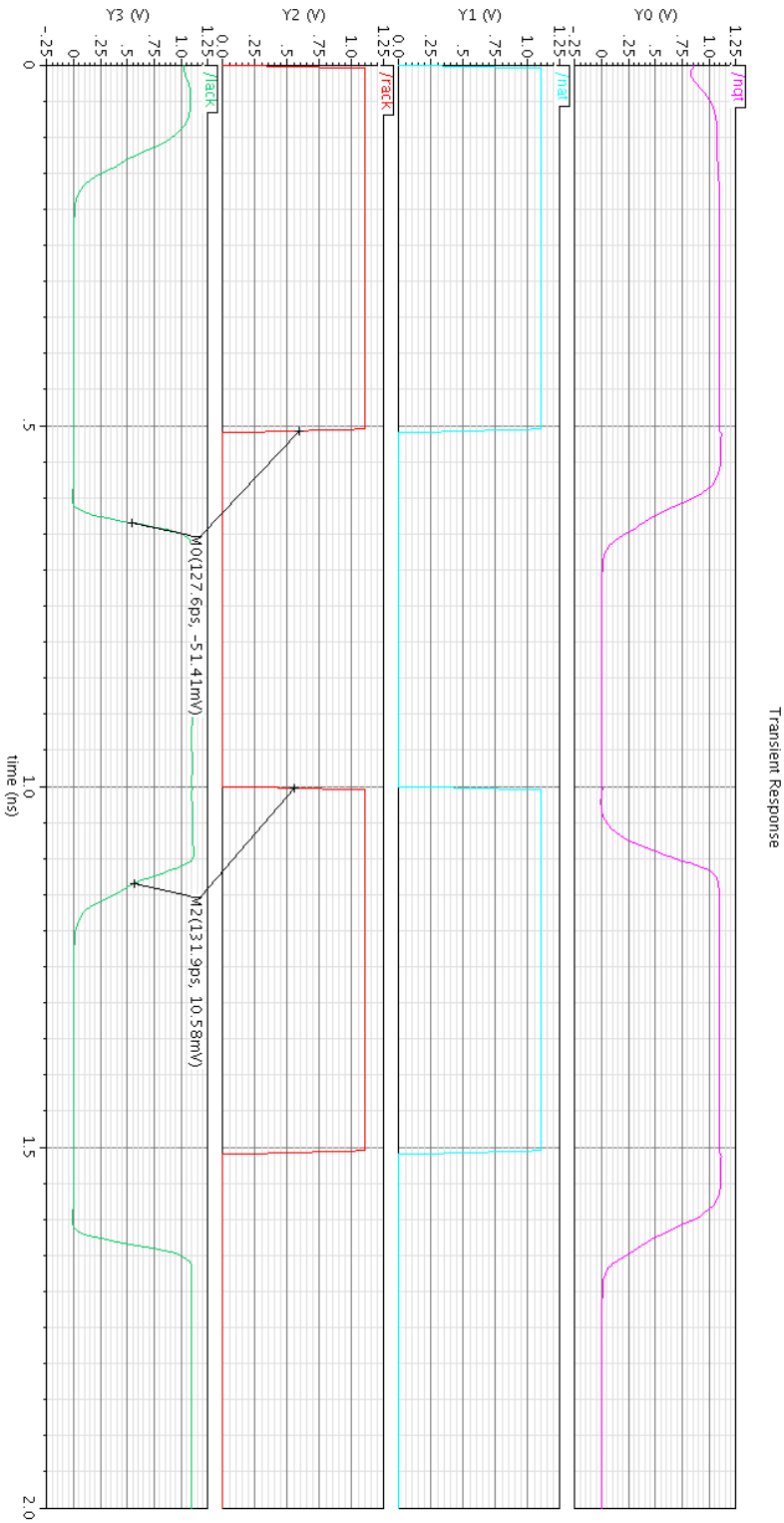


Fig. 4.15 Propagation delay of Improved SAHB MUX/IMUX logic cell

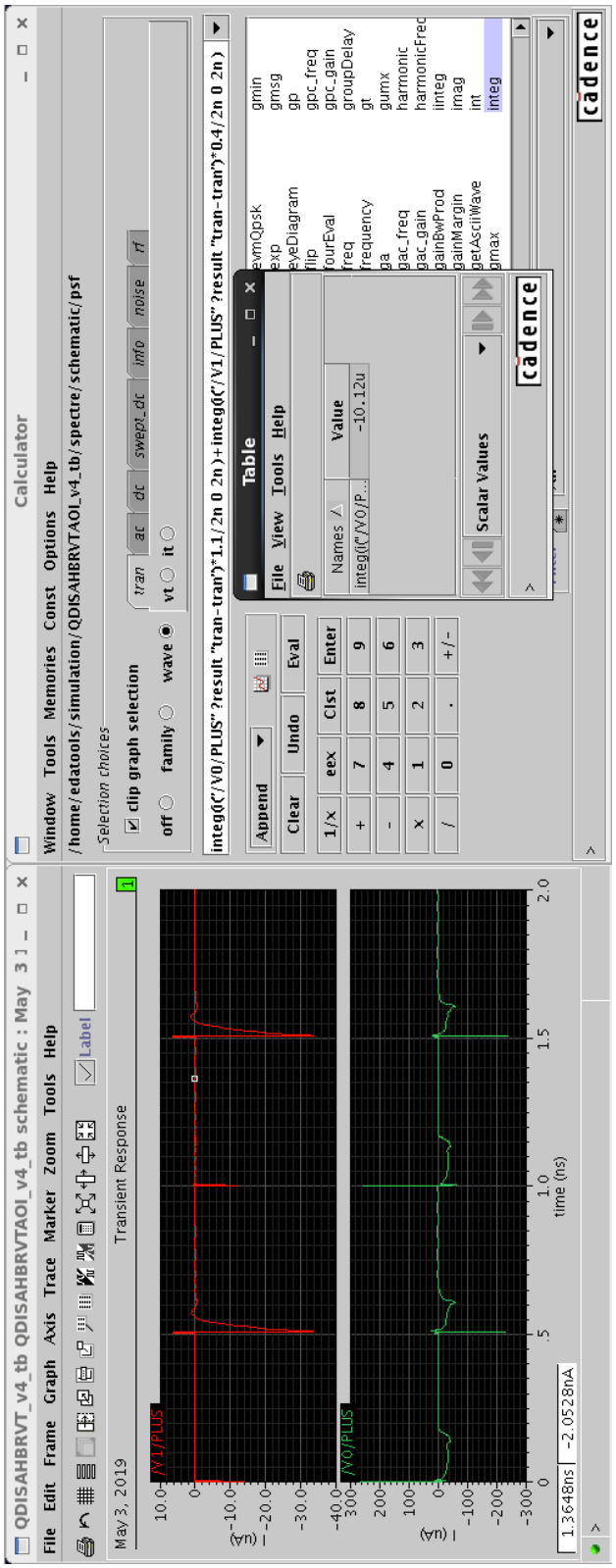


Fig. 4.16 Power consumption of Improved SAHB MUX/IMUX logic cell

Chapter 5 Simulation setup and results

This chapter explains the simulations used for verifying the functionality before and after layout design. Simulations are performed for each logic cells using designed circuit by sampling 1 GHz of frequency at 1.1 V nominal and 400mV subthreshold voltage with variant temperatures. The simulation figures for all the remaining logic cells are presented in previous chapter. This chapter present the simulation setup and results of improved QDI SAHB buffer logic cell.

5.1 Simuation setup

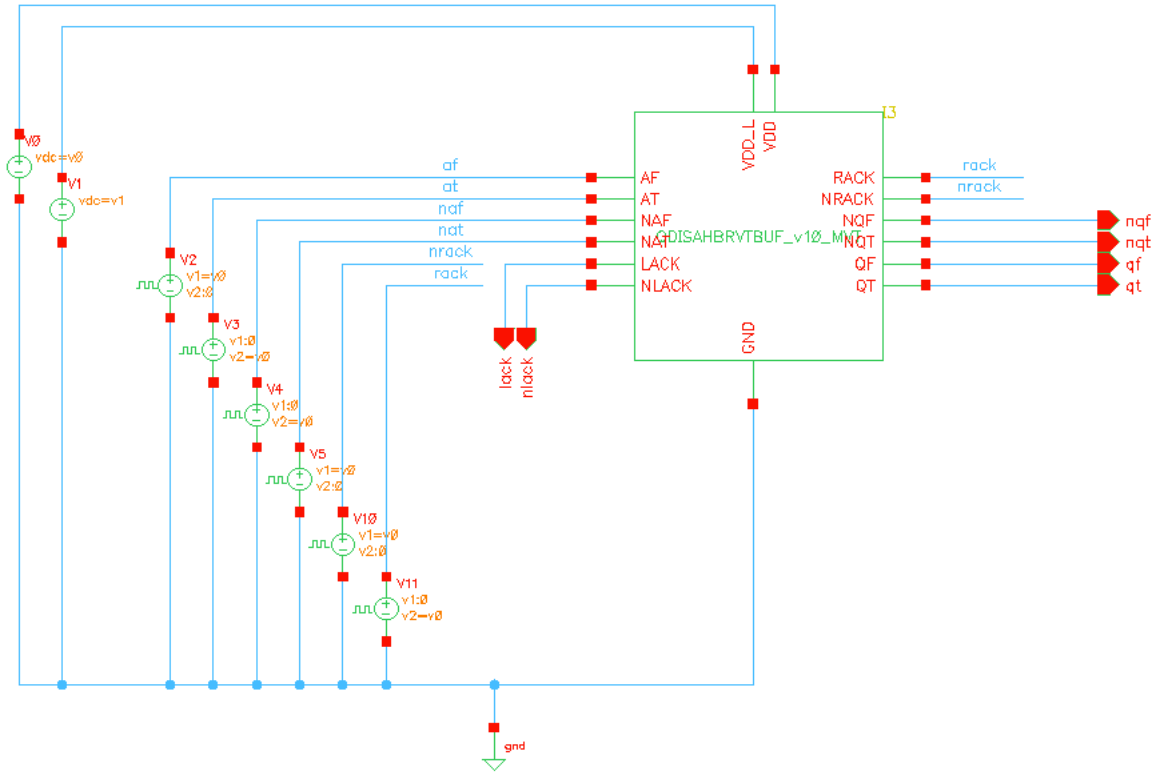


Fig. 5.1 Test bench of SAHB buffer logic cell

To perform simulation of logic cells in library a test bench was created using Cadence Virtuoso for each logic cell due to variant number of input/output signals. The logic cell is connected to nominal and subthreshold voltage sources of 1.1V and 400mV respectively. The input signals are connected to the pulse generators with variables for voltage, period and pulse width. This work samples at 1GHz frequency, therefore the pulse width is set to 500ps and period is set to 1ns. Furthermore, the outputs of the logic cell are connected to the outputs of schematic. Test bench circuit for the SAHB buffer

cell is shown in Figure 5.1.

Cadence Analog Design Environment (ADE) is used to simulate the logic cell with Spectre model files. Transient simulation is performed with 2 nanoseconds of stop time. As shown in Figure 5.2 the PLUS terminal of nominal (V0) and subthreshold (V1) voltages are probed along with RACK, LACK, NAF, and NQF for verification. The PLUS terminals of the voltage supplies are used to calculate power. The handshaking signals (RACK, LACK) and data signals (NAF, NQF) are probed for functional verification. The rest of the signals are omitted for simplicity and can be consulted in previous chapter. Temperature values are manually changed from *System -> Temeprature* menu option for -40c, 0c, 27c and 100c temperatures. Furthermore, the variables are copied from schematic using *Variables -> Copy from cellview* menu option in Cadence ADE window. Variables for the supply voltages and frequency sampling are set using the *Design Variables* section in Cadence ADE window.

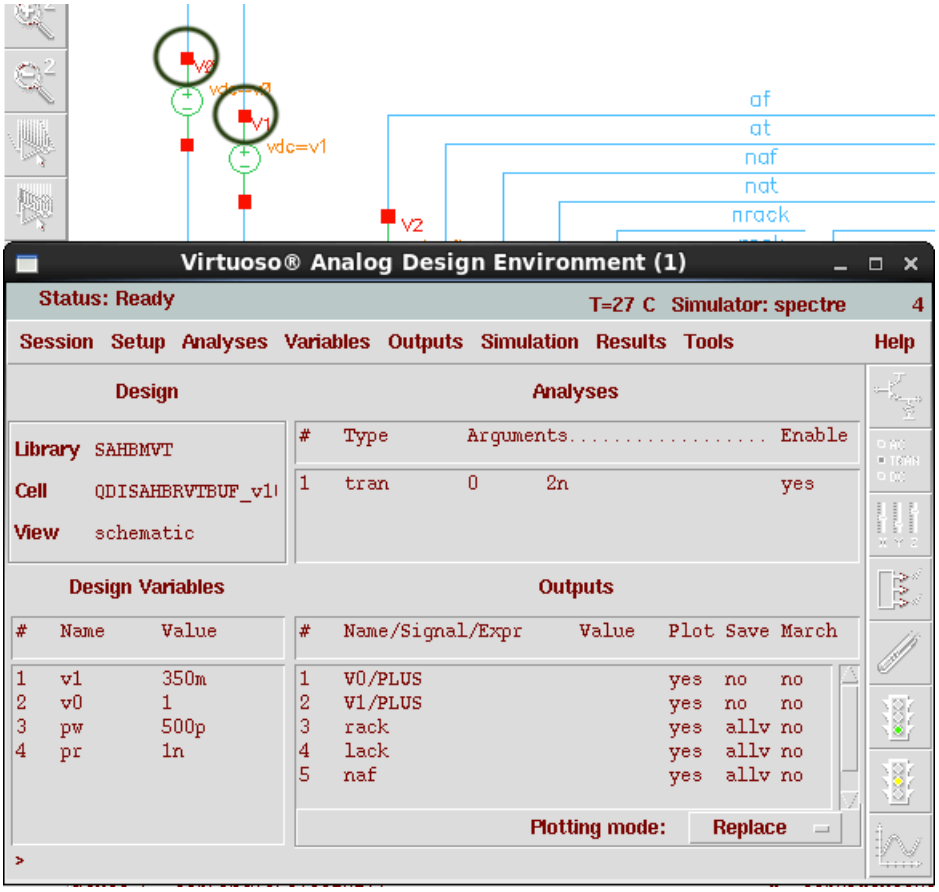


Fig. 5.2 Simulation setup of SAHB buffer logic cell

5.2 Results

Functional simulation is the first level of verification of logic cells. This simulation does not include the parasitics and hence are ideal. While performing the simulation on base design the resulting logic cell did not perform correct under temperatures of -40c and 100c. This shows that the development of logic cell library requires balancing and improvements to achieve better performance.

The improvement using techniques in the logic cell development leads to accurate and faster operations. The post-layout simulation for propagation delay are shown in Figures 5.4, 5.5, 5.6, and 5.7 for different temperature values. Furthermore, the power consumption with post-layout simulation are shown in Figures 5.8, 5.9, 5.10, and 5.11.

To verify the functionality of improved SAHB buffer cell, test bench was created for the cell. Transient simulation was performed for 2 nanoseconds with supply voltages and data/control inputs as variables. Since the nominal supply voltage provided was 1.1V, the inputs voltage level corresponds to the similar voltage levels. The subthreshold voltage levels are only provided to a sub-block of the cell known as evaluation block.

Verification of function is performed at several levels. The transient simulation plots the waveform with all the input and output signals. The important point to note here is that the waveform must adhere to 4-phase handshaking protocol. In case of QDI SAHB cells, a complete cycle would take approximately same time duration as the frequency period. In work the frequency applied is 1GHz, which implies that a complete cycle must complete in approximately 1ns. Moreover, QDI SAHB use 4-phase handshaking protocol which is also known as Return-to-Zero (RTZ). The cell waveform must provide an empty token as well as valid token. The token status is directly controlled by the handshaking control signals provided as input to the cell.

The input completeness implies that the resulting signals will not be amplified and remains empty even if the input handshaking control signals is set to valid. This guarantee that for each QDI 4-phase protocol dual-rail encoding cycle, all input data signals must change before evaluated for output amplifications. It can be observed from the propagation delay figures 5.4, 5.5, 5.7, 5.6 below that for each stage the input data signals switch between high and low voltage supplies to satisfy asynchronous circuit requirements.

The input handshaking control signals provided to the cell are named RACK and NRACK. To verify the handshaking control signal operation, the waveform must carefully be observed for signal transitions. When RACK is high and NRACK is low, the

token is empty and the data on output lines are not valid. In such a case the resulting LACK and NLACK signals highlight this information. In simulation waveform figures of improved buffer cell below, the complemented and some data signals are truncated for ease of concept. The figures of propagation delay show the transitions of handshaking control output signal LACK based on the handshaking control input signal RACK. Once the data signals are all available, the LACK signal will set high indicating data invalidity. In second half signal when RACK signal is low, the inputs are computed and amplified toward the output while setting LACK to low. Once the LACK is low the data on output is considered valid and ready for the next component to pick up.

Finally, the functional verification includes a set of input structure and an appropriate response on outputs. The functional and post-layout simulations of the buffer cell must adhere to data empty token on output signals when the input handshaking control signal is set to high and data valid token on output signals when the input handshaking control signal is set to low. The complete cycle must perform accurately in the constrained time duration of the sampling frequency with additional cell delay and parasitic delay. The similar waveform is used to compute the propagation delay of the cell.

The propagation delay of the cell is computed from the waveform in Cadence ADE tool by running transient simulation for 2 nanoseconds. Usually the propagation delay is the average sum of the forward and backward delay at 50% of the voltage levels, however in case of QDI SAHB it is slightly different. To calculate the propagation delay which completes one full cycle of empty and valid tokens, the difference in the transitions of voltage levels at 50% for empty token is multiplied by 2. Similarly, the difference between the voltage transitions at 50% for the valid token is multiplied by 2. These both values are summed up to extract the propagation delay of a QDI SAHB cell which operates at 4-phase protocol and dual-rail encoding scheme.

To evaluate performance under temperature variations, the waveforms show output behaviors at different temperature levels. The temperature levels are -40c, 0c, 27c, and 100c. For an asynchronous QDI SAHB circuit to pass the temperature tests, it must perform correct in different environment temperatures. According to the figures of simulation waveforms, there is a slight difference in propagation delays, but the operational correctness remains valid. The implementations before improvement of the QDI SAHB cell showed poor performance in extreme temperatures.

The second most important performance factor in circuits is the power consumption. It is important for the designed cell to consume as little power as possible. The MVT technique used in the cell design assist in reducing the power consumption of the

cell which mainly target the static power consumption or sometimes known as leakage power. Since, leakage power consumption is a growing concern in nanometer designs, it is equally important for evolution of low-power circuit techniques.

The figures 5.8, 5.9, 5.11, 5.10 below show the power consumption of buffer cell at different voltage environments. Similar to the propagation delay case, the power consumption of the cell is computed for -40c, 0c, 27c, and 100c.

Power consumption is performed in Cadence ADE tool using transient simulation for 2 nanoseconds. The voltage supplied are probed at the positive terminals for resistance calculations. Upon running the transient simulation, the calculator from plot windows is used for entering power consumption calculation. This calculation is performed using the equation specified in chapter 3. In calculator window the “integ” type for data is selected and “wave” is selected from “selection choices” section. This brings the waveform to front with option to select a signal. First, the v0 is selected which is the nominal voltage supplied to cell using the testbench circuit. The automatically equation is further modified by adding the voltage value of 1.1 by 2ns time duration. Furthermore, the start and end time is set as 0 and 2n, respectively. Upon clicking “Eval” in the keypad section of calculator window, the equation is evaluated and presented in the text box. Similar process is repeated for the subthreshold voltage by selecting v1 with 0.4mV value and 2n time duration. Upon evaluation, the equation is overwritten in the text box. The plus sign in used in keypad section to add previous equation together with new.

For any QDI SAHB logic cell the power consumption, this equation calculates the average static and dynamic power consumption of the cell in a specific time duration. In this work only 2 nanosecond time duration is calculated which results in complete 2 cycles of QDI handshaking operations. The power consumption is performed for all variant temperatures and shown in figures at the end of this chapter.

The table 5.2 show improved SAHB logic cell library with performance parameters of power consumption, propagation delay, PDP, and EDP. The resulting performance values are due to the proposed design flow in sizing/balancing and utilizing different flavors of transistors. These performance parameters listed in tables are only for idea case of temperature value 27c, while other temperature values of -40c, 0c, and 100c can be found in the figures at the end of this chapter. The power consumption is calculated for each logic cell, first the power consumption for 2ns is calculated for each voltage supply node; nominal and subthreshold supply voltage. The power consumption of each supply node is summed up to obtain total average power consumption.

The propagation delay is calculated by individually calculating the forward and backward propagation delay for operation of each cycle. Each delay value is multiplied by 2 and summed up to acquire total delay. This is important since the cell use 4-phase handshaking protocol and multiple transitions for each complete operation cycle. Finally, the PDP is calculated using the product of power consumption and propagation delay, while EDP is calculated using the product of power consumption with delay squared.

The performance parameters from figure 5.1 and 5.2, show improvement in power consumption and propagation delay when compared to the predecessor design implementation in [9] and PCHB based QDI logic library cells from [19]. However, the difference in design of this work and implementations of previous work are negligible where due to the availability of the process design kit used for this work suit best at nominal voltage of 1.1V. Finally, the implementations of [9,18] were performed using TSMC 65nm CMOS technology and this work was developed using SMIC 40nm CMOS technology.

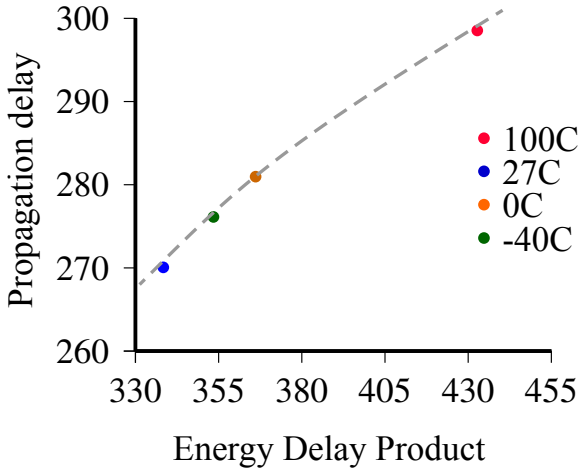


Fig. 5.3 Propagation delay vs EDP for improved SAHB buffer logic cell

The improved design of buffer logic cell perform correct under different temperatures with improvement in propagation delay and show reduced power consumption. Table 5.3 show performance of SAHB buffer logic cell by plotting propagation delay against EDP. The results are bench marked against PCHB, original SAHB logic cell at 65nm from[9], base design and improved design in Table 5.1.

Finally, the appendix section shows layouts of all the cells and previous chapter shows schematics, propagation delay and power consumption of logic cells in library. Due to increased number of input and output signals during simulation, signals are truncated and only the signals in waveform are shown which are crucial to calculation of

propagation delay. However, the ports list for each cell are mentioned in schematic design figures in previous chapter.

Table 5.1 Improved SAHB buffer logic cell comparison

Ref	**Dual-rail Buffer**	**Power (μw)**	**Delay (ps)**	**PDP (10^{-12} J)**	**EDP (10^{-21} Js)**	**Area (μm x μm)**
[18]	PCHB (65nm)	23.9	405.7	9.67	3,929	25.07
[9]	SAHB (65nm)	7.1	294	2.08	612	23
-	SAHB (40nm)	9.73	386	3.75	1,449.7	21.6
-	ISAHB (40nm)	4.74	282	1.22	377	21.6

The parameters of the library contents are summarized in Table 5.2. The table further summarize the power delay product and energy delay product of the library logic cells. The improvement is the result of using the proposed flow via techniques which trade-offs between power consumption and propagation delay to achieve the best possible point for efficient design. The proposed design flow can be used to individually control the trade-offs for high-performance or low-power applications as well.

Table 5.2 Improved SAHB logic cell library parameters

No	SAHB logic cell	Power (μw) @1.1V, 1GHz	Delay (ps) @1.1V	PDP (10^{-12} J)	EDP (10^{-21} J)
1	1-input buffer	4.7	282	1.22	377
2	2-input AND/NAND	6.7	377	2.52	952
3	2-input XOR/XNOR	7.2	475	3.42	1624
4	2-input MUX/IMUX	10.1	516	5.21	2689
5	3-input AO/AOI	8.2	448	3.67	1645

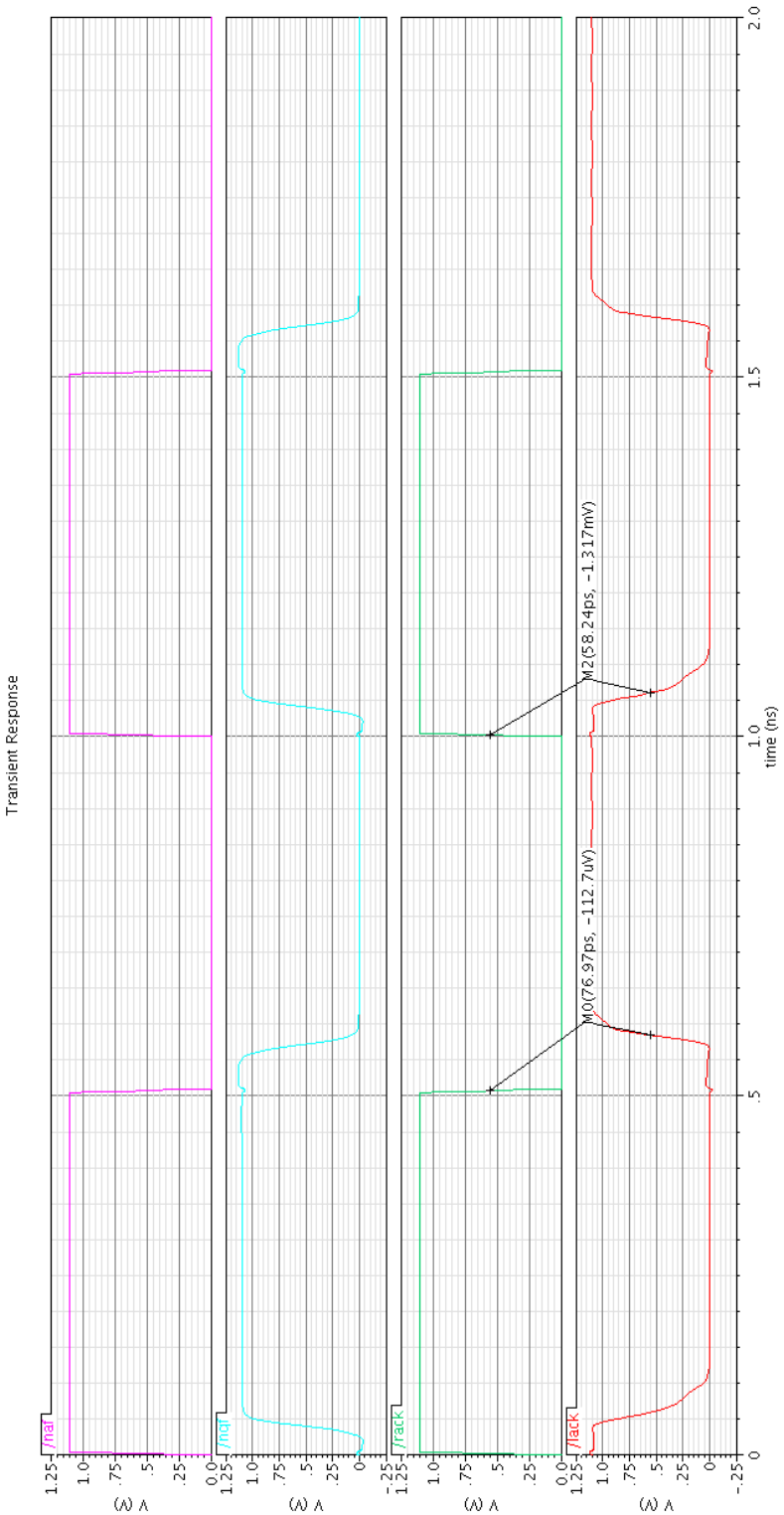


Fig. 5.4 Propagation delay of SAHB buffer logic cell at -40C

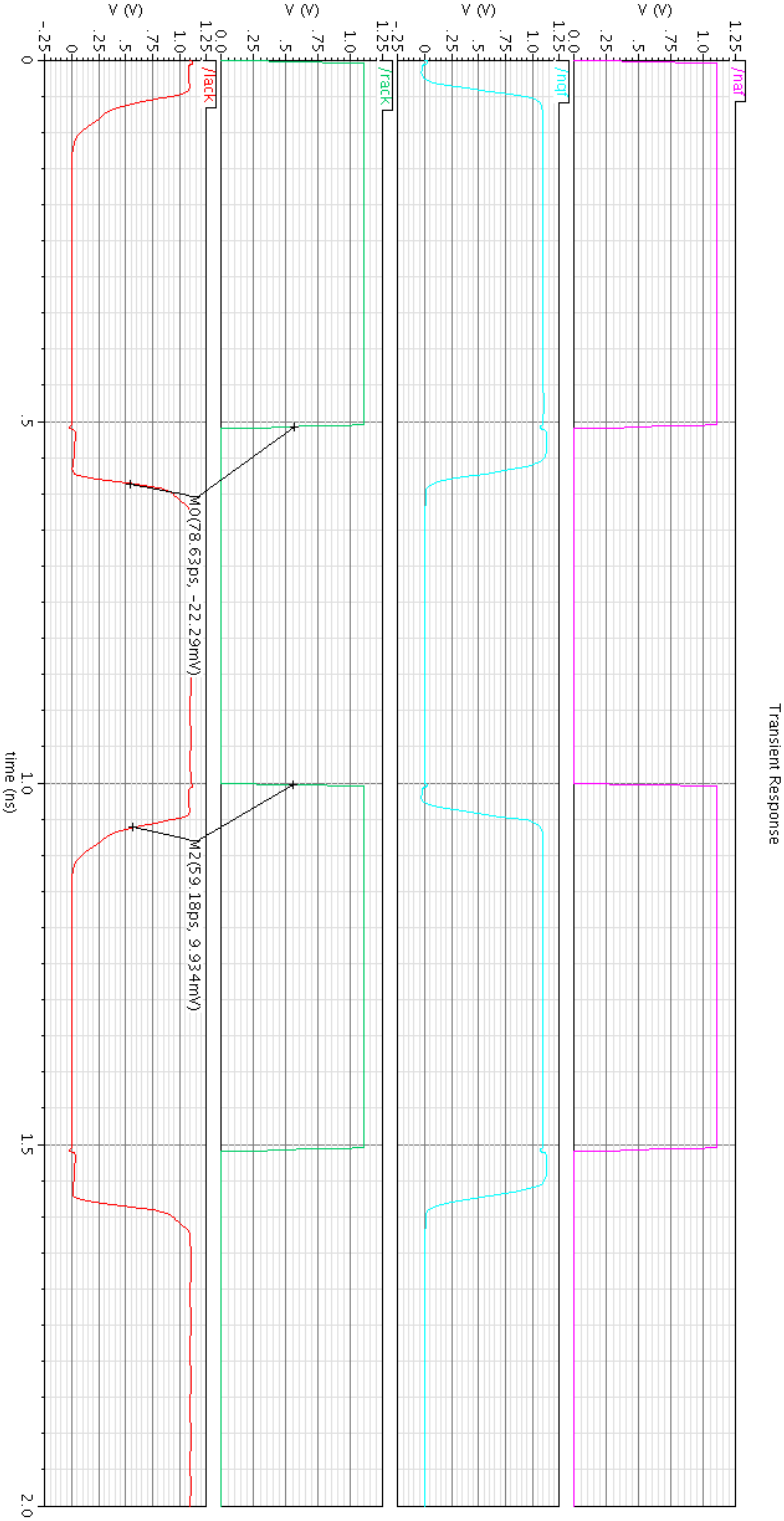


Fig. 5.5 Propagation delay of SAHB buffer logic cell at 0C

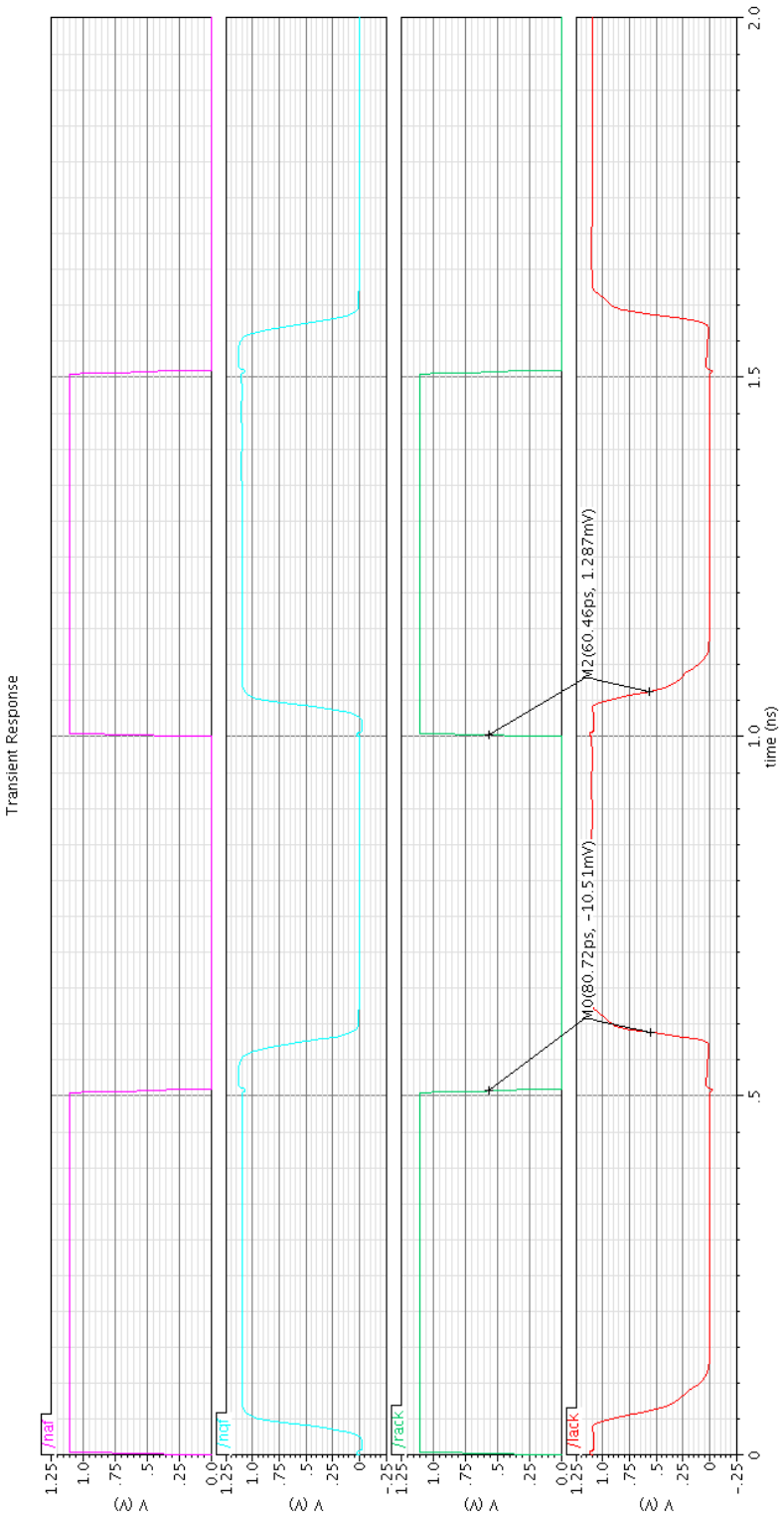


Fig. 5.6 Propagation delay of SAHB buffer logic cell at 27C

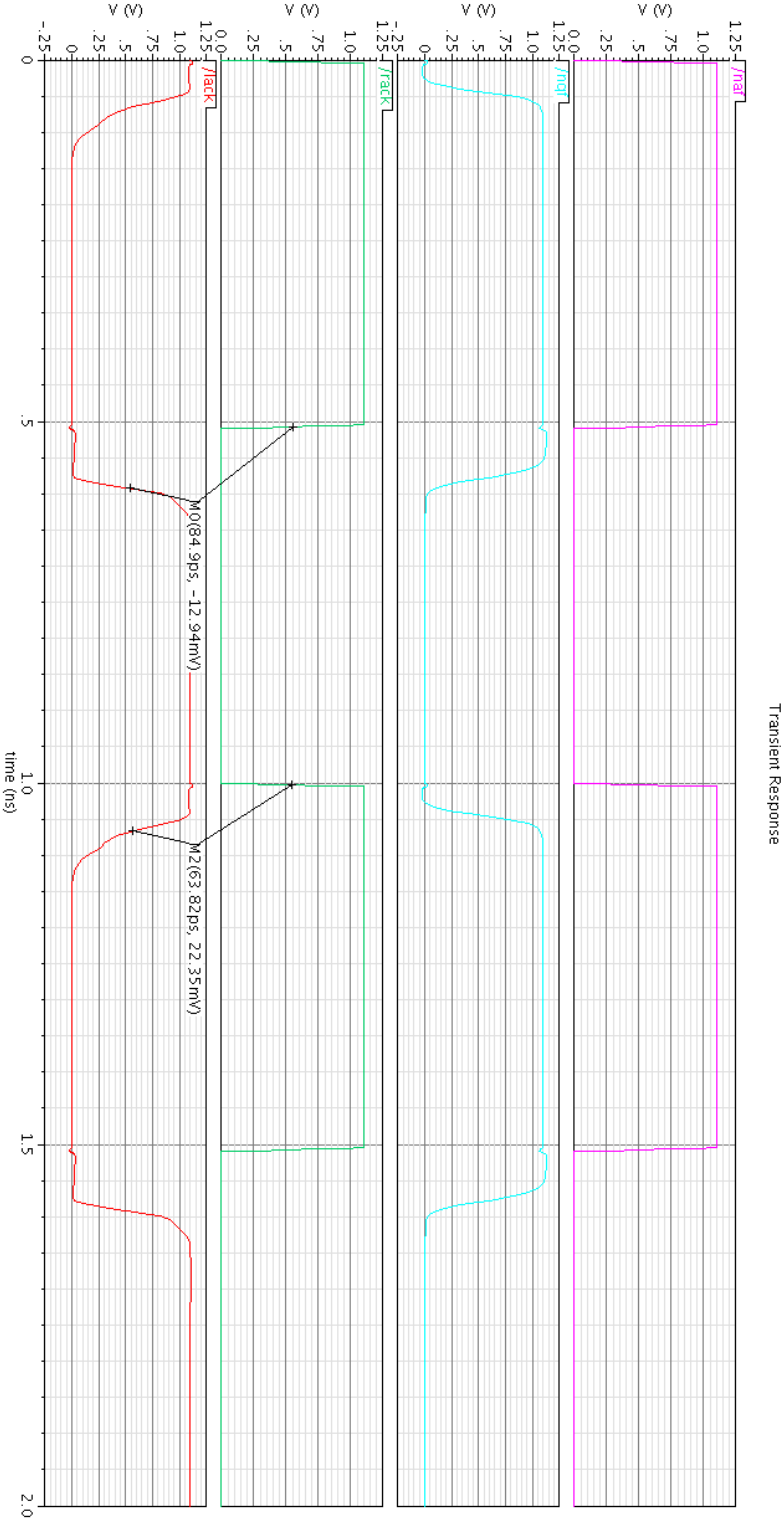


Fig. 5.7 Propagation delay of SAHB buffer logic cell at 100C

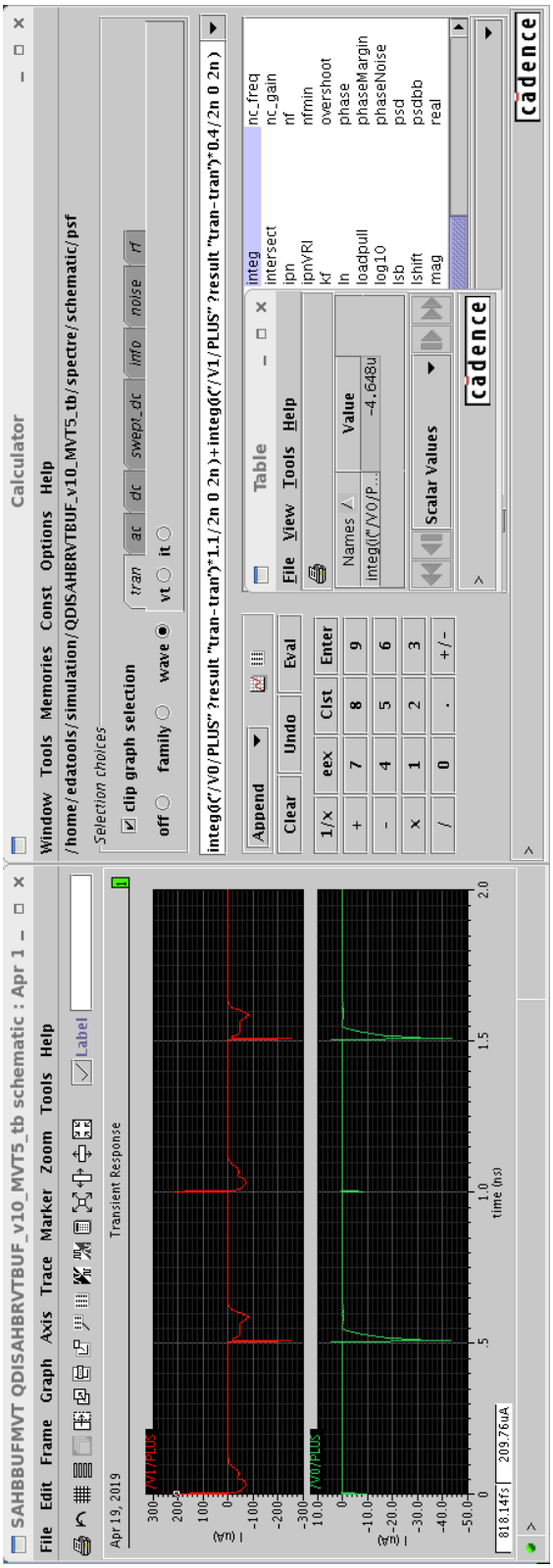


Fig. 5.8 Power consumption of SAHB buffer logic cell at -40C

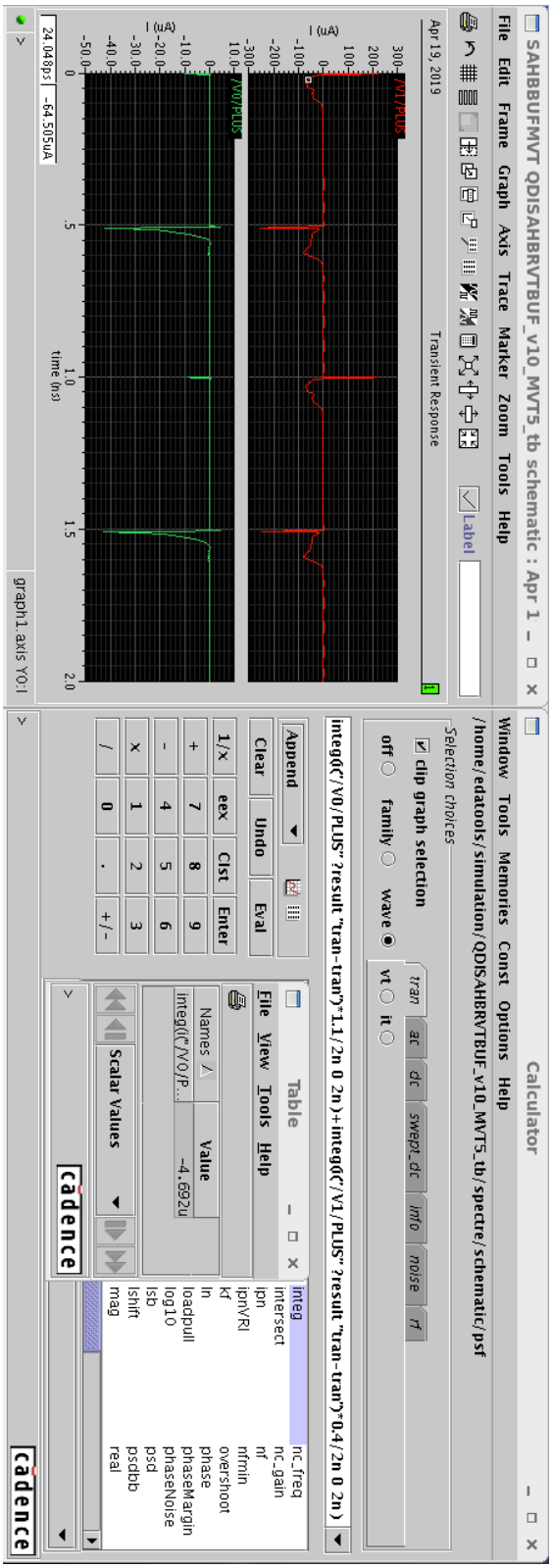


Fig. 5.9 Power consumption of SAHB buffer logic cell at 0C

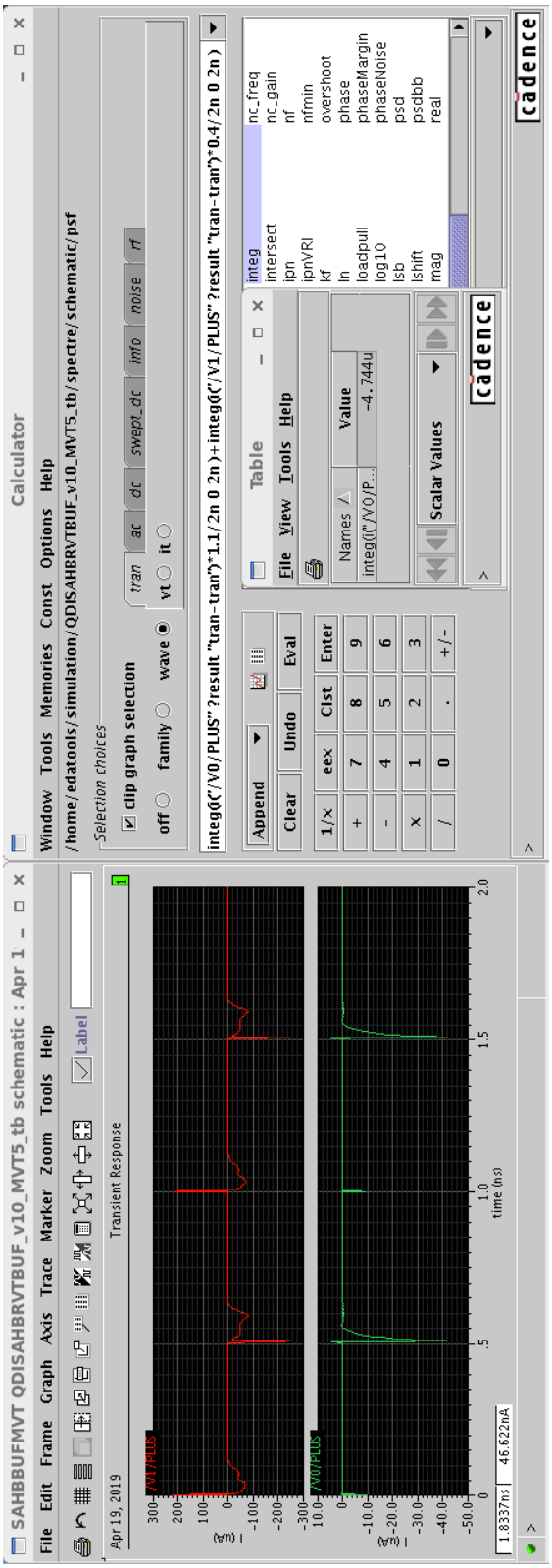


Fig. 5.10 Power consumption of SAHB buffer logic cell at 27C

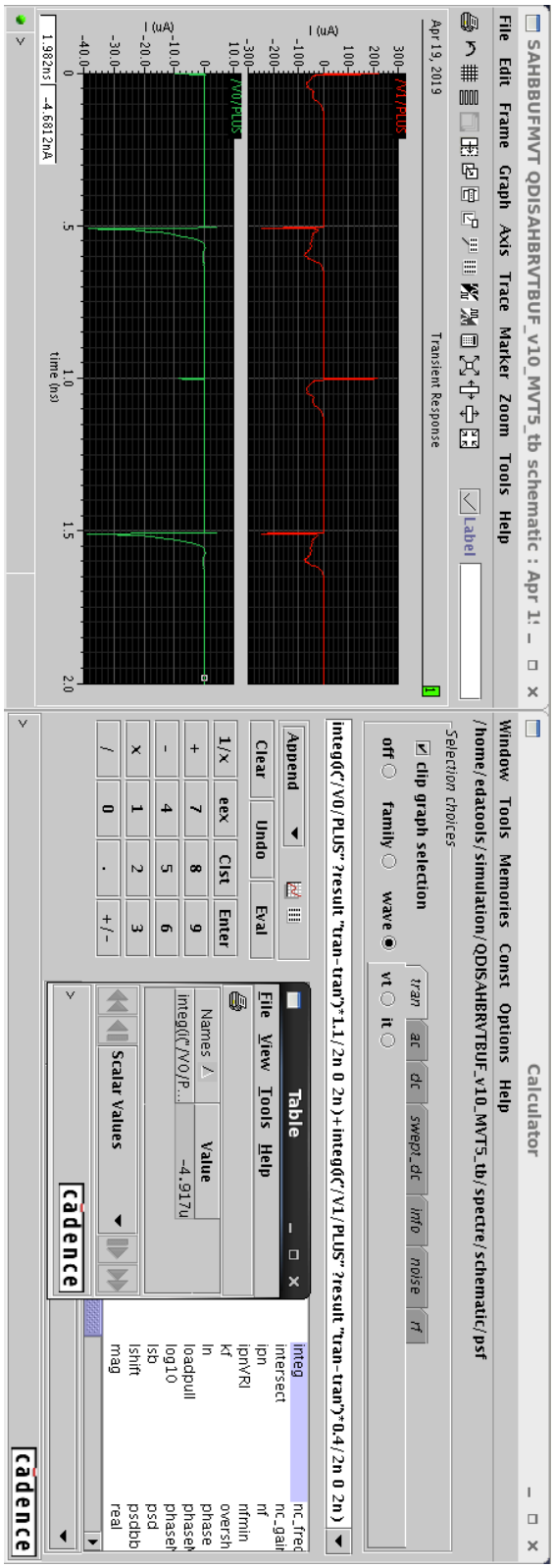


Fig. 5.11 Power consumption of SAHB buffer logic cell at 100C

Chapter 6 Conclusion and Future Work

6.1 Conclusion

This work present a design flow suitable for designing improved architecture of quasi-delay-insensitive based sense amplifier half buffer logic cells. The library is called Improved SAHB (ISAHB) which contains total of 6 logic cells with X1 strength. One of these 6 logic cells is a Muller C element used for synchronization of signals connecting more than one ISAHB logic cell signals. These cells consist Schematic, Symbol, Layout, and Calibre views. Each cell also have its test bench simulation pre-configured for testing. A pdf help file consist of each listed cell characteristics including drive strength, propagation delay and power consumption under different temperatures.

The major contribution of this work is the design flow suitable for asynchronous quasi-delay-insensitive based ISAHB logic cell design with transistor sizing technique called logical effort and multi-voltage threshold technique for speeding up the transistors while reducing power consumption. To validate the views functional and post-layout simulations were performed for each logic cell. Moreover, a test circuit of ring oscillator using the buffer logic cell was designed with even number of cells.

This work is concluded by using a proposed design flow via logical effort and muti-voltage threshold trechniques to design improved quasi-delay-insensitive based sense amplifier half buffer logic cells at 40 nanometer CMOS technology. Functional and physical verification is performed to verify the operation correctness along with a test circuit of ring oscillator using odd number of buffer logic cells.

6.2 Future Work

The work done in this document pave ways for multiple areas of future work. The feedback signals used in the logic cells restrict it from using automated layout tools. Layouting is the most tedious work in this research and it can be minimized by modifying the architecture without affecting the provided features. Moreover, exploration of different types of transistors can contribute to reducing the design complexity i.e. multi-gate transistors which can reduce the design complexity and area overhead. Industry EDA tool Cadence provide SKILL programming language which can be very helpful in automating the complete design flow and substantially reducing the design time using schematic design, layouting and characterization algorithms.

These areas are yet to be explored and can contribute to reducing the gap between asynchronous circuit and industry adoption.

Bibliography

[1] D. Rossi, C. Mucci, M. Pizzotti, L. Perugini, R. Canegallo, and R. Guerrieri, "Multicore signal processing platform with heterogeneous configurable hardware accelerators," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 22, no. 9, pp. 1990–2003, 2014.

[2] D. N. Truong, W. H. Cheng, T. Mohsenin, Z. Yu, A. T. Jacobson, G. Landge, M. J. Meeuwsen, C. Watnik, A. T. Tran, Z. Xiao *et al.*, "A 167-processor computational platform in 65 nm cmos," *IEEE Journal of Solid-State Circuits*, vol. 44, no. 4, pp. 1130–1144, 2009.

[3] G. Jiang, Z. Li, F. Wang, and S. Wei, "A low-latency and low-power hybrid scheme for on-chip networks," *IEEE Transactions on very large scale Integration (VLSI) Systems*, vol. 23, no. 4, pp. 664–677, 2015.

[4] "International technology roadmap for semiconductors (itrs),semi- cond. ind. assoc." ITRS, Tech. Rep., 2009.

[5] "International technology roadmap for semiconductors (itrs),semi- cond. ind. assoc." ITRS, Tech. Rep., 2013.

[6] U. Golze, *VLSI Chip Design with the Hardware Description Language VERILOG: An Introduction Based on a Large RISC Processor Design*. Springer Science & Business Media, 2013.

[7] J. Spars and S. Furber, *Principles asynchronous circuit design*. Springer, 2002.

[8] R. O. Ozdag and P. A. Beerel, "A channel based asynchronous low power high performance standard-cell based sequential decoder implemented with qdi templates," in *10th International Symposium on Asynchronous Circuits and Systems, 2004. Proceedings.* IEEE, 2004, pp. 187–197.

[9] K. S. Chong, W. G. Ho, T. Lin, B. H. Gwee, and J. S. Chang, "Sense Amplifier Half-Buffer (SAHB) A Low-Power High-Performance Asynchronous Logic QDI Cell Template," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 25, no. 2, pp. 402–415, 2017.

[10] "International technology roadmap for semiconductors (itrs),semi- cond. ind. assoc." ITRS, Tech. Rep., 2001.

[11] I. Sutherland, R. F. Sproull, B. Sproull, D. Harris, and E. D. Harris, *Logical effort: designing fast CMOS circuits*. Morgan Kaufmann, 1999.

[12] F. Meinel, N. Kluge, and R. Wollowski, "Improving transistor sizing for asynchronous circuits."

[13] I. Sutherland and S. Fairbanks, "Gasp: A minimal fifo control," in *Proceedings Seventh Inter-*

national Symposium on Asynchronous Circuits and Systems. ASYNC 2001. IEEE, 2001, pp. 46–53.

[14] I. E. Sutherland and J. K. Lexau, "Designing fast asynchronous circuits," in *Proceedings Seventh International Symposium on Asynchronous Circuits and Systems. ASYNC 2001*. IEEE, 2001, pp. 184–193.

[15] J. Ebergen, J. Gainsley, and P. Cunningham, "Transistor sizing: How to control the speed and energy consumption of a circuit," in *10th International Symposium on Asynchronous Circuits and Systems, 2004. Proceedings.* IEEE, 2004, pp. 51–61.

[16] A. D. Bailey, J. Di, S. C. Smith, and H. A. Mantooth, "Ultra-low power delay-insensitive circuit design," in *2008 51st Midwest Symposium on Circuits and Systems*. IEEE, 2008, pp. 503–506.

[17] J.-Y. Lin, L.-R. Wang, C.-L. Hu, and S.-J. Jou, "Mixed-vth (mvt) cmos circuit design for low power cell libraries," in *2007 IEEE International SOC Conference*. IEEE, 2007, pp. 181–184.

[18] M. Ferretti, R. O. Ozdag, and P. A. Beerel, "High performance asynchronous asic back-end design flow using single-track full-buffer standard cells," in *10th International Symposium on Asynchronous Circuits and Systems, 2004. Proceedings.* IEEE, 2004, pp. 95–105.

[19] M. Moreira, B. Oliveira, J. Pontes, and N. Calazans, "A 65nm standard cell set and flow dedicated to automated asynchronous circuits design," in *2011 IEEE International SOC Conference*. IEEE, 2011, pp. 99–104.

[20] C. Hsu, Y. Hong, and J. Kuo, "Mtcmos low-power optimization technique (lpot) for 1v pipelined risc cpu circuit," in *2014 21st IEEE International Conference on Electronics, Circuits and Systems (ICECS)*. IEEE, 2014, pp. 60–63.

[21] F. Sill, C. Cornelius, S. Kubisch, and D. Timmermann, "Mixed gates: Leakage reduction techniques applied to switches for on-chip networks."

[22] S. Kushwah and S. Mishra, "Low power high performance 10t full adder for low voltage cmos technology using dual threshold voltage," 2016.

[23] S. N. Pradhan, A. Chakraborty, A. Nag, and D. Nath, "Layout-oriented look up table-based dual threshold approach to reduce leakage," *International Journal of Computer Aided Engineering and Technology*, vol. 7, no. 4, pp. 456–480, 2015.

[24] P. Verma, A. Noor, A. K. Sharma *et al.*, "Power gating and its repercussions—a review," in *2016 IEEE 1st International Conference on Power Electronics, Intelligent Control and Energy Systems (ICPEICES)*. IEEE, 2016, pp. 1–6.

[25] G. Lin and J. B. Kuo, "Novel power consumption reduction strategy (pcrs) using mixed-vth cells for optimizing the cells on critical paths for low-power soc," *IERI Procedia*, vol. 4, pp. 231–236, 2013.

[26] C. Hsu and J. Kuo, “Power consumption optimization methodology (pcom) for low-power/low-voltage 32-bit microprocessor circuit design via mtcmos,” in *2014 IEEE 57th International Midwest Symposium on Circuits and Systems (MWSCAS)*. IEEE, 2014, pp. 921–924.

[27] P. Larsson-Edefors, H. Eriksson, D. Eckerbert, and A. Alvandpour, “Low-power design of delay-constrained circuits using dual-vt process technology,” in *International Workshop on Power and Timing Modeling, Optimization and Simulation*, 2001, pp. 7–1.

[28] C. Hsu and J. Kuo, “Mtcmos low-power design technique (lpdt) for low-voltage pipelined microprocessor circuits,” in *2014 International Symposium on Integrated Circuits (ISIC)*. IEEE, 2014, pp. 328–331.

[29] D. Saha, S. Basak, S. Mukherjee, and C. K. Sarkar, “A low-voltage, low-power 4-bit bcd adder, designed using the clock gated power gating, and the dvt scheme,” in *2013 IEEE International Conference on Signal Processing, Computing and Control (ISPCC)*. IEEE, 2013, pp. 1–6.

[30] K. Dhar, “Design of a low power, high speed, energy efficient full adder using modified gdi and mvt scheme in 45nm technology,” in *2014 International Conference on Control, Instrumentation, Communication and Computational Technologies (ICCICCT)*. IEEE, 2014, pp. 36–41.

[31] N. Chabini and S. Belkouch, “An algorithm for reducing leakage power dissipation in combinational digital designs using dual threshold voltages,” in *2011 International Conference on Multimedia Computing and Systems*. IEEE, 2011, pp. 1–6.

[32] G. J. Lin, C. B. Hsu, and J. B. Kuo, “Critical-path aware power consumption optimization methodology (capcom) using mixed-v th cells for low-power soc designs,” in *2014 IEEE International Symposium on Circuits and Systems (ISCAS)*. IEEE, 2014, pp. 1740–1743.

[33] R. P. Santos, G. S. Clemente, A. Silva-Filho, C. Araújo, A. Sarmento, M. Lima, and E. Barros, “An optimization mechanism intended for static power reduction using dual-v th technique,” *Journal of Electrical and Computer Engineering*, vol. 2012, p. 1, 2012.

[34] L.-Y. Lu, K.-Y. Chen, and T.-Y. Wu, “High performance and low leakage design using cell replacement and hybrid vt standard cell libraries,” in *Proceedings of the International Multi-Conference of Engineers and Computer Scientists*, vol. 1. Citeseer, 2008, pp. 248–252.

[35] S. Zhou, H. Yao, Q. Zhou, and Y. Cai, “Minimization of circuit delay and power through gate sizing and threshold voltage assignment,” in *2011 IEEE Computer Society Annual Symposium on VLSI*. IEEE, 2011, pp. 212–217.

[36] F. Sill, F. Grassert, and D. Timmermann, “Reducing leakage with mixed-v/sub th/(mvt),” in *18th International Conference on VLSI Design held jointly with 4th International Conference on Embedded Systems Design*. IEEE, 2005, pp. 874–877.

[37] C. S. Nagarajan, L. Yuan, G. Qu, and B. G. Stamps, “Leakage optimization using transistor-

level dual threshold voltage cell library," in *2009 10th International Symposium on Quality Electronic Design*. IEEE, 2009, pp. 62–67.

[38] J. Jaffari and A. Afzali-Kusha, "New dual-threshold voltage assignment technique for low-power digital circuits," in *Proceedings. The 16th International Conference on Microelectronics, 2004. ICM 2004.* IEEE, 2004, pp. 413–416.

[39] F. Sill, F. Grassert, and D. Timmermann, "Total leakage power optimization with improved mixed gates," in *Proceedings of the 18th annual symposium on Integrated circuits and system design*. ACM, 2005, pp. 154–159.

[40] P. Lakshmikanthan and A. Nunez, "Vclearit: A vlsi cmos circuit leakage reduction technique for nanoscale technologies," *ACM Sigarch computer architecture news*, vol. 35, no. 5, pp. 10–16, 2007.

[41] M. T. Moreira, "Design and implementation of a standard cell library for building asynchronous asics," *Pontificia Universidade Catolica Do Rio Grande Do Sul*, 2010.

[42] M. Prakash, *Library characterization and static timing analysis of asynchronous circuits*. University of Southern California, 2007.

Appendix A Improved SAHB logic cell library layouts

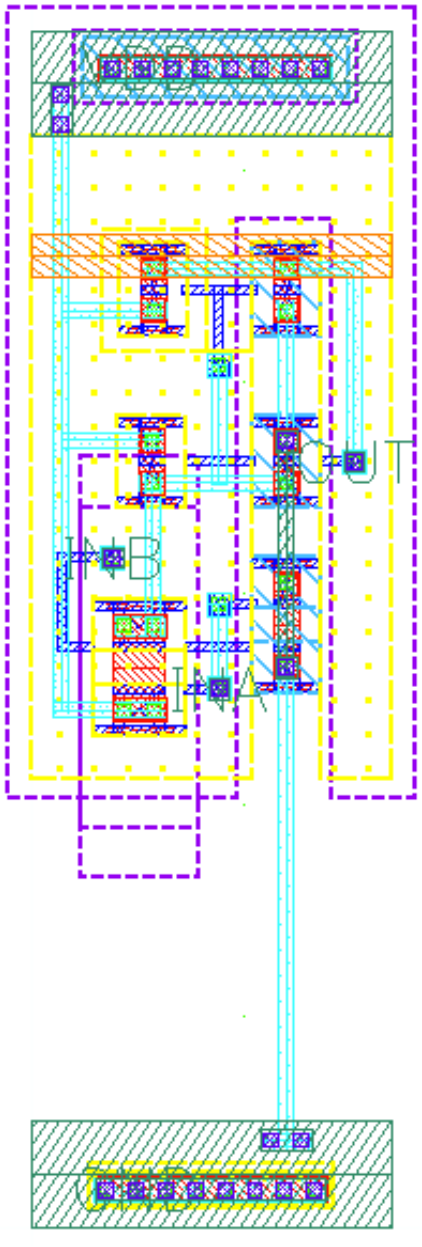


Fig. A.1 Muller C element logic cell layout

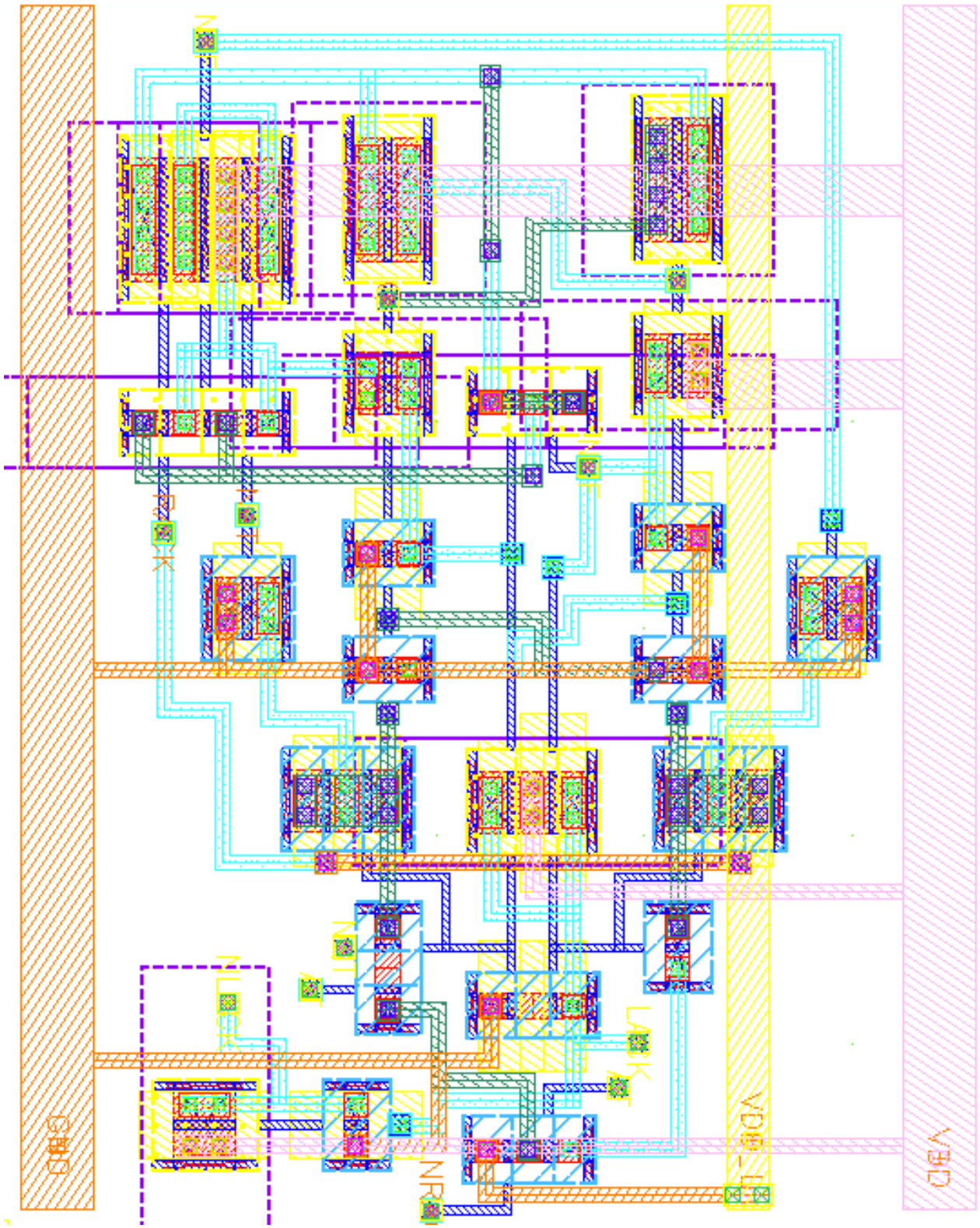


Fig. A.2 Improved SAHB Inverter/Buffer logic cell layout

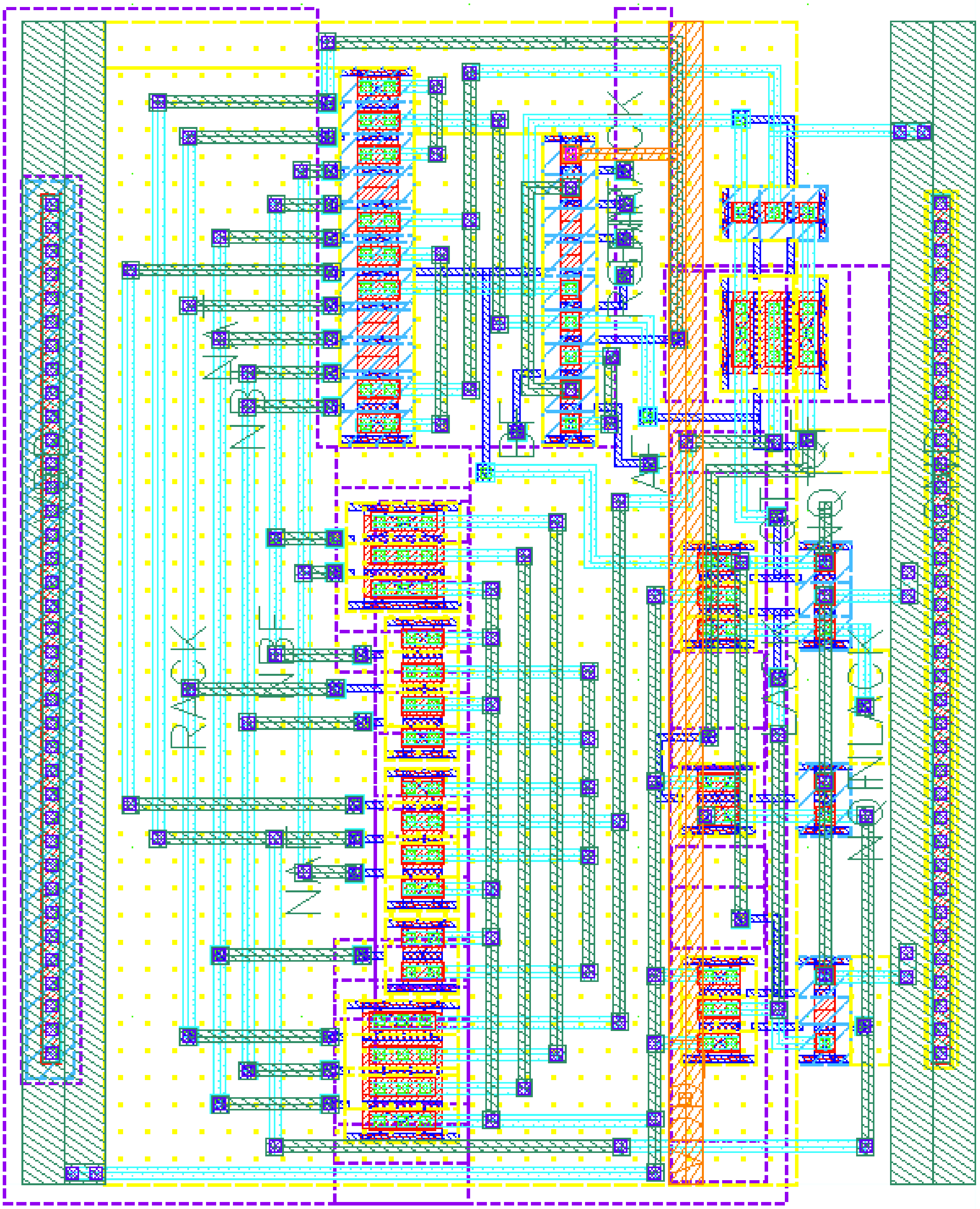


Fig. A.3   Improved SAHB AND/NAND logic cell layout

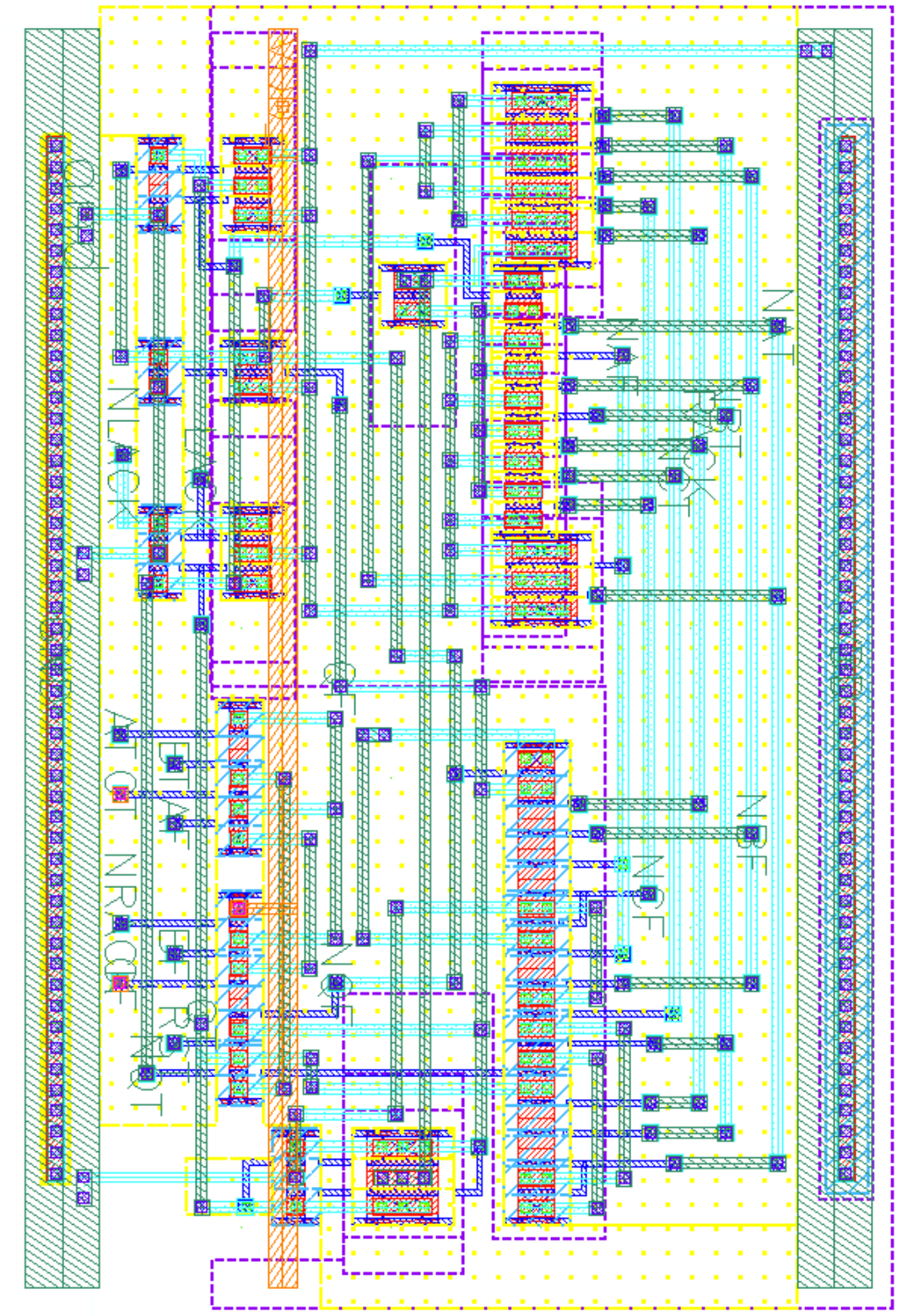


Fig. A.4 Improved SAHB AO/AOI logic cell layout

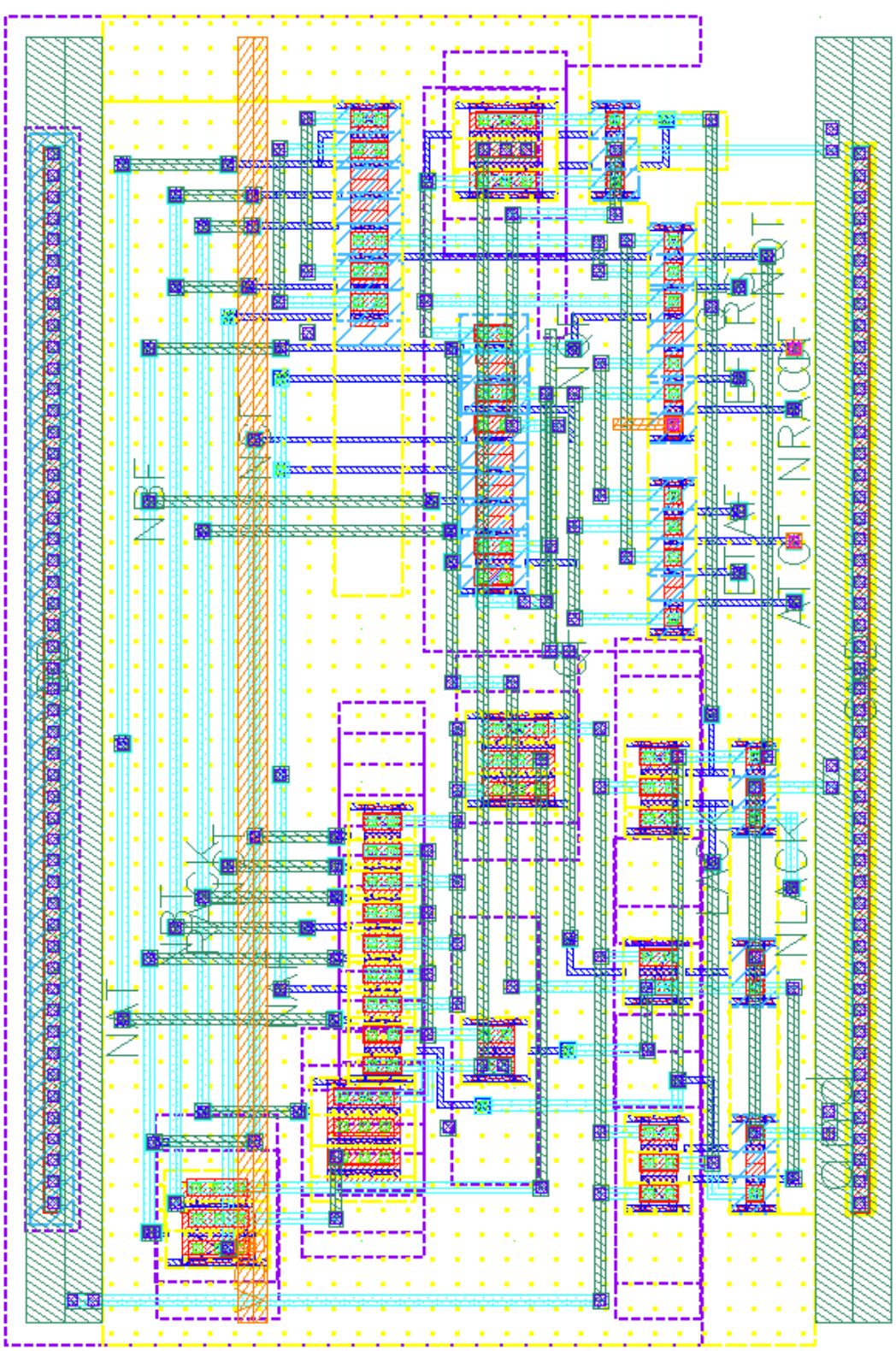


Fig. A.5 Improved SAHB NOR/XNOR logic cell layout

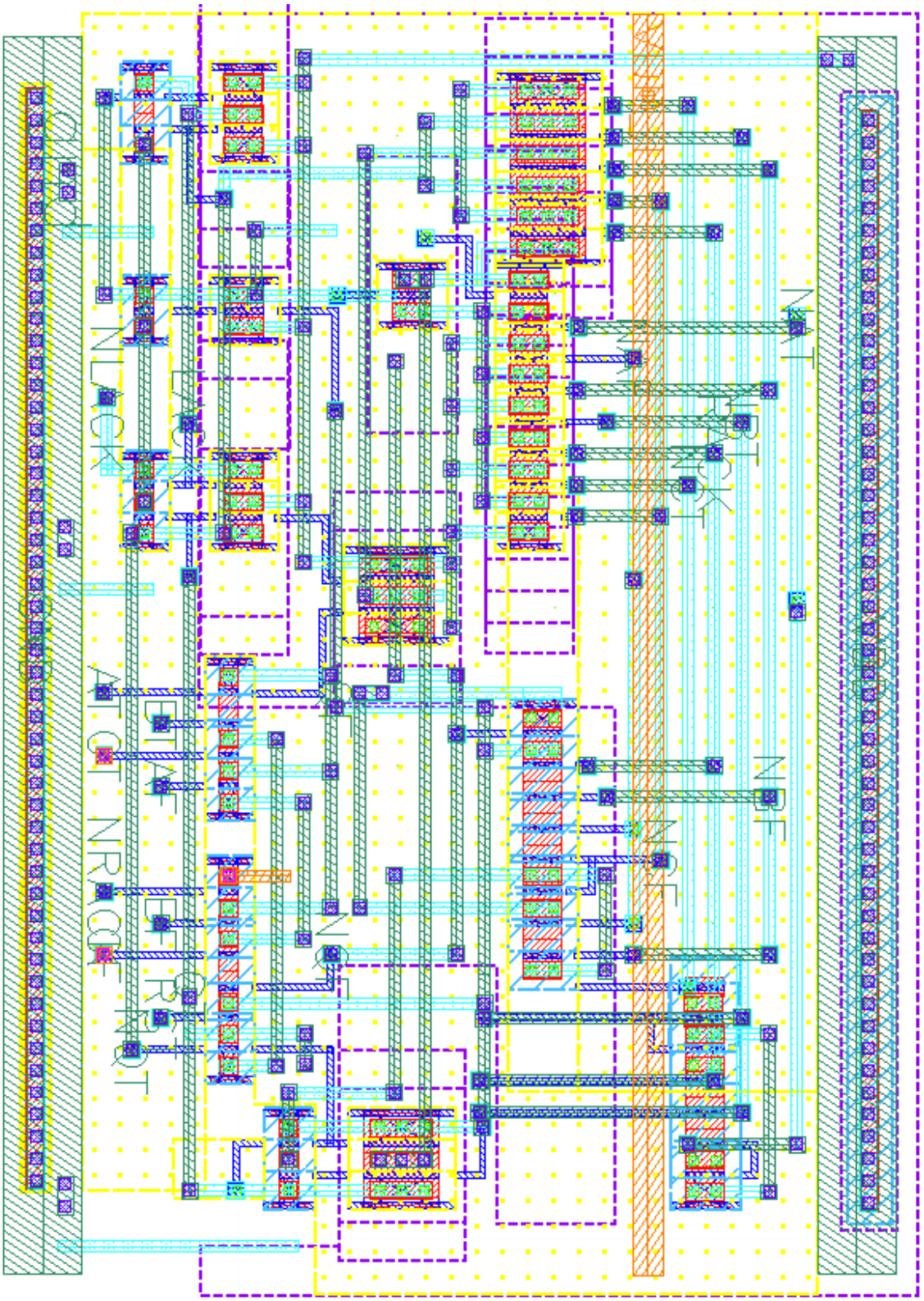


Fig. A.6 Improved SAHB MUX/IMUX logic cell layout

Acknowledgements

I would like to thank my adviser Assistant Professor Song Chen who has always been an inspiration for me in pursuing my research and this thesis. He has been an excellent teacher and mentor for me. I would like to thank Professor Cheng Lin for his valuable inputs and suggestions in my research work and paper. I acknowledge the help in form of lectures and mentoring from Professor Fujiang Lin, Professor Lu Huang and Professor Bai Xuefei. Furthermore, I would like to extend my acknowledgment to MESIC team at University of Science and Technology of China for providing me with the opportunity and facilities of hardware and software which made this research possible. I would like to thank Chunling Li, Yan Xu, and Liu Bai Cheng for their help and support during my research work and thesis writing.

I thank Cadence and SMIC for providing us the software and technology data which were used in this research work. I am grateful to the thesis review committee members for their valuable feedbacks. I would like to thank Chinese Scholarship Council (CSC) for funding and supported in part by the National Natural Science Foundation of China under Grant 61732020 and Grant 61874102.

My parents, my wife, and my siblings have always supported and believed in me with unconditional love, not only in this stage of life but always.