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| **DRE TDM firmware requirements** |

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| **Prepared by** | *Signature* |  | **Accepted by** | *Signature* |
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| **Concerned Models** | **BB** |  | **DM** |  | **EM** |  | **STM** |  | **QM** |  | **FM** |  | **FS** |  | **All** |  |

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| **Approved by** | ***Function*** | ***Date*** | ***Signature*** |
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| **Summary** |  |
| **Annexes** |  |

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| 0.5 | 31/05/2021 | / | Updated accorded to RIDs from Sylvain  Document template updated |
| 0.4 | 14/01/2021 | / | Update of req. format |
| 0.3 | 08/01/2021 | / | Fully updated |
| 0.2 | 17/08/2020 | / | After Yann’s comments |
| 0.1 | 15/06/2020 | / | First issue |

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| **Applicable Documents (AD)** | | | |
| **AD** | **Title** | **Reference** | **Version** |
| **AD01** | XIFU DRE requirements document | XIFU-RD-13200-00420-CNES | 2.0 |
| **AD02** | Design and VHDL handbook for VLSI development, CNES Edition |  | 2.1 |
| **AD03** | DRE Inter-Modules Telemetry And Commands Definition | IRAP/XIFU-DRE/FM/SP/0069 |  |

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| **Reference Documents (RD)** | | | |
| **RD** | **Title** | **Reference** | **Version** |
| **RD01** | Transition edge sensors | Irwin and Hilton 2005 |  |
| **RD02** | XIFU TDM detection chain definition document | XIFU-DD-10000-00422-CNES | 1 |
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| **List of Abbreviations** | | | |
| **ADC** | **A**nalogue to **D**igital **C**onverter | **SQUID** | **S**uperconducting **QU**antum **I**nterference **D**evice |
| **AMP SQUID** | **AMP**lifier **SQUID** | **TDM** | **T**ime **D**omain **M**ultiplexing |
| **DAC** | **D**igital to **A**nalogue **C**onverter | **TES** | **T**ransition **E**dge **S**ensor |
| **FPGA** | **F**ield **P**rogrammable **G**ate **A**rray | **TC** | **T**ele**C**ommands |
| **HK** | **H**ouse**K**eepings | **TM** | **T**ele**M**etry |
| **MUX SQUID** | **MU**ltiple**X**er **SQUID** |  |  |

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# INTRODUCTION

## Scope of the document

This document defines the requirements of the firmware which drives the Time Domain Multiplexed (TDM) readout of the detector array onboard Athena X-IFU.

## Description of the X-IFU and the DRE

Athena is designed to implement the Hot and Energetic Universe science theme selected by the European Space Agency for the second large mission of its Cosmic Vision program. The Athena science payload consists of a large aperture high angular resolution X-ray optics and twelve meters away, two interchangeable focal plane instruments: The X-ray Integral Field Unit (X-IFU) and the Wide Field Imager. The X-IFU is a cryogenic X-ray spectrometer, based on a large array of Transition Edge Sensors (TES) micro-calorimeters operated at 90 mK and offering a 2.5 eV spectral resolution.

In the X-IFU, the "Digital Readout Electronics" (DRE) drives the TDM readout of the 3168 superconducting TES of the detector array. For this, it reads the TES current measured by the instrument amplification chain (MUX SQUIDs, AMP SQUIDS and LNA) and it linearizes the entire detection chain with an active feedback loop. The DRE performs both, analogue and digital signal processing (A/D and D/A conversion, analogue filtering, digital filtering, feedback management...). The digital processing is done by the firmware of the DRE-DEMUX.

## The Time Domain Multiplexing (TDM)

In order to readout the 3168 TES of the X-IFU Focal Plan Array (FPA) a multiplexed readout technique is mandatory. For the X-IFU a Time Domain Multiplexing (TDM) method is used. The FPA is arranged in 96 detection chains (so-called “columns”) of 34 pixels (see Figure 1). The pixels of a columns are readout sequentially. This sequence is called “a frame”.

Each TES pixel (which is equivalent to a resistor) is biased with a DC-voltage provided by the WFEE. The detection of an X-ray photon changes the TES resistance and modulates its current at a low frequency (in the kHz range). In each detection chain a column of SQUIDs (so-called MUX SQUIDs or SQUIDs SQ1) reads sequentially the current of the TESs. The MUX SQUID addressing is driven by rows. For redundancy reasons it is common to 16 columns.

Each detection chain includes a “blind” TES for calibration purposes. The MUX SQUID output is amplified by a second stage SQUID (so-called AMP SQUID or SQUID SQ2) and a low noise amplifier in the WFEE. From this signal the DRE-DEMUX shall derive:

* A feedback to be applied at the MUX SQUID in order to linearize the detection chain. The feedback to be applied to the MUX SQUID to readout a pixel is derived from the value that has been readout at the previous frame.
* The measurement of the TES current.

The DRE shall apply a feedback to the AMP SQUID in order to compensate for the SQ1 offset variations across the column.

Details about the TDM technique can be found in RD02 section 3.1.

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| Figure 1: TDM cold front-end electronics with the TES, the FAS and the MUX SQUIDs. |

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| Figure 2: TDM detection chain with a focus on the AMP SQUIDs, the WFEE and the DRE. |

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| Figure 3: Diagram of the detection chain with a focus on the DRE functionalities. |

# Format of the requirements

In this document the requirements have the following format:

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| **Title:** | **Title of the requirement** |
| **Reference:** | Reference of the requirement as follows: DRE-DMX-FW-REQ-XXXX.  Where:  - DRE-DMX-FW defines the applicability of the requirement:  DRE (DRE) |  |> DEMUX (DMX) |  |> Firmware (FW)  - REQ stands for ‘requirement’  - XXXX is a four-digit number aiming to define a specific reference for each requirement. |
| **Description:** | Short, clear, unambiguous description of the requirement. |
| **Type:** | Type of requirement (number):   * 1=Informational * 2=Feature * 3=Use Case * 4=User Interface * 5=Non Functional * 6=Constraint * 7=System Function |
| **Status:** | Status of the requirement (letter):   * D=Draft * R=Review * W=Rework * F=Finish * I= Implemented * V=Valid * N=Non Testable * O=Obsolete |
| **Higher level req.:** | Reference of the higher-level requirement which implies this one. |
| **Verification level:** | At which level of the integration flow will it be possible to verify this requirement? |
| **Verification method:** | What will be the verification methods:   * Analysis * Tests * Review of design |
| **Comment:** | Complementary description if needed. |

# Requirements

## General requirements

These requirements are design constraints for the FPGA.

|  |  |
| --- | --- |
| **Title:** | **Host FPGA** |
| **Reference:** | DRE-DMX-FW-REQ-0010 |
| **Description:** | The firmware shall be operated on a NG-Large FPGA (ref. NX1H140TSP). |
| **Type:** | 6 |
| **Status:** |  |
| **Higher level req.:** |  |
| **Verification level:** |  |
| **Verification method:** | Review of design |
| **Comment:** |  |

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| --- | --- |
| **Title:** | **CNES VHDL handbook** |
| **Reference:** | DRE-DMX-FW-REQ-0020 |
| **Description:** | The firmware shall be compliant with the design and VHDL handbook for VLSI developments, CNES edition, (AD02) |
| **Type:** | 6 |
| **Status:** |  |
| **Higher level req.:** |  |
| **Verification level:** |  |
| **Verification method:** | Review of design |
| **Comment:** |  |

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| **Title:** | **Testability** |
| **Reference:** | DRE-DMX-FW-REQ-0030 |
| **Description:** | TBD |
| **Type:** | 5 |
| **Status:** |  |
| **Higher level req.:** |  |
| **Verification level:** |  |
| **Verification method:** | Review of design |
| **Comment:** |  |

## System requirements

These requirements are high level requirements for the firmware.

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| **Title:** | **External reference clock** |
| **Reference:** | DRE-DMX-FW-REQ-0040 |
| **Description:** | The firmware shall use an external reference clock CLK\_REF whose frequency C\_CLK\_REF\_FREQ is equal to 60 MHz ±TBD ppm (TBD). |
| **Type:** | 2 |
| **Status:** |  |
| **Higher level req.:** |  |
| **Verification level:** |  |
| **Verification method:** | Review of design |
| **Comment:** | The external reference clock is provided by the row address module. |

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| **Title:** | **Asynchronous reset** |
| **Reference:** | DRE-DMX-FW-REQ-0050 |
| **Description:** | An asynchronous reset, activated on '0' logical level, shall be available on a FPGA input for the internal reset(s) generation. |
| **Type:** | 2 |
| **Status:** |  |
| **Higher level req.:** |  |
| **Verification level:** |  |
| **Verification method:** | Review of design |
| **Comment:** |  |

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| **Title:** | **Pin allocation** |
| **Reference:** | DRE-DMX-FW-REQ-0060 |
| **Description:** | The FPGA pin allocation shall be as defined in Appendix A – Pin allocation |
| **Type:** | 2 |
| **Status:** |  |
| **Higher level req.:** |  |
| **Verification level:** |  |
| **Verification method:** | Review of design |
| **Comment:** |  |

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| --- | --- |
| **Title:** | **Number of columns** |
| **Reference:** | DRE-DMX-FW-REQ-0070 |
| **Description:** | The firmware shall process a number of columns C\_NB\_COL = 4 |
| **Type:** | 2 |
| **Status:** |  |
| **Higher level req.:** |  |
| **Verification level:** |  |
| **Verification method:** | Test |
| **Comment:** | A column is equivalent to a detection chain. |

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| **Title:** | **Multiplexing factor** |
| **Reference:** | DRE-DMX-FW-REQ-0080 |
| **Description:** | The firmware shall apply a multiplexing factor C\_MUX\_FACT = 34. |
| **Type:** | 2 |
| **Status:** |  |
| **Higher level req.:** |  |
| **Verification level:** |  |
| **Verification method:** | Test |
| **Comment:** | The multiplexing factor is the number of pixels per column. Among the 34 pixels to be processed by the firmware, 33 are “science” pixels and one is used for calibration purposes. |

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| **Title:** | **Readout synchronization** |
| **Reference:** | DRE-DMX-FW-REQ-0090 |
| **Description:** | The firmware shall synchronize the pixel sequence processing with an external synchronization signal (SYNC). A rising edge of SYNC indicates that the next pixel to be processed is pixel 1. Afterward the pixels are processed sequentially from 1 to C\_MUX\_FACT. |
| **Type:** | 2 |
| **Status:** |  |
| **Higher level req.:** |  |
| **Verification level:** |  |
| **Verification method:** | Test |
| **Comment:** | The SYNC signal is provided by the row address and synchronization module to the DEMUX modules. It lasts at least one period of CLK\_REF and its frequency is:  C\_FRAME\_FREQ = C\_ROW\_FREQ / C\_MUX\_FACT |

## Error signal requirements

These requirements are specific to the handling of the TDM error signal.

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| **Title:** | **Error signal: Reference of the ADC** |
| **Reference:** | DRE-DMX-FW-REQ-0100 |
| **Description:** | For each column, the firmware shall drive an ADC AD9254S to do the acquisition of the error signal from the detection chain |
| **Type:** | 2 |
| **Status:** |  |
| **Higher level req.:** |  |
| **Verification level:** |  |
| **Verification method:** | Test |
| **Comment:** |  |

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| **Title:** | **Error signal: Clock for the ADC** |
| **Reference:** | DRE-DMX-FW-REQ-0110 |
| **Description:** | For every column, the firmware shall provide the clock signal to the ADC in charge of the acquisition of the error. It shall be possible the enable and disable this clock signal with the command TBD of AD03. |
| **Type:** | 2 |
| **Status:** |  |
| **Higher level req.:** |  |
| **Verification level:** |  |
| **Verification method:** | Test |
| **Comment:** |  |

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| **Title:** | **Error signal: Sampling frequency of the ADC** |
| **Reference:** | DRE-DMX-FW-REQ-0120 |
| **Description:** | The sampling frequency of the ADCs in charge of the acquisition of the error signals shall be equal to:  C\_CLK\_ADC\_FREQ = C\_CLK\_ADC\_MULT \* C\_CLK\_REF\_FREQ  with C\_CLK\_ADC\_MULT = 2 (TBC) |
| **Type:** | 2 |
| **Status:** |  |
| **Higher level req.:** |  |
| **Verification level:** |  |
| **Verification method:** | Test |
| **Comment:** | The baseline is C\_CLK\_ADC\_FREQ = 120 MHz |

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| **Title:** | **Time allocation for pixel acquisition** |
| **Reference:** | DRE-DMX-FW-REQ-0130 |
| **Description:** | The number of ADC clock cycles allocated to the acquisition of the C\_MUX\_FACT-1 pixels shall be C\_PIXEL\_ADC\_NB\_CYC = XXX. |
| **Type:** | 2 |
| **Status:** |  |
| **Higher level req.:** |  |
| **Verification level:** |  |
| **Verification method:** | Test |
| **Comment:** | The duration allocated to the first C\_MUX\_FACT-1 pixels is:  1/C\_ROW\_FREQ = C\_PIXEL\_ADC\_NB\_CYC / C\_CLK\_ADC\_FREQ  With:  C\_CLK\_ADC\_FREQ=120 MHz (TBC)  C\_PIXEL\_ADC\_NB\_CYC = TBD between 18 and 22  C\_ROW\_FREQ = TBD between 6.67 MHz and 5.45 MHz  The duration allocated to the last pixel depends on SYNC signal. |

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| **Title:** | **Error signal: Boxcar filter** |
| **Reference:** | DRE-DMX-FW-REQ-0140 |
| **Description:** | The firmware shall compute one value of the error signal per pixel by averaging ADC\_BOXCAR\_NB\_CYC consecutive ADC values. ADC\_BOXCAR\_NB\_CYC shall be tunable between 1 and 32 with the command TBD of AD03. |
| **Type:** | 2 |
| **Status:** |  |
| **Higher level req.:** |  |
| **Verification level:** |  |
| **Verification method:** | Test |
| **Comment:** |  |

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| **Title:** | **Error signal: Fine timing correction** |
| **Reference:** | DRE-DMX-FW-REQ-0150 |
| **Description:** | For each column, the firmware shall have the ability to select which ADC data shall be used to compute the average by applying a delay ADC\_DELAY\_NB\_CYC to the input signal. ADC\_DELAY\_NB\_CYC shall be tunable between 0 and 31 periods of CLK\_ADC according to the command CX\_SAMPLING\_DELAY of AD03 (X is the column number). |
| **Type:** | 2 |
| **Status:** |  |
| **Higher level req.:** |  |
| **Verification level:** |  |
| **Verification method:** | Test |
| **Comment:** |  |

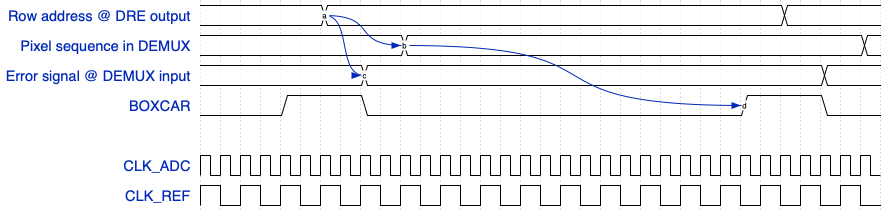


Figure 4: Timings of error signal input. Timings a to b and a to c depend on the environment of the firmware, they may change. Once these timings are characterized, ADC\_DELAY\_NB\_CYC (between labels b and d) is used to align the valid data with the boxcar sequence. ADC\_BOXCAR\_NB\_CYC is the width of the boxcar.

## SQ1 feedback requirements

These requirements are specific to the computation and the handling of the feedback signal for the MUX SQUID.

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| **Title:** | **SQ1 feedback: computation of the feedback in close loop mode** |
| **Reference:** | DRE-DMX-FW-REQ-0160 |
| **Description:** | For each column, for each frame, and sequentially for each pixel, the firmware shall compute a feedback value over 14 bits (unsigned int format) according to the following formulas:  FB(p, n+1) = FB(p, lp) + FB(p, n) + ki(p).[E(p, n) - E(p, lp)] + dFB(p, n)  dFB(p, n) = a(p).ki(p).E(p, n-1) + dFB(p, n-1)  p is the pixel index, n is the frame index  E(p, lp) is the value of the error signal for pixel p at the lock point  FB(p, lp) is the value of the feedback signal for pixel p at the lock point |
| **Type:** | 2 |
| **Status:** |  |
| **Higher level req.:** |  |
| **Verification level:** |  |
| **Verification method:** | Test |
| **Comment:** | This is the so-called “Predictive Compensation 1” algorithm (PC1).  a(p)=1/(1+τ) with τ = 1/(2π.fc’)  fc’ is the normalized cutoff frequency:  fc’ = fc / (C\_ROW\_FREQ / C\_MUX\_FACT) = fc / C\_FRAME\_FREQ  fc is the cutoff frequency (in Hz) of the low pass filter.  FB(p, lp) and E(p, lp) are provided to the firmware with dedicated commands  The SQ1 feedback loop is illustrated on Figure 6. |

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| Figure 5 : Illustration of the feedback signal which brings the SQUID back to its lock point. |

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| **Title:** | **SQ1 feedback: Setting of ki** **parameters** |
| **Reference:** | DRE-DMX-FW-REQ-0170 |
| **Description:** | For every column and every pixel the parameter ki of the feedback formula shall be configurable by the command CX\_KI of AD03 (X is the column number) between TBD and TBD, with a resolution TBD. |
| **Type:** | 2 |
| **Status:** |  |
| **Higher level req.:** |  |
| **Verification level:** |  |
| **Verification method:** | Test |
| **Comment:** | The global loop gain shall be configurable between 1 and 2. The parameter ki of the firmware is only one contribution among others to the loop gain. |

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| **Title:** | **SQ1 feedback: Setting of “a” parameters** |
| **Reference:** | DRE-DMX-FW-REQ-0180 |
| **Description:** | For every column and every pixel (TBC) The parameter “a” of the feedback formula shall be configurable by the command TBD from AD03 for each pixel between TBD and TBD, with a resolution TBD. |
| **Type:** | 2 |
| **Status:** |  |
| **Higher level req.:** |  |
| **Verification level:** |  |
| **Verification method:** | Test |
| **Comment:** |  |

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| **Title:** | **SQ1 feedback: Setting of E(p, lp)** **parameters** |
| **Reference:** | DRE-DMX-FW-REQ-0190 |
| **Description:** | For every column and every pixel, the parameter E(p, lp) of the feedback formula shall be configurable by the command CX\_SQ1\_LOCKPOINT\_V of AD03 (X is the column number) between TBD and TBD, with a resolution TBD. |
| **Type:** | 2 |
| **Status:** |  |
| **Higher level req.:** |  |
| **Verification level:** |  |
| **Verification method:** | Test |
| **Comment:** |  |

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| **Title:** | **SQ1 feedback: Setting of FB(p, lp)** **parameters** |
| **Reference:** | DRE-DMX-FW-REQ-0200 |
| **Description:** | For every column and every pixel, the parameter FB(p, lp) of the feedback formula shall be configurable by the command CX\_SQ1\_LOCKPOINT\_PHI of AD03 (X is the column number) between TBD and TBD, with a resolution TBD. |
| **Type:** | 2 |
| **Status:** |  |
| **Higher level req.:** |  |
| **Verification level:** |  |
| **Verification method:** | Test |
| **Comment:** |  |

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| **Title:** | **SQ1 feedback: mode selection** |
| **Reference:** | DRE-DMX-FW-REQ-0210 |
| **Description:** | For each column, it shall be possible to configure the SQ1 feedback mode with the command SQ1\_FB\_MODE of AD03 to:  - Off: 0  - Open loop: FB(p,lp)  - Locked: FB(p,n)  - Test: Test pattern |
| **Type:** | 2 |
| **Status:** |  |
| **Higher level req.:** |  |
| **Verification level:** |  |
| **Verification method:** | Test |
| **Comment:** |  |

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| **Title:** | **SQ1 feedback: pulse shaping** |
| **Reference:** | DRE-DMX-FW-REQ-0220 |
| **Description:** | For every column, the firmware shall “up-sample” the MUX SQUID feedback data at the rate 1/C\_PIXEL\_DAC\_NB\_CYC and apply a digital filter according to the following formula:  Y[k] = Xfinal(p) + (Xinit(p) - Xfinal(p)) \* a[k]  With:  k in the range 0 to C\_PIXEL\_DAC\_NB\_CYC-1  Xfinal: the previous value of the SQ1 feedback  Xinit: the next value of the SQ1 feedback  Xinit(p) = Xfinal(p-1) |
| **Type:** | 2 |
| **Status:** |  |
| **Higher level req.:** |  |
| **Verification level:** |  |
| **Verification method:** |  |
| **Comment:** | This so-called “pulse shaping” allows to digitally control the shape of the signal edges.  If a[k]= (1-b)^k then y[k] is strictly equivalent to the digital filter:  y(n) = (1+b).x(n) – b.y(n-1) |

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| **Title:** | **SQ1 feedback: Setting of the pulse shaping parameters “a”** |
| **Reference:** | DRE-DMX-FW-REQ-0230 |
| **Description:** | For every column, it shall be possible to load in the firmware 3 set of pulse shaping parameters “a” (C\_PIXEL\_DAC\_NB\_CYC values each) with the command TBD of AD03. |
| **Type:** | 2 |
| **Status:** |  |
| **Higher level req.:** |  |
| **Verification level:** |  |
| **Verification method:** | Test |
| **Comment:** |  |

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| **Title:** | **SQ1 feedback: Reference of the DAC** |
| **Reference:** | DRE-DMX-FW-REQ-0240 |
| **Description:** | For each column, the firmware shall drive a DAC DAC5675A-SP to output the feedback signal for the SQUID SQ1. |
| **Type:** | 2 |
| **Status:** |  |
| **Higher level req.:** |  |
| **Verification level:** |  |
| **Verification method:** | Test |
| **Comment:** |  |

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| **Title:** | **SQ1 feedback: Clock for the DAC** |
| **Reference:** | DRE-DMX-FW-REQ-0250 |
| **Description:** | For every column, the firmware shall provide the clock signal to the DAC in charge of the SQUID SQ1 feedback. It shall be possible the enable and disable this clock signal with the command TBD of AD03. |
| **Type:** | 2 |
| **Status:** |  |
| **Higher level req.:** |  |
| **Verification level:** |  |
| **Verification method:** | Test |
| **Comment:** |  |

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| **Title:** | **SQ1 feedback: DAC sleep mode** |
| **Reference:** | DRE-DMX-FW-REQ-0260 |
| **Description:** | For every column, the firmware shall drive the sleep signal of the DAC in charge of the SQUID SQ1 feedback according to the command TBD of AD03. |
| **Type:** | 2 |
| **Status:** |  |
| **Higher level req.:** |  |
| **Verification level:** |  |
| **Verification method:** | Test |
| **Comment:** |  |

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| **Title:** | **SQ1 feedback: frequency of the DAC** |
| **Reference:** | DRE-DMX-FW-REQ-0270 |
| **Description:** | The frequency of the DACs in charge of the production of the SQ1 feedback signals shall be equal to:  C\_CLK\_DAC\_FREQ = C\_CLK\_DAC\_MULT \* C\_CLK\_REF\_FREQ  with C\_CLK\_DAC\_MULT = 2 (TBC) |
| **Type:** | 2 |
| **Status:** |  |
| **Higher level req.:** |  |
| **Verification level:** |  |
| **Verification method:** | Test |
| **Comment:** | The baseline is C\_CLK\_DAC\_FREQ = 120 MHz  Such a high frequency is mandatory to apply the pulse shaping. |

|  |  |
| --- | --- |
| **Title:** | **SQ1 feedback: Fine timing correction** |
| **Reference:** | DRE-DMX-FW-REQ-0280 |
| **Description:** | For each column, the firmware shall have the ability to delay the SQ1 feedback signal by 0 to 31 periods of CLK\_DAC according to the command CX\_FB\_SQ1\_DELAY of AD03 (X is the column number). |
| **Type:** | 2 |
| **Status:** |  |
| **Higher level req.:** |  |
| **Verification level:** |  |
| **Verification method:** | Test |
| **Comment:** | Compensation of analog propagation delays.  Only positive delays need to be considered. Negative shifts are obtained by delaying the row address signals in the row address and synchronization module. |

## SQ2 feedback requirements

These requirements are specific to the handling of the feedback signal for the AMP SQUID (MUX SQUID offset compensation).

|  |  |
| --- | --- |
| **Title:** | **SQ2 feedback: delivery of an offset compensation feedback per column** |
| **Reference:** | DRE-DMX-FW-REQ-0290 |
| **Description:** | For every column the firmware shall deliver a 16-bit (TBC) column offset feedback for the AMP SQUID:  SQ2\_FB\_column(column) |
| **Type:** | 2 |
| **Status:** |  |
| **Higher level req.:** |  |
| **Verification level:** |  |
| **Verification method:** | Test |
| **Comment:** | SQ2\_FB\_column(column) defines the position of the offset compensation range. This value is common for all the pixels. It is applied with a slow DAC. |

|  |  |
| --- | --- |
| **Title:** | **SQ2 feedback: delivery of an offset compensation feedback per pixel** |
| **Reference:** | DRE-DMX-FW-REQ-0300 |
| **Description:** | For every column, and sequentially for every pixel, the firmware shall deliver a 3-bit (TBC) pixel offset feedback:  SQ2\_FB\_pixel(column, pixel) |
| **Type:** | 2 |
| **Status:** |  |
| **Higher level req.:** |  |
| **Verification level:** |  |
| **Verification method:** | Test |
| **Comment:** | SQ2\_FB\_pixel(column, pixel) is the fine offset correction. This value is specific for each pixel. It is applied with a high-speed low-resolution DAC (high speed = C\_ROW\_FREQ). |

|  |  |
| --- | --- |
| **Title:** | **SQ2 feedback: Setting of the offset compensation feedback per column** |
| **Reference:** | DRE-DMX-FW-REQ-0310 |
| **Description:** | For every column, the common offset compensation feedback value (SQ2\_FB\_column) shall be configurable by the command TBD of AD03 (X is the column number) between TBD and TBD, with a resolution TBD. |
| **Type:** | 2 |
| **Status:** |  |
| **Higher level req.:** |  |
| **Verification level:** |  |
| **Verification method:** | Test |
| **Comment:** |  |

|  |  |
| --- | --- |
| **Title:** | **SQ2 feedback: Setting of the offset compensation feedback per pixel** |
| **Reference:** | DRE-DMX-FW-REQ-0320 |
| **Description:** | For every column and every pixel, the pixel specific offset compensation feedback values (SQ2\_FB\_pixel) shall be configurable by the command CX\_SQ2\_PXL\_LOCKPOINT of AD03 (X is the column number) between TBD and TBD, with a resolution TBD. |
| **Type:** | 2 |
| **Status:** |  |
| **Higher level req.:** |  |
| **Verification level:** |  |
| **Verification method:** | Test |
| **Comment:** |  |

|  |  |
| --- | --- |
| **Title:** | **SQ2 feedback: mode selection** |
| **Reference:** | DRE-DMX-FW-REQ-330 |
| **Description:** | For each column, it shall be possible to configure the SQ2 feedback mode with the command SQ2\_FB\_MODE of AD03 to:  - Off: 0  - Offset correction: Offset feedback of each pixel sequentially  - Test: Test pattern |
| **Type:** | 2 |
| **Status:** |  |
| **Higher level req.:** |  |
| **Verification level:** |  |
| **Verification method:** | Test |
| **Comment:** |  |

|  |  |
| --- | --- |
| **Title:** | **SQ2 feedback: Reference of the slow DAC** |
| **Reference:** | DRE-DMX-FW-REQ-0340 |
| **Description:** | For each column, the firmware shall drive a DAC DAC121S101 to output the column specific offset compensation feedback signal for the SQUID SQ2. |
| **Type:** | 2 |
| **Status:** |  |
| **Higher level req.:** |  |
| **Verification level:** |  |
| **Verification method:** | Test |
| **Comment:** |  |

|  |  |
| --- | --- |
| **Title:** | **SQ2 feedback: Driving the slow DAC** |
| **Reference:** | DRE-DMX-FW-REQ-0350 |
| **Description:** | The firmware shall provide the serial link clock to the DACs in charge of the column specific offset compensation feedback signal. A single FPGA output will be driven to the slow DACs of the different detection chains.  The firmware shall provide a SYNC signal to each slow DAC. |
| **Type:** | 2 |
| **Status:** |  |
| **Higher level req.:** |  |
| **Verification level:** |  |
| **Verification method:** | Test |
| **Comment:** |  |

|  |  |
| --- | --- |
| **Title:** | **SQ2 feedback: Reference of the fast DAC** |
| **Reference:** | DRE-DMX-FW-REQ-0360 |
| **Description:** | For each column, the firmware shall drive a custom 3-bit DAC to output the pixel specific offset compensation feedback signal for the SQUID SQ2. |
| **Type:** | 2 |
| **Status:** |  |
| **Higher level req.:** |  |
| **Verification level:** |  |
| **Verification method:** | Test |
| **Comment:** | The custom 3-bit DAC is a R2R network which requires a 3-bit command from the FPGA and no clock. |

|  |  |
| --- | --- |
| **Title:** | **SQ2 feedback: Rate of the fast DAC** |
| **Reference:** | DRE-DMX-FW-REQ-0370 |
| **Description:** | The FPGA shall maintain the value of the offset compensation feedback of the first C\_MUX\_FACT-1 pixels during 1/C\_ROW\_FREQ  The duration allocated to the last pixel depends on SYNC signal. |
| **Type:** | 2 |
| **Status:** |  |
| **Higher level req.:** |  |
| **Verification level:** |  |
| **Verification method:** | Test |
| **Comment:** |  |

|  |  |
| --- | --- |
| **Title:** | **SQ2 feedback: Fine timing correction** |
| **Reference:** | DRE-DMX-FW-REQ-0380 |
| **Description:** | For each column, the firmware shall have the ability to delay the SQ2 offset compensation feedback signal by 0 to 31 periods of CLK\_DAC according to the command CX\_FB\_SQ2\_DELAY of AD03 (X is the column number). |
| **Type:** | 2 |
| **Status:** |  |
| **Higher level req.:** |  |
| **Verification level:** |  |
| **Verification method:** | Test |
| **Comment:** | Only positive delays need to be considered. Negative shifts are obtained by delaying the row address signals in the row address and synchronization module. |

## Science data requirements

These requirements are specific to the computation of the science data.

|  |  |
| --- | --- |
| **Title:** | **Science data in closed loop mode** |
| **Reference:** | DRE-DMX-FW-REQ-0390 |
| **Description:** | For each column, each frame and sequentially for each pixel, the firmware shall compute the science data over 16 bits (unsigned int format) according to the following formula:  SC(p, n) = [FB(p, n) – FB(p, lp)] + kmix(p).[E(p, n) – E(p, lp)]  p is the pixel index, n is the frame index  E(p, lp) is the value of the error signal for pixel p at lock point  FB(p, lp) is the value of the feedback signal of pixel p at lock point |
| **Type:** | 2 |
| **Status:** |  |
| **Higher level req.:** |  |
| **Verification level:** |  |
| **Verification method:** | Test |
| **Comment:** |  |

## Auto-relock requirements

Because of the SQUID characteristic periodicity, the DRE measures the SQUID flux modulo Φ0. According to the slope of the characteristic at the lock point (the SQUID can be operated in the “falling” or in the “rising” slope) a positive or a negative feedback is applied to shift the operating point back to the initial lock position. If the skew rate of the input signal is too high the feedback loop may converge to a secondary lock point of the SQUID characteristic one (or even more) Φ0 away from the initial lock point. This should be avoided because, in this case, the steady state of the feedback signal is far from *IFB*=0 and this is an issue with respect to the dissipation at the 50 mK stage. The delock of the TDM feedback is explained in RD02 section 8.3.1 and in Figure 7.

The following requirements are specific to the auto-relock functionality.

|  |  |
| --- | --- |
|  | Figure 7: Illustration of the TDM delock in the case of a lock point in the SQUID “falling slope”. During normal operations the skew rate at SQUID input is such that the feedback loop converges to the initial lock point. This is illustrated by the feedback “*FB1*” which corrects the error “*E1*” and brings the SQUID back to its lock point. For too high skew rates (in the case of energies above the X-IFU energy range for example) the error can cross the *Vlock* level. In this case the feedback loop converges on another lock point k.Φ0 away from the initial lock point (k=1 in this plot for *E2* and *FB2*). |

|  |  |
| --- | --- |
|  | Figure 8:  Relock process. |

|  |  |
| --- | --- |
| **Title:** | **Auto-relock** |
| **Reference:** | DRE-DMX-FW-REQ-0400 |
| **Description:** | For every column and every pixel, if the SQUID remains too far from its lock point (i.e. FB(p, n) - FB(p, lp) > FB\_THRESHOLD) during too long (i.e. delay higher than RELOCK\_DELAY) the firmware shall reset FB(p, n) and E(p, n) to their lock point values (respectively FB(p, lp) and E(p, lp)). |
| **Type:** | 2 |
| **Status:** |  |
| **Higher level req.:** |  |
| **Verification level:** |  |
| **Verification method:** | Test |
| **Comment:** | See Figure 8 |

|  |  |
| --- | --- |
| **Title:** | **Relock delay** |
| **Reference:** | DRE-DMX-FW-REQ-0410 |
| **Description:** | For every column, the parameter RELOCK\_DELAY shall be configurable with the command CX\_RELOCK\_DELAY of AD03 (X is the column number) between TBD and TBD with a resolution TBD. |
| **Type:** | 2 |
| **Status:** |  |
| **Higher level req.:** |  |
| **Verification level:** |  |
| **Verification method:** | Test |
| **Comment:** | See Figure 8 |

|  |  |
| --- | --- |
| **Title:** | **Feedback Threshold** |
| **Reference:** | DRE-DMX-FW-REQ-0420 |
| **Description:** | For every column, the parameter FB\_THRESHOLD shall be configurable with the command CX\_RELOCK\_THRESHOLD of AD03 (X is the column number) between TBD and TBD with a resolution TBD. |
| **Type:** | 2 |
| **Status:** |  |
| **Higher level req.:** |  |
| **Verification level:** |  |
| **Verification method:** | Test |
| **Comment:** | See Figure 8 |

|  |  |
| --- | --- |
| **Title:** | **Delock monitoring** |
| **Reference:** | DRE-DMX-FW-REQ-0430 |
| **Description:** | The firmware shall monitor the number of Auto-relocks PIX\_RELOCK\_NB for each pixel and report these values in the housekeeping. The number of bits allocated to these counters is 4 bits (TBC). |
| **Type:** | 2 |
| **Status:** |  |
| **Higher level req.:** |  |
| **Verification level:** |  |
| **Verification method:** | Test |
| **Comment:** | Shall we count the delocks per pixel or per column ?  We believe that a 4 bit counter is enough. i.e. count from 0 to 14 and 15 means “15 delocks or more”. It this OK ? |

## Diagnostic function requirements

Specific diagnostic functions are needed in order to characterize the detection chain and to define the optimal configuration of the instrument. The following requirements are specific to these diagnostic functions.

|  |  |
| --- | --- |
| **Title:** | **SQ1 test patterns** |
| **Reference:** | DRE-DMX-FW-REQ-0440 |
| **Description:** | For each column, the firmware shall have the ability to load a test pattern for the SQ1 feedback output with the command SQ1\_TEST\_PATTERN of AD03. |
| **Type:** | 2 |
| **Status:** |  |
| **Higher level req.:** |  |
| **Verification level:** |  |
| **Verification method:** | Test |
| **Comment:** |  |

|  |  |
| --- | --- |
| **Title:** | **SQ2 test patterns** |
| **Reference:** | DRE-DMX-FW-REQ-0450 |
| **Description:** | For each column, the firmware shall have the ability to load a test pattern for the SQ1 feedback output with the command SQ2\_TEST\_PATTERN of AD03. |
| **Type:** | 2 |
| **Status:** |  |
| **Higher level req.:** |  |
| **Verification level:** |  |
| **Verification method:** | Test |
| **Comment:** |  |

|  |  |
| --- | --- |
| **Title:** | **TM test patterns** |
| **Reference:** | DRE-DMX-FW-REQ-0460 |
| **Description:** | The firmware shall have the ability to load a test pattern for the TM output with the command TM\_TEST\_PATTERN of AD03. |
| **Type:** | 2 |
| **Status:** |  |
| **Higher level req.:** |  |
| **Verification level:** |  |
| **Verification method:** | Test |
| **Comment:** |  |

|  |  |
| --- | --- |
| **Title:** | **Loop gain characterization for SQ1 feedback signal** |
| **Reference:** | DRE-DMX-FW-REQ-0470 |
| **Description:** | For each column, the firmware shall have the ability to characterize the gain in the SQ1 feedback loop (i.e. ki). |
| **Type:** | 2 |
| **Status:** |  |
| **Higher level req.:** |  |
| **Verification level:** |  |
| **Verification method:** | Test |
| **Comment:** | The way to do it is still TBD. |

|  |  |
| --- | --- |
| **Title:** | **Loop delay characterization for SQ1 feedback signal** |
| **Reference:** | DRE-DMX-FW-REQ-0480 |
| **Description:** | For each column, the firmware shall have the ability to characterize the delay in the SQ1 feedback loop (i.e. delay between the SQ1 feedback signal at firmware output and the Error signal at firmware input). |
| **Type:** | 2 |
| **Status:** |  |
| **Higher level req.:** |  |
| **Verification level:** |  |
| **Verification method:** | Test |
| **Comment:** | The way to do it is still TBD.  If the functionalities needed for this measurement are already in the firmware requirements this requirement will become obsolete at firmware level. |

|  |  |
| --- | --- |
| **Title:** | **Loop delay characterization for SQ2 feedback signal** |
| **Reference:** | DRE-DMX-FW-REQ-0490 |
| **Description:** | For each column, the firmware shall have the ability to characterize the delay in the SQ2 feedback loop (i.e. delay between the SQ2 feedback signal at firmware output and the Error signal at firmware input). |
| **Type:** | 2 |
| **Status:** |  |
| **Higher level req.:** |  |
| **Verification level:** |  |
| **Verification method:** | Test |
| **Comment:** | The way to do it is still TBD.  If the functionalities needed for this measurement are already in the firmware requirements this requirement will become obsolete at firmware level. |

## Telecommands and housekeepings requirements

These requirements are specific to the management of the DEMUX telecommands and housekeepings management.

|  |  |
| --- | --- |
| **Title:** | **Telecommands** |
| **Reference:** | DRE-DMX-FW-REQ-0500 |
| **Description:** | The firmware shall receive its telecommands according to AD03 |
| **Type:** | 2 |
| **Status:** |  |
| **Higher level req.:** |  |
| **Verification level:** |  |
| **Verification method:** | Test |
| **Comment:** |  |

|  |  |
| --- | --- |
| **Title:** | **Analogue housekeepings and parameters readout** |
| **Reference:** | DRE-DMX-FW-REQ-0510 |
| **Description:** | The firmware shall have the ability to transmit the values of the firmware parameters and of the digital and analogue housekeepings on request according to AD03. |
| **Type:** | 2 |
| **Status:** |  |
| **Higher level req.:** |  |
| **Verification level:** |  |
| **Verification method:** | Test |
| **Comment:** |  |

|  |  |
| --- | --- |
| **Title:** | **Firmware version** |
| **Reference:** | DRE-DMX-FW-REQ-0520 |
| **Description:** | The firmware shall embed its version number. This version number shall be part of the firmware parameters that can be readout in the housekeepings. |
| **Type:** | 2 |
| **Status:** |  |
| **Higher level req.:** |  |
| **Verification level:** |  |
| **Verification method:** | Test |
| **Comment:** |  |

|  |  |
| --- | --- |
| **Title:** | **DEMUX board id** |
| **Reference:** | DRE-DMX-FW-REQ-0530 |
| **Description:** | The firmware shall read from the board a TBD-bit identifier. This board identifier shall be part of the firmware parameters that can be readout in the housekeepings. |
| **Type:** | 2 |
| **Status:** |  |
| **Higher level req.:** |  |
| **Verification level:** |  |
| **Verification method:** | Test |
| **Comment:** |  |

|  |  |
| --- | --- |
| **Title:** | **Analogue housekeepings: measurements** |
| **Reference:** | DRE-DMX-FW-REQ-0540 |
| **Description:** | The firmware shall continuously measure its analogue housekeepings. The measurements shall be stored in a memory to allow a readout on request. |
| **Type:** | 2 |
| **Status:** |  |
| **Higher level req.:** |  |
| **Verification level:** |  |
| **Verification method:** | Test |
| **Comment:** |  |

|  |  |
| --- | --- |
| **Title:** | **Analogue housekeepings: reference of the ADC** |
| **Reference:** | DRE-DMX-FW-REQ-0550 |
| **Description:** | The firmware shall drive an ADC (ref ADC128S102) to do the acquisition of the analogue housekeepings. |
| **Type:** | 2 |
| **Status:** |  |
| **Higher level req.:** |  |
| **Verification level:** |  |
| **Verification method:** | Test |
| **Comment:** |  |

|  |  |
| --- | --- |
| **Title:** | **Analogue housekeepings: reference of the analogue multiplexer** |
| **Reference:** | DRE-DMX-FW-REQ-0560 |
| **Description:** | The firmware shall drive an analogue multiplexer (ref 74HC4051) to do the acquisition of the analogue housekeepings. |
| **Type:** | 2 |
| **Status:** |  |
| **Higher level req.:** |  |
| **Verification level:** |  |
| **Verification method:** | Test |
| **Comment:** |  |

|  |  |
| --- | --- |
| **Title:** | **Analogue housekeepings: update rate** |
| **Reference:** | DRE-DMX-FW-REQ-0570 |
| **Description:** | The update rate of each analogue HK shall be higher than 10 samples per second. |
| **Type:** | 2 |
| **Status:** |  |
| **Higher level req.:** |  |
| **Verification level:** |  |
| **Verification method:** | Test |
| **Comment:** |  |

## Science data telemetry requirements

The TM link between the TDM firmware and the EP shall optimize the number of wires with an acceptable signal frequency (i.e. lower than 100 MHz). With 4 columns per FPGA, 34 pixels per columns, 16 bits per value and a sampling rate of about 150 Ksps, the data rate at the firmware output is 340 Mbits/s. 8 serial lines are needed to reduce the data rate per line below 100 Msps. The interface is handled with the following signals (see details on Figure 10 and Table 15):

* A clock (CLK)
* A control line (CTRL)
* 8 data lines

|  |  |
| --- | --- |
| **Title:** | **Telemetry: mode selection** |
| **Reference:** | DRE-DMX-FW-REQ-0580 |
| **Description:** | It shall be possible to configure the TM mode with the command TM\_MODE of AD03 to:  - Dump: ADC values of the four columns sampled at C\_CLK\_ADC\_FREQ during two frames. The record shall be synchronized with the SYNC signal.  - Open loop: Averaged error of all pixels sampled at C\_ROW\_FREQ  - Closed loop: SC(p, n) of all pixels at the rate C\_ROW\_FREQ  - Test: Test pattern |
| **Type:** | 2 |
| **Status:** |  |
| **Higher level req.:** |  |
| **Verification level:** |  |
| **Verification method:** | Test |
| **Comment:** | Is a duration of 2 frames long enough for the dumps ? |

|  |  |
| --- | --- |
| **Title:** | **Telemetry: Transfer of science data** |
| **Reference:** | DRE-DMX-FW-REQ-0590 |
| **Description:** | The firmware shall transmit the science data according to the protocol described in Figure 8 and Table 15. |
| **Type:** | 2 |
| **Status:** |  |
| **Higher level req.:** |  |
| **Verification level:** |  |
| **Verification method:** | Test |
| **Comment:** |  |

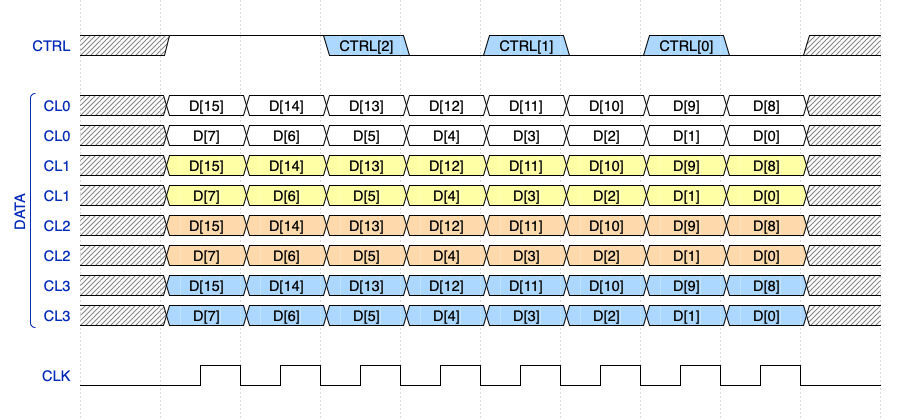


Figure 8: TM protocol for the transmission of science data. Each pair of lines is dedicated to a column.

Table 15: Description of TM control parameter (CTRL).

|  |  |  |
| --- | --- | --- |
| CTRL |  | Type of Data |
| 000 | DAT | DATA word |
| 001 |  | First word of science data packet |
| 010 |  | First word of ADC Col0 dump packet |
| 011 |  | First word of ADC Col1 dump packet |
| 100 |  | First word of ADC Col2 dump packet |
| 101 |  | First word of ADC Col3 dump packet |
| 110 |  | First word of test pattern data packet |
| 111 | EOD | End of data |

# Appendix A – Pin allocation