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| **DRE TDM firmware requirements** |

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| **Concerned Models** | **BB** |  | **DM** |  | **EM** |  | **STM** |  | **QM** |  | **FM** |  | **FS** |  | **All** |  |

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| **Summary** |  |
| **Annexes** |  |

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| 0.5 | 31/05/2021 | / | Updated accorded to RIDs from Sylvain  Document template updated |
| 0.4 | 14/01/2021 | / | Update of req. format |
| 0.3 | 08/01/2021 | / | Fully updated |
| 0.2 | 17/08/2020 | / | After Yann’s comments |
| 0.1 | 15/06/2020 | / | First issue |

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| **Applicable Documents (AD)** | | | |
| **AD** | **Title** | **Reference** | **Version** |
| **AD01** | XIFU DRE requirements document | XIFU-RD-13200-00420-CNES | 2.0 |
| **AD02** | Design and VHDL handbook for VLSI development, CNES Edition |  | 2.1 |
| **AD03** | DRE Inter-Modules Telemetry And Commands Definition | IRAP/XIFU-DRE/FM/SP/0069 |  |

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| **Reference Documents (RD)** | | | |
| **RD** | **Title** | **Reference** | **Version** |
| **RD01** | Transition edge sensors | Irwin and Hilton 2005 |  |
| **RD02** | XIFU TDM detection chain definition document | XIFU-DD-10000-00422-CNES | 1 |
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| **List of Abbreviations** | | | |
| **ADC** | **A**nalogue to **D**igital **C**onverter | **SQUID** | **S**uperconducting **QU**antum **I**nterference **D**evice |
| **AMP SQUID** | **AMP**lifier **SQUID** | **TDM** | **T**ime **D**omain **M**ultiplexing |
| **DAC** | **D**igital to **A**nalogue **C**onverter | **TES** | **T**ransition **E**dge **S**ensor |
| **FPGA** | **F**ield **P**rogrammable **G**ate **A**rray | **TC** | **T**ele**C**ommands |
| **HK** | **H**ouse**K**eepings | **TM** | **T**ele**M**etry |
| **MUX SQUID** | **MU**ltiple**X**er **SQUID** |  |  |

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# INTRODUCTION

## Scope of the document

This document defines the requirements of the firmware which drives the Time Domain Multiplexed (TDM) readout of the detector array onboard Athena X-IFU.

## Description of the X-IFU and the DRE

Athena is designed to implement the Hot and Energetic Universe science theme selected by the European Space Agency for the second large mission of its Cosmic Vision program. The Athena science payload consists of a large aperture high angular resolution X-ray optics and twelve meters away, two interchangeable focal plane instruments: The X-ray Integral Field Unit (X-IFU) and the Wide Field Imager. The X-IFU is a cryogenic X-ray spectrometer, based on a large array of Transition Edge Sensors (TES) micro-calorimeters operated at 90 mK and offering a 2.5 eV spectral resolution.

In the X-IFU, the "Digital Readout Electronics" (DRE) drives the TDM readout of the 3168 superconducting TES of the detector array. For this, it reads the TES current measured by the instrument amplification chain (MUX SQUIDs, AMP SQUIDS and LNA) and it linearizes the entire detection chain with an active feedback loop. The DRE performs both, analogue and digital signal processing (A/D and D/A conversion, analogue filtering, digital filtering, feedback management...). The digital processing is done by the firmware of the DRE-DEMUX.

## The Time Domain Multiplexing (TDM)

In order to readout the 3168 TES of the X-IFU Focal Plan Array (FPA) a multiplexed readout technique is mandatory. For the X-IFU a Time Domain Multiplexing (TDM) method is used. The FPA is arranged in 96 detection chains (so-called “columns”) of 34 pixels (see Figure 1). The pixels of a columns are readout sequentially. This sequence is called “a frame”.

Each TES pixel (which is equivalent to a resistor) is biased with a DC-voltage provided by the WFEE. The detection of an X-ray photon changes the TES resistance and modulates its current at a low frequency (in the kHz range). In each detection chain a column of SQUIDs (so-called MUX SQUIDs or SQUIDs SQ1) reads sequentially the current of the TESs. The MUX SQUID addressing is driven by rows. For redundancy reasons it is common to 16 columns.

Each detection chain includes a “blind” TES for calibration purposes. The MUX SQUID output is amplified by a second stage SQUID (so-called AMP SQUID or SQUID SQ2) and a low noise amplifier in the WFEE. From this signal the DRE-DEMUX shall derive:

* A feedback to be applied at the MUX SQUID in order to linearize the detection chain. The feedback to be applied to the MUX SQUID to readout a pixel is derived from the value that has been readout at the previous frame.
* The measurement of the TES current.

The DRE shall apply a feedback to the AMP SQUID in order to compensate for the SQ1 offset variations across the column.

Details about the TDM technique can be found in RD02 section 3.1.

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| Figure 1: TDM cold front-end electronics with the TES, the FAS and the MUX SQUIDs. |

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| Figure 2: TDM detection chain with a focus on the AMP SQUIDs, the WFEE and the DRE. |

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| Figure 3: Diagram of the detection chain with a focus on the DRE functionalities. |

# Format of the requirements

In this document the requirements have the following format:

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| **Title:** | **Title of the requirement** |
| **Reference:** | Reference of the requirement as follows: DRE-DMX-FW-REQ-XXXX.  Where:  - DRE-DMX-FW defines the applicability of the requirement:  DRE (DRE) |  |> DEMUX (DMX) |  |> Firmware (FW)  - REQ stands for ‘requirement’  - XXXX is a four-digit number aiming to define a specific reference for each requirement. |
| **Description:** | Short, clear, unambiguous description of the requirement. |
| **Type:** | Type of requirement (number or full text):   * 1=Informational * 2=Feature * 3=Use Case * 4=User Interface * 5=Non Functional * 6=Constraint * 7=System Function |
| **Status:** | Status of the requirement (First letter or full text):   * D=Draft * R=Review * W=Rework * F=Finish * I= Implemented * V=Valid * N=Non Testable * O=Obsolete |
| **Higher level req.:** | Reference of the higher-level requirement which implies this one. |
| **Verification level:** | At which level of the integration flow will it be possible to verify this requirement? |
| **Verification method:** | What will be the verification methods:   * Analysis * Tests * Review of design |
| **Comment:** | Complementary description if needed. |

# Requirements

## General requirements

These requirements are design constraints for the FPGA.

|  |  |
| --- | --- |
| **Title:** | **Host FPGA** |
| **Reference:** | DRE-DMX-FW-REQ-0010 |
| **Description:** | The firmware shall be operated on a NG-Large FPGA (ref. NX1H140TSP). |
| **Type:** | Constraint |
| **Status:** | Valid |
| **Higher level req.:** |  |
| **Verification level:** |  |
| **Verification method:** | Review of design |
| **Comment:** |  |

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| --- | --- |
| **Title:** | **CNES VHDL handbook** |
| **Reference:** | DRE-DMX-FW-REQ-0020 |
| **Description:** | The firmware shall be compliant with the design and VHDL handbook for VLSI developments, CNES edition, (AD02) |
| **Type:** | Constraint |
| **Status:** | Valid |
| **Higher level req.:** |  |
| **Verification level:** |  |
| **Verification method:** | Review of design |
| **Comment:** |  |

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| **Title:** | **Testability** |
| **Reference:** | DRE-DMX-FW-REQ-0030 |
| **Description:** | TBD |
| **Type:** | Non Functional |
| **Status:** | Valid |
| **Higher level req.:** |  |
| **Verification level:** |  |
| **Verification method:** | Review of design |
| **Comment:** |  |

## System requirements

These requirements are high level requirements for the firmware.

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| **Title:** | **External reference clock** |
| **Reference:** | DRE-DMX-FW-REQ-0040 |
| **Description:** | The firmware shall use an external reference clock CLK\_REF whose frequency C\_CLK\_REF\_FREQ is equal to 60 MHz ±TBD ppm (TBD). |
| **Type:** | Feature |
| **Status:** | Valid |
| **Higher level req.:** |  |
| **Verification level:** |  |
| **Verification method:** | Review of design |
| **Comment:** | The external reference clock is provided by the row address module. |

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| **Title:** | **Asynchronous reset** |
| **Reference:** | DRE-DMX-FW-REQ-0050 |
| **Description:** | An asynchronous reset, activated on '0' logical level, shall be available on a FPGA input for the internal reset(s) generation. |
| **Type:** | Feature |
| **Status:** | Valid |
| **Higher level req.:** |  |
| **Verification level:** |  |
| **Verification method:** | Review of design |
| **Comment:** |  |

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| **Title:** | **Pin allocation** |
| **Reference:** | DRE-DMX-FW-REQ-0060 |
| **Description:** | The FPGA pin allocation shall be as defined in Appendix A – Pin allocation |
| **Type:** | Feature |
| **Status:** | Valid |
| **Higher level req.:** |  |
| **Verification level:** |  |
| **Verification method:** | Review of design |
| **Comment:** |  |

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| **Title:** | **Number of columns** |
| **Reference:** | DRE-DMX-FW-REQ-0070 |
| **Description:** | The firmware shall process a number of columns C\_NB\_COL = 4 |
| **Type:** | Feature |
| **Status:** | Valid |
| **Higher level req.:** |  |
| **Verification level:** |  |
| **Verification method:** | Test |
| **Comment:** | A column is equivalent to a detection chain. |

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| **Title:** | **Multiplexing factor** |
| **Reference:** | DRE-DMX-FW-REQ-0080 |
| **Description:** | The firmware shall apply a multiplexing factor C\_MUX\_FACT = 34. |
| **Type:** | Feature |
| **Status:** | Valid |
| **Higher level req.:** |  |
| **Verification level:** |  |
| **Verification method:** | Test |
| **Comment:** | The multiplexing factor is the number of pixels per column. Among the 34 pixels to be processed by the firmware, 33 are “science” pixels and one is used for calibration purposes. |

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| **Title:** | **Readout synchronization** |
| **Reference:** | DRE-DMX-FW-REQ-0090 |
| **Description:** | The firmware shall synchronize the pixel sequence processing with an external synchronization signal (SYNC). A rising edge of SYNC indicates that the next pixel to be processed is pixel 1. Afterward the pixels are processed sequentially from 1 to C\_MUX\_FACT. |
| **Type:** | Feature |
| **Status:** | Valid |
| **Higher level req.:** |  |
| **Verification level:** |  |
| **Verification method:** | Test |
| **Comment:** | The SYNC signal is provided by the row address and synchronization module to the DEMUX modules. It lasts at least one period of CLK\_REF and its frequency is:  C\_FRAME\_FREQ = C\_ROW\_FREQ / C\_MUX\_FACT |

## Error signal requirements

These requirements are specific to the handling of the TDM error signal.

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| **Title:** | **Error signal: Reference of the ADC** |
| **Reference:** | DRE-DMX-FW-REQ-0100 |
| **Description:** | For each column, the firmware shall drive an ADC AD9254S to do the acquisition of the error signal from the detection chain |
| **Type:** | Feature |
| **Status:** | Valid |
| **Higher level req.:** |  |
| **Verification level:** |  |
| **Verification method:** | Test |
| **Comment:** |  |

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| **Title:** | **Error signal: Clock for the ADC** |
| **Reference:** | DRE-DMX-FW-REQ-0110 |
| **Description:** | For every column, the firmware shall provide the clock signal to the ADC in charge of the acquisition of the error. It shall be possible the enable and disable this clock signal with the command TBD of AD03. |
| **Type:** | Feature |
| **Status:** | Valid |
| **Higher level req.:** |  |
| **Verification level:** |  |
| **Verification method:** | Test |
| **Comment:** |  |

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| **Title:** | **Error signal: Sampling frequency of the ADC** |
| **Reference:** | DRE-DMX-FW-REQ-0120 |
| **Description:** | The sampling frequency of the ADCs in charge of the acquisition of the error signals shall be equal to:  C\_CLK\_ADC\_FREQ = C\_CLK\_ADC\_MULT \* C\_CLK\_REF\_FREQ  with C\_CLK\_ADC\_MULT = 2 (TBC) |
| **Type:** | Feature |
| **Status:** | Valid |
| **Higher level req.:** |  |
| **Verification level:** |  |
| **Verification method:** | Test |
| **Comment:** | The baseline is C\_CLK\_ADC\_FREQ = 120 MHz |

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| **Title:** | **Time allocation for pixel acquisition** |
| **Reference:** | DRE-DMX-FW-REQ-0130 |
| **Description:** | The number of ADC clock cycles allocated to the acquisition of the C\_MUX\_FACT-1 pixels shall be C\_PIXEL\_ADC\_NB\_CYC = XXX. |
| **Type:** | Feature |
| **Status:** | Valid |
| **Higher level req.:** |  |
| **Verification level:** |  |
| **Verification method:** | Test |
| **Comment:** | The duration allocated to the first C\_MUX\_FACT-1 pixels is:  1/C\_ROW\_FREQ = C\_PIXEL\_ADC\_NB\_CYC / C\_CLK\_ADC\_FREQ  With:  C\_CLK\_ADC\_FREQ=120 MHz (TBC)  C\_PIXEL\_ADC\_NB\_CYC = TBD between 18 and 22  C\_ROW\_FREQ = TBD between 6.67 MHz and 5.45 MHz  The duration allocated to the last pixel depends on SYNC signal. |

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| **Title:** | **Error signal: Boxcar filter** |
| **Reference:** | DRE-DMX-FW-REQ-0140 |
| **Description:** | The firmware shall compute one value of the error signal per pixel by averaging ADC\_BOXCAR\_NB\_CYC consecutive ADC values. ADC\_BOXCAR\_NB\_CYC shall be tunable between 1 and 32 with the command TBD of AD03. |
| **Type:** | Feature |
| **Status:** | Valid |
| **Higher level req.:** |  |
| **Verification level:** |  |
| **Verification method:** | Test |
| **Comment:** |  |

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| **Title:** | **Error signal: Fine timing correction** |
| **Reference:** | DRE-DMX-FW-REQ-0150 |
| **Description:** | For each column, the firmware shall have the ability to select which ADC data shall be used to compute the average by applying a delay ADC\_DELAY\_NB\_CYC to the input signal. ADC\_DELAY\_NB\_CYC shall be tunable between 0 and 31 periods of CLK\_ADC according to the command CX\_SAMPLING\_DELAY of AD03 (X is the column number). |
| **Type:** | Feature |
| **Status:** | Valid |
| **Higher level req.:** |  |
| **Verification level:** |  |
| **Verification method:** | Test |
| **Comment:** |  |

Figure 4: Timings of error signal input. Timings a to b and a to c depend on the environment of the firmware, they may change. Once these timings are characterized, ADC\_DELAY\_NB\_CYC (between labels b and d) is used to align the valid data with the boxcar sequence. ADC\_BOXCAR\_NB\_CYC is the width of the boxcar.