Design of a Low-Noise, High Power Efficiency Neural Recording Front-end With an Integrated Real-Time Compressed Sensing Unit

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***Abstract*—This paper presents a 12-channel, low-power, high efficiency neural signal acquisition front-end for local field potential and action potential signals recording. The proposed neural front-end integrates low noise instrumentation amplifiers, low-power filter stages with configurable gain and cut-off frequencies, a successive approximation register (SAR) ADC, and a real-time compressed sensing processing unit. A capacitor coupled instrumentation amplifier integrated input impedance boosting has been designed, dissipating 1μA quiescent current. An input referred noise of 1.63μV was measured in the frequency band of 1Hz to 7kHz. The noise efficiency factor (NEF) of the amplifier is 0.76. The SAR ADC achieves an ENOB of 10.6-bit at a sampling rate of 1MS/s. A compressed sensing processing unit with configurable compression ratio, up to 8x, was integrated in the design. The design has been fabricated in 180nm CMOS, occupying 4.5mm$\times$1.5mm silicon area. A portable neural recorder has been built with the custom IC and a commercial low-power wireless module. A 4.6g lithium battery supports the device for a continuous compressed sensing recording up to 70 hours.**

***Index Terms*—Neural amplifier, high noise efficiency, compressed sensing, SAR ADC.**

I. Introduction

Simultaneously recording of large-scale brain activities down to the multi-unit level revolutionizes our understanding of the human brain [1]. The recording of high bandwidth neural signals (eg. local field potential, action potentials, etc.) in a multiple channels microelectrode array places a big challenge in existing electronic technology and design techniques in terms of instrumentation noise, power, data transmission and storage. Thus a low-noise, high efficiency neural recording front-end design is needed.

The physiological information is presented in a neural signal in terms of dynamic range and bandwidth. First, the dynamic range of a signal recording system is determined by the maximum presentable signal and the system noise. In the design of a portable neural recorder, the maximum signal swing is restricted by the low supply voltage from a battery, or recovered from the wireless transmission. On the other hand, the noise origins from the electrode-tissue interface, the environmental interference, and semiconductor devices (thermal, flicker noises, etc.). In addition, the high impedance and mismatch from the microelectrode array raises the requirement of the input impedance and common mode rejection (CMR) capability of the analog front-end circuits. A poor CMR often results in a waste of dynamic range in common mode interference. Secondly, the bandwidth requirement of a recording system is determined by the maximum frequency presented in the signal according to Nyquist-Shannon sampling theorem. Data compression techniques can be used to reduce the bandwidth of the digitized data. On-chip real-time data compression is widely used to reduce the power consumption on the wireless data transmission.

In the design of a neural recording front-end, the circuits need to meet the dynamic range and bandwidth requirement of the neural signal. Low power, low noise neural front-end designs have been reported in literature [2–4, 7], as well as data compression implemented in hardware [5, 6, 8–10]. In this paper, we present the design of a neural recording front-end, with emphasis on the noise and power efficiency optimization. An instrumentation amplifier has been optimized for a low noise efficiency factor (NEF), achieving a noise floor in a power efficiency close to the limitation in theory. An on-chip compressed sensing unit is used to reduce the data rate down to 1/8 of the Nyquist sampling rate without greatly sacrificing the quality of the original signal. A wireless portable neural recorder was implemented using the proposed neural front-end and commercial low-power wireless transceiver.

The paper is organized as follows. Section II presents the architecture of the neural front-end, including the instrumentation amplifier, the successive approximation register (SAR) ADC, and the compressed sensing digital processing unit. Section III shows the measurement results, while section IV concludes the paper.

II. Design of The Neural Recording Front-end

A. System Overview

The architecture of the proposed neural recording front-end is illustrated in Fig. 1. The system consists of 12-channel instrumentation amplifiers, bandpass filters with programmable gain and cut-off frequencies, a 12-bit SAR ADC, and a compressed sensing digital processing unit. A portable wireless neural recorder is built using the proposed IC and a commercial low power wireless transceiver. The digitized data is transmitted wirelessly to a computer host. The computer reconstructs the neural signal.

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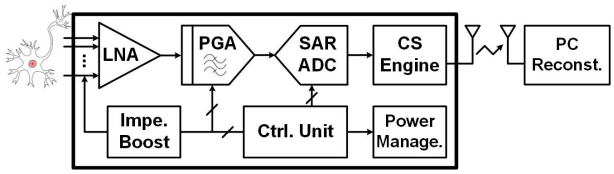

Fig. 1. The block diagram of the proposed neural front-end. A wireless portable neural recorder was built using the neural front-end IC and off-chip transmitter.

B. Design of The Noise Efficient Amplifier

Fig. 2(a) shows the circuit schematic of the fully differential, capacitor coupled instrumentation amplifier implemented in this work. The input capacitors block the electrode offset and the half-cell potential from the electrode-tissue interface. The closed-loop differential gain is set to be 40dB to relieve the noise requirement for the following stages. Positive current feedback [4] is used to boost the input impedance, which reduces the signal attenuation due to the high impedance electrode, and the mismatch between the signal and reference electrodes.

The circuit schematic of the operational transconductance amplifier (OTA) is shown in Fig. 2(b). The OTA has been designed to maximize the noise and power efficiency. A single-stage amplifier with a high gain is used to avoid the stability compensation in two-stage structures, thus a high transconductance (g_m) is required. Three methods have been used in this design to improve the power efficiency (g_m/I_{tot}): i) a complementary input stage (M1-M4) is used to increase the overall transconductance without increasing the quiescent current. All the input transistors are biased in the sub-threshold region to achieve a high efficiency [7]; ii) cascode transistors (M5-M8) are used to increase the voltage gain, as well as to reduce the equivalent input capacitance that origins from the Miller effect of the input transistors' drain to gate capacitance; iii) common mode feedback (CMFB) loop is merged in the main current path to further reduce the total current. Simulation shows an open loop gain of 90dB is achieved in this OTA under 1μA.

The total input referred noise power of the OTA can be expressed as

$$\overline{v_{i,n,tot}^2} = \frac{1}{(g_{m1}+g_{m3})^2}[8KT\gamma(g_{m1}+g_{m3})+ 2(\frac{K_N g_{m3}}{C_{ox,N} f W_N L_N}+\frac{K_P g_{m1}}{C_{ox,P} f W_P L_P})]\Delta f \quad (1)$$

where gm1 (=gm2) are the transconductance of M1 (M2), and gm3 (=gm4) are the transconductance of M3 (M4). The flicker noise can be reduced by increasing the width and length of the input transistors, but resulting in a larger parasitic capacitance. If only thermal noise is considered in the following design optimization, the input referred noise voltage equals to

$$\overline{V_{i,n,rms}} = \sqrt{\frac{8kT\gamma}{gm_1+gm_3}\frac{\pi}{2}BW} \quad (2)$$

The noise efficiency factor (NEF) [3] for this amplifier can be derived using eq. (2):

$$\begin{aligned} NEF &= \overline{V_{i,n,rms}}\sqrt{\frac{2I_{tot}}{\pi\Phi_t\cdot 4kT\cdot BW}} \\ &= \sqrt{\frac{8kT\gamma}{gm_1+gm_3}\frac{\pi}{2}BW\frac{2I_{tot}}{\pi\Phi_t\cdot 4kT\cdot BW}} \\ &= \sqrt{\frac{2\gamma I_{tot}}{(gm_1+gm_3)\Phi_t}} \end{aligned} \quad (3)$$

Thus, a lower NEF can be expected if a higher power efficiency (g_m/I_{tot}) is achieved.

C. Successive Approximation Register Data Convertor

A 12-bit successive approximation register (SAR) analog-to-digital converter (ADC), featuring a conversion rate of 1MS/s, is implemented in this design for local data conversion. The architecture of the SAR ADC is as shown in Fig. 2(c). A capacitive charge sharing digital-to-analog converter (DAC) is integrated. The DAC is divided into two parts to reduce capacitor area and the power consumption. The 6 most significant bits (MSB) of the DAC is implemented with a 6-bit binary-weighted capacitor array. The 6 least significant bits (LSB) of the DAC is implemented with C-2C structured capacitor array, in which the capacitors are realized as dual layer metal-insulator-metal (MIM). According to simulations, the DAC achieves a linearity higher than 72dB. The sample and hold processing is implemented together with the capacitor array DAC, thus, no additional sampling capacitor is required. The DAC outputs the subtraction result of the input voltage and the weighted reference voltage. The comparator compares the DAC output with a constant common mode voltage, $V_{ref}/2$. This design reduces the circuit complexity since no wide common-mode input range comparator is needed.

D. Design of the Compressed Sensing Digital Processing Unit

Compressive sensing enables to sample signals at a rate lower than the Nyquist rate without greatly sacrificing the quality of the original signal. The digitized neural signal, D_{in}, output from the SAR ADC, of a single channel is feeded into the digital processing unit.

$$Y = \Phi D_{in} \quad (4)$$

which is

$$\begin{bmatrix} Y_0 \\ Y_1 \\ \vdots \\ Y_M \end{bmatrix} = \begin{bmatrix} \Phi_{11} & \Phi_{12} & \cdots & \Phi_{1N} \\ \Phi_{21} & \Phi_{22} & \cdots & \Phi_{2N} \\ \vdots & \vdots & \ddots & \vdots \\ \Phi_{M1} & \Phi_{M2} & \cdots & \Phi_{MN} \end{bmatrix} \begin{bmatrix} D_{in_0} \\ D_{in_1} \\ \vdots \\ D_{in_N} \end{bmatrix} \quad (5)$$

Eq. (6) can be rewritten in the form of a summary of vector multiplications

$$\begin{bmatrix} Y_0 \\ Y_1 \\ \vdots \\ Y_M \end{bmatrix} = \sum_{i=1}^{M} \left(\begin{bmatrix} \Phi_{1i} \\ \Phi_{2i} \\ \vdots \\ \Phi_{Mi} \end{bmatrix} D_{in_{i-1}} \right) \quad (6)$$

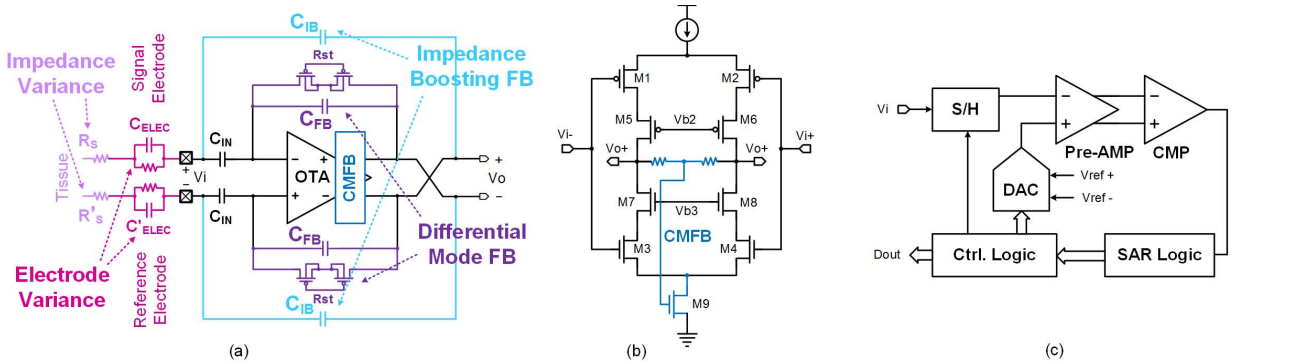

Fig. 2. Architecture of (a) the capacitor coupled instrumentation amplifier with impedance boosting, (b) the fully differential complementary input operational transconductance amplifier (OTA), and (c) the architecture of the 12-bit resolution successive approximation register (SAR) analog-to-digital converter (ADC).

The entries of the sampling matrix Φ are assigned to be equal to either 0 or ± 1. The compression ratio can be evaluated from $\frac{M}{N}$. In order to avoid large on-chip storage for the sampling matrix, a linear congruential pseudo random number generator is used to generate all the entries of the sampling matrix. Fig. 3 illustrates the block diagram of the compressive sensing processing unit. There are M vector multiplication units integrated in the system. The entries of Φ is randomly generated and used for the logic control inside of each vector multiplication unit. The output measurement Y is reset after every N iteration. The dimension of D_{in} is controlled by the iteration times. Parallel to serial convertor is integrated in the system for the readout of the measurements.

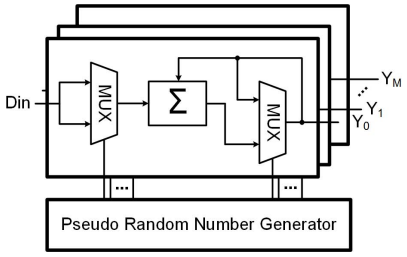

Fig. 3. Block diagram of the compressive sensing processing unit. A linear congruential pseudo random number generator is used to generate all the entries of the sampling matrix.

The original matrix can be reconstructed from the sampling results by performing Block Sparse Bayesian Learning [11, 12]. Fig. 4 shows reconstructed neural signals with different compression ratios. The normalized mean squared error (NMSE) is calculated to evaluate the quality of reconstructed signal, as shown in Fig. 5.

III. Experimental Results

The proposed design has been fabricated in IBM 180nm standard CMOS technology, occupying a silicon area of 4.5mm×1.5mm. A microphotography of the die and a photograph of the wireless neural recorder are shown in Fig. 6. The measured performance is summarised in Table I. The measured frequency responses in differential mode and common mode are shown in Fig. 7 (a) and (b), respectively. The inaccuracy of the measured gain is 0.24%. A CMRR of 111dB is achieved

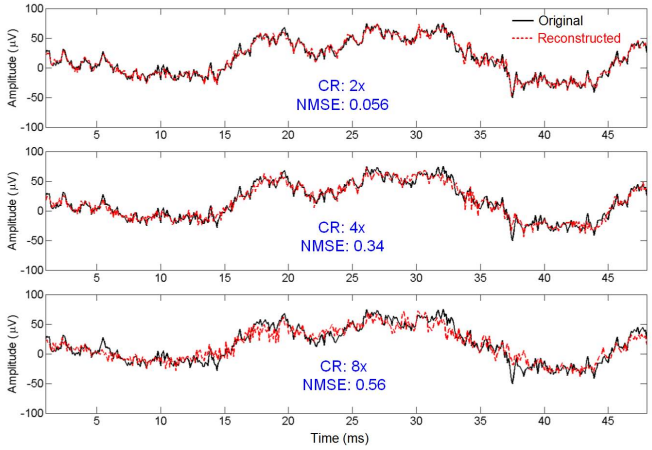

Fig. 4. Reconstructed neural signals with a compression ratio of 2, 4 and 8, respect

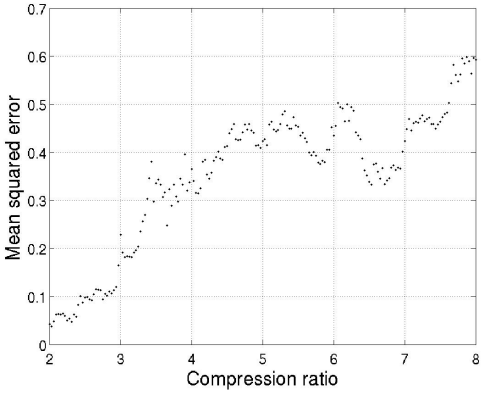

Fig. 5. Normalized mean squared error (NMSE) between the raw neural signal and the reconstructed signal from compressed sensing with different compression ratios.

with impedance boosting. The total power of the assembled wireless neural recorder is 3mA for 1 channel recording. A 4.6g lithium battery supports the device for up to 70 hours continuous neural recording.

Fig. 8 compares the measured input-referred noise spectrum of the neural amplifier with the simulation result. An integrated input referred noise of 1.63μV is achieved in the frequency band from 1Hz to 7kHz. The NEF is calculated to be 0.76. Reference circuits' power is not included since the biasing

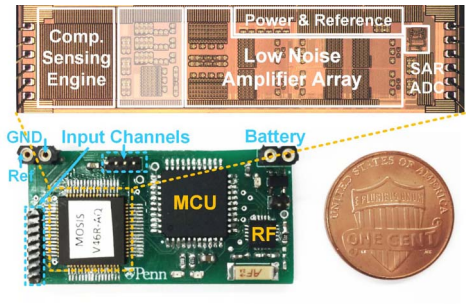

Fig. 6. Microscope photo of the fabricated IC (top), and the PCB based wireless portable neural recorder device (bottom).

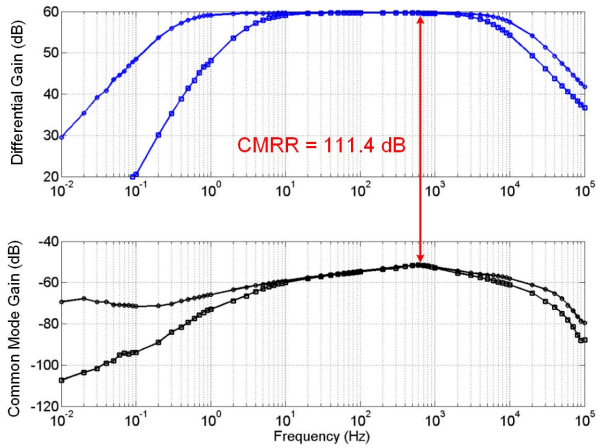

Fig. 7. Differential and common mode frequency response under different cutoff frequencies. A CMRR of 111dB is achieved.

voltages can be used in an arbitrary number of amplifiers.

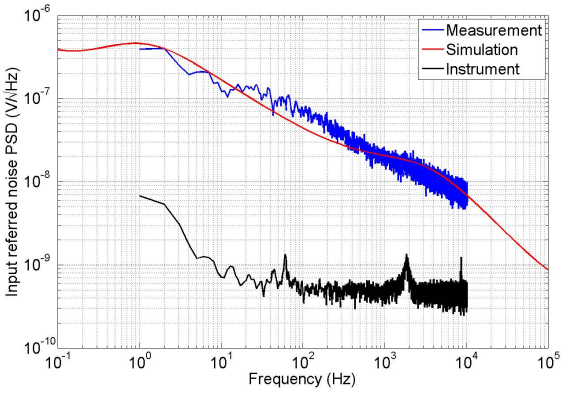

Fig. 8. Measured and simulated input referred noise spectrum. Integration under this curve from 1Hz to 7kHz yields an rms noise of 1.63μV.

TABLE I
CHIP SPECIFICATIONS SUMMARY

IA current	1uA	ADC ENOB	10.6 bit
IA Noise RMS	1.63uV	ADC FOM	0.85pJ/conversion-step
Bandwidth	7kHz	ADC INL	<+1.2/-1.3 LSB
THD (2mVpp)	-64.3dB	ADC DNL	< +1.1/-0.8 LSB
CMRR	111dB	CS Ratio	1x - 8x

Table II compares the performance of the proposed work with prior published compressed neural signal recording front-end designs.

TABLE II
COMPARISON WITH OTHER WORKS

Chateristic	[8]	[9]	[10]	This work
No. of Channels	16	1	16	12
Noise μVrms	5.4	2.84	4.2	1.63
NEF	4.9	2.16	4.12	0.76
ADC resolution	7	8	10	12
Compression method	Spike det.	Spike det.	CS	CS
Compression ratio	48	NA	<16	<8

IV. CONCLUSION

In this work, a low-noise, high efficiency neural signal recording front-end integrated compressed sensing uint was designed and fabricated in 180nm CMOS technology. A noise floor of 1.63μV was achieved in a bandwidth of 7kHz, with an NEF of 0.76. A SAR ADC is implemented with an ENOB of 10.6 bit at a sampling rate of 1MS/s. The sampled neural signal is compressed in a digital processing unit with a configurable compression ratio up to 8x. A miniature size wireless neural recorder has been built for long time recording. This work shows one of the highest noise and power efficiency neural recorder design.

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