HW1 P&R Tool

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Different configurations

core_util	clock_period	drc_violations	slack	chip_area	wire_length
0.50	1850	0	0.5	41107.357	208818.260
0.51	1850	1	-0.4	40323.806	206139.140
0.55	1850	0	-0.5	37595.032	206416.404
0.58	1850	0	0.1	35775.323	203183.744
0.59	1850	2	-0.5	35204.751	207529.052
0.50	1820	2	-6.2	41107.357	220285.660
0.50	1830	3	-0.3	41107.357	211932.440
0.50	1850	0	0.5	41107.357	208818.260
0.50	1900	0	0.9	41107.357	202823.192
0.50	2000	0	1.5	41107.357	198541.712
0.55	1950	0	1.7	37595.032	199719.892
0.60	1950	0	3.7	34640.234	196312.148
0.55	2000	0	3.8	37595.032	198050.712
0.60	2050	0	8.7	34640.234	194462.404
0.58	1835	0	0.0	35775.323	209925.192
0.58	1865	0	1.5	35775.323	202369.956
0.40	1900	0	0.2	50689.193	207794.024
0.46	1900	0	1.1	44443.199	205036.868
0.50	1900	0	0.9	41107.357	202823.192
0.55	1900	0	0.1	37595.032	203930.336

> **Clock period**: **Smaller** → harder timing, more DRCs, bigger wire length, negative slack. **Larger** → better slack, fewer DRCs, smaller wire length, but doesn't improve area.

> **Core utilization**: **Smaller** → larger area and wirelength, but routing easier. **Larger** → smaller area and wirelength, but risk of congestion.

Purpose of inserting well tap cell

- Prevent Latch-Up
- Ensure stable well biasing
- Provide direct connection to power and ground

Best Result

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--- Summary of the Current Result ---
 Slack Time:          0.100
 DRC Violations:      0
 Clock Period:        1850.000
 Total area of chip: 35775.323
 Total wire length:  203183.7440
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Final chip layout