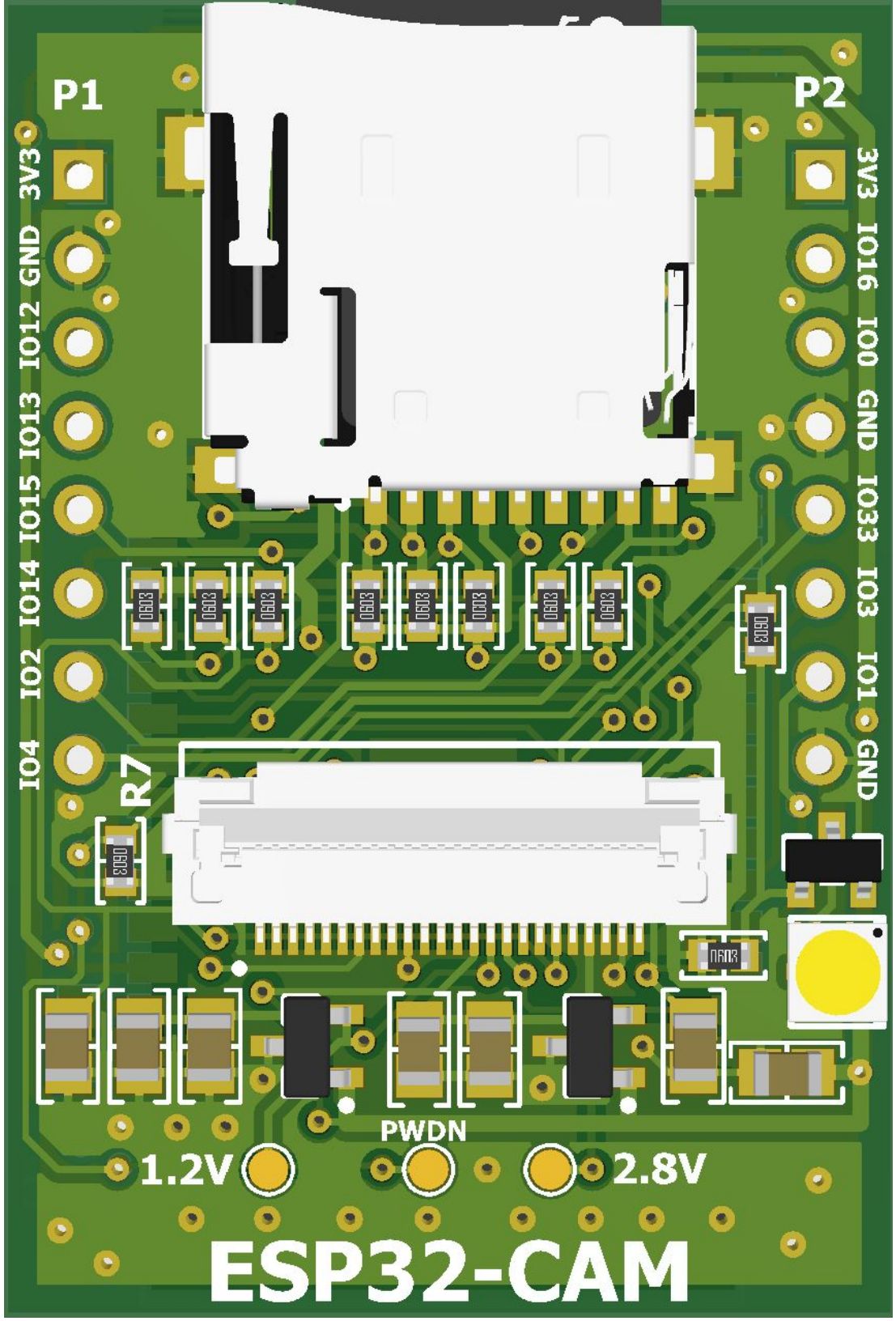
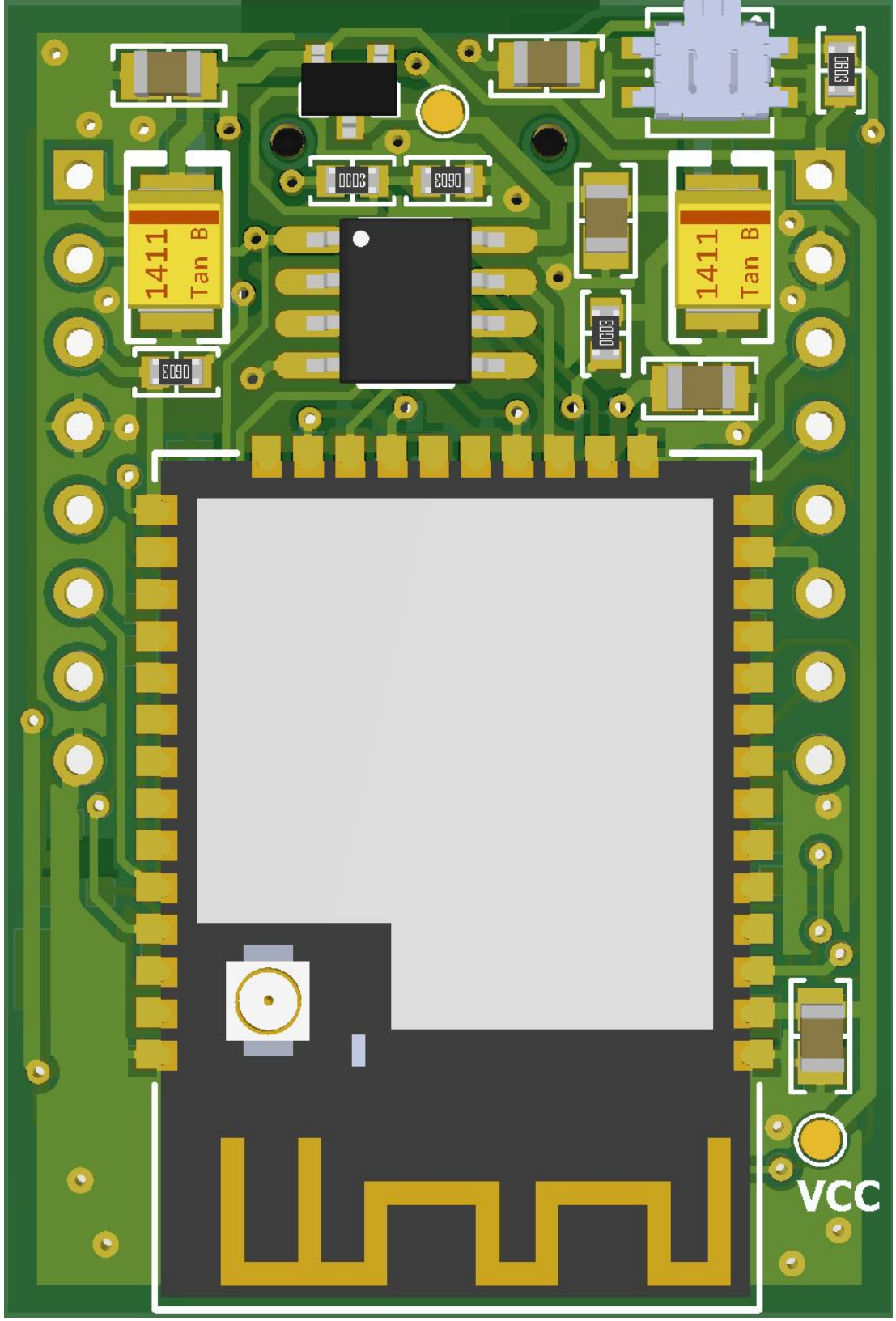
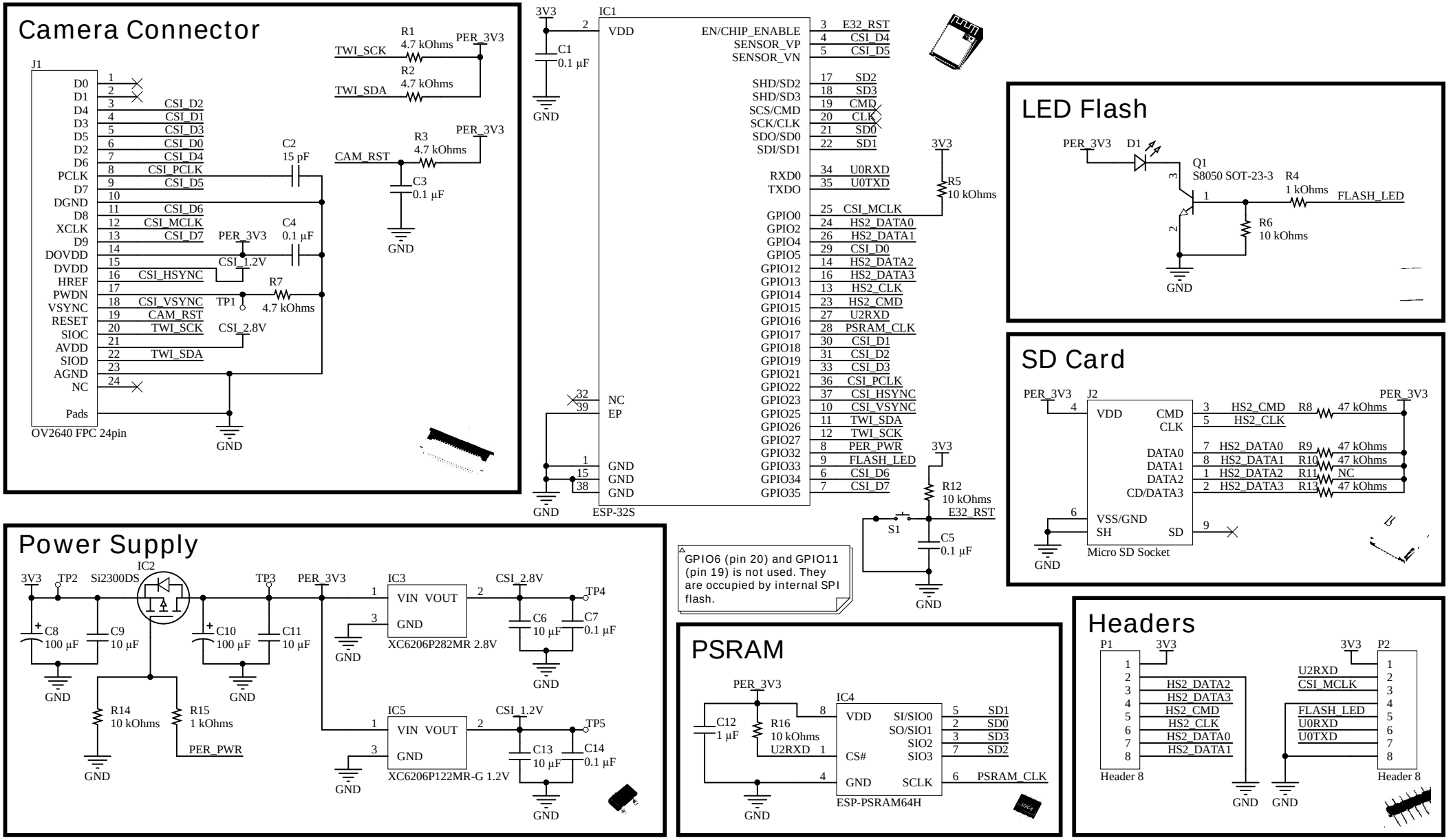
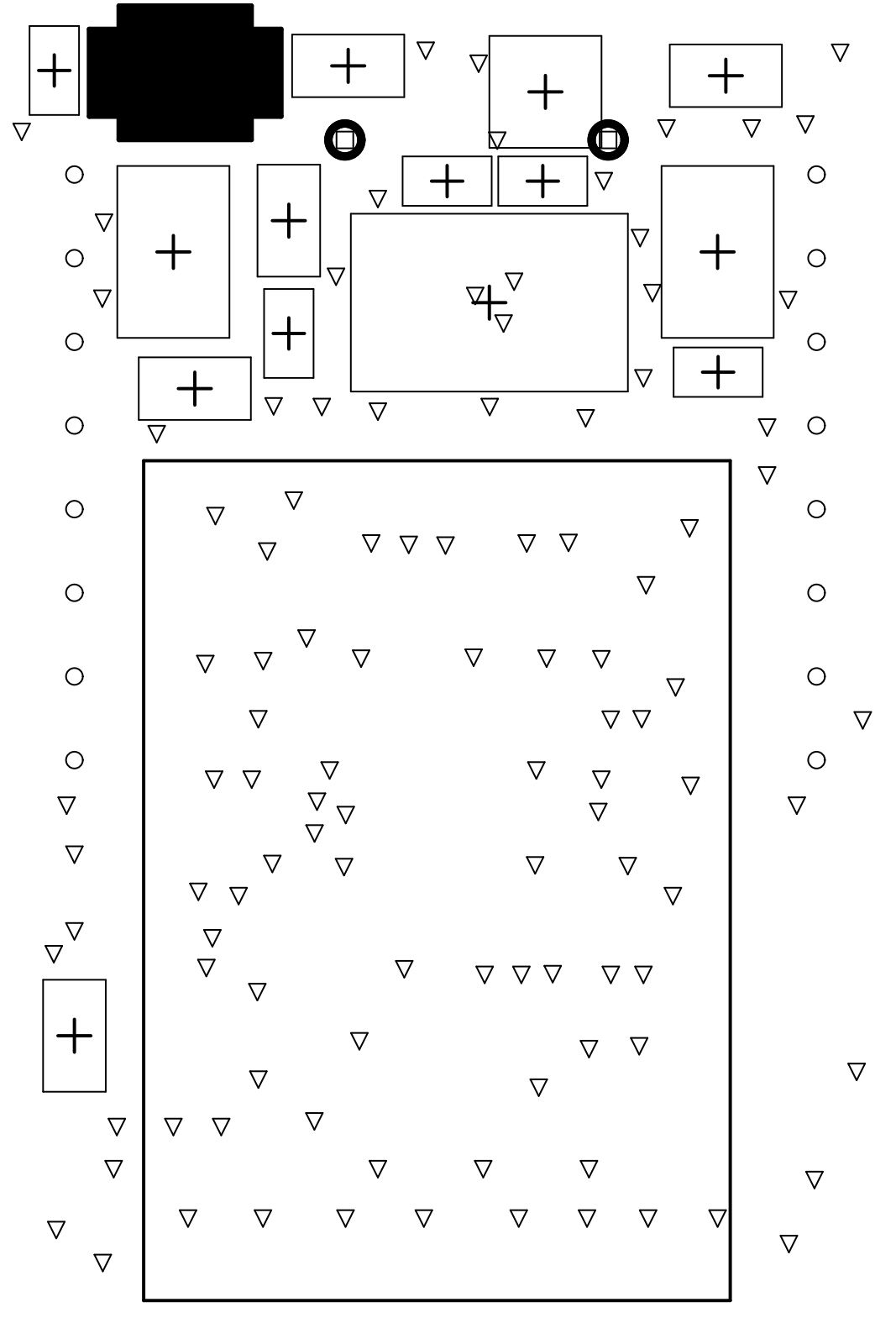
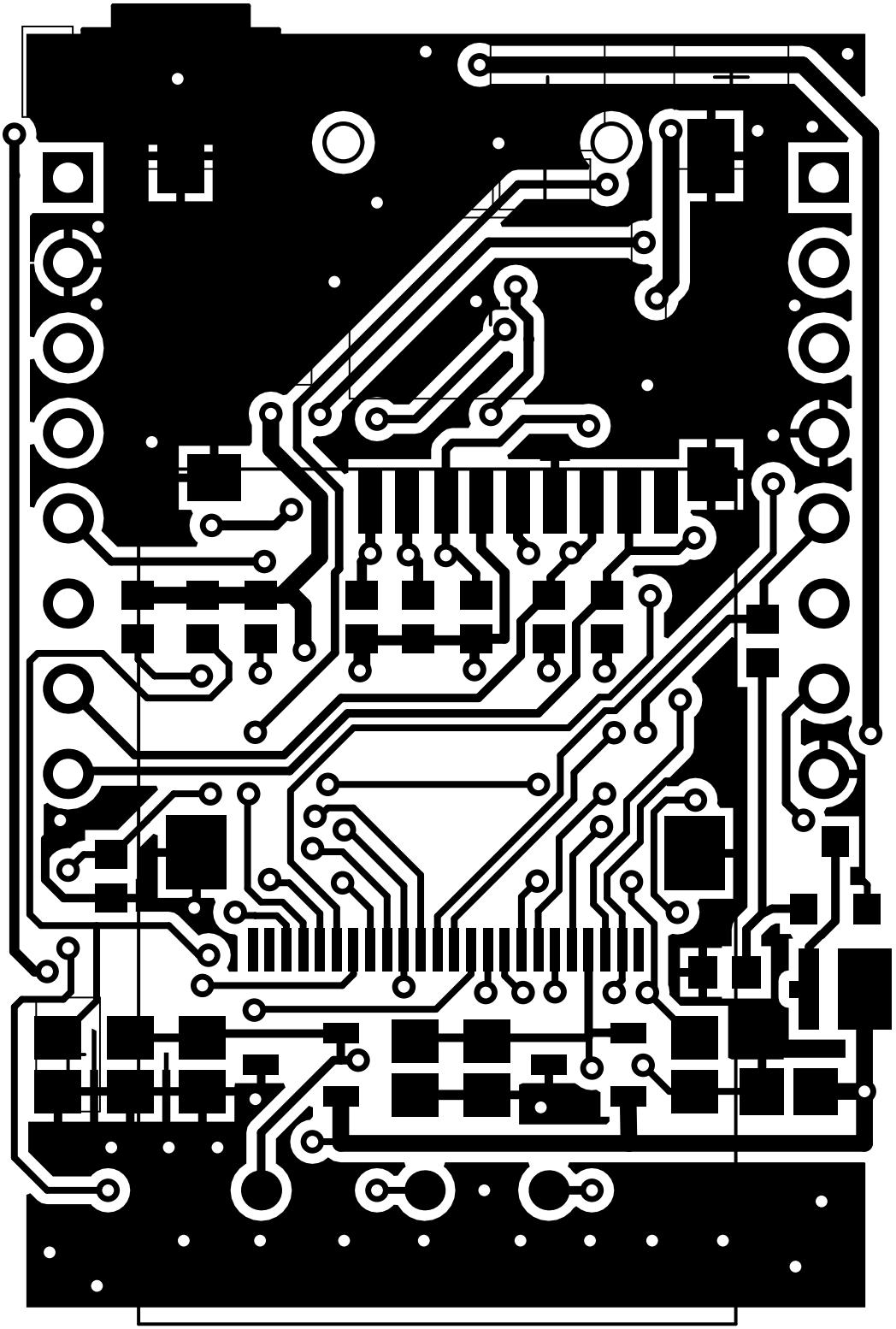
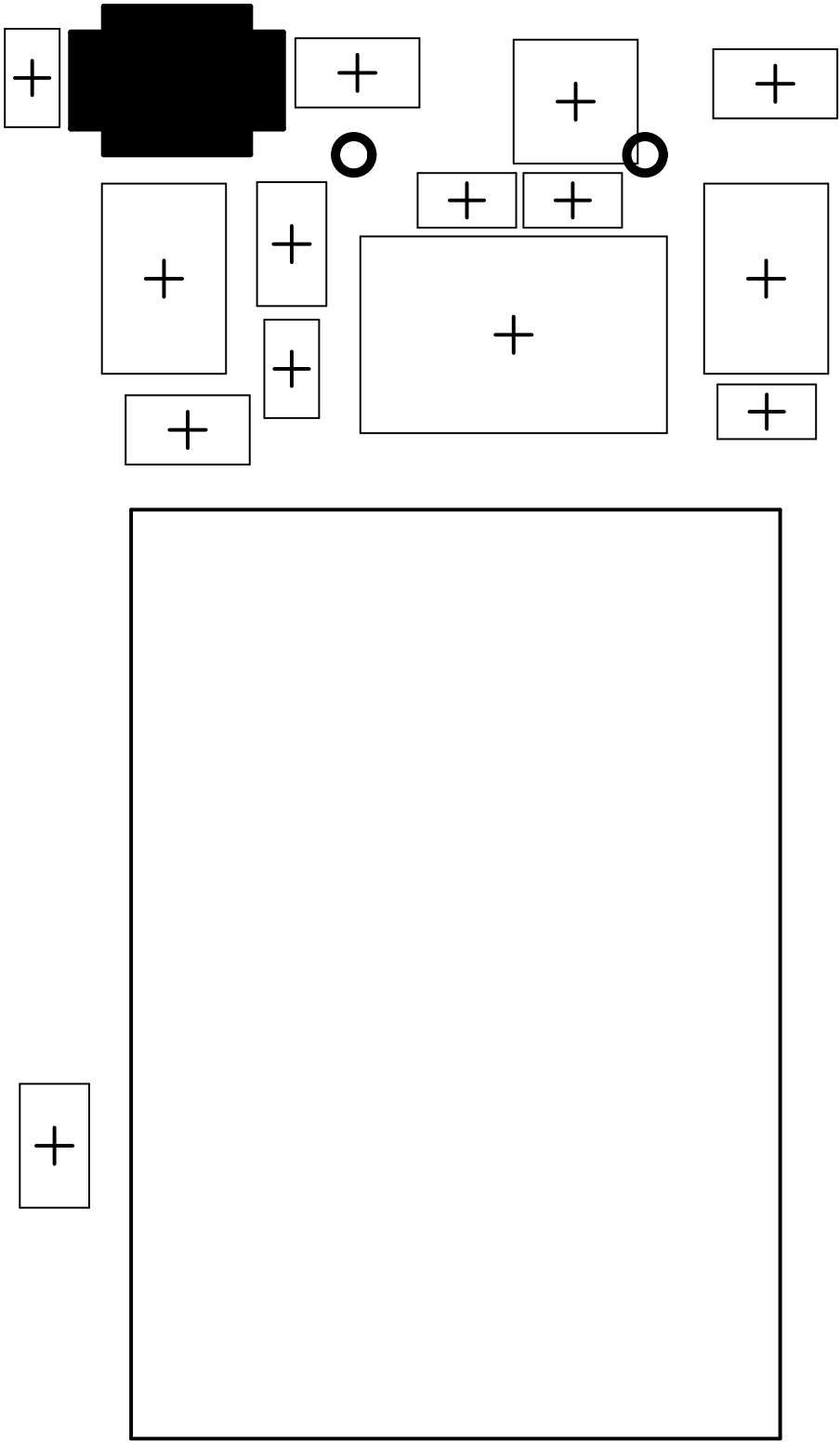

P1
P2
3V3
GND
IO12
IO13
IO15
IO14
IO2
IO4
R7
3V3
IO16
IO0
GND
IO33
IO3
IO1
GND
PWDN
1.2V
2.8V
ESP32-CAM

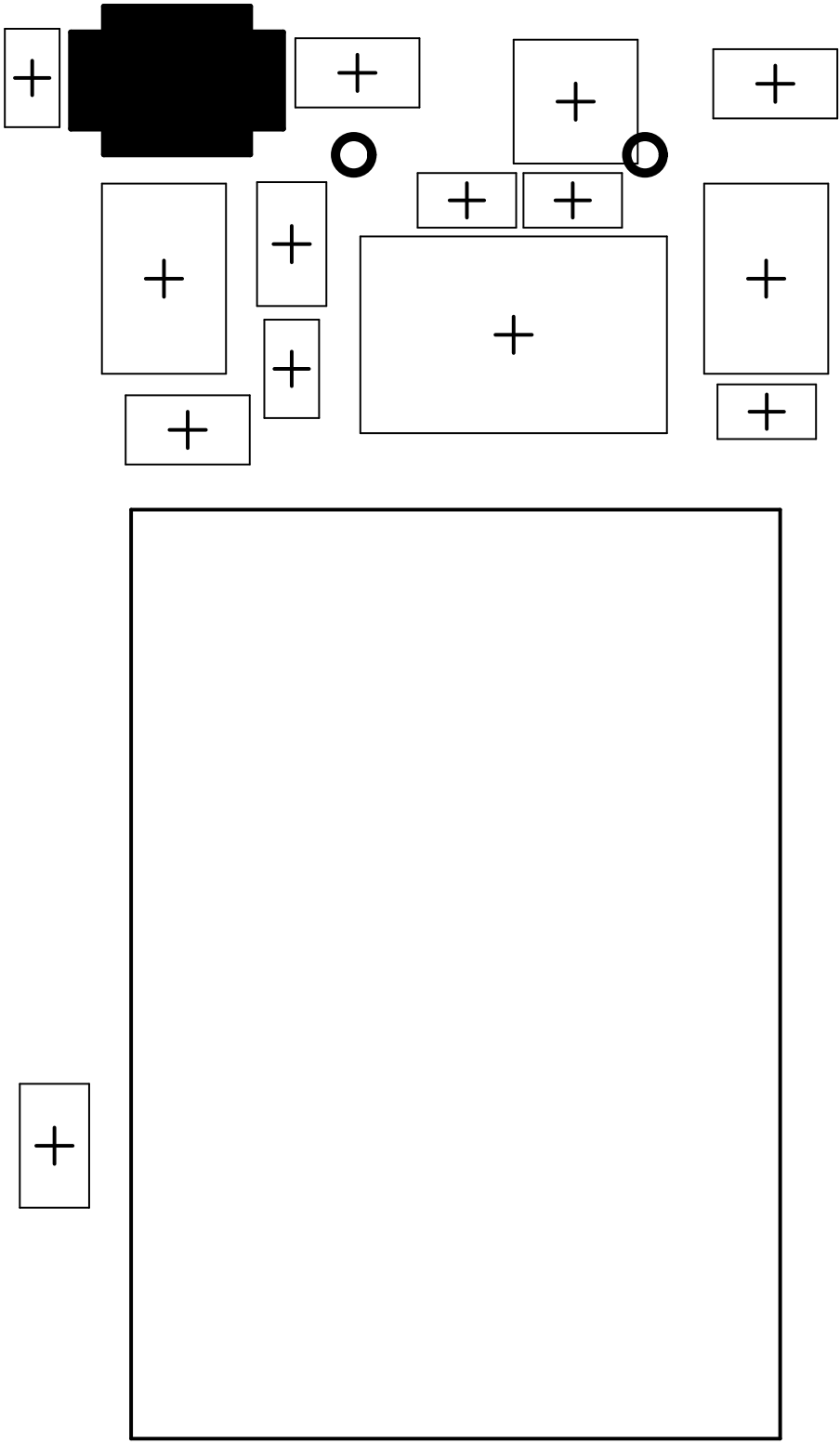

1411
Tan B
1411
Tan B
VCC

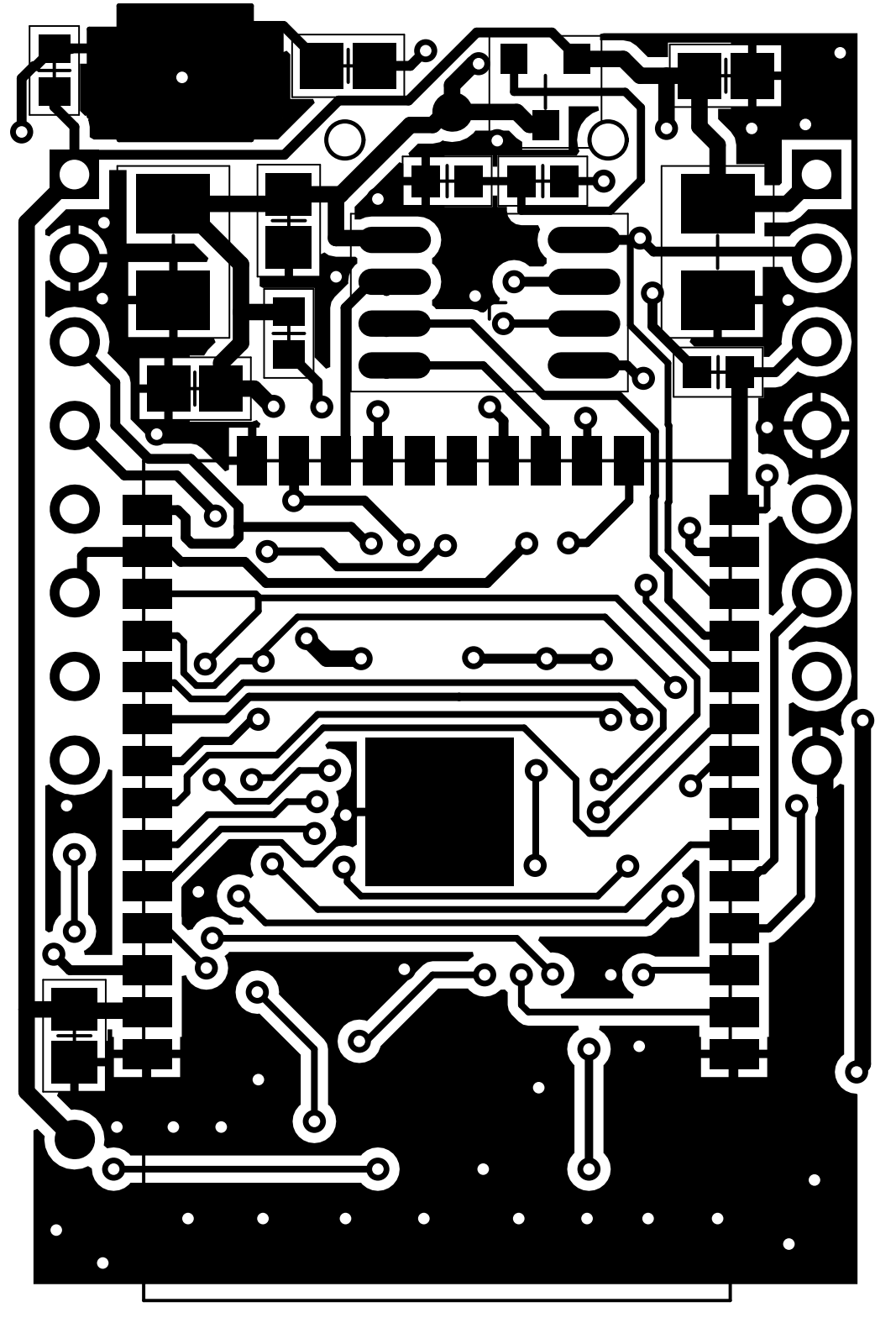

Camera Connector
J1
D0 1
D1 2
D4 3 CSI_D2
D3 4 CSI_D1
D5 5 CSI_D3
D2 6 CSI_D0
D6 7 CSI_D4
PCLK 8 CSI_PCLK
D7 9 CSI_D5
DGND 10
D8 11 CSI_D6
XCLK 12 CSI_MCLK
D9 13 CSI_D7
DOVDD 14
DVDD 15 CSI_1.2V
HREF 16 CSI_HSYNC
PWDN 17
VSYNC 18 CSI_VSYNC
RESET 19 CAM_RST
SIOC 20 TWI_SCK
AVDD 21 CSI_2.8V
SIOD 22 TWI_SDA
AGND 23
NC 24
Pads
OV2640 FPC 24pin
C2 15 pF
C4 0.1 µF
R7 4.7 kOhms
TP1
PER_3V3
GND
R1 4.7 kOhms
R2 4.7 kOhms
TWI_SCK
TWI_SDA
R3 4.7 kOhms
CAM_RST
C3 0.1 µF
IC1
3V3
C1 0.1 µF
VDD
EN/CHIP_ENABLE 3 E32_RST
SENSOR_VP 4 CSI_D4
SENSOR_VN 5 CSI_D5
SHD/SD2 17 SD2
SHD/SD3 18 SD3
SCS/CMD 19 CMD
SCK/CLK 20 CLK
SDO/SD0 21 SD0
SDI/SD1 22 SD1
RXD0 34 U0RXD
TXDO 35 U0TXD
GPIO0 25 CSI_MCLK
GPIO2 24 HS2_DATA0
GPIO4 26 HS2_DATA1
GPIO5 29 CSI_D0
GPIO12 14 HS2_DATA2
GPIO13 16 HS2_DATA3
GPIO14 13 HS2_CLK
GPIO15 23 HS2_CMD
GPIO16 27 U2RXD
GPIO17 28 PSRAM_CLK
GPIO18 30 CSI_D1
GPIO19 31 CSI_D2
GPIO21 33 CSI_D3
GPIO22 36 CSI_PCLK
GPIO23 37 CSI_HSYNC
GPIO25 10 CSI_VSYNC
GPIO26 11 TWI_SDA
GPIO27 12 TWI_SCK
GPIO32 8 PER_PWR
GPIO33 9 FLASH_LED
GPIO34 6 CSI_D6
GPIO35 7 CSI_D7
32 NC
39 EP
1 GND
15 GND
38 GND
ESP-32S
R5 10 kOhms
R12 10 kOhms
E32_RST
S1
C5 0.1 µF
GPIO6 (pin 20) and GPIO11 (pin 19) is not used. They are occupied by internal SPI flash.
LED Flash
PER_3V3
D1
Q1
S8050 SOT-23-3
R4 1 kOhms
FLASH_LED
R6 10 kOhms
SD Card
J2
PER_3V3
VDD
CMD HS2_CMD R8 47 kOhms
CLK HS2_CLK
DATA0 HS2_DATA0 R9 47 kOhms
DATA1 HS2_DATA1 R10 47 kOhms
DATA2 HS2_DATA2 R11 NC
CD/DATA3 HS2_DATA3 R13 47 kOhms
VSS/GND
SH
SD
Micro SD Socket
Power Supply
3V3
TP2
Si2300DS
IC2
TP3
PER_3V3
IC3
VIN VOUT
GND
XC6206P282MR 2.8V
CSI_2.8V
TP4
C8 100 µF
C9 10 µF
C10 100 µF
C11 10 µF
C6 10 µF
C7 0.1 µF
R14 10 kOhms
R15 1 kOhms
PER_PWR
IC5
XC6206P122MR-G 1.2V
CSI_1.2V
TP5
C13 10 µF
C14 0.1 µF
PSRAM
PER_3V3
IC4
C12 1 µF
R16 10 kOhms
U2RXD
VDD
CS#
GND
SI/SIO0 5 SD1
SO/SIO1 2 SD0
SIO2 3 SD3
SIO3 7 SD2
SCLK 6 PSRAM_CLK
ESP-PSRAM64H
Headers
P1
3V3
HS2_DATA2
HS2_DATA3
HS2_CMD
HS2_CLK
HS2_DATA0
HS2_DATA1
Header 8
P2
U2RXD
CSI_MCLK
FLASH_LED
U0RXD
U0TXD
By default all peripherial devices is disabled by pulling mosfet to ground. Enable them programatically by MCU
Title: ESP32-S CAM
Size: A4
Project: ESP32
Date: 13.01.2024 15:22:04
Sheet 000 of 999
Git Hash: Not in version control
File: C:\Users\Stason\Desktop\Projects\ESP32\ai-meter\esp32-cam\main.SchDot
Author: Stanislav Vodolagin
Approved: Stanislav Vodolagin
Edited: 13.01.2024
Variant: [No Variations]
SW Version: 19.1.8.144
Stason Corp
Riga
Latvia

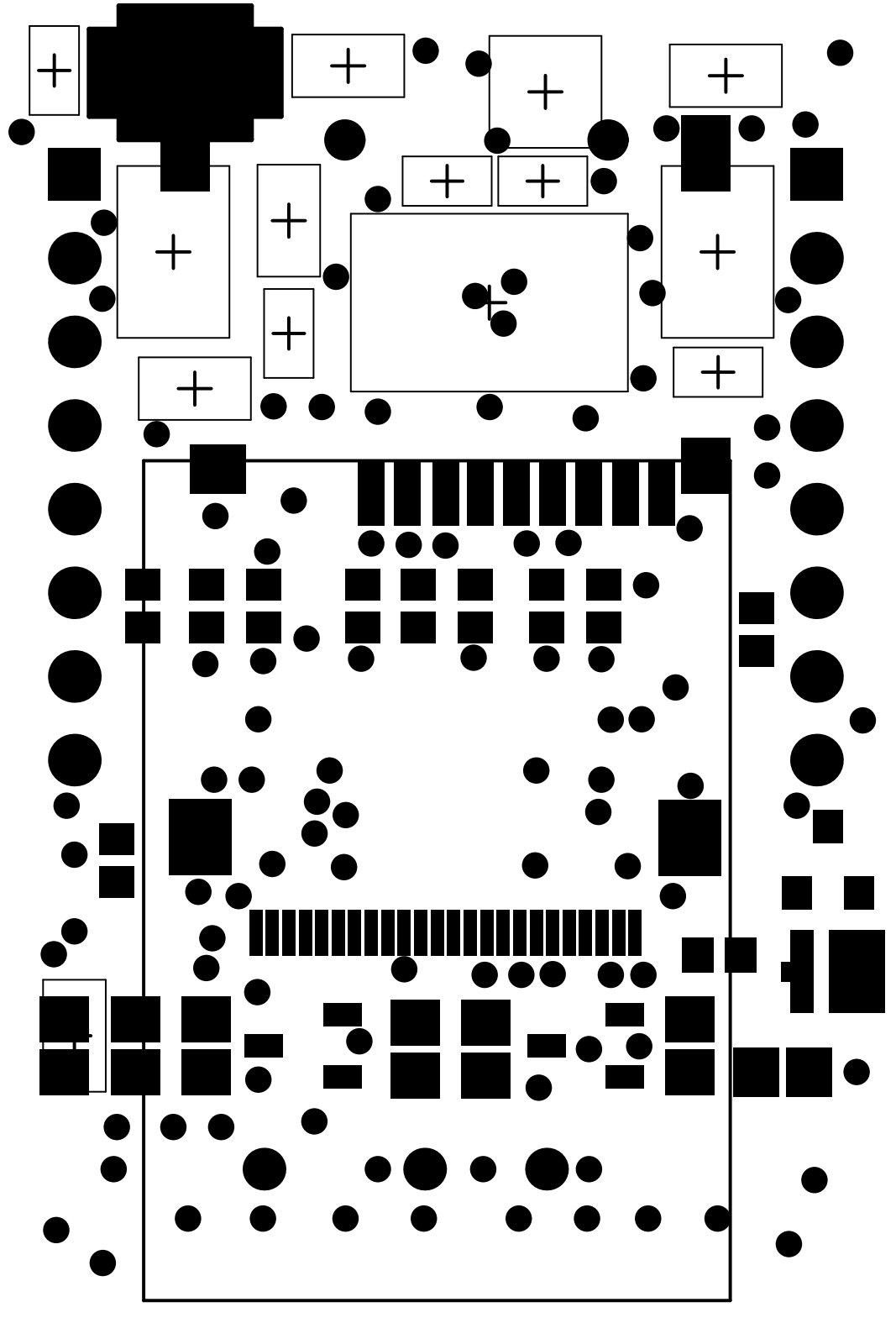


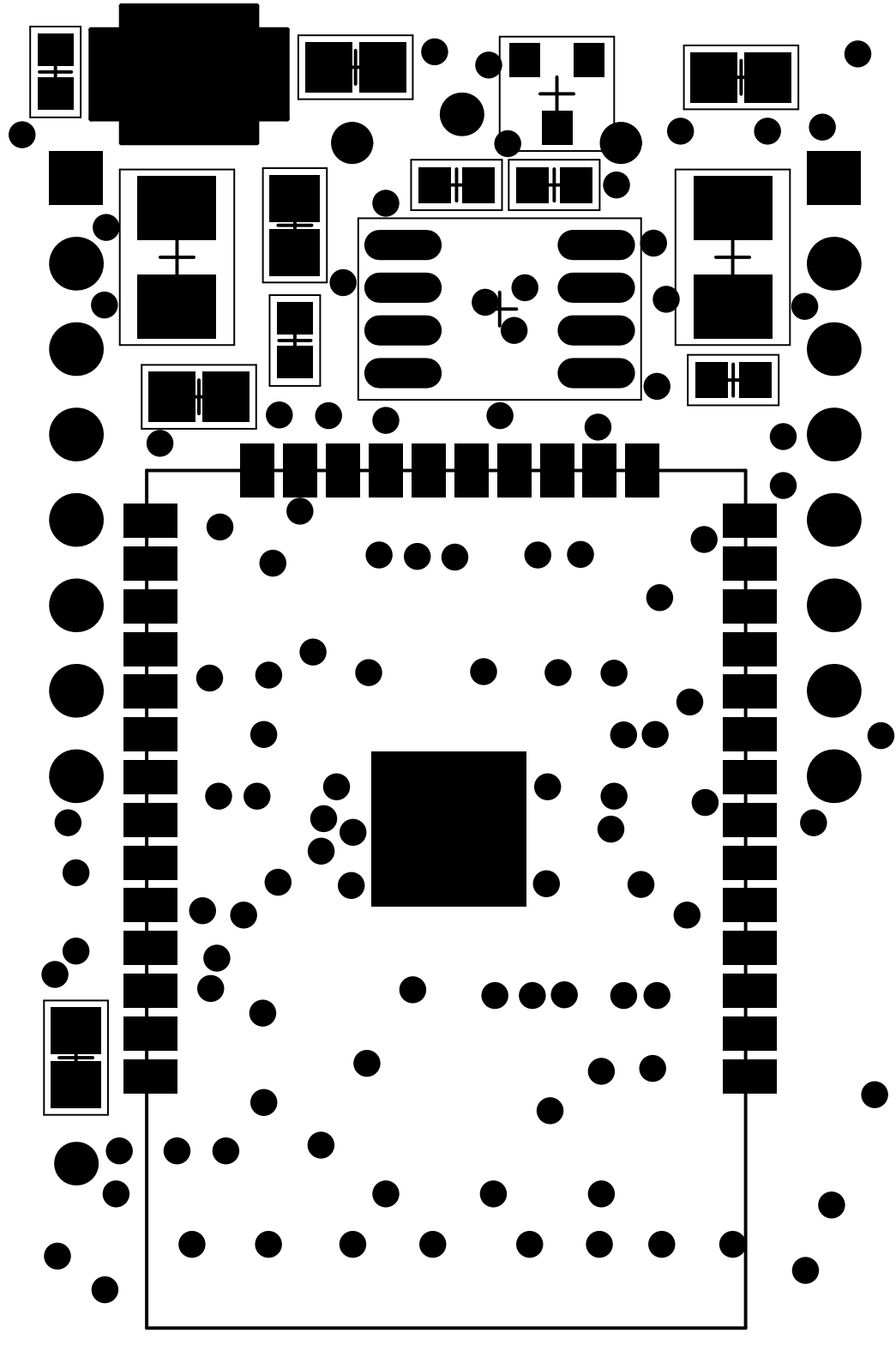


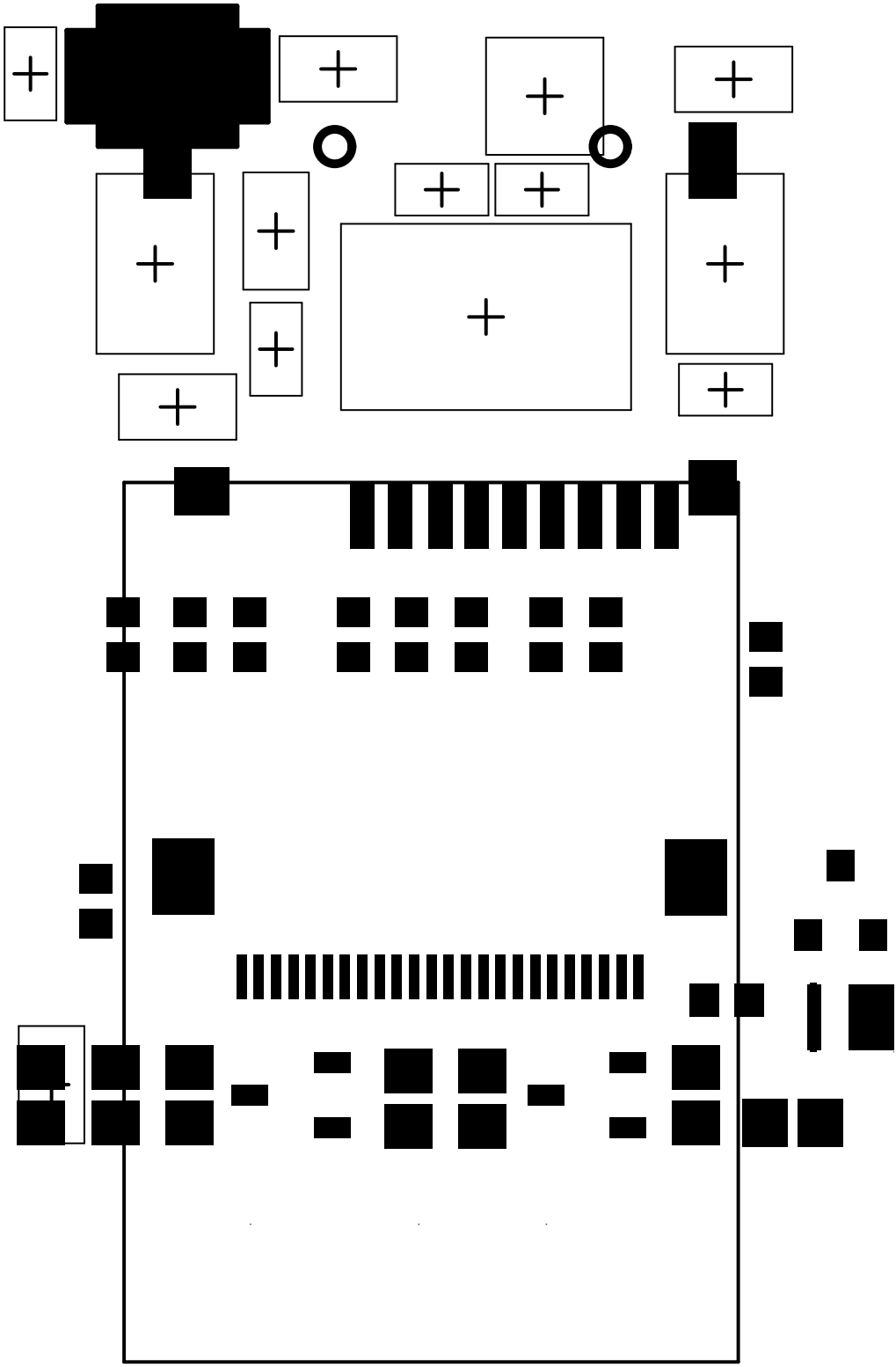


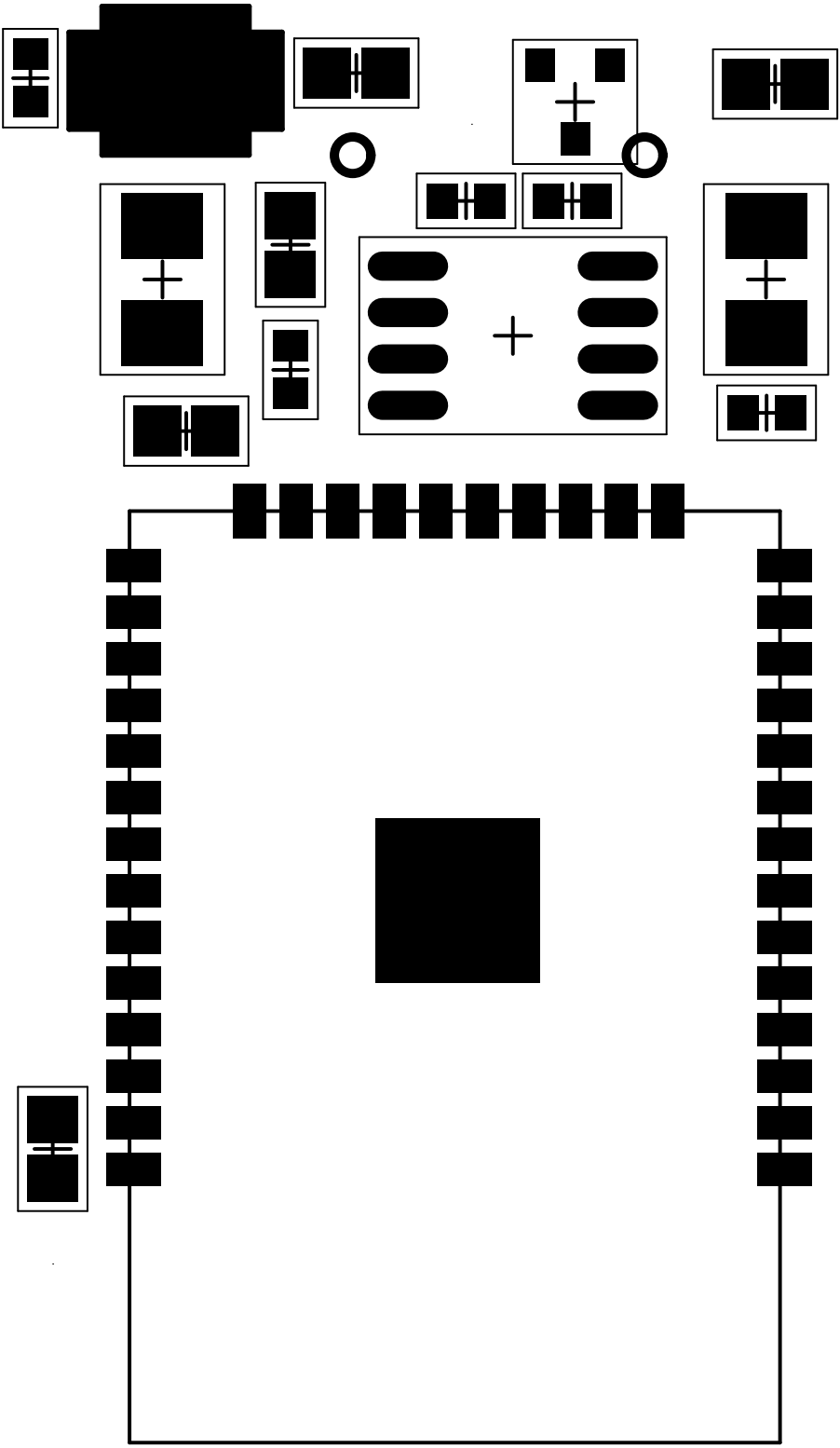




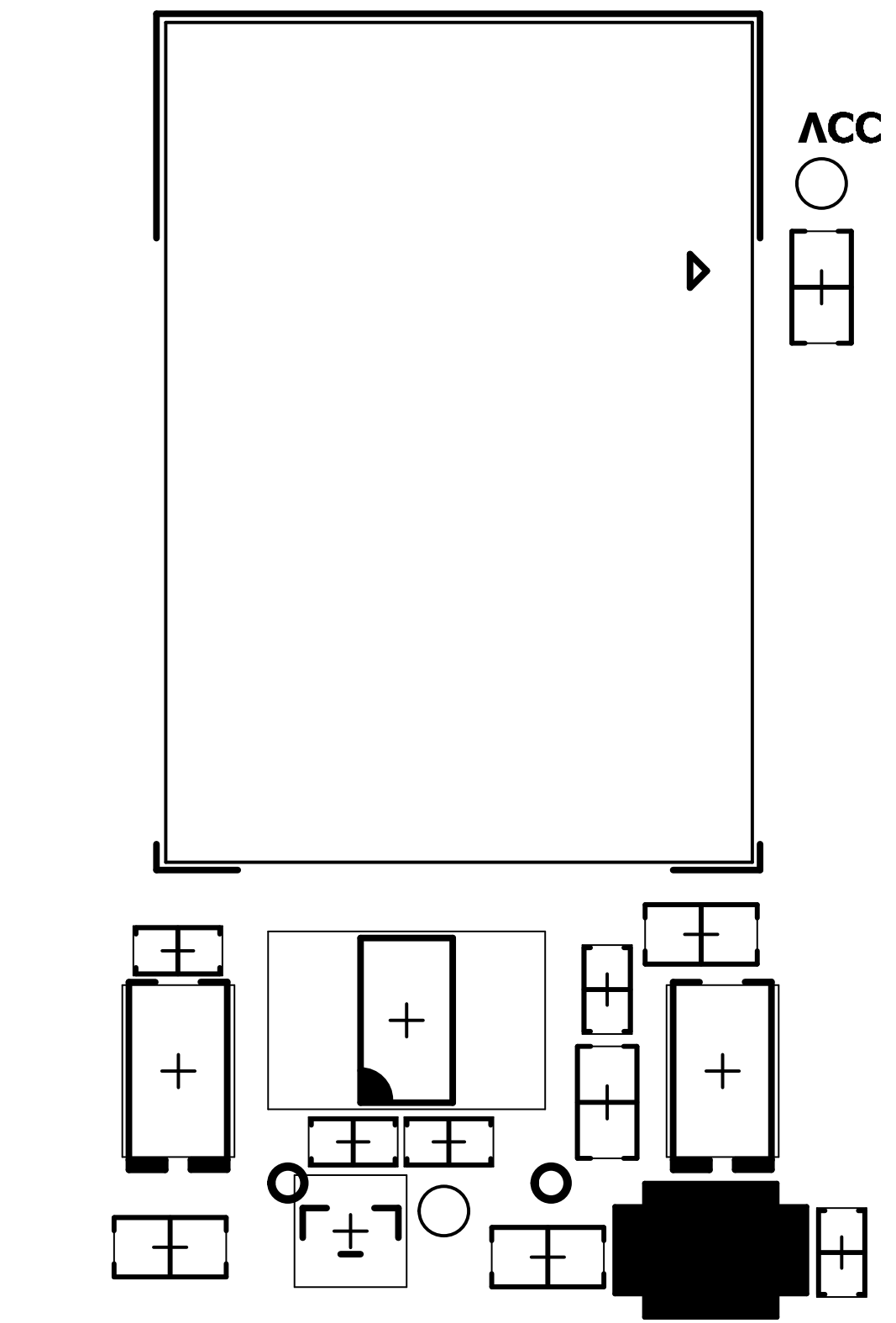


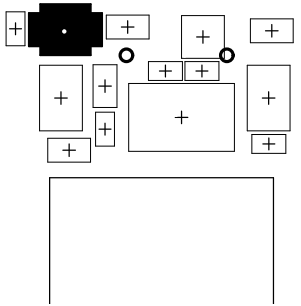


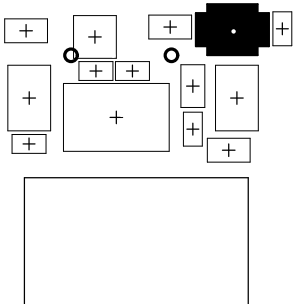




P1
P2
3V3
GND
IO12
IO13
IO15
IO14
IO2
IO4
3V3
IO16
IO0
GND
IO33
IO3
IO1
GND
R7
PWDN
1.2V
2.8V
ESP32-CAM


ACC





Design Rules Verification Report

Filename : C:\Users\Stason\Desktop\Projects\ESP32\ai-meter\esp32-cam\PCB.PcbDoc

Warnings 0
Rule Violations 152

Warnings	
Total	0

Rule Violations	
Clearance Constraint (Gap=0.025mm) (IsVia and not IsComponentVia),(IsPad)	0
Clearance Constraint (Gap=6mm) (InNetClass('NOTSELV')),(NOT InNetClass('NOTSELV'))	0
Clearance Constraint (Gap=0.203mm) (All),(All)	0
Short-Circuit Constraint (Allowed=No) (All),(not IsBoardCutoutRegion)	0
Un-Routed Net Constraint ((All))	0
Modified Polygon (Allow modified: No), (Allow shelved: No)	0
Width Constraint (Min=0.203mm) (Max=12.7mm) (Preferred=0.254mm) (All)	0
SMD To Corner (Distance=0.025mm) (All)	0
SMD To Plane Constraint (Distance=0mm) (All)	0
SMD Neck-Down Constraint (Percent=90%) (not IsTestpoint)	0
SMD Entry (Side = Allowed) (Corner = Allowed) (Any Angle = Not Allowed) (Ignore First Corner = Allowed)	23
Power Plane Connect Rule(Relief Connect)(Expansion=0.508mm) (Conductor Width=0.254mm) (Air Gap=0.254mm)	0
Fabrication Testpoint Style (Under Component=Yes) (All)	0
Fabrication Testpoint Usage (Valid =Don't care, Allow multiple per net=No) (All)	0
Assembly Testpoint Style (Under Component=Yes) (All)	0
Assembly Testpoint Usage (Valid =Don't care, Allow multiple per net=Yes) (InNetClass('NOTESTPOINTS'))	0
Assembly Testpoint Usage (Valid =One Required, Allow multiple per net=Yes) ((not InNetClass('NOTESTPOINTS')))	43
Minimum Annular Ring (Minimum=0.15mm) (All)	0
Hole Size Constraint (Min=0.3mm) (Max=6.35mm) (All)	0
Hole To Hole Clearance (Gap=0mm) (InPadClass('NetTieVias')),(InPadClass('NetTieVias'))	0
Hole To Hole Clearance (Gap=0.25mm) (All),(All)	0
Minimum Solder Mask Sliver (Gap=0.2mm) (All),(All)	69
Net Antennae (Tolerance=0mm) (All)	0
Board Clearance Constraint (Gap=0mm) ((OnLayer('Top Layer') OR OnLayer('Bottom Layer')))	17
Height Constraint (Min=0mm) (Max=25.4mm) (Prefered=12.7mm) (All)	0
Total	152

SMD Entry (Side = Allowed) (Corner = Allowed) (Any Angle = Not Allowed) (Ignore First Corner = Allowed)
SMD Entry Constraint: Between Pad C1-1(2.25mm,9.35mm) on Bottom Layer And Track (2.29mm,9.31mm)(4.41mm,9.31mm) on Bottom Layer Track Entry
SMD Entry Constraint: Between Pad C12-1(8.75mm,34.1mm) on Bottom Layer And Track (5.465mm,33.81mm)(8.46mm,33.81mm) on Bottom Layer Track
SMD Entry Constraint: Between Pad C13-2(6.25mm,9.05mm) on Top Layer And Track (6.288mm,9.175mm)(10.258mm,9.175mm) on Top Layer Track
SMD Entry Constraint: Between Pad C7-2(12.585mm,8.945mm) on Top Layer And Track (12.35mm,9.05mm)(17.75mm,9.05mm) on Top Layer Track Entry
SMD Entry Constraint: Between Pad IC1-10(4.45mm,19.43mm) on Bottom Layer And Track (4.608mm,19.272mm)(5.283mm,19.272mm) on Bottom Layer
SMD Entry Constraint: Between Pad IC1-13(4.45mm,23.24mm) on Bottom Layer And Track (4.937mm,23.476mm)(5.473mm,22.94mm) on Bottom Layer
SMD Entry Constraint: Between Pad IC1-17(10.18mm,26.01mm) on Bottom Layer And Track (10.469mm,26.549mm)(10.469mm,30.654mm) on Bottom
SMD Entry Constraint: Between Pad IC1-2(4.45mm,9.27mm) on Bottom Layer And Track (2.29mm,9.31mm)(4.41mm,9.31mm) on Bottom Layer Track Entry
SMD Entry Constraint: Between Pad IC1-25(22.25mm,24.51mm) on Bottom Layer And Track (22.416mm,24.676mm)(22.416mm,28.699mm) on Bottom
SMD Entry Constraint: Between Pad IC1-31(22.25mm,16.89mm) on Bottom Layer And Track (20.931mm,16.138mm)(21.683mm,16.89mm) on Bottom
SMD Entry Constraint: Between Pad IC1-5(4.45mm,13.08mm) on Bottom Layer And Track (4.696mm,12.834mm)(6.69mm,14.828mm) on Bottom Layer
SMD Entry Constraint: Between Pad IC3-1(18.935mm,7.3mm) on Top Layer And Track (18.925mm,7.3mm)(18.95mm,5.9mm) on Top Layer Track Entry to
SMD Entry Constraint: Between Pad IC4-8(11.96mm,32.715mm) on Bottom Layer And Track (10.18mm,32.77mm)(11.374mm,32.77mm) on Bottom Layer
SMD Entry Constraint: Between Pad IC5-2(10.37mm,9.2mm) on Top Layer And Track (6.288mm,9.175mm)(10.258mm,9.175mm) on Top Layer Track Entry
SMD Entry Constraint: Between Pad J1-20(17.25mm,11.675mm) on Top Layer And Track (17.279mm,11.704mm)(17.279mm,14.492mm) on Top Layer
SMD Entry Constraint: Between Pad R11-1(11mm,20.95mm) on Top Layer And Track (11.047mm,20.903mm)(14.353mm,20.903mm) on Top Layer Track
SMD Entry Constraint: Between Pad R2-1(8mm,20.95mm) on Top Layer And Track (7.973mm,19.927mm)(7.973mm,20.923mm) on Top Layer Track Entry
SMD Entry Constraint: Between Pad R4-1(22.921mm,21.542mm) on Top Layer And Track (22.971mm,21.542mm)(22.971mm,22.617mm) on Top Layer
SMD Entry Constraint: Between Pad R8-1(14.4mm,20.95mm) on Top Layer And Track (11.047mm,20.903mm)(14.353mm,20.903mm) on Top Layer Track
SMD Entry Constraint: Between Pad R8-1(14.4mm,20.95mm) on Top Layer And Track (14.353mm,20.029mm)(14.353mm,20.903mm) on Top Layer Track
SMD Entry Constraint: Between Pad R9-1(16.575mm,20.95mm) on Top Layer And Track (16.565mm,20mm)(16.565mm,20.897mm) on Top Layer Track
SMD Entry Constraint: Between Pad R9-2(16.575mm,22.25mm) on Top Layer And Track (16.625mm,22.25mm)(16.625mm,22.789mm) on Top Layer Track
SMD Entry Constraint: Between Pad TP3-TP?(13.7mm,36.6mm) on Bottom Layer And Track (12.432mm,36.205mm)(13.115mm,36.205mm) on Bottom

Assembly Testpoint Usage (Valid =One Required, Allow multiple per net=Yes) ((not InNetClass('NOTESTPOINTS')))
Assembly Testpoint Usage: Net 3V3 - Missing required testpoint
Assembly Testpoint Usage: Net CAM_RST - Missing required testpoint
Assembly Testpoint Usage: Net CLK - Missing required testpoint
Assembly Testpoint Usage: Net CMD - Missing required testpoint
Assembly Testpoint Usage: Net CSI_1.2V - Missing required testpoint
Assembly Testpoint Usage: Net CSI_2.8V - Missing required testpoint
Assembly Testpoint Usage: Net CSI_D0 - Missing required testpoint
Assembly Testpoint Usage: Net CSI_D1 - Missing required testpoint
Assembly Testpoint Usage: Net CSI_D2 - Missing required testpoint
Assembly Testpoint Usage: Net CSI_D3 - Missing required testpoint
Assembly Testpoint Usage: Net CSI_D4 - Missing required testpoint
Assembly Testpoint Usage: Net CSI_D5 - Missing required testpoint
Assembly Testpoint Usage: Net CSI_D6 - Missing required testpoint
Assembly Testpoint Usage: Net CSI_D7 - Missing required testpoint
Assembly Testpoint Usage: Net CSI_HSYNC - Missing required testpoint
Assembly Testpoint Usage: Net CSI_MCLK - Missing required testpoint
Assembly Testpoint Usage: Net CSI_PCLK - Missing required testpoint
Assembly Testpoint Usage: Net CSI_VSYNC - Missing required testpoint
Assembly Testpoint Usage: Net E32_RST - Missing required testpoint
Assembly Testpoint Usage: Net FLASH_LED - Missing required testpoint
Assembly Testpoint Usage: Net GND - Missing required testpoint
Assembly Testpoint Usage: Net HS2_CLK - Missing required testpoint
Assembly Testpoint Usage: Net HS2_CMD - Missing required testpoint
Assembly Testpoint Usage: Net HS2_DATA0 - Missing required testpoint
Assembly Testpoint Usage: Net HS2_DATA1 - Missing required testpoint
Assembly Testpoint Usage: Net HS2_DATA2 - Missing required testpoint
Assembly Testpoint Usage: Net HS2_DATA3 - Missing required testpoint
Assembly Testpoint Usage: Net IO16 - Missing required testpoint
Assembly Testpoint Usage: Net NetD1_2 - Missing required testpoint
Assembly Testpoint Usage: Net NetIC2_1 - Missing required testpoint
Assembly Testpoint Usage: Net NetJ1_17 - Missing required testpoint
Assembly Testpoint Usage: Net NetQ1_1 - Missing required testpoint
Assembly Testpoint Usage: Net PER_3V3 - Missing required testpoint
Assembly Testpoint Usage: Net PER_PWR - Missing required testpoint
Assembly Testpoint Usage: Net PSRAM_CLK - Missing required testpoint
Assembly Testpoint Usage: Net SD0 - Missing required testpoint
Assembly Testpoint Usage: Net SD1 - Missing required testpoint
Assembly Testpoint Usage: Net SD2 - Missing required testpoint
Assembly Testpoint Usage: Net SD3 - Missing required testpoint
Assembly Testpoint Usage: Net TWI_SCK - Missing required testpoint
Assembly Testpoint Usage: Net TWI_SDA - Missing required testpoint
Assembly Testpoint Usage: Net U0RXD - Missing required testpoint
Assembly Testpoint Usage: Net U0TXD - Missing required testpoint

Minimum Solder Mask Sliver (Gap=0.2mm) (All),(All)
Minimum Solder Mask Sliver Constraint: (0.01mm < 0.2mm) Between Pad IC1-16(8.91mm,26.01mm) on Bottom Layer And Via (8.9mm,24.8mm) from Top
Minimum Solder Mask Sliver Constraint: (0.09mm < 0.2mm) Between Pad IC1-23(17.8mm,26.01mm) on Bottom Layer And Via (17.75mm,27.3mm) from
Minimum Solder Mask Sliver Constraint: (0.152mm < 0.2mm) Between Pad IC1-25(22.25mm,24.51mm) on Bottom Layer And Via (20.9mm,23.958mm) from
Minimum Solder Mask Sliver Constraint: (0.189mm < 0.2mm) Between Pad IC1-25(22.25mm,24.51mm) on Bottom Layer And Via (23.251mm,25.563mm)
Minimum Solder Mask Sliver Constraint: (0.192mm < 0.2mm) Between Pad IC1-26(22.25mm,23.24mm) on Bottom Layer And Via (20.9mm,23.958mm) from
Minimum Solder Mask Sliver Constraint: (0.177mm < 0.2mm) Between Pad IC1-31(22.25mm,16.89mm) on Bottom Layer And Via (20.931mm,16.138mm)
Minimum Solder Mask Sliver Constraint: (0.12mm < 0.2mm) Between Pad IC1-32(22.25mm,15.62mm) on Bottom Layer And Via (20.931mm,16.138mm)
Minimum Solder Mask Sliver Constraint: (0.191mm < 0.2mm) Between Pad IC1-39(13.315mm,15.346mm) on Bottom Layer And Via (10.424mm,13.671mm)
Minimum Solder Mask Sliver Constraint: (0.139mm < 0.2mm) Between Pad IC1-39(13.315mm,15.346mm) on Bottom Layer And Via (10.476mm,15.251mm)
Minimum Solder Mask Sliver Constraint: (0.181mm < 0.2mm) Between Pad IC3-1(18.935mm,7.3mm) on Top Layer And Via (19.373mm,8.231mm) from Top
Minimum Solder Mask Sliver Constraint: (0.151mm < 0.2mm) Between Pad IC4-1(17.7mm,32.715mm) on Bottom Layer And Via (19.4mm,32.77mm) from
Minimum Solder Mask Sliver Constraint: (0.068mm < 0.2mm) Between Pad IC5-2(10.37mm,9.2mm) on Top Layer And Via (10.889mm,8.382mm) from Top
Minimum Solder Mask Sliver Constraint: (0.1mm < 0.2mm) Between Pad J1-1(7.75mm,11.675mm) on Top Layer And Pad J1-2(8.25mm,11.675mm) on Top
Minimum Solder Mask Sliver Constraint: (0.126mm < 0.2mm) Between Pad J1-1(7.75mm,11.675mm) on Top Layer And Via (7.228mm,12.791mm) from
Minimum Solder Mask Sliver Constraint: (0.1mm < 0.2mm) Between Pad J1-10(12.25mm,11.675mm) on Top Layer And Pad J1-11(12.75mm,11.675mm) on
Minimum Solder Mask Sliver Constraint: (0.1mm < 0.2mm) Between Pad J1-10(12.25mm,11.675mm) on Top Layer And Pad J1-9(11.75mm,11.675mm) on
Minimum Solder Mask Sliver Constraint: (0.005mm < 0.2mm) Between Pad J1-10(12.25mm,11.675mm) on Top Layer And Via (12.25mm,10.57mm) from
Minimum Solder Mask Sliver Constraint: (0.1mm < 0.2mm) Between Pad J1-11(12.75mm,11.675mm) on Top Layer And Pad J1-12(13.25mm,11.675mm) on
Minimum Solder Mask Sliver Constraint: (0.104mm < 0.2mm) Between Pad J1-11(12.75mm,11.675mm) on Top Layer And Via (12.25mm,10.57mm) from
Minimum Solder Mask Sliver Constraint: (0.1mm < 0.2mm) Between Pad J1-12(13.25mm,11.675mm) on Top Layer And Pad J1-13(13.75mm,11.675mm) on
Minimum Solder Mask Sliver Constraint: (0.1mm < 0.2mm) Between Pad J1-13(13.75mm,11.675mm) on Top Layer And Pad J1-14(14.25mm,11.675mm) on
Minimum Solder Mask Sliver Constraint: (0.1mm < 0.2mm) Between Pad J1-14(14.25mm,11.675mm) on Top Layer And Pad J1-15(14.75mm,11.675mm) on
Minimum Solder Mask Sliver Constraint: (0.1mm < 0.2mm) Between Pad J1-15(14.75mm,11.675mm) on Top Layer And Pad J1-16(15.25mm,11.675mm) on
Minimum Solder Mask Sliver Constraint: (0.176mm < 0.2mm) Between Pad J1-15(14.75mm,11.675mm) on Top Layer And Via (14.688mm,10.399mm) from
Minimum Solder Mask Sliver Constraint: (0.1mm < 0.2mm) Between Pad J1-16(15.25mm,11.675mm) on Top Layer And Pad J1-17(15.75mm,11.675mm) on
Minimum Solder Mask Sliver Constraint: (0.1mm < 0.2mm) Between Pad J1-17(15.75mm,11.675mm) on Top Layer And Pad J1-18(16.25mm,11.675mm) on
Minimum Solder Mask Sliver Constraint: (0.176mm < 0.2mm) Between Pad J1-17(15.75mm,11.675mm) on Top Layer And Via (15.8mm,10.399mm) from
Minimum Solder Mask Sliver Constraint: (0.1mm < 0.2mm) Between Pad J1-18(16.25mm,11.675mm) on Top Layer And Pad J1-19(16.75mm,11.675mm) on
Minimum Solder Mask Sliver Constraint: (0.1mm < 0.2mm) Between Pad J1-19(16.75mm,11.675mm) on Top Layer And Pad J1-20(17.25mm,11.675mm) on
Minimum Solder Mask Sliver Constraint: (0.154mm < 0.2mm) Between Pad J1-19(16.75mm,11.675mm) on Top Layer And Via (16.75mm,10.421mm) from
Minimum Solder Mask Sliver Constraint: (0.1mm < 0.2mm) Between Pad J1-2(8.25mm,11.675mm) on Top Layer And Pad J1-3(8.75mm,11.675mm) on Top
Minimum Solder Mask Sliver Constraint: (0.1mm < 0.2mm) Between Pad J1-20(17.25mm,11.675mm) on Top Layer And Pad J1-21(17.75mm,11.675mm) on
Minimum Solder Mask Sliver Constraint: (0.1mm < 0.2mm) Between Pad J1-21(17.75mm,11.675mm) on Top Layer And Pad J1-22(18.25mm,11.675mm) on
Minimum Solder Mask Sliver Constraint: (0.1mm < 0.2mm) Between Pad J1-22(18.25mm,11.675mm) on Top Layer And Pad J1-23(18.75mm,11.675mm) on
Minimum Solder Mask Sliver Constraint: (0.18mm < 0.2mm) Between Pad J1-22(18.25mm,11.675mm) on Top Layer And Via (18.513mm,10.399mm) from
Minimum Solder Mask Sliver Constraint: (0.1mm < 0.2mm) Between Pad J1-23(18.75mm,11.675mm) on Top Layer And Pad J1-24(19.25mm,11.675mm) on
Minimum Solder Mask Sliver Constraint: (0.177mm < 0.2mm) Between Pad J1-23(18.75mm,11.675mm) on Top Layer And Via (18.513mm,10.399mm) from
Minimum Solder Mask Sliver Constraint: (0.178mm < 0.2mm) Between Pad J1-24(19.25mm,11.675mm) on Top Layer And Via (19.501mm,10.399mm) from
Minimum Solder Mask Sliver Constraint: (0.1mm < 0.2mm) Between Pad J1-3(8.75mm,11.675mm) on Top Layer And Pad J1-4(9.25mm,11.675mm) on Top
Minimum Solder Mask Sliver Constraint: (0.1mm < 0.2mm) Between Pad J1-4(9.25mm,11.675mm) on Top Layer And Pad J1-5(9.75mm,11.675mm) on Top
Minimum Solder Mask Sliver Constraint: (0.1mm < 0.2mm) Between Pad J1-5(9.75mm,11.675mm) on Top Layer And Pad J1-6(10.25mm,11.675mm) on
Minimum Solder Mask Sliver Constraint: (0.1mm < 0.2mm) Between Pad J1-6(10.25mm,11.675mm) on Top Layer And Pad J1-7(10.75mm,11.675mm) on
Minimum Solder Mask Sliver Constraint: (0.1mm < 0.2mm) Between Pad J1-7(10.75mm,11.675mm) on Top Layer And Pad J1-8(11.25mm,11.675mm) on
Minimum Solder Mask Sliver Constraint: (0.1mm < 0.2mm) Between Pad J1-8(11.25mm,11.675mm) on Top Layer And Pad J1-9(11.75mm,11.675mm) on
Minimum Solder Mask Sliver Constraint: (0.104mm < 0.2mm) Between Pad J1-9(11.75mm,11.675mm) on Top Layer And Via (12.25mm,10.57mm) from
Minimum Solder Mask Sliver Constraint: (0.038mm < 0.2mm) Between Pad J1-S(20.9mm,14.55mm) on Top Layer And Via (20.931mm,16.138mm) from
Minimum Solder Mask Sliver Constraint: (0.105mm < 0.2mm) Between Pad J1-S(6.075mm,14.575mm) on Top Layer And Via (6.008mm,12.92mm) from
Minimum Solder Mask Sliver Constraint: (0.153mm < 0.2mm) Between Pad J2-1(11.25mm,25.05mm) on Top Layer And Via (11.25mm,23.497mm) from
Minimum Solder Mask Sliver Constraint: (0.194mm < 0.2mm) Between Pad J2-2(12.35mm,25.05mm) on Top Layer And Via (12.385mm,23.456mm) from
Minimum Solder Mask Sliver Constraint: (0.153mm < 0.2mm) Between Pad J2-5(15.65mm,25.05mm) on Top Layer And Via (15.963mm,23.497mm) from
Minimum Solder Mask Sliver Constraint: (0.141mm < 0.2mm) Between Pad J2-6(16.75mm,25.05mm) on Top Layer And Via (17.23mm,23.515mm) from
Minimum Solder Mask Sliver Constraint: (0.179mm < 0.2mm) Between Pad J2-7(17.85mm,25.05mm) on Top Layer And Via (17.23mm,23.515mm) from

Minimum Solder Mask Sliver (Gap=0.2mm) (All),(All)
Minimum Solder Mask Sliver Constraint: (0.059mm < 0.2mm) Between Pad J2-9(20.05mm,25.05mm) on Top Layer And Via (20.9mm,23.958mm) from Top
Minimum Solder Mask Sliver Constraint: (0.05mm < 0.2mm) Between Pad J2-SH(21.4mm,35.35mm) on Top Layer And Via (20.2mm,36.1mm) from Top
Minimum Solder Mask Sliver Constraint: (0.118mm < 0.2mm) Between Pad Q1-3(25.1mm,14.9mm) on Top Layer And Via (24.15mm,15.536mm) from Top
Minimum Solder Mask Sliver Constraint: (0.091mm < 0.2mm) Between Pad R10-1(18.301mm,20.95mm) on Top Layer And Via (18.226mm,19.984mm) from
Minimum Solder Mask Sliver Constraint: (0.075mm < 0.2mm) Between Pad R11-1(11mm,20.95mm) on Top Layer And Via (10.942mm,20mm) from Top
Minimum Solder Mask Sliver Constraint: (0.148mm < 0.2mm) Between Pad R2-1(8mm,20.95mm) on Top Layer And Via (7.973mm,19.927mm) from Top
Minimum Solder Mask Sliver Constraint: (0.129mm < 0.2mm) Between Pad R2-2(8mm,22.25mm) on Top Layer And Via (8.096mm,23.254mm) from Top
Minimum Solder Mask Sliver Constraint: (0.046mm < 0.2mm) Between Pad R8-1(14.4mm,20.95mm) on Top Layer And Via (14.353mm,20.029mm) from
Minimum Solder Mask Sliver Constraint: (0.075mm < 0.2mm) Between Pad R9-1(16.575mm,20.95mm) on Top Layer And Via (16.565mm,20mm) from Top
Minimum Solder Mask Sliver Constraint: (0.134mm < 0.2mm) Between Via (1.625mm,11.026mm) from Top Layer to Bottom Layer And Via
Minimum Solder Mask Sliver Constraint: (0.161mm < 0.2mm) Between Via (10.476mm,15.251mm) from Top Layer to Bottom Layer And Via
Minimum Solder Mask Sliver Constraint: (0.15mm < 0.2mm) Between Via (15.8mm,10.399mm) from Top Layer to Bottom Layer And Via
Minimum Solder Mask Sliver Constraint: (0.184mm < 0.2mm) Between Via (18.134mm,15.346mm) from Top Layer to Bottom Layer And Via
Minimum Solder Mask Sliver Constraint: (0.188mm < 0.2mm) Between Via (18.513mm,10.399mm) from Top Layer to Bottom Layer And Via
Minimum Solder Mask Sliver Constraint: (0.137mm < 0.2mm) Between Via (18.51mm,18.148mm) from Top Layer to Bottom Layer And Via
Minimum Solder Mask Sliver Constraint: (0.121mm < 0.2mm) Between Via (6.25mm,10.607mm) from Top Layer to Bottom Layer And Via
Minimum Solder Mask Sliver Constraint: (0.17mm < 0.2mm) Between Via (9.53mm,14.691mm) from Top Layer to Bottom Layer And Via

Board Clearance Constraint (Gap=0mm) ((OnLayer('Top Layer') OR OnLayer('Bottom Layer')))
Board Outline Clearance(Outline Edge): (1.25mm < 1.5mm) Between Board Edge And Pad C3-1(1.95mm,9.05mm) on Top Layer
Board Outline Clearance(Outline Edge): (1.25mm < 1.5mm) Between Board Edge And Pad C3-2(1.95mm,7.45mm) on Top Layer
Board Outline Clearance(Outline Edge): (1.3mm < 1.5mm) Between Board Edge And Pad C5-1(11.35mm,38mm) on Bottom Layer
Board Outline Clearance(Outline Edge): (1.3mm < 1.5mm) Between Board Edge And Pad C5-2(9.75mm,38mm) on Bottom Layer
Board Outline Clearance(Outline Edge): (0.235mm < 1.5mm) Between Board Edge And Pad D1-1(25.965mm,10.5mm) on Top Layer
Board Outline Clearance(Outline Edge): (1.34mm < 1.5mm) Between Board Edge And Pad IC2-1(15.58mm,38.21mm) on Bottom Layer
Board Outline Clearance(Outline Edge): (1.34mm < 1.5mm) Between Board Edge And Pad IC2-2(17.48mm,38.21mm) on Bottom Layer
Board Outline Clearance(Outline Edge): (0.55mm < 1.5mm) Between Board Edge And Pad Q1-2(26.05mm,12.9mm) on Top Layer
Board Outline Clearance(Outline Edge): (Collision < 1.5mm) Between Board Edge And Pad Q1-3(25.1mm,14.9mm) on Top Layer
Board Outline Clearance(Outline Edge): (1.065mm < 1.5mm) Between Board Edge And Pad R12-1(1.64mm,38.51mm) on Bottom Layer
Board Outline Clearance(Outline Edge): (1.165mm < 1.5mm) Between Board Edge And Pad R12-2(1.64mm,37.21mm) on Bottom Layer
Board Outline Clearance(Outline Edge): (1.14mm < 1.5mm) Between Board Edge And Pad S1-3(3.576mm,38.53mm) on Bottom Layer
Board Outline Clearance(Outline Edge): (1.14mm < 1.5mm) Between Board Edge And Pad S1-3*(7.64mm,38.53mm) on Bottom Layer
Board Outline Clearance(Outline Edge): (Collision < 0.5mm) Between Board Edge And Track (0.65mm,34.765mm)(0.65mm,34.765mm) on Top Layer
Board Outline Clearance(Outline Edge): (Collision < 0.5mm) Between Board Edge And Track (0.65mm,34.765mm)(0.65mm,35.993mm) on Top Layer
Board Outline Clearance(Outline Edge): (Collision < 0.5mm) Between Board Edge And Track (0.65mm,35.993mm)(0.65mm,37.619mm) on Bottom Layer
Board Outline Clearance(Outline Edge): (Collision < 0.5mm) Between Board Edge And Track (0.65mm,37.619mm)(1.024mm,37.993mm) on Bottom Layer

Quantity	Designator	Comment	Footprint
6	C1, C3, C4, C5, C7, C14	0.1 µF	CAP 0805_2012
1	C2	15 pF	CAP 0805_2012
4	C6, C9, C11, C13	10 µF	CAP 0805_2012
2	C8, C10	100 µF	CAP POL 1411_3528
1	C12	1 µF	CAP 0805_2012
1	D1	LED MID PWR 5600K 95CRI 3030	LUMINUS MP-3030-110
1	IC1	ESP-32S	ESP32s
1	IC2	Si2300DS	DIODES SOT-23-3
1	IC3	XC6206P282MR 2.8V	TI SOT-23-3 DBZ
1	IC4	ESP-PSRAM64H	ALPHAOMEGA SO8 SOP-8L
1	IC5	XC6206P122MR-G 1.2V	TI SOT-23-3 DBZ
1	J1	OV2640 FPC 24pin	GCT FFC2B28-24
1	J2	Micro SD Socket	OOTDTY Y98E7HH800293
2	P1, P2	Header 8	HDR1X8
1	Q1	S8050 SOT-23-3	MCCSEMI SOT-23-3
4	R1, R2, R3, R7	4.7 kOhms	RES 0603_1608
2	R4, R15	1 kOhms	RES 0603_1608
5	R5, R6, R12, R14, R16	10 kOhms	RES 0603_1608
4	R8, R9, R10, R13	47 kOhms	RES 0603_1608
1	R11	NC	RES 0603_1608
1	S1	EVQ-P7A01P	EVQ-P7A01P
5	TP1, TP2, TP3, TP4, TP5	Test point	TEST_POINT