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Graphene Barristor, a Triode Device with a Gate-Controlled Schottky Barrier

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Despite several years of research into graphene electronics, sufficient on/off current ratio I_{on}/I_{off} in graphene transistors with conventional device structures has been impossible to obtain. We report on a three-terminal active device, a graphene variable-barrier "barristor" (GB), in which the key is an atomically sharp interface between graphene and hydrogenated silicon. Large modulation on the device current (on/off ratio of 10^5) is achieved by adjusting the gate voltage to control the graphene-silicon Schottky barrier. The absence of Fermi-level pinning at the interface allows the barrier's height to be tuned to 0.2 electron volt by adjusting graphene's work function, which results in large shifts of diode threshold voltages. Fabricating GBs on respective 150-mm wafers and combining complementary p- and n-type GBs, we demonstrate inverter and half-adder logic circuits.

The triode, composed of a diode and a grid in a vacuum tube, was the first three-terminal active device that had been used to amplify and to switch electric signals, which led to the technical innovations for modern electronics in the early 20th century (*1*). Solid-state transistors and integrated circuits (ICs) based on silicon were more practical for complicated logic circuits and thus replaced triodes. Although silicon transistors have continued to improve their speed and integration density, they now near the potential limit where further reduction of channel length causes inevitable leakage currents (*2*). To present an alternative route for overcoming these challenges, we introduce a class of three-terminal devices based on a graphene-silicon hybrid device that mimics a triode operation. The key device function takes place at the electrostatically gated graphene/silicon interface where a tunable Schottky barrier controls charge transport across a vertically stacked structure. We named this barrier variable device, which is a solid-state descendant of the triode, "barristor."

Graphene is a zero-gap semiconductor whose Fermi energy can be adjusted by electrostatic gating owing to its two-dimensional (2D) nature (*3*–*5*). Because graphene is metallic at a sufficiently large Fermi energy, a Schottky barrier (SB) forms at the interface between the doped graphene and the semiconductor (*6*–*10*). However, SB between graphene and a well-controlled semiconductor surface, such as hydrogen-terminated Si, is different from a conventional metal-semiconductor SB in two important ways. First, the formation of interface states is suppressed in graphene-semiconductor junctions (*11*) because the interaction between chemically inert graphene and a completely saturated semiconductor surface—that is, one without dangling bonds—is negligible (*12*). Second, graphene's work function (WF) can be adjusted electrostatically over a wide range by tuning the Fermi energy (E_F) via the electrostatic field effect (*13*, *14*). We could realize a graphene barristor (GB) by combining these two effects, as also shown in (*15*).

A schematic diagram of the GB structure and its top view are shown in Fig. 1, A and B. Single-layer graphene in contact with the source electrode forms the SB at its interface with the silicon surface at the drain contact. Two kinds of GBs can be formed depending on the silicon doping type: n-type GB at n-type silicon and p-type GB at p-type silicon. We used transmission electron microscopy (TEM) to develop an optimal transfer process for graphene onto Si substrates to create atomically sharp interfaces (inset of Fig. 1C), which minimizes atomic defects or silicon dioxide formation that can create charge trapping sites. Figure 1C displays a typical Schottky diode characteristic of a p-type GB with an optimized graphene/Si interface. The forward characteristic at a low bias showed a diode ideality factor $\eta_{id} \approx 1.1$ for this particular device. The ideality factor we obtained in our GB is considerably better than those reported in exfoliated graphene-Si junctions (*9*), confirming the high interfacial quality in our GBs.

The recent availability of large-scale graphene growth through chemical vapor deposition (CVD) techniques (*16*–*20*) allowed us to integrate graphene devices at wafer scales using conventional semiconductor microfabrication processes (*21*). Large-scale integration has not been possible for similar devices such as p-n diodes demonstrated in highly customized and suspended semiconducting

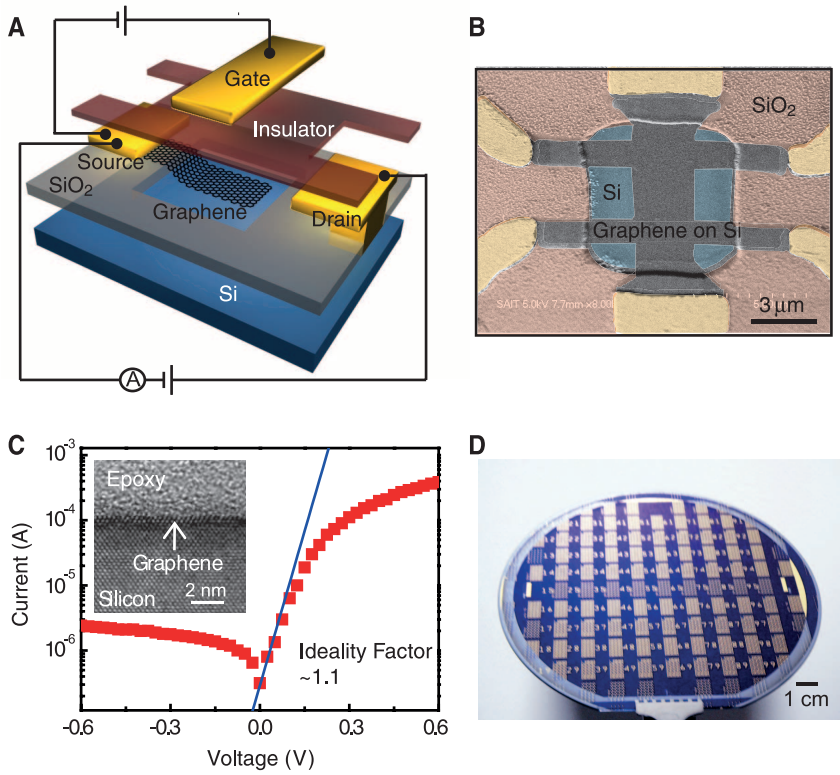

Fig. 1. Graphene barristor. (**A**) A schematic diagram to show the concept of a GB. (**B**) False-colored scanning electron microscopy image of the GB before the top gate fabrication process. (**C**) Current versus bias voltage characteristic of a GB at a fixed gate voltage V_{gate} = 0 V, showing a Schottky diode characteristic. The inset shows a TEM image of graphene/silicon junction. No native oxide or defect is seen in the image. (**D**) A photograph of ~2000 GB arrays implemented on a 6-inch wafer.

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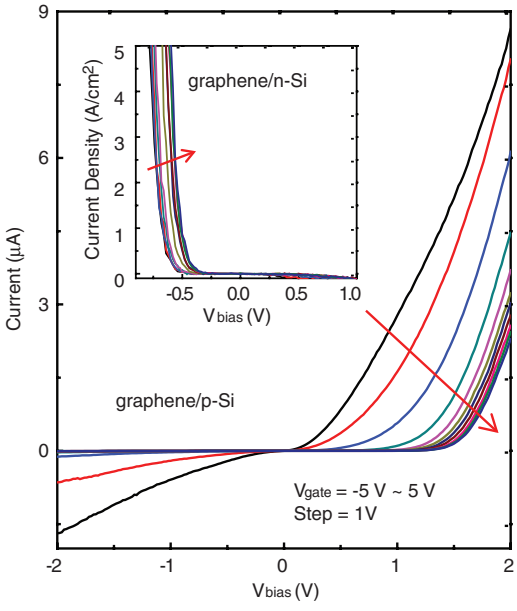

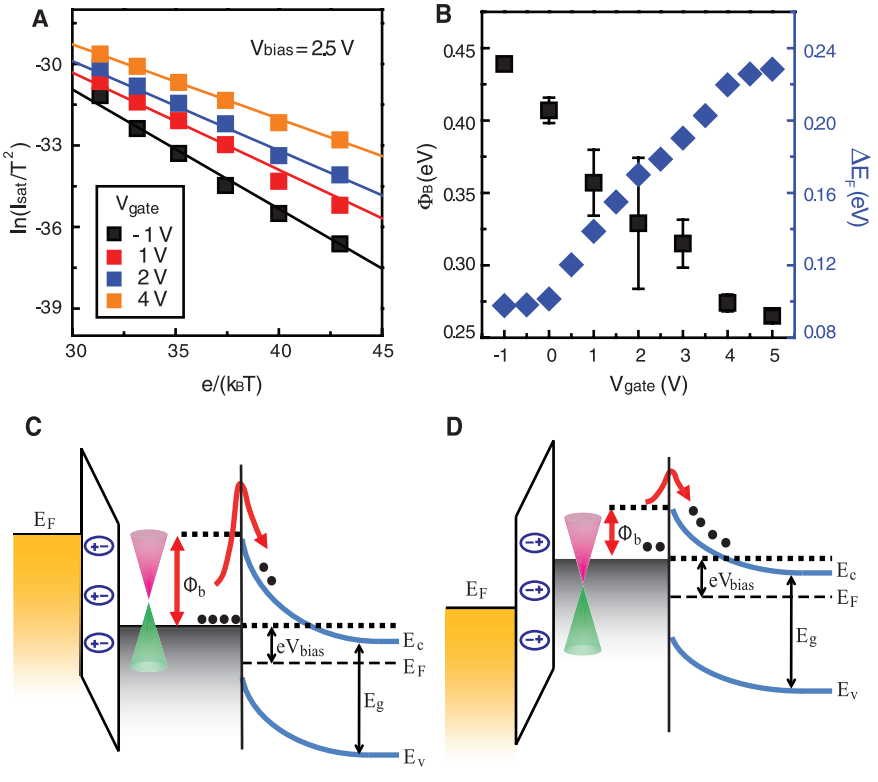

Fig. 2. Graphene barristor characteristics. The current and bias voltage characteristics of p-type (main panel) and n-type (inset) GBs at various fixed V_{gate} values. V_{gate} varies in the range –5 to 5 V, with a step size of 1 V for each curve. The red arrow indicates the direction of increasing V_{gate}.

Fig. 3. (**A**) Temperature-dependent diode characteristic. The saturation current of the n-type GB, I_{sat}, is obtained by measuring the current at V_{bias} = 2.5 V at various temperature and gate voltage values. Different colors are used for different V_{gate} from –1 to 4 V with 1- to 2-V step variation. The line fit for each V_{gate} value is drawn to yield the Schottky barrier height from the slope of the fitted line. (**B**) The SB height obtained from the fit in (A) as a function of V_{gate} (black squares, left *y* axis). The graphene Fermi energy on the right *y* axis is obtained from Hall measurement at the same gate voltage V_{gate}. Monotonic increase and decrease of observed SB height is consistent with the band diagrams in (C) and (D), respectively. (**C** and **D**) Schematic band diagrams of GB with the EFE generated by the gate on the top of graphene. Applying negative voltage on the gate induces holes in graphene, increasing its work function and increasing the Schottky barrier height. As a result, the reverse current across the Schottky barrier decreases (C). Positive gate voltage decreases the Schottky barrier height and increases reversed current (D).

nanotubes (*22*, *23*). We demonstrated integration of gate-tunable GB arrays on a 6-inch wafer by transferring a single-layer graphene grown by CVD (*20*, *24*) onto a prepatterned Si substrate. Figure 1D shows an array of 2000 devices on a 6-inch (150-mm) wafer. At room temperature, the range of the ideality factor and the current density of GBs are found to be 1.1 to 4.0 and 10^1 to 10^4 A/cm^2, respectively (see figs. S3 to S5 in the supplementary materials) (*25*), where the variation is due to the different wafer batches. These GB devices exhibited >90% device yield, with excellent uniformity in terms of device characteristics across the wafer with appropriate current level (fig. S2).

We could electrostatically modulate the graphene's WF through the top gate electrode and gate dielectric above the graphene (*14*), which resulted in a variation on the SB height. Because the injection of the majority carriers from graphene to silicon is determined by the SB height ϕ_b, the top gate then directly controls the magnitude of the current across the source and the drain. The main panel of Fig. 2 shows the characteristic of p-type GB at various gate voltages (V_{gate}). The rectification behavior of the GB was demonstrated in that the GB current (I_{SD}) increased steeply as the bias voltage (V_{bias}) surpassed the "turn-on" voltage, V_{TO}. V_{TO} could be adjusted between 0 V and 1.3 V as V_{gate} was modulated between –5 and 5 V, the range needed to keep this GB in p-type operation. Similar triode behavior was observed in n-type GBs (Fig. 2 inset), where the bias polarity was reversed because electrons become the majority carrier. The large modulation of the GB current was indicative of a large variation in the SB height, caused by the electric field effect (EFE) from V_{gate}.

To quantitatively analyze the device characteristic, we used the diode equation

$$I = AA^*T^2\exp\left(\frac{-q\phi_b}{k_BT}\right)\left[\exp\left(\frac{qV_{bias}}{\eta_{id}k_BT}\right) - 1\right]$$

where A is the area of the Schottky junction, A* is the effective Richardson constant, q is the elementary charge, k_B is the Boltzmann constant, and T is the temperature. Quantitative analysis of the SB height ϕ_b can be done by investigating the temperature dependence of the GB current in the reverse bias saturation regime [$\exp(qV_{bias}/\eta_{id}k_BT) << 1$]. Here, the diode current becomes insensitive to V_{bias} and $I_{sat} \propto T^2\exp\left(\frac{-q\phi_b}{k_BT}\right)$. Figure 3A shows a plot of ln (I_{sat}/T^2) versus q/k_BT in the reverse bias saturation regime. We estimated the SB height ϕ_b for a given gate voltage V_{gate} from the slope of each curve. Figure 3B shows the resulting SB heights obtained as a function of V_{gate}. V_{gate} increased from 0 to 5 V, and ϕ_b decreased substantially from 0.45 eV to 0.25 eV. We attributed the drastic change in ϕ_b to the EFE-induced Fermi level change, ΔE_F. Indeed, as shown in Fig. 3B, the measured variation of ϕ_b, $\Delta\Phi_B$ =

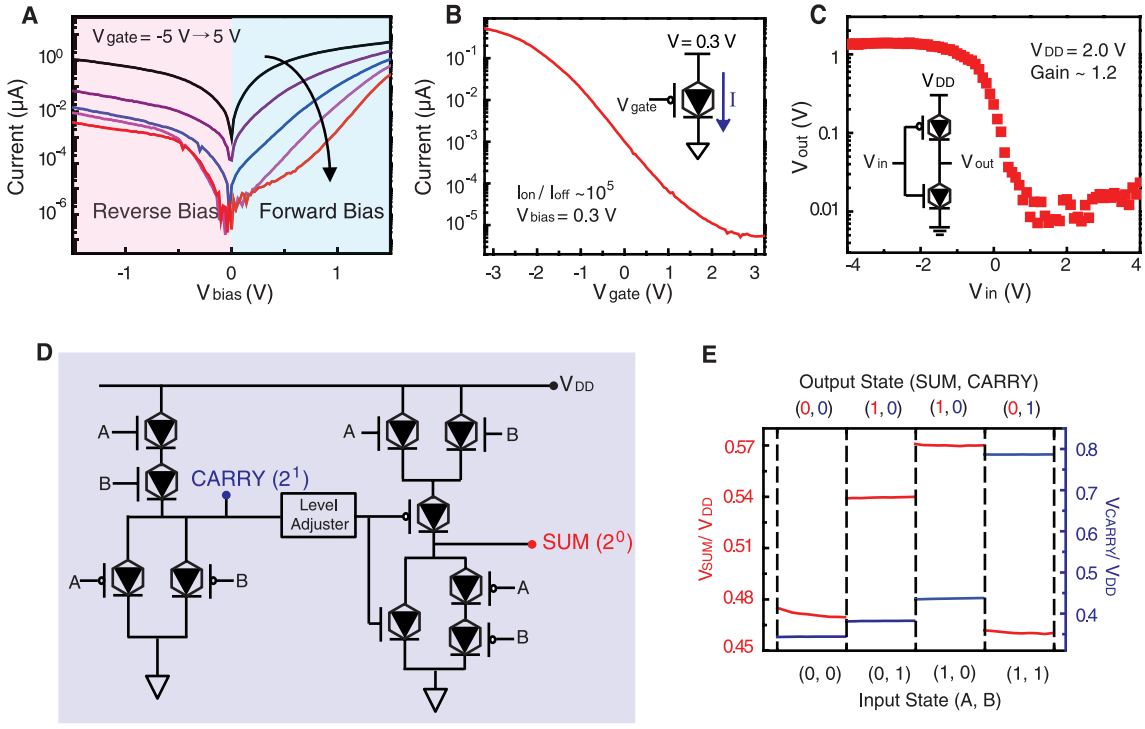

Fig. 4. (**A**) Switching behavior of p-type GB in reverse (orange background) and forward (blue background) bias regimes. The GB current is plotted against the source drain bias at various fixed gate voltages. V_{gate} varies in the range of −5 to 5 V, with a step of 2 V. The black arrow indicates the direction of increasing V_{gate}. (**B**) The forward diode current as a function of gate V_{gate} at fixed bias V_{bias} = 0.3 V. Unipolar control of forward current with the ratio of 10^5 is obtained. (**C**) Inverter characteristics obtained from integrated n- and p-type GBs and schematic circuit diagram for the inverter. Positive supply voltage (V_{DD}) is connected to p-type GB, and the gain of the inverter is ~1.2. (**D**) Schematic of circuit design of a half-adder implemented with n- and p-type GBs. (**E**) Output voltage levels for SUM and CARRY for four typical input states.

$\phi_b - \phi_b(\Delta E_F = 0)$, was well correlated to the change of ΔE_F, obtained independently by converting the measured Hall carrier density (n_H) using $\Delta E_F = \hbar v_F \sqrt{\pi n_H}$, where $v_F = 10^6$ m/sec was used for the Fermi velocity of graphene. We observed that $\Delta\Phi_B \approx -\Delta E_F$ for a wide range of V_{gate} (fig. S7), which suggests that the WF modulation of graphene in the absence of Fermi-level pinning is fully responsible for the variation of ϕ_b as depicted in Fig. 3, C and D.

The absence of Fermi-level pinning, one of the major sources for high device resistance in silicon electronics (*26*), comes from the suppression of the surface states at the interface of silicon and graphene. In our GB, we could eliminate the "Fermi-level pinning" and manipulate the SB height as in the ideal Schottky-Mott limit (Fig. 3B), where the SB height is controlled through the selection of metal and semiconductor with appropriate WFs (*27*, *28*).

Two different types of GB operations are possible, as shown in Fig. 4A. The first type uses the GB in the reverse-biased regime (orange shaded region in Fig. 4A). Here, a conventional FET-like device operation could be possible; that is, the GB current, I, had the tendency to saturate at large reverse bias voltages, and the on-state current, I_{on}, had been modulated by V_{gate}. The off-state current, I_{off}, was determined at the greatest attainable SB, which yielded an I_{on}/I_{off} ratio of ~300 in Fig. 4A. The second type of operation could be realized by using the device in the forward biasing region (the blue shaded region in Fig. 4A). In this regime, the diode current did not saturate as V_{bias} increased but deviated from a typical FET-like device operation. However, near the diode turn-on regime, I varied by several orders of magnitude as V_{gate} changed, resulting in a switching operation with a large I_{on}/I_{off} ratio. Figure 4B shows the switching characteristic of the diode current in a forward-biased p-type GB, demonstrating a high I_{on}/I_{off} ratio of ~10^5. We note that the large I_{on}/I_{off} ratio and small off-state current overcame the key obstacle in graphene-based electronics.

Three-terminal operation of GB offers various integrated device functionalities. Similar to the complementary metal-oxide semiconductor inverter operation, a series connection of n- and p-type complimentary GBs inverted the input signal V_{in} to its inverse V_{out} (Fig. 4C). The low V_{out} originated from the high on/off current ratio of GBs, which implies that only a small amount of static off-state power would be consumed. As for more complicated logic applications, we demonstrated a half-adder circuit built from n- and p-type 10 GBs. The schematic with two inputs (A and B) and two outputs (SUM and CARRY) is shown in Fig. 4D. The measured output voltage levels are represented in Fig. 4E. These results suggest that the GB can provide a route to realize high-speed logic applications (*29*, *30*) based on graphene-semiconductor hybrid devices.

In conclusion, our GB suggests the possibility of a graphene logic device by achieving a high on/off ratio of ~10^5, which exceeds the minimum requirement for logic transistors. Furthermore, the on/off ratio and the current density can be improved with well-developed semiconductor processes because there is not a fundamental (or structural) limit. GB also has an advantage in lateral scaling because the barrier is formed vertically.

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Supplementary Materials

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Materials and Methods
Supplementary Text
Figs. S1 to S10
References

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Tailoring Electrical Transport Across Grain Boundaries in Polycrystalline Graphene

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Graphene produced by chemical vapor deposition (CVD) is polycrystalline, and scattering of charge carriers at grain boundaries (GBs) could degrade its performance relative to exfoliated, single-crystal graphene. However, the electrical properties of GBs have so far been addressed indirectly without simultaneous knowledge of their locations and structures. We present electrical measurements on individual GBs in CVD graphene first imaged by transmission electron microscopy. Unexpectedly, the electrical conductance improves by one order of magnitude for GBs with better interdomain connectivity. Our study suggests that polycrystalline graphene with good stitching may allow for uniformly high electrical performance rivaling that of exfoliated samples, which we demonstrate using optimized growth conditions and device geometry.

Most three-dimensional electronic materials produced in macroscopic quantities are not homogeneous but incorporate numerous classes of dislocations and defects that degrade electrical performance (*1*). Although large-scale graphene films produced by chemical vapor deposition (CVD) (*2*, *3*) might be expected to be nearly defect free, recent transmission electron microscopy (TEM) studies (*4*, *5*) have shown that these films are polycrystalline. Electrical transport between single-crystal domains could be affected by scattering at the grain boundary (GB), as has been shown theoretically (*6*–*9*). Although TEM has provided a fast and accurate means to identify and image the structure of GBs in CVD graphene, the electrical impact of GBs has so far been studied only indirectly in experiments. Previous work by Huang *et al*. detects no measurable electrical resistance from GBs within instrument limits (*4*), and ensemble measurements done by various groups find very weak correlation between the average domain size of the graphene film and overall device mobility (*4*, *10*). In contrast, Yu *et al*. and Jauregui *et al*. inferred the presence of GBs from the shape of partially grown graphene islands and extracted a finite GB resistance from their measurements (*11*, *12*). The ambiguity in these findings arose from a lack of knowledge of the precise domain morphology for the graphene measured. To this end, we have devised an experimental scheme to first image (using TEM) and then electrically address individual domains and GBs in polycrystalline graphene. Such a capability is crucial, because graphene domain structures generated during synthesis form nontrivial patterns that are strongly dependent on growth conditions and difficult to predict a priori.

In Fig. 1A, we show false-color dark-field TEM (DF-TEM) images of graphene films grown under three different conditions [see supplementary materials (*13*)] taken in a manner similar to Huang *et al*. (*4*). Each colored region corresponds to a separate graphene crystalline domain with distinct lattice orientation. The image is generated by using an aperture in the back-focal plane of the microscope to collect electrons diffracted from only a narrow range of angles by the graphene lattice. In general, different graphene domains produce a diffraction pattern rotated with respect to one another, so each domain can be imaged separately, colorized, and then combined.

In growth A, graphene was synthesized under high reactant flow rates, which produced fast growth and also small average domain size $D \approx 1$ μm. Graphene from growth B was synthesized in a diluted methane environment, whereas growth C was further enclosed in copper foil, after Li *et al*. (*14*), resulting in slower growths. The latter films were terminated after only partial surface coverage to highlight their growth structures. In subsequent microscopy and electrical measurements, however, we used continuous films, for which growth B yielded $D \approx 10$ μm and growth C, $D \approx 50$ μm. The overall shapes of partially grown graphene islands in growth B were polygons, whereas growth C generally formed flowered islands (fig. S1). Despite

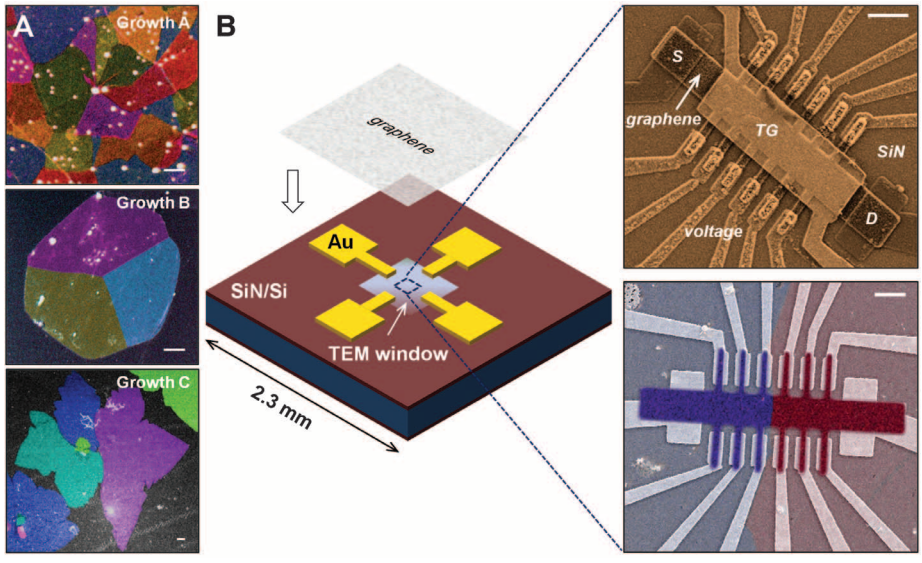

Fig. 1. (**A**) Composite false-color DF-TEM images of CVD graphene produced using three different growth conditions—A, B, and C—yielding average domain size *D* of 1, 10, and 50 μm, respectively, in continuous films. (**B**) (Left) Schematic of specially fabricated TEM chip compatible with electron-beam lithography and electrical measurements. (Top right) SEM image of top-gated, graphene Hall bar device. (Bottom right) Overlaid SEM and DF-TEM images showing device crossing a single GB of two domains from growth C. Scale bars, 1 μm.

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