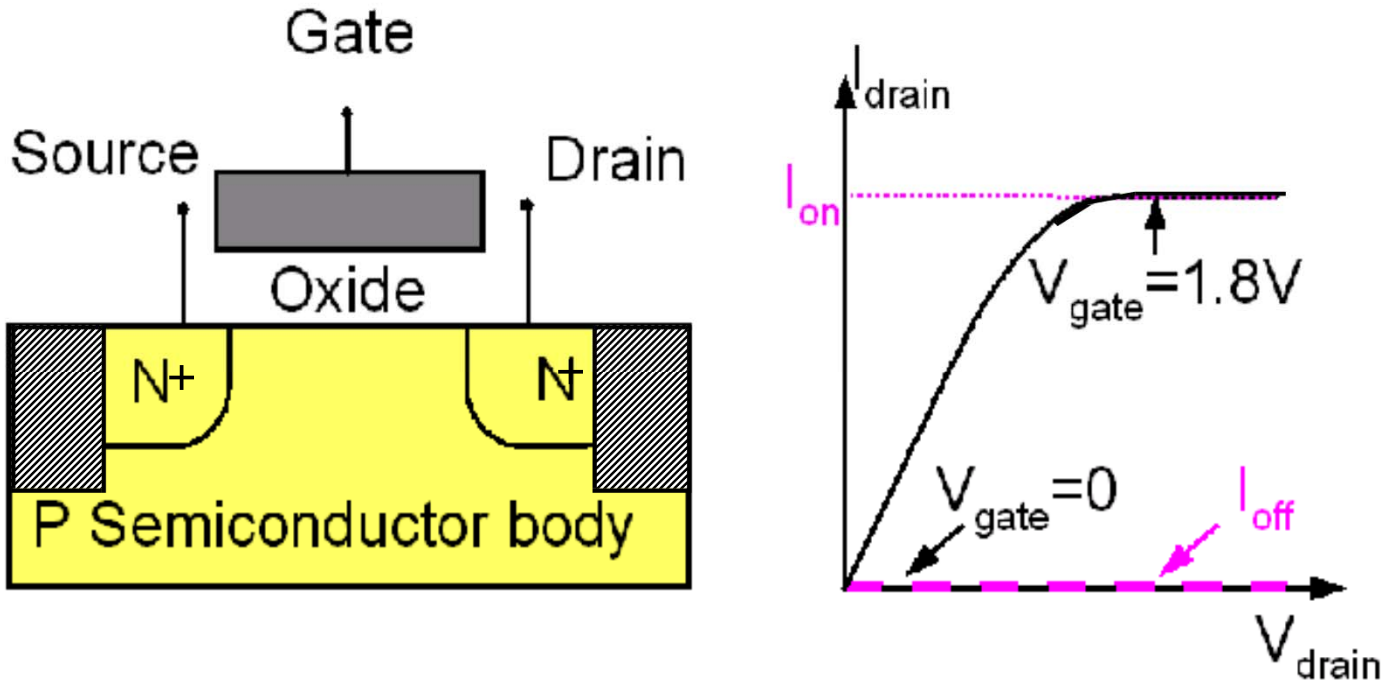
MOSFET

The MOSFET (MOS Field-Effect Transistor) is the building block of Gb memory chips, GHz microprocessors, analog, and RF circuits.

Match the following MOSFET characteristics with their applications:

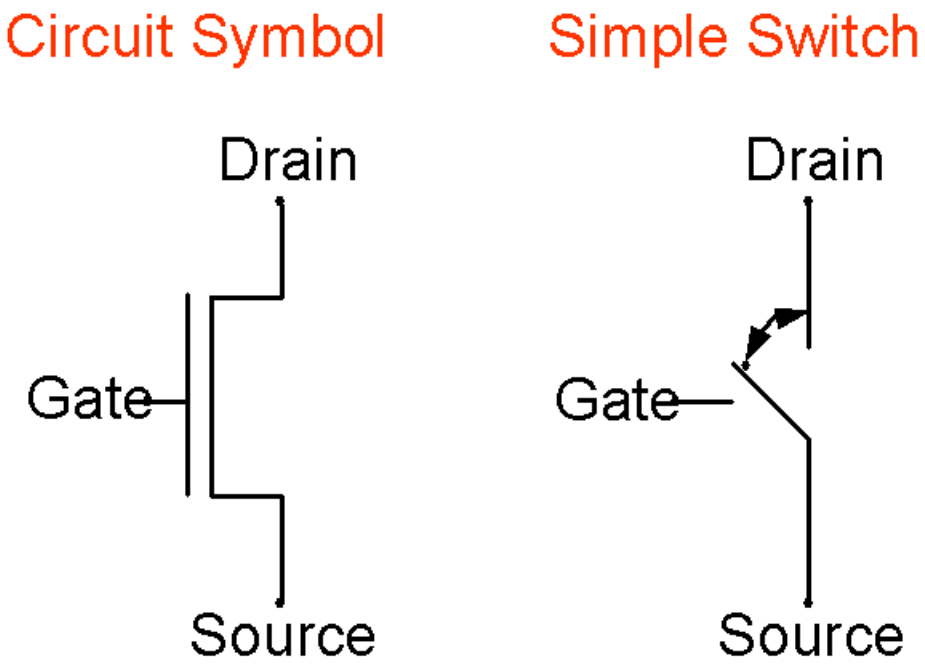
- small size
- high speed
- low power
- high gain

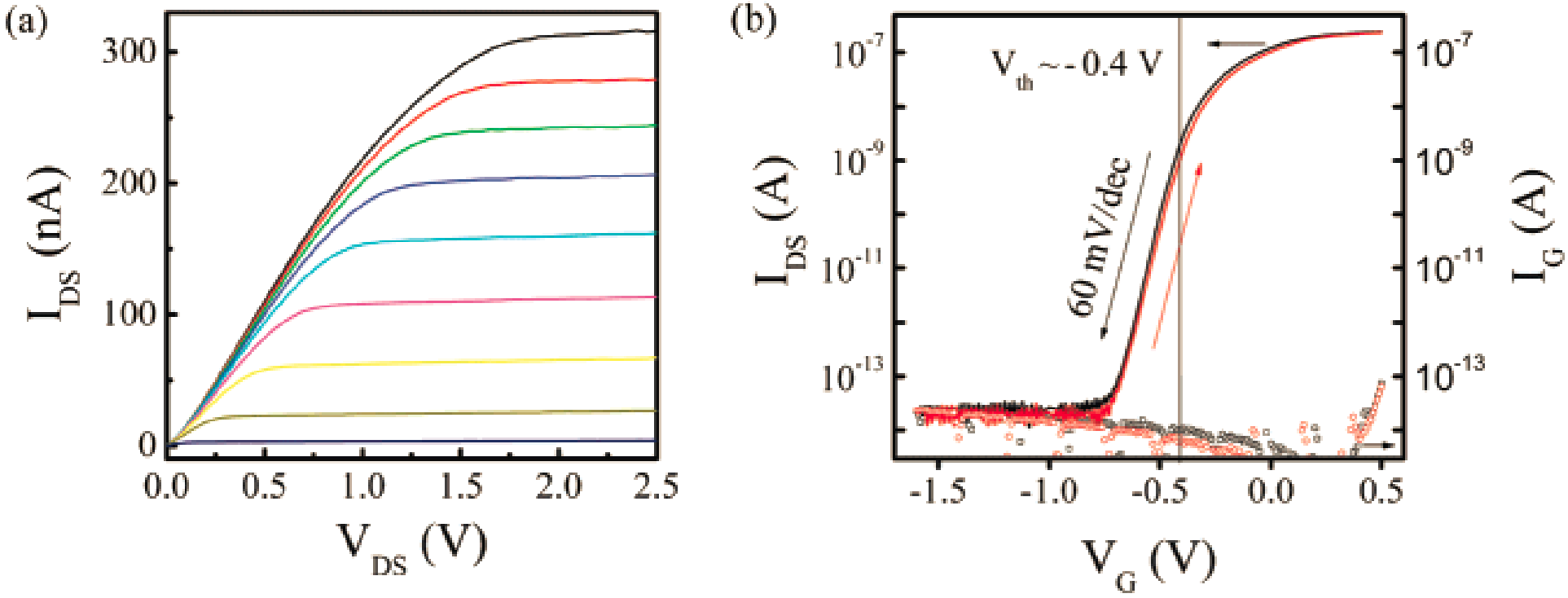
Basic MOSFET structure and IV characteristics



What is desirable: large I_{on}, small I_{off}

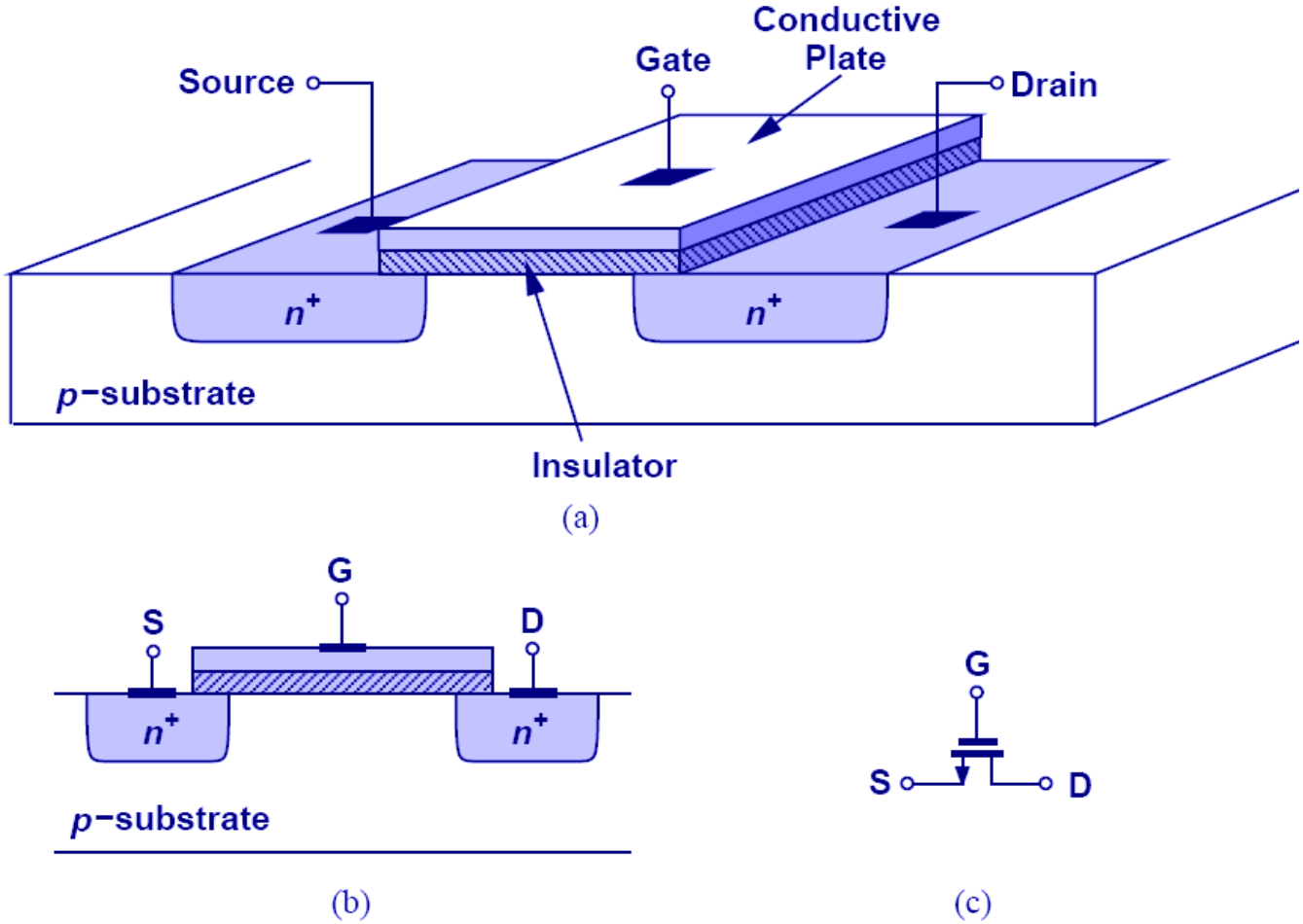
Two ways of representing a MOSFET:





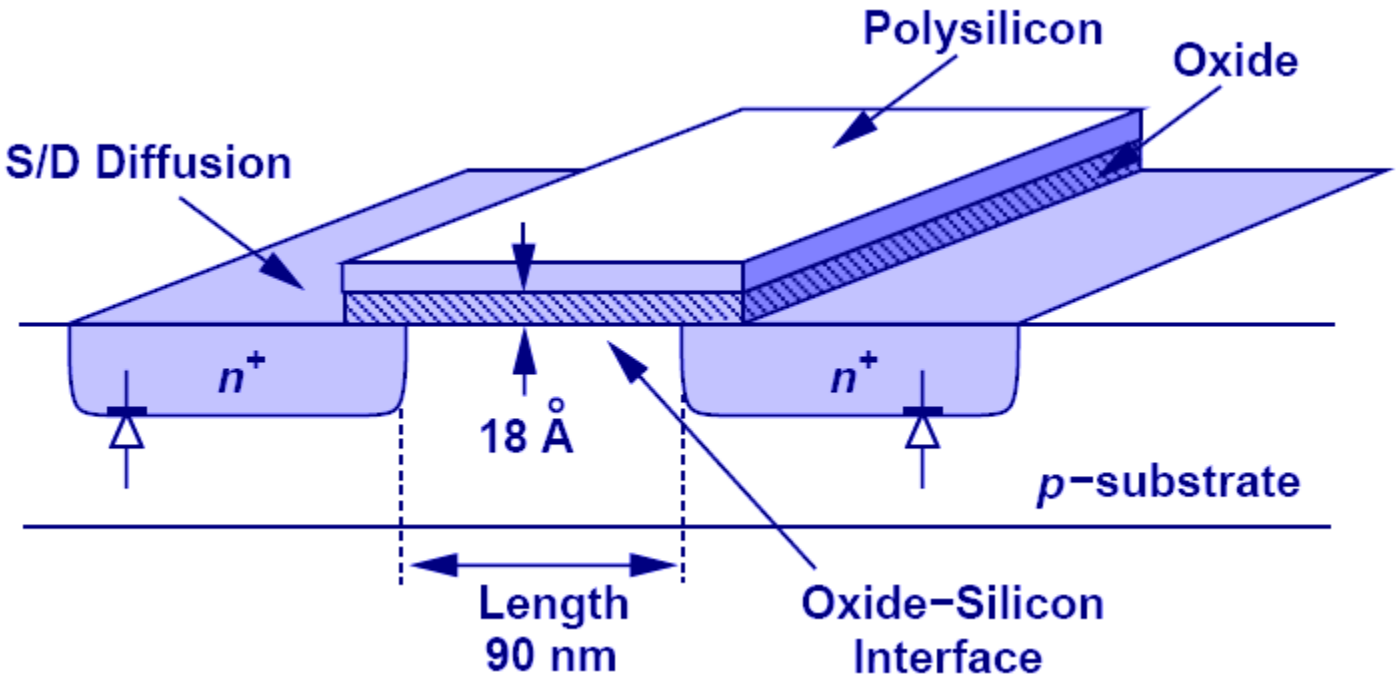
R. M. Ma et al. *Nano Lett.* 7 (2007) 3300

Structure and Symbol of MOSFET



- This device is symmetric, so either of the n+ regions can be source or drain.

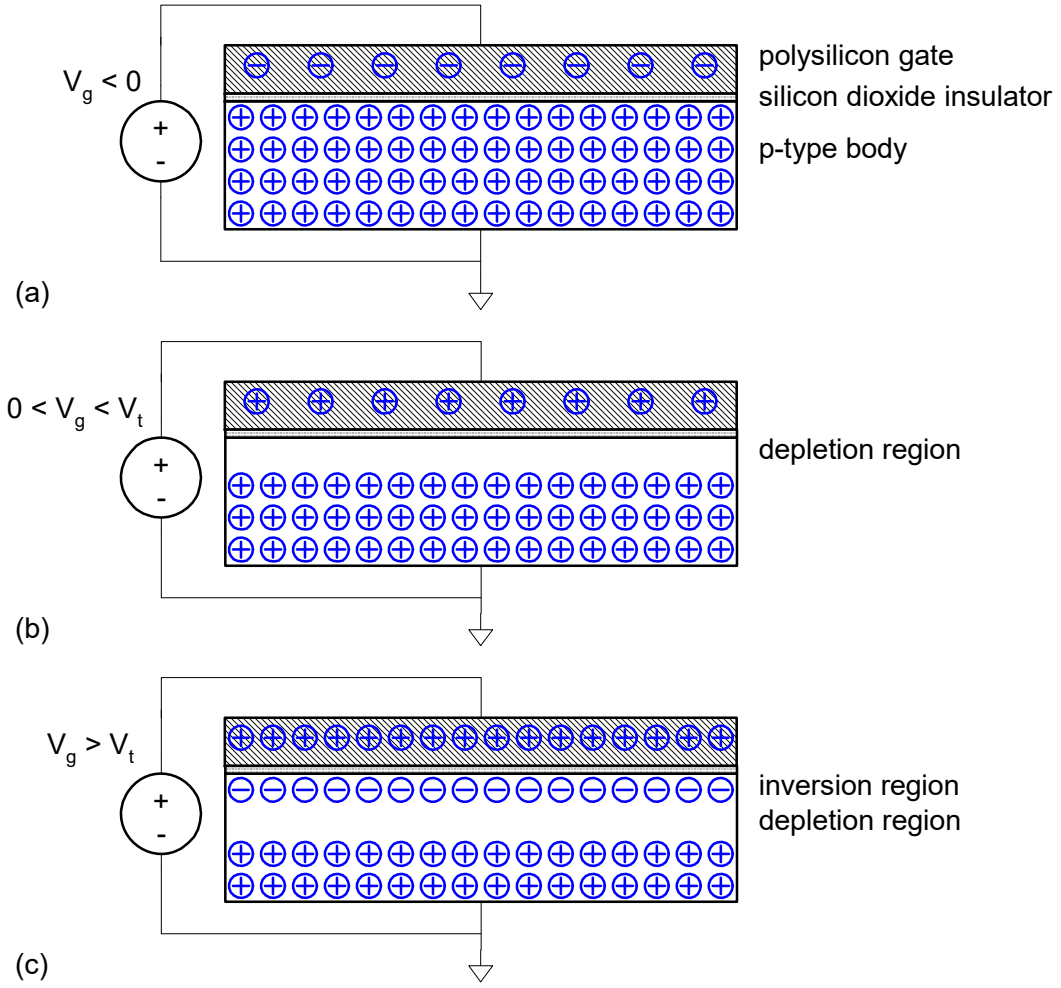
State of the Art MOSFET Structure



- The gate is formed by polysilicon, and the insulator by Silicon dioxide.

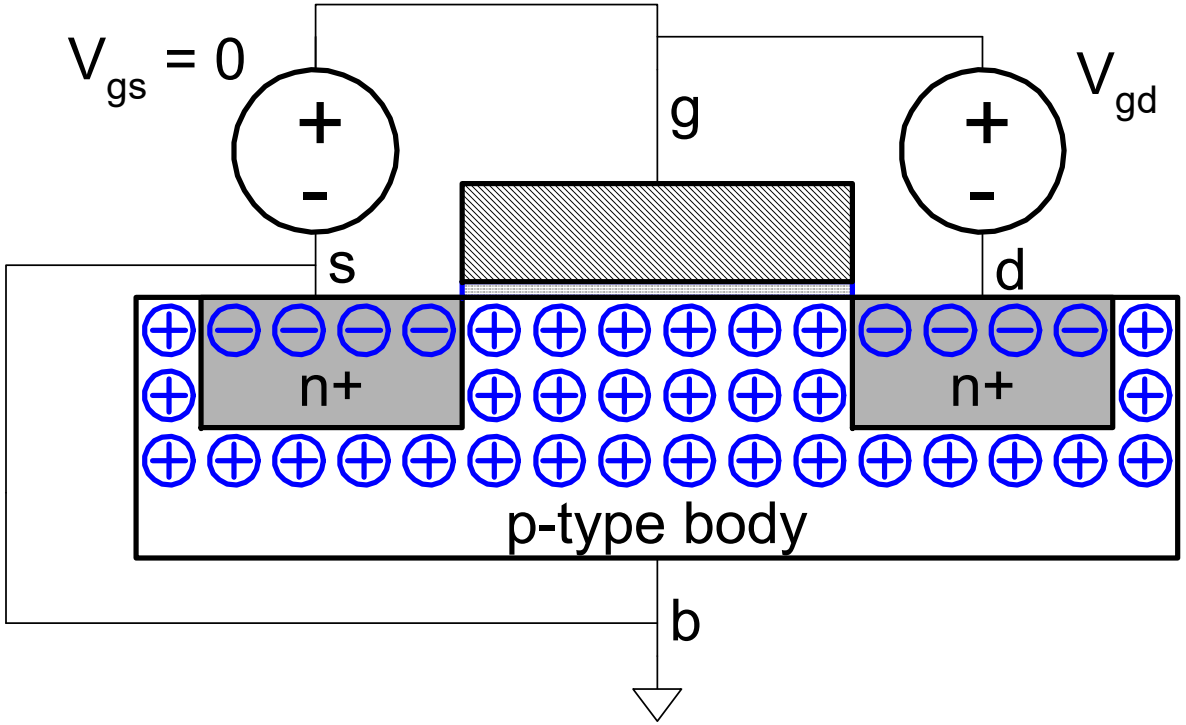
MOS Capacitor

- Gate and body form MOS capacitor
- Operating modes
  - Accumulation
  - Depletion
  - Inversion



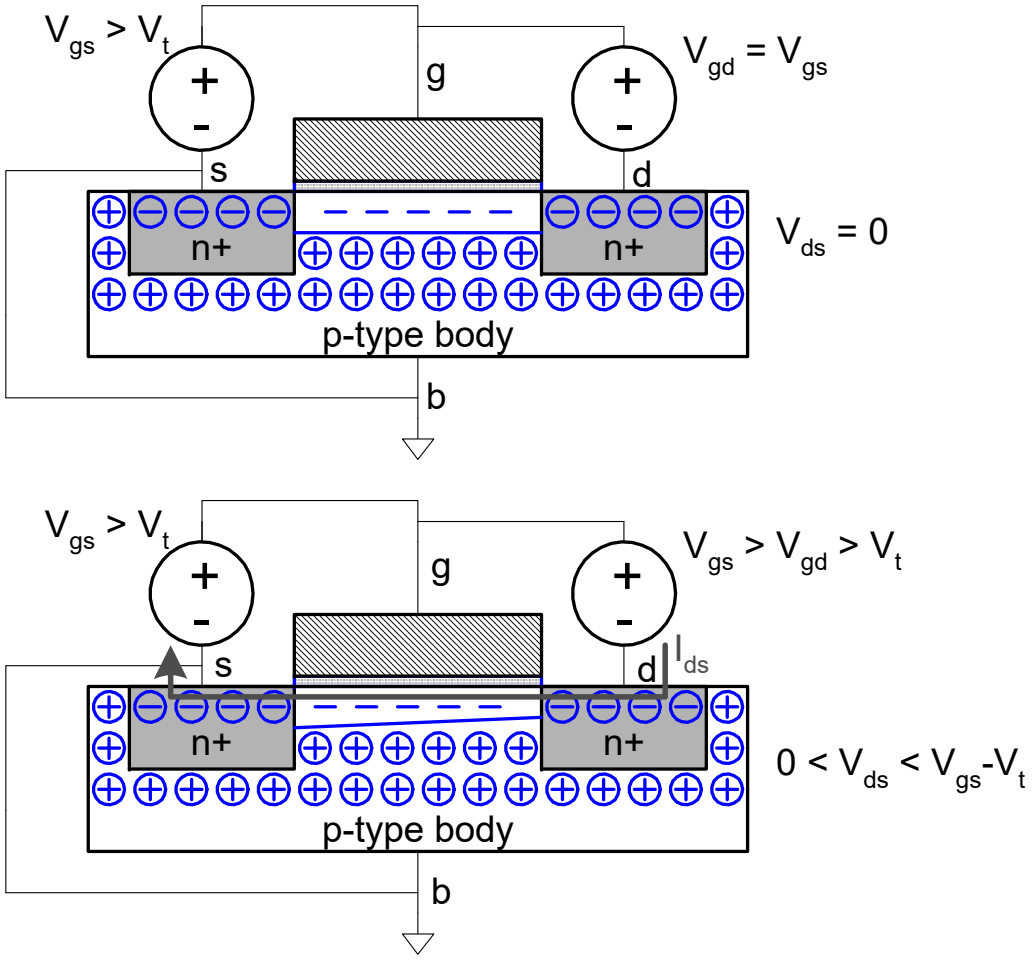
nMOS Cutoff

- No channel
- $I_{ds} = 0$



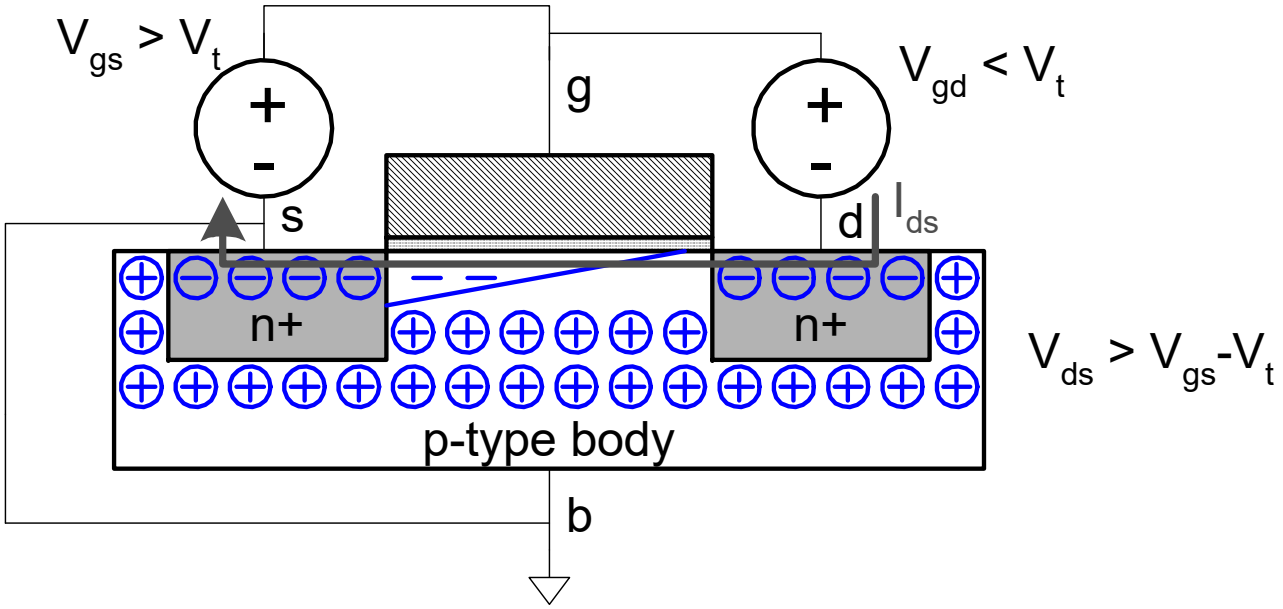
nMOS Linear

- Channel forms
- Current flows from d to s
  - e^- from s to d
- I_{ds} increases with V_{ds}
- Similar to linear resistor

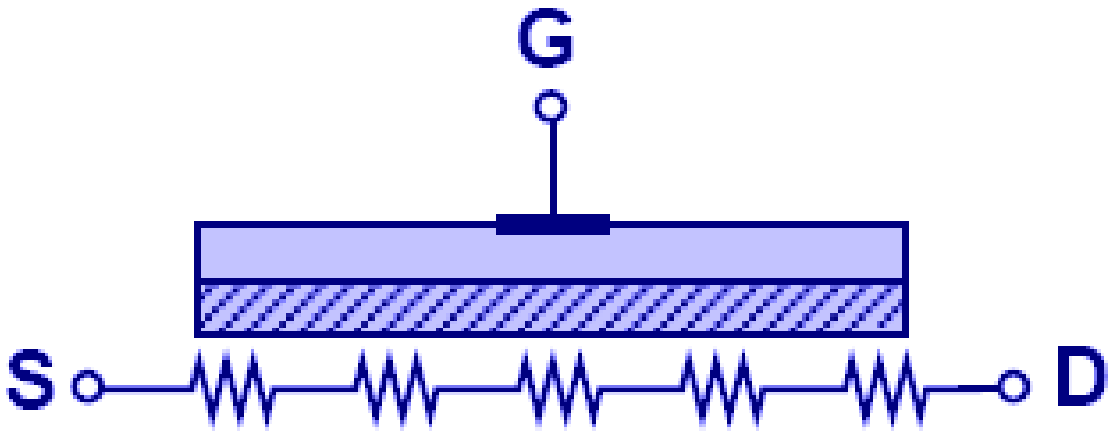


nMOS Saturation

- Channel pinches off
- I_{ds} independent of V_{ds}
- We say current saturates
- Similar to current source

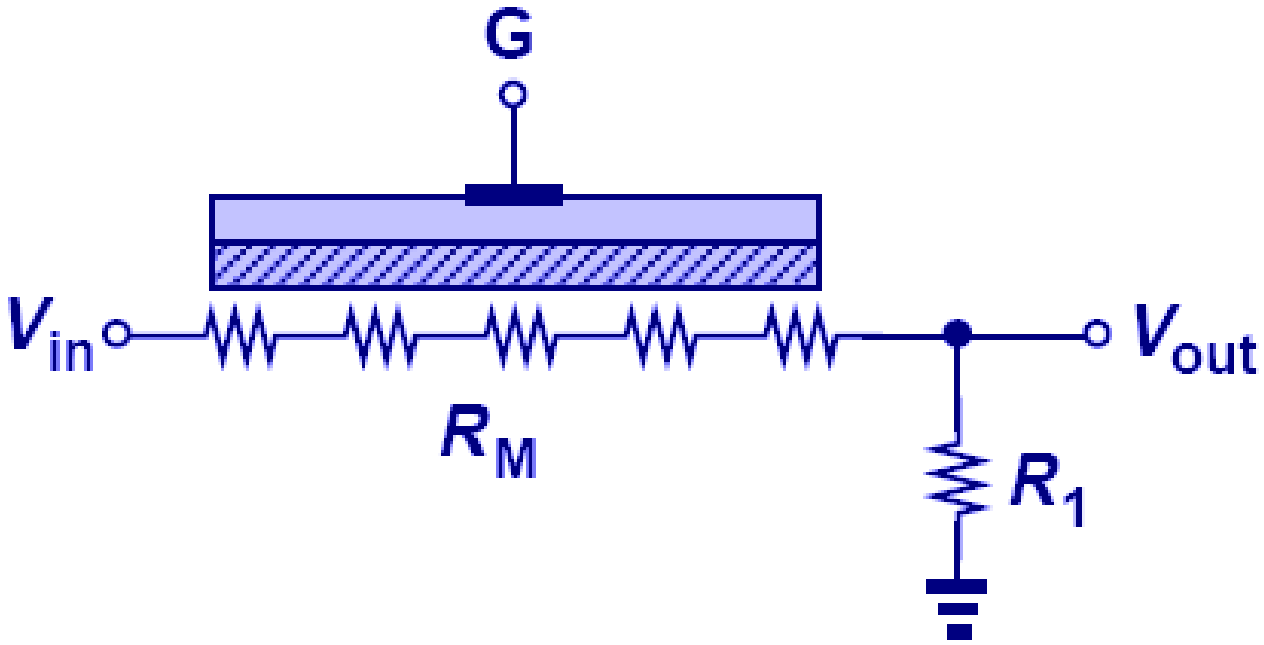


Voltage-Dependent Resistor



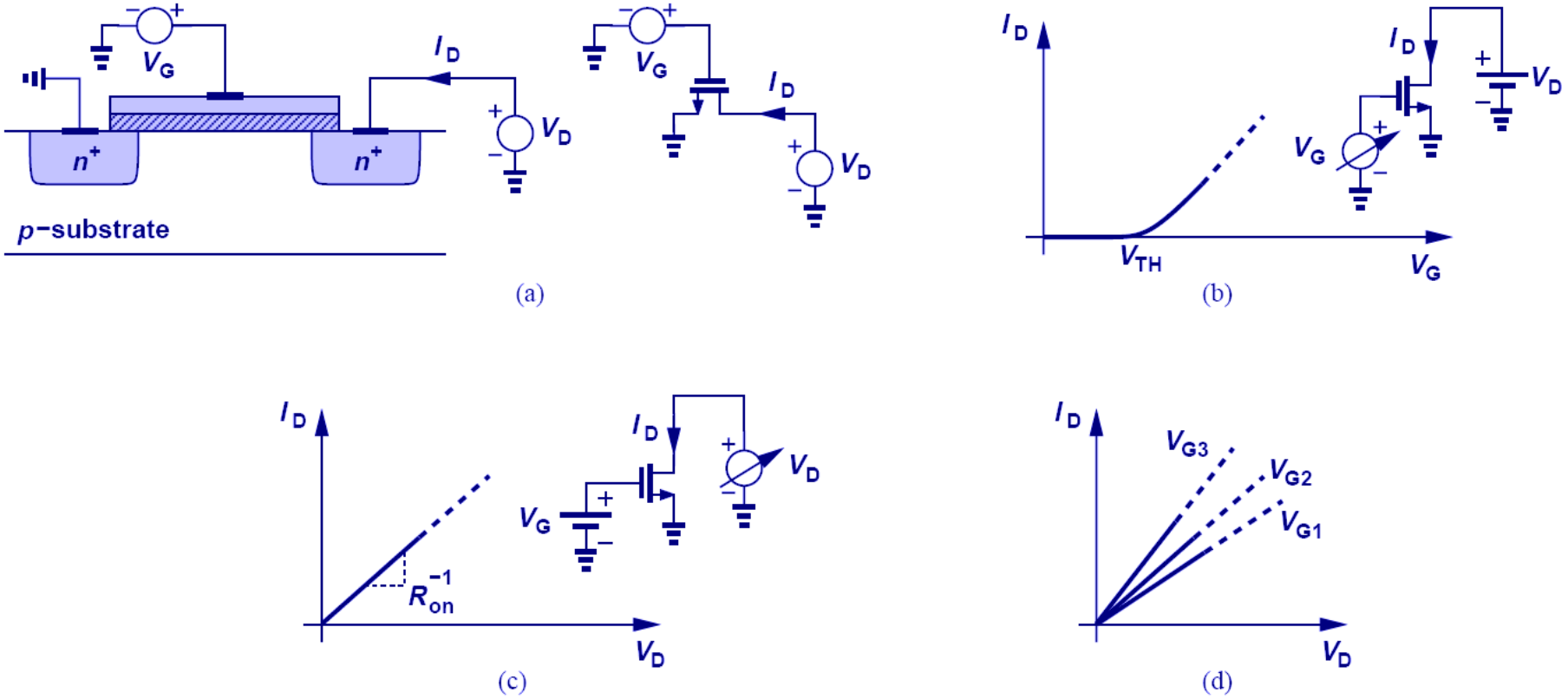
- The inversion channel of a MOSFET can be seen as a resistor.
- Since the charge density inside the channel depends on the gate voltage, this resistance is also voltage-dependent.

Voltage-Controlled Attenuator



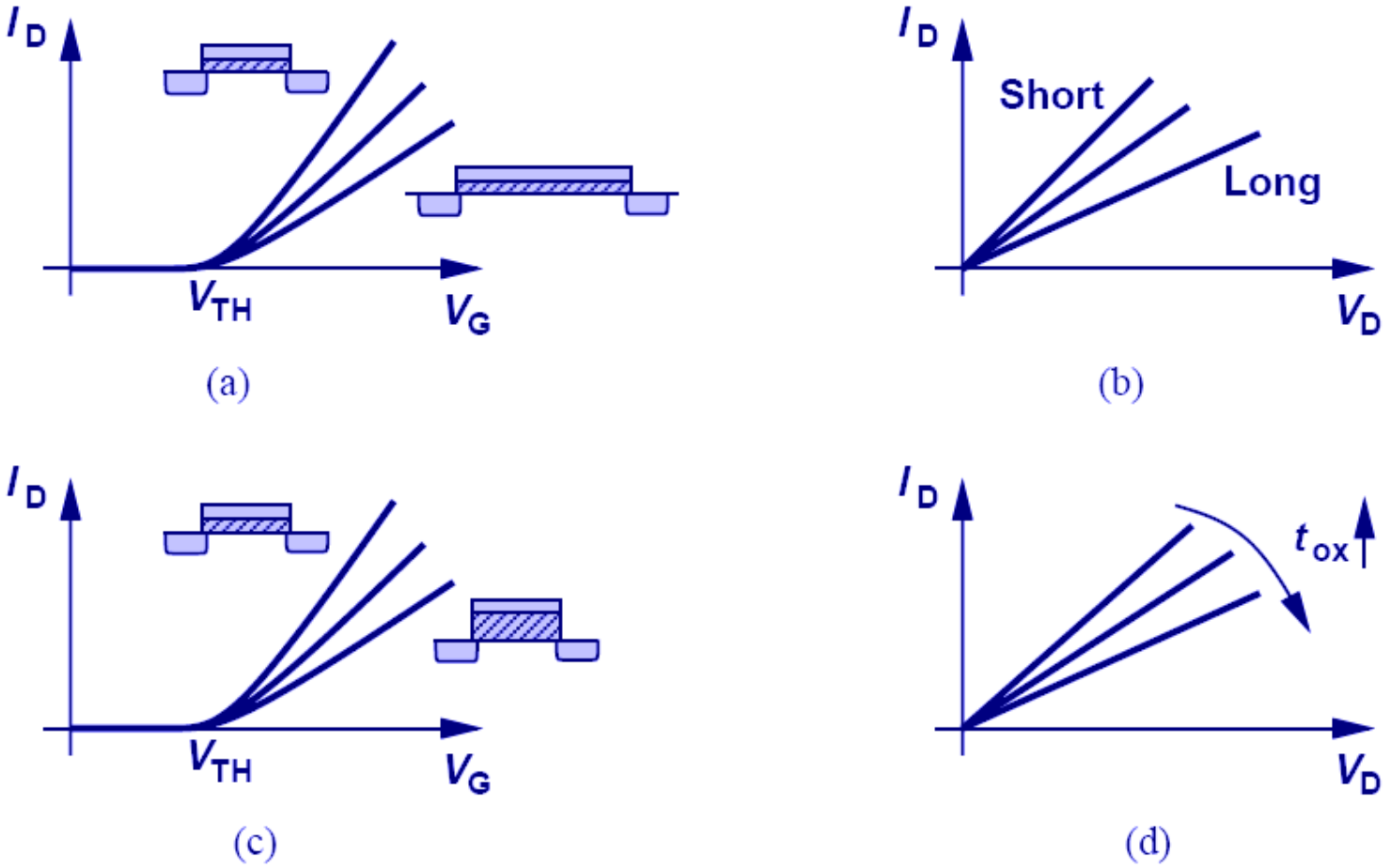
- As the gate voltage decreases, the output drops because the channel resistance increases.
- This type of gain control finds application in cell phones to avoid saturation near base stations.

MOSFET Characteristics



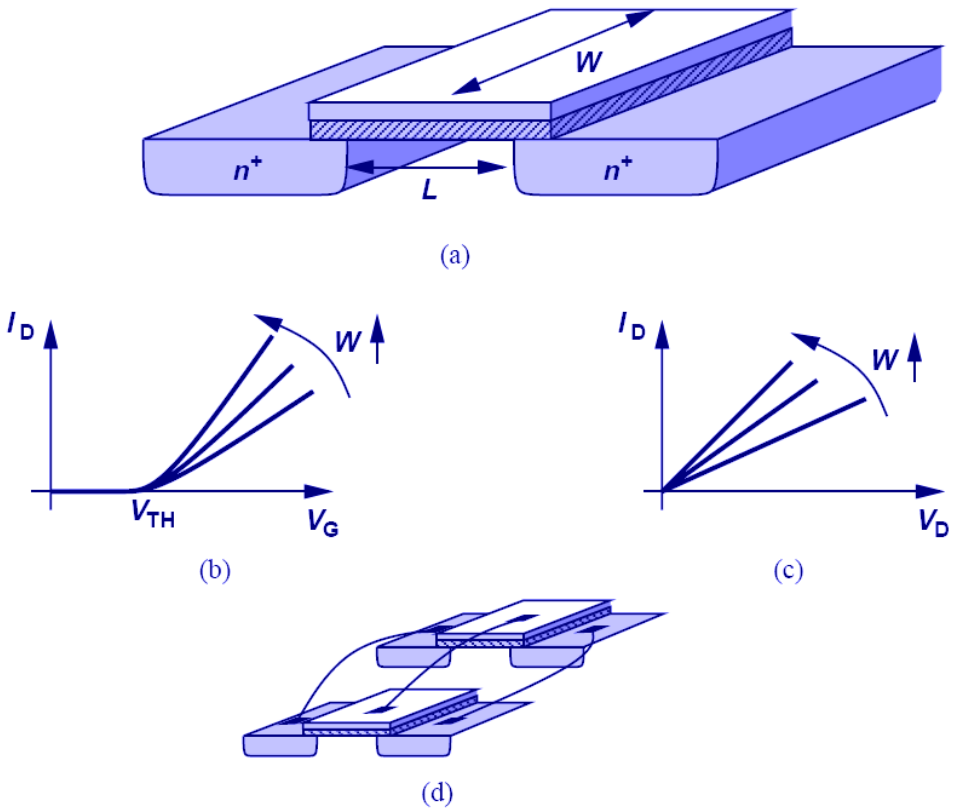
- The MOS characteristics are measured by varying V_G while keeping V_D constant, and varying V_D while keeping V_G constant.
- (d) shows the voltage dependence of channel resistance.

L and t_{ox} Dependence



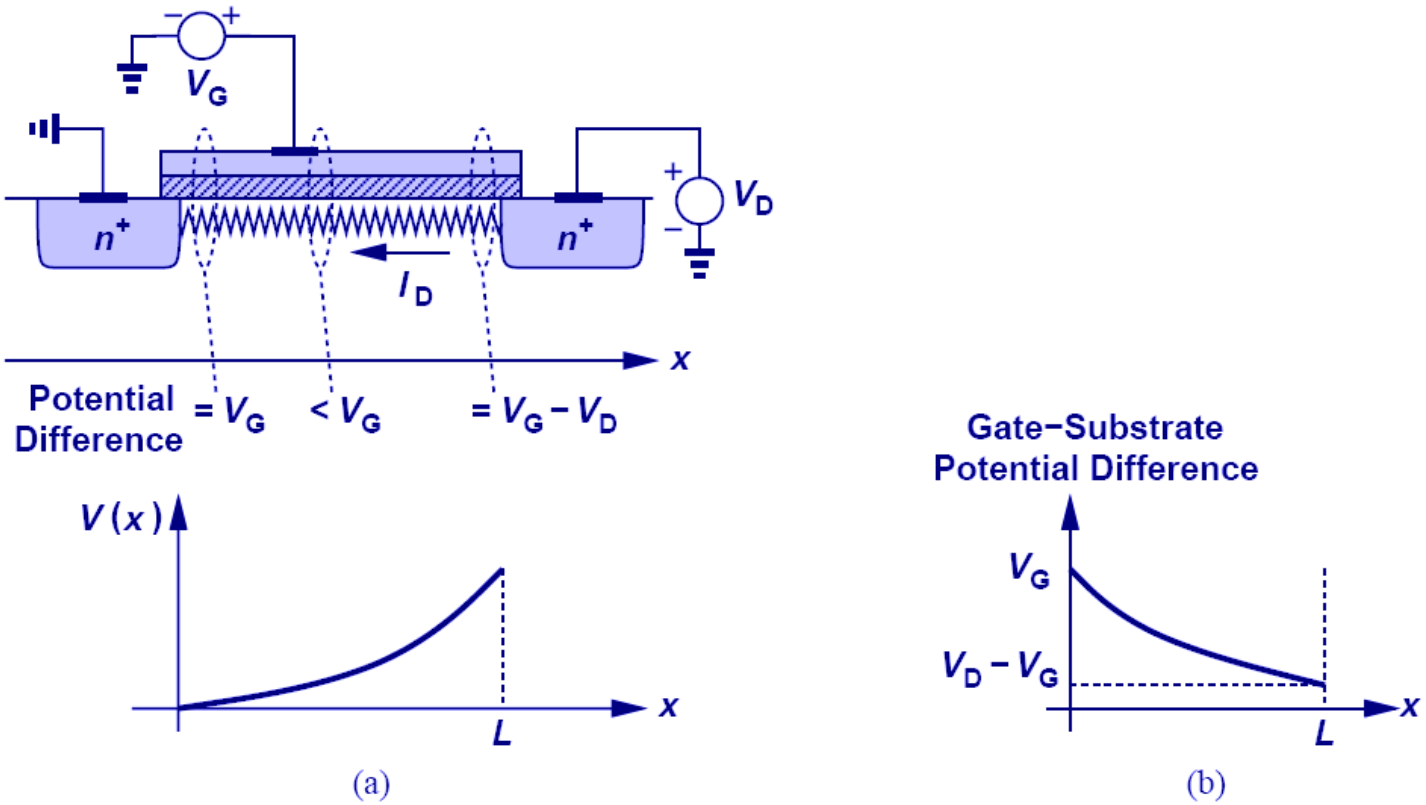
- Small gate length and oxide thickness yield low channel resistance, which will increase the drain current.

Effect of W



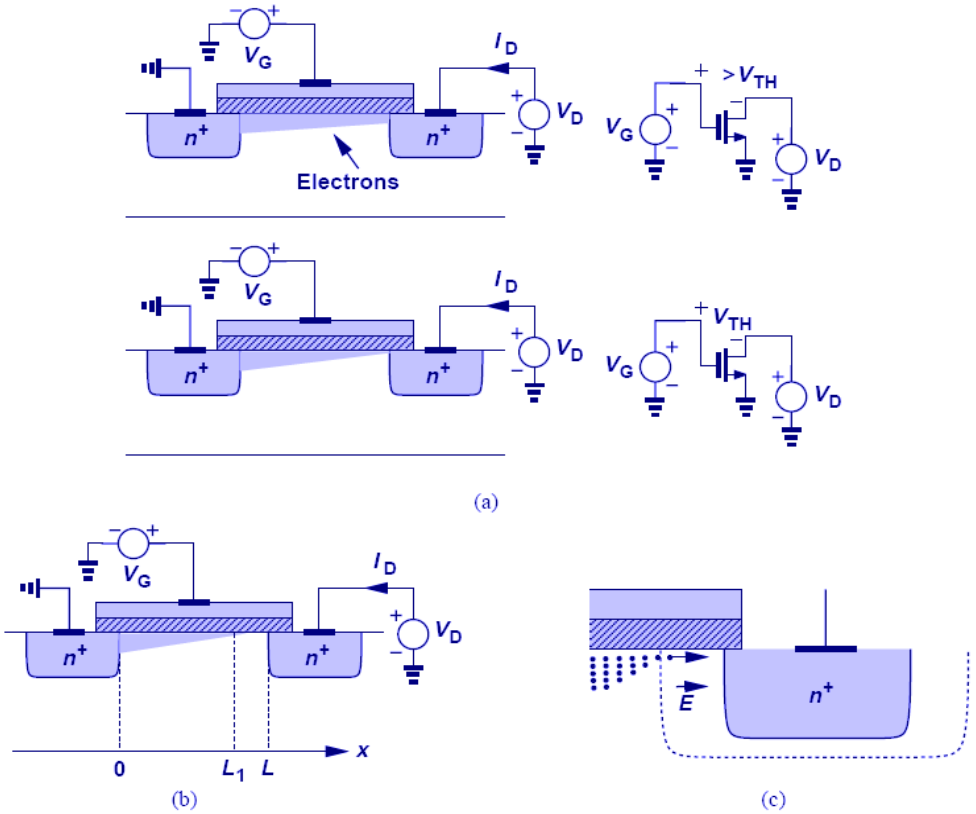
- As the gate width increases, the current increases due to a decrease in resistance. However, gate capacitance also increases thus, limiting the speed of the circuit.
- An increase in W can be seen as two devices in parallel.

Channel Potential Variation



- Since there's a channel resistance between drain and source, and if drain is biased higher than the source, channel potential increases from source to drain, and the potential between gate and channel will decrease from source to drain.

Channel Pinch-Off

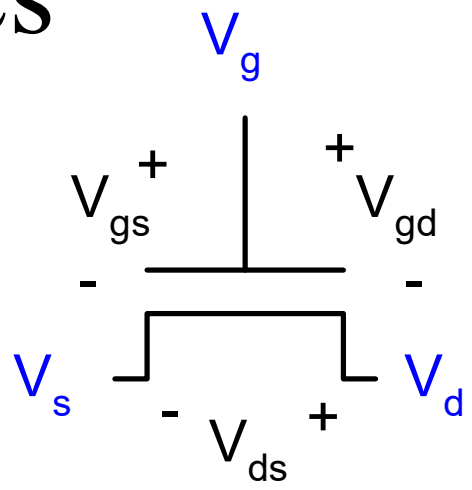


- As the potential difference between drain and gate becomes more positive, the inversion layer beneath the interface starts to pinch off around drain.
- When $V_D - V_G = V_{th}$, the channel at drain totally pinches off, and when $V_D - V_G > V_{th}$, the channel length starts to decrease.

I-V Characteristics

- In Linear region, I_{ds} depends on
  - How much charge is in the channel?
  - How fast is the charge moving?

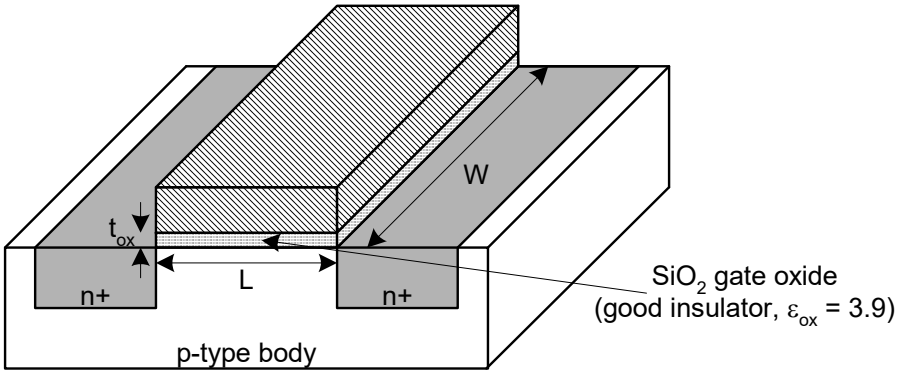
Terminal Voltages

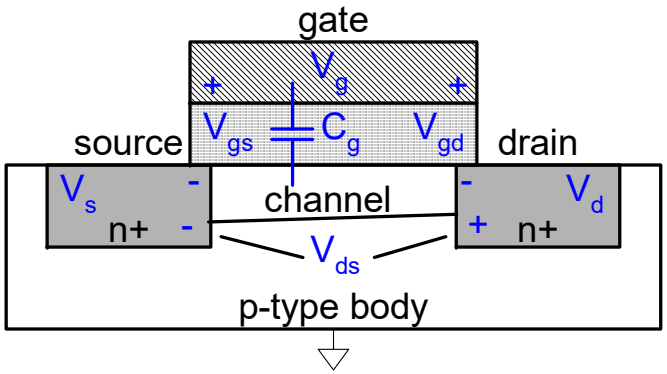


- Mode of operation depends on V_g, V_d, V_s
  - $V_{gs} = V_g - V_s$
  - $V_{gd} = V_g - V_d$
  - $V_{ds} = V_d - V_s = V_{gs} - V_{gd}$
- Source and drain are symmetric diffusion terminals
  - By convention, source is terminal at lower voltage
  - Hence $V_{ds} \geq 0$
- Three regions of operation
  - *Cutoff*
  - *Linear*
  - *Saturation*

Channel Charge

- MOS structure looks like parallel plate capacitor while operating in inversion
  - Gate – oxide – channel
- $Q_{channel} = CV$
- $C = C_g = \varepsilon_{ox} WL/t_{ox} = C_{ox} WL$ $\qquad C_{ox} = \varepsilon_{ox} / t_{ox}$
- $V = V_{gc} - V_t = (V_{gs} - V_{ds}/2) - V_t$





Carrier velocity

- Charge is carried by e-
- Carrier velocity *v* proportional to lateral E-field between source and drain
- $v = \mu E$ μ called mobility
- $E = V_{ds}/L$
- Time for carrier to cross channel:
  - $t = L / v$

nMOS Linear I-V

- Now we know
  - How much charge $Q_{channel}$ is in the channel
  - How much time *t* each carrier takes to cross

$$I_{ds} = \frac{Q_{\text{channel}}}{t}$$

$$= \mu C_{\text{ox}} \frac{W}{L}\left(V_{gs} - V_t - V_{ds}/2\right)V_{ds}$$

$$= \beta\left(V_{gs} - V_t - V_{ds}/2\right)V_{ds} \qquad \beta = \mu C_{\text{ox}} \frac{W}{L}$$

nMOS Saturation I-V

- If $V_{gd} < V_t$, channel pinches off near drain
  - When $V_{ds} > V_{dsat} = V_{gs} - V_t$
- Now drain voltage no longer increases current

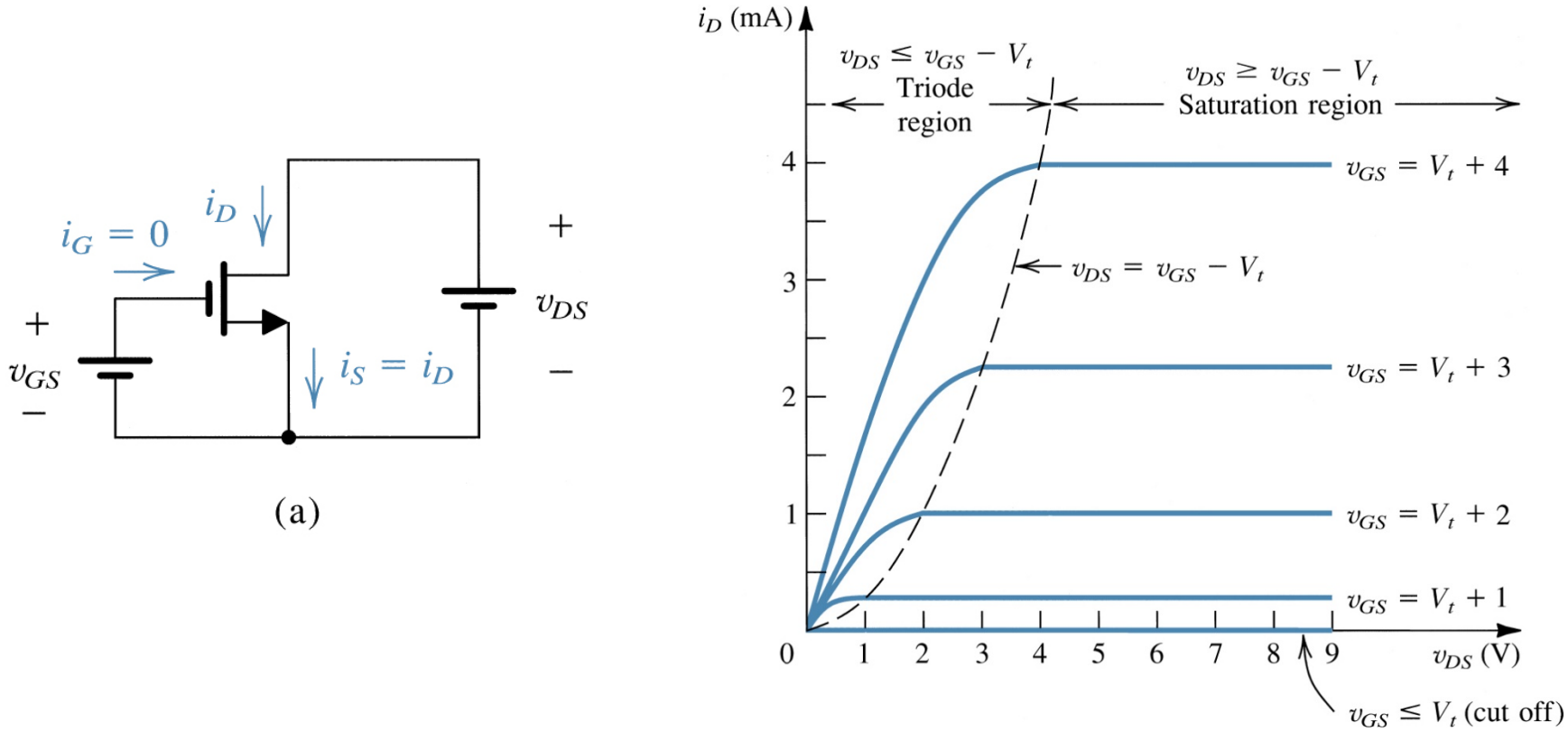
$$I_{ds} = \beta\left(V_{gs} - V_t - V_{dsat}/2\right)V_{dsat}$$

$$= \frac{\beta}{2}\left(V_{gs} - V_t\right)^2$$

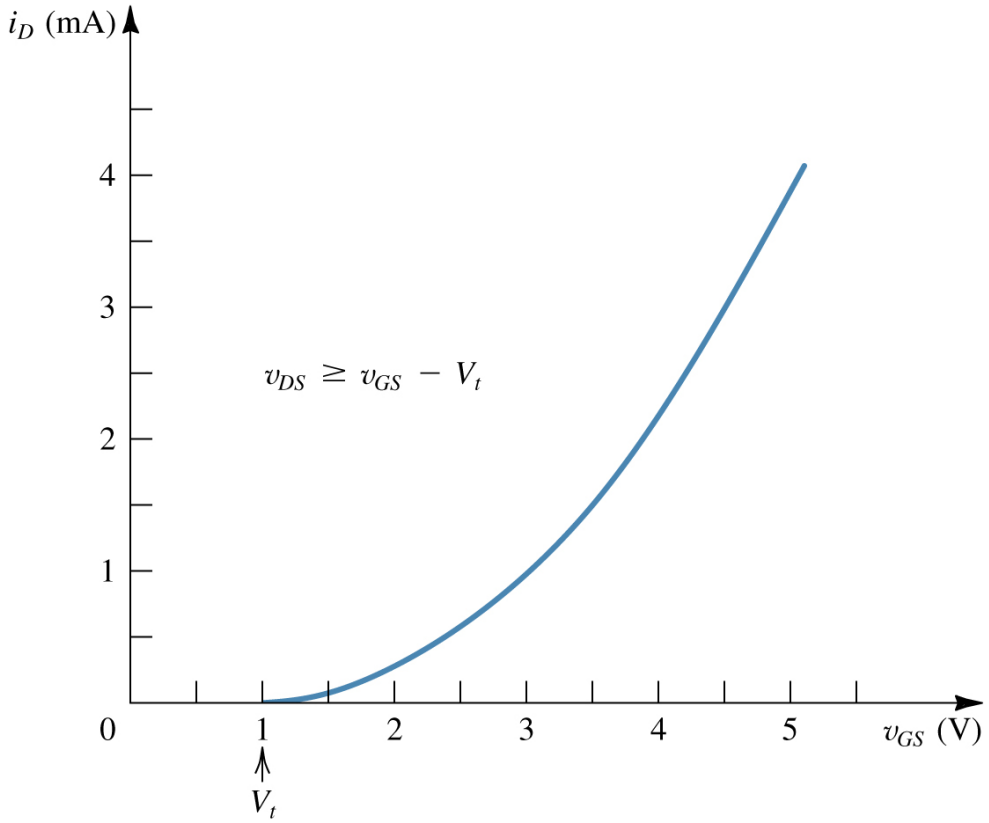
nMOS I-V Summary

- *Shockley* 1st order transistor models

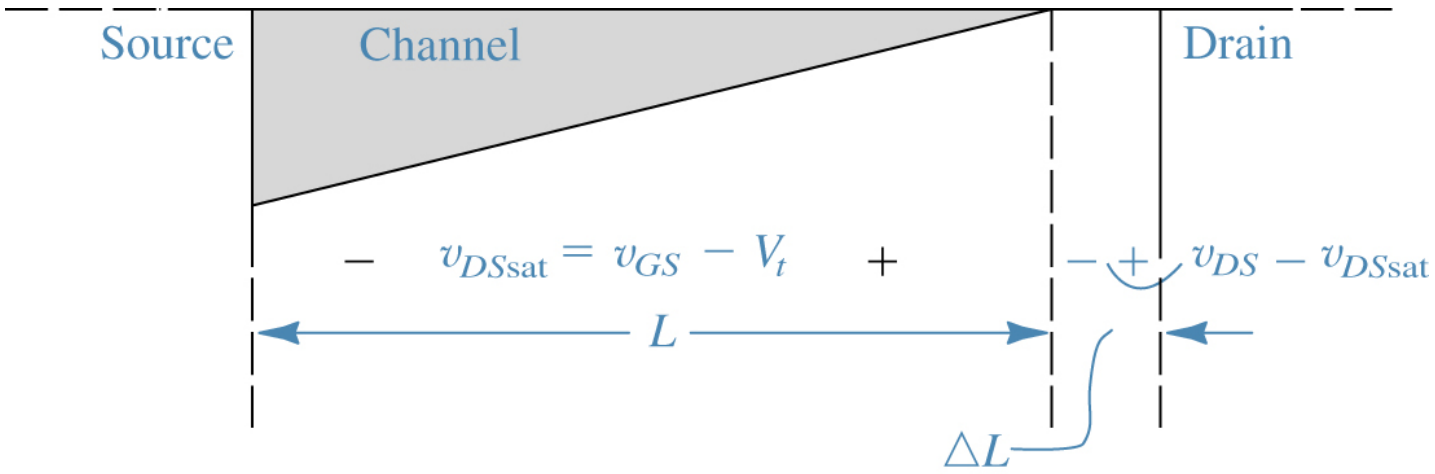
$$I_{ds} = \begin{cases} 0 & V_{gs} < V_t \quad \text{cutoff} \\ \beta\left(V_{gs} - V_t - V_{ds}/2\right)V_{ds} & V_{ds} < V_{dsat} \quad \text{linear} \\ \frac{\beta}{2}\left(V_{gs} - V_t\right)^2 & V_{ds} > V_{dsat} \quad \text{saturation} \end{cases}$$



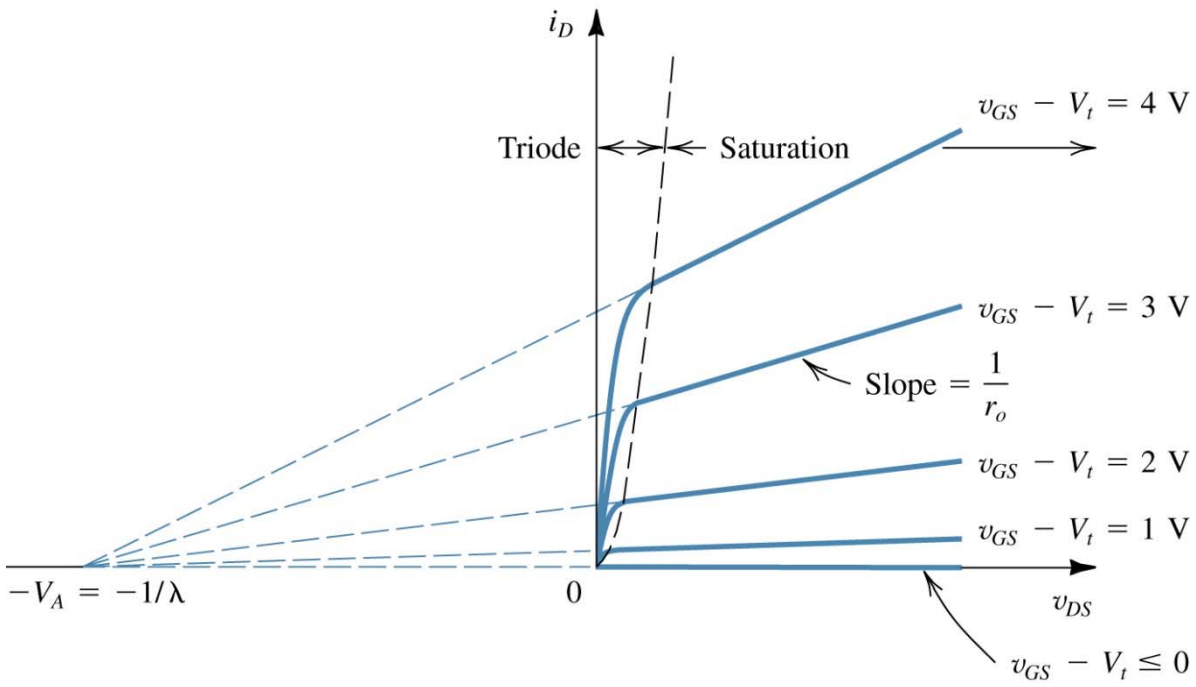
(a) An n-channel enhancement-type MOSFET with v_{GS} and v_{DS} applied and with the normal directions of current flow indicated. **(b)** The i_D - v_{DS} characteristics for a device with $V_t = 1$ V and $k'_n(W/L) = 0.5$ mA/V^2.



The i_D - v_{GS} characteristic for an enhancement-type NMOS transistor in saturation (V_t = 1 V and $k'_n(W/L)$ = 0.5 mA/V^2).



Increasing v_{DS} beyond v_{DSsat} causes the channel pinch-off point to move slightly away from the drain, thus reducing the effective channel length (by ΔL).



Effect of v_{DS} on i_D in the saturation region. The MOSFET parameter V_A is typically in the range of 30 to 200 V.

~the end~