HM6116

2Kx8 CMOS STATIC RAM

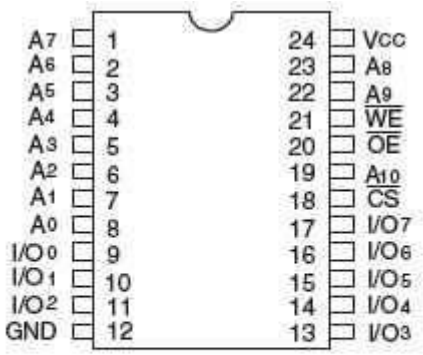
General description

The HM6116P is a 16,384-bit static random access memory organized as 2,048 by 8 bits and operates from a single 5 volt supply. It is built with performance COMS process. full CMOS memory cell provides low stand by current and high-reliability Inputs and three-state outputs are TTL compatible and allow for direct interfacing with common system bus structures.

Features

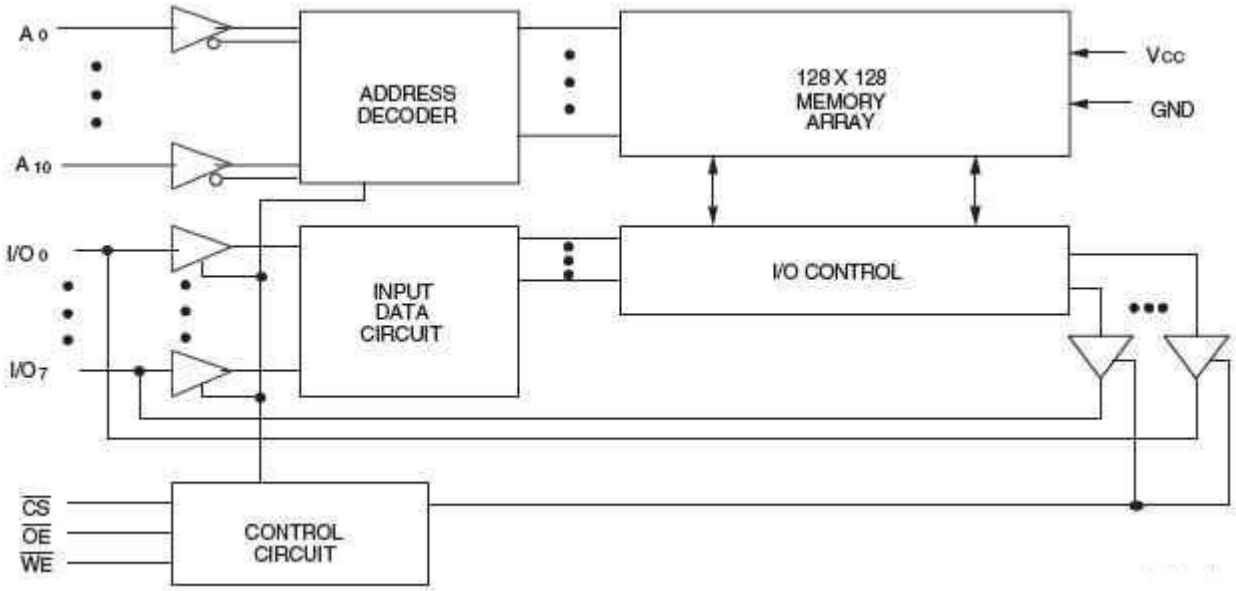
- Operation voltage: 4.5 ~ 5.5V
- Ultra low power consumption:
- High speed access time: 55~70ns.
- Automatic power down when chip is deselected.
- Three state outputs and TTL compatible.
- Data retention supplies voltage as low as 2.0V.
- Easy expansion with /CS and /OE options.

■ Pin configurations



DIP/SOIC/SOJ
Top View

■ Functional block diagram



■ PIN DESCRIPTION

SYMBOL	DESCRIPTION
A0–A10	Address Inputs
I/O0–I/O7	Data Inputs/Outputs
$\overline{CS}$	Chip Select Input
$\overline{WE}$	Write Enable Input
$\overline{OE}$	Output Enable Input
Vcc	Power Supply
Vss	Ground

TRUTH TABLE

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	MODE	I/O	Vcc CURRENT
H	X	X	Not Selected	High Z	I_{SB}, I_{SB1}
L	H	H	Output Disable	High Z	Icc
L	L	H	Read	Data Out	Icc
L	X	L	Write	Data In	Icc

■ Absolute maximum ratings(1)

Symbol	Parameter	Rating	Unit
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to Vcc+0.5	V
T_{BIAS}	Temperature Under Bias	-40 to +125	^{O}C
T_{STG}	Storage Temperature	-65 to +150	^{O}C
P_T	Power Dissipation	1.0	W
I_{OUT}	DC Output Current	50	mA

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

■ Operating range

Range	Ambient Temperature	Vcc
Commercial	0~70^{o}C	4.5 ~ 5.5V
Industrial	-40~85^{o}C	4.5 ~ 5.5V

■ Cpacitance(1)(TA=25℃,f=1.0MHz)

Symbol	Parameter	Conduction	MAX.	Unit
C_{IN}	Input Capacitance	Vin=0V	8	pF
C_{DQ}	Input/Output Capacitance	Vout=0V	10	pF

■ Dc electrical characteristics(Over Operating Range)

Name	Parameter	Test Condition	MIN	TYP(1)	MAX	Unit
V_{IL}	Guaranteed Input Low Voltage (2)		-0.5		0.6	V
V_{IH}	Guaranteed Input High Voltage (2)		3.5		Vcc+0.5	V
I_{IL}	Input Leakage Current	V_{CC}=Max, V_{IN}=0 to V_{CC}	-1		1	uA
I_{OL}	Output Leakage Current	V_{CC}=Max, /CS=V_{Ih}, or /OE=V_{Ih} ,or /WE= V_{IL} Vout=0V to V_{CC}	-1		1	uA
V_{OL}	Output Low Voltage	V_{CC}=Max, I_{OL} = 1mA			0.4	V
V_{OH}	Output High Voltage	V_{CC}=Min, I_{OH} = -1mA	2.4			V
I_{CC}	Operating Power Supply Current	/CS=V_{IL}, I_{DQ}=0mA, F=F_{MAX} =1/ t_{RC}		20	30	mA
I_{SB}	TTL Standby Supply	/CS=V_{IH}, I_{DQ}=0mA,			3	mA
I_{SB1}	CMOS Standby Current	/CS≧V_{CC}-0.2V, or V_{IN}≧V_{CC}-0.2V or V_{IN}≦0.2V,			1	uA

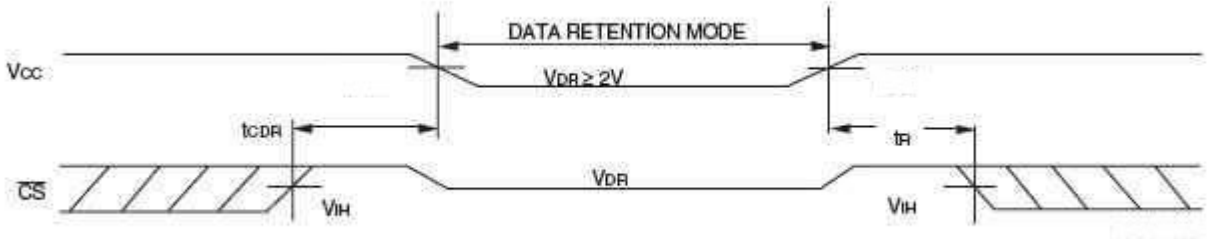
1. Typical characteristics are at Ta = 25°C.
2. These are absolute values with respect to device ground and all overshoots due to system or tester notice are included.
3. Vcc operating range at 5V: 4.5v ~ 5.5v

■ Data retention characteristics(Over Operating Range)

Name	Parameter	Test Condition	MIN	TYP(1)	MAX	Unit
V_{DR}	V_{CC} for Data Retention	/CS ≧ V_{CC}-0.2V, V_{IN} ≧ V_{CC}-0.2V or V_{IN}≦0.2V	2.0			V
I_{CCDR}	Data Retention Current	/CS≧V_{CC}-0.2V, V_{IN}≧ V_{CC}-0.2V or V_{IN}≦0.2V		0.5	20	**uA**
T_{CDR}	Chip Deselect to Data Retention Time	Refer to Retention Waveform	0			ns
t_R	Operation Recovery Time		t_{RC} (2)			ns

1. Ta = 25°C
2. t_{RC}= Read Cycle Time
3. Vcc operating range at 5V: 4.5v ~ 5.5v

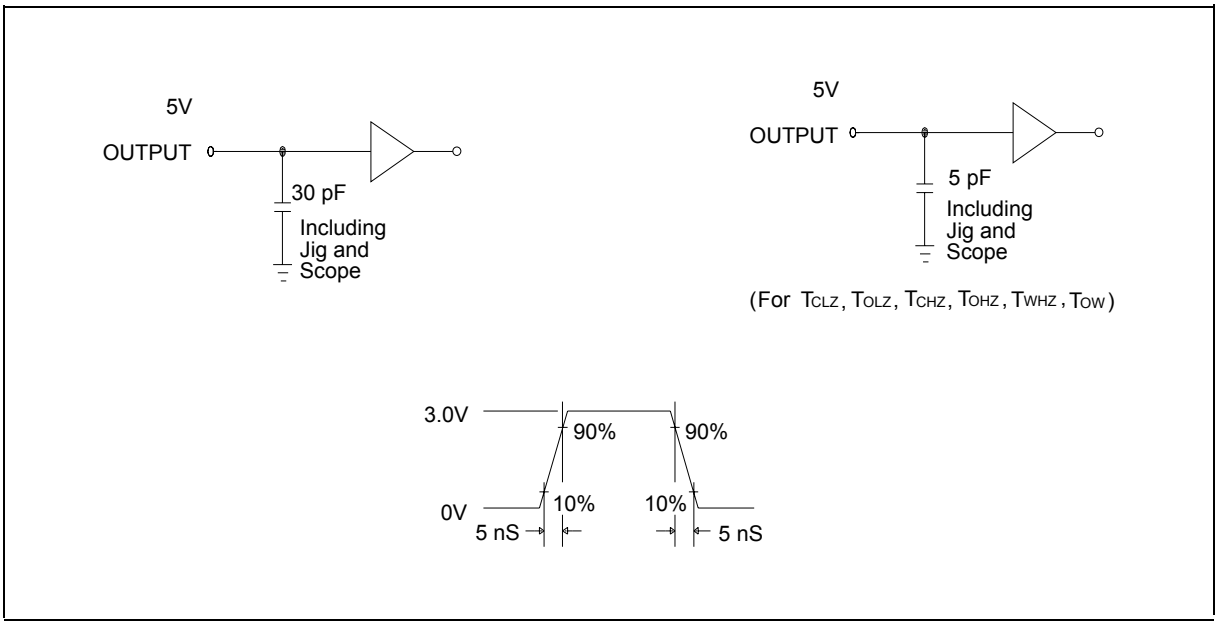
■ Low Vcc Data Retention Waveform



AC TEST CONDITIONS

PARAMETER	CONDITIONS
Input Pulse Levels	0V to 3V
Input Rise and Fall Times	5 nS
Input and Output Timing Reference Level	1.5V
Output Load	C_L = 30 pF + 1 TTL, I_{OH}/I_{OL} = -1 mA/2.1 mA

■ Ac test loads and waveforms



AC CHARACTERISTICS

(Vcc = 5V ±10%, V_{SS} = 0V, T_A = 0 to 70° C)

Read Cycle

PARAMETER	SYM.	HM6116-70L/LL		UNIT
		MIN.	MAX.	
Read Cycle Time	T_{RC}	70	-	nS
Address Access Time	T_{AA}	-	70	nS
Chip Select Access Time	T_{ACS}	-	70	nS
Output Enable to Output Valid	T_{AOE}	-	30	nS
Chip Selection to Output in Low Z	T_{CLZ}*	5	-	nS
Output Enable to Output in Low Z	T_{OLZ}*	5	-	nS
Chip Deselection to Output in High Z	T_{CHZ}*	-	20	nS
Output Disable to Output in High Z	T_{OHZ}*	-	20	nS
Output Hold from Address Change	T_{OH}	3	-	nS

* These parameters are sampled but not 100% tested.

■ Write Cycle

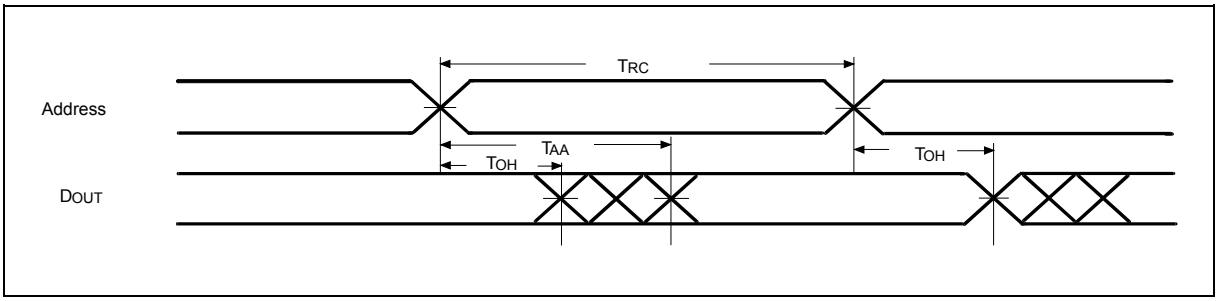
PARAMETER		SYM.	HM6116-70L/LL		UNIT
			MIN.	MAX.	
Write Cycle Time		T_{WC}	70	-	nS
Chip Selection to End of Write		T_{CW}	70	-	nS
Address Valid to End of Write		T_{AW}	70	-	nS
Address Setup Time		T_{AS}	0	-	nS
Write Pulse Width		T_{WP}	50	-	nS
Write Recovery Time	$\overline{CS}$, $\overline{WE}$	T_{WR}	0	-	nS
Data Valid to End of Write		T_{DW}	30	-	nS
Data Hold from End of Write		T_{DH}	0	-	nS
Write to Output in High Z		T_{WHZ}*	-	25	nS
Output Disable to Output in High Z		T_{OHZ}*	-	30	nS
Output Active from End of Write		T_{OW}	5	-	nS

* These parameters are sampled but not 100% tested.

TIMING WAVEFORMS

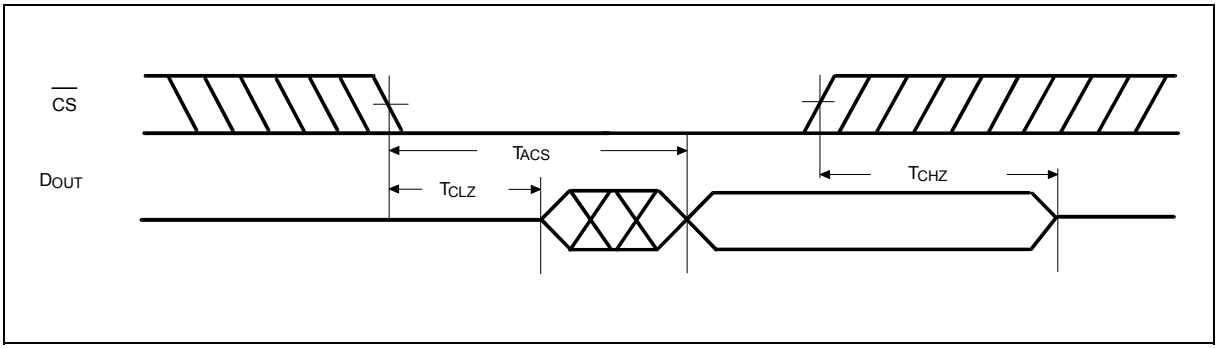
Read Cycle 1

(Address Controlled)



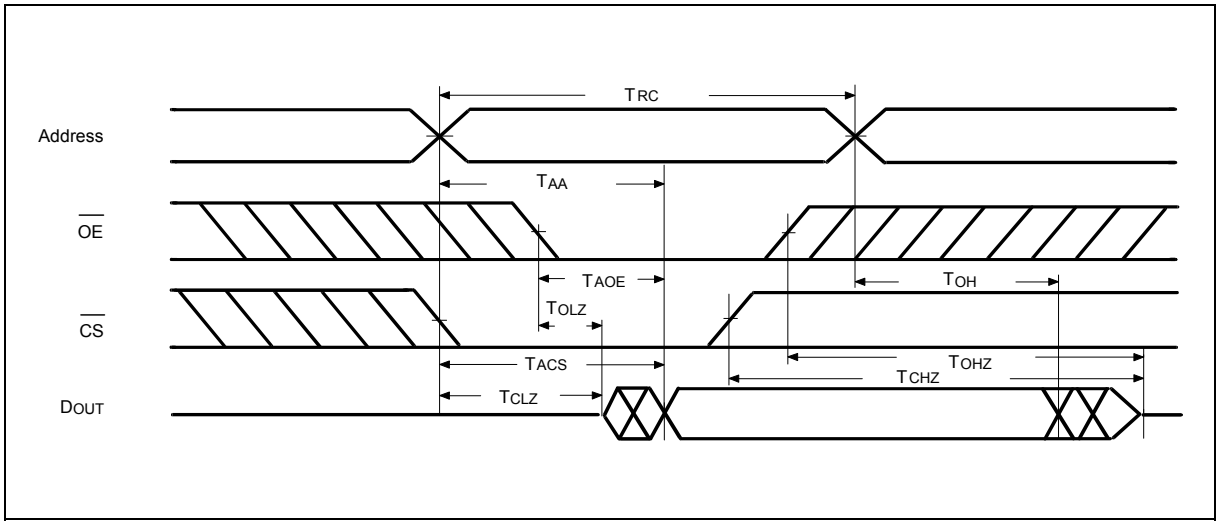
Read Cycle 2

(Chip Select Controlled)



Read Cycle 3

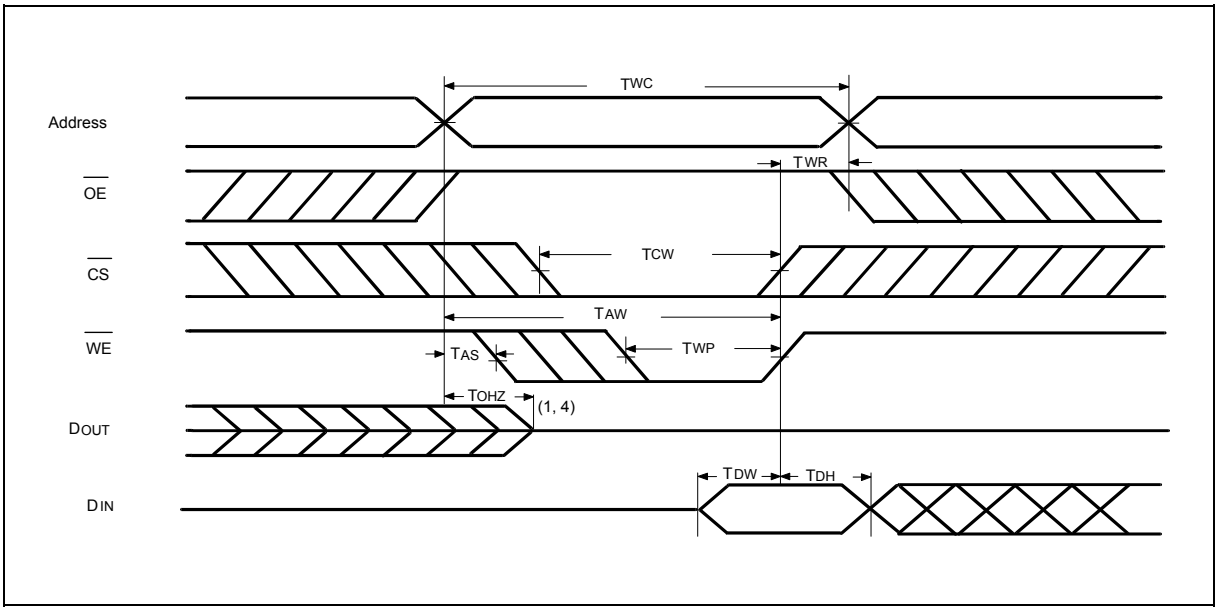
(Output Enable Controlled)



Timing Waveforms, continued

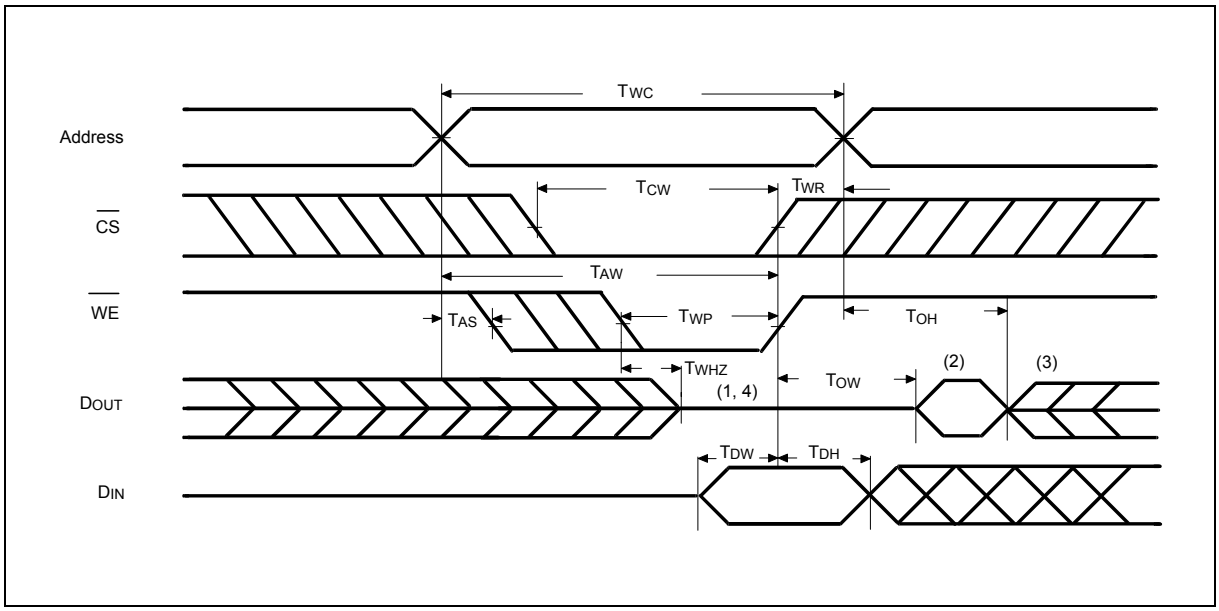
Write Cycle 1

($\overline{OE}$ Clock)



Write Cycle 2

($\overline{OE}$ = V_{IL} Fixed)



Notes:

1. During this period, I/O pins are in the output state, so input signals of opposite phase to the outputs should not be applied.

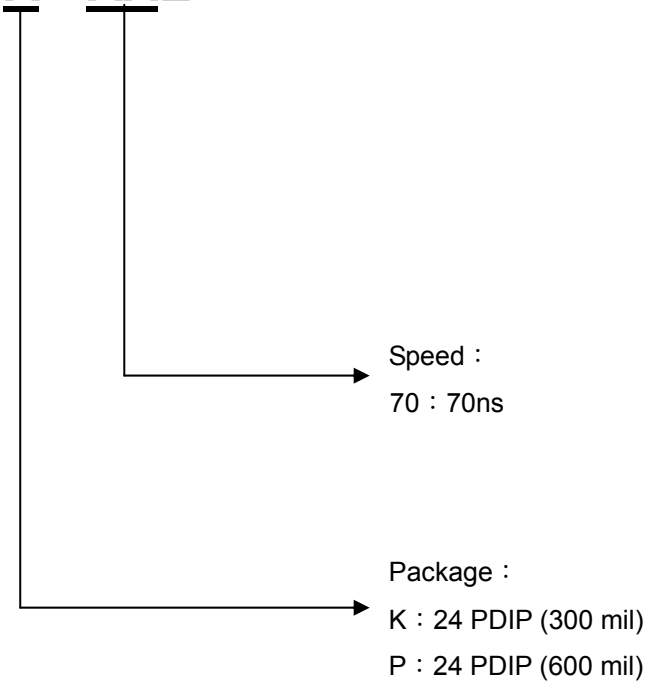
2. The data output from D_{OUT} are the same as the data written to D_{IN} during the write cycle.

3. D_{OUT} provides the read data for the next address.

4. Transition is measured ±500 mV from steady state with C_L = 5 pF. This parameter is guaranteed but not 100% tested.

ORDER INFORMATION

HM6116 X - XXL



Lot No: X X X X X X X X X
① ②

① : Manufacturing tracking code

② — : Normal package

R : Lead free package

G : Green (RoHS compatible) package

Test Report

GET-TEAM TECH CORPORATION
NO.122-8, CHUNG HUA RD., HSIN CHU INDUSTRIAL PARK, HSINCHU HSIEN, TAIWAN, R. O. C.

Report No. : CE/2005/B4965B
Date : 2005/11/29

The following merchandise was (were) submitted and identified by the client as :

Type of Product	:	GET-TEAM LEAD-FREE PLATING PRODUCT #3
Style/Item No	:	P-DIP
PART NAME NO.	:	PLEASE REFER TO THE PHOTO ATTACHED (MIXED ALL PARTS)
Sample Received	:	2005/11/22
Testing Date	:	2005/11/22 TO 2005/11/29

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Test Result : - Please see the next page -

Daniel Yeh, M.R. / Operation Manager
Signed for and on behalf of
SGS TAIWAN LTD.

Test Report

GET-TEAM TECH CORPORATION
NO.122-8, CHUNG HUA RD., HSIN CHU INDUSTRIAL PARK, HSINCHU HSIEN, TAIWAN, R. O. C.

Report No. : CE/2005/B4965B
Date : 2005/11/29

Test Result

PART NAME NO.1 : SILVER-WHITE COLORED METAL (PLEASE REFER TO THE PHOTO ATTACHED(MIXED ALL PARTS))

Test Item (s):	Unit	Method	MDL	Result
				No.1
Monobromobiphenyl	%	With reference to USEPA3540C or USEPA3550C. Analysis was performed by HPLC/DAD, LC/MS or GC/MS. (prohibited by 2002/95/EC (RoHS), 83/264/EEC, and 76/769/EEC)	0.0005	N.D.
Dibromobiphenyl	%		0.0005	N.D.
Tribromobiphenyl	%		0.0005	N.D.
Tetrabromobiphenyl	%		0.0005	N.D.
Pentabromobiphenyl	%		0.0005	N.D.
Hexabromobiphenyl	%		0.0005	N.D.
Heptabromobiphenyl	%		0.0005	N.D.
Octabromobiphenyl	%		0.0005	N.D.
Nonabromobiphenyl	%		0.0005	N.D.
Decabromobiphenyl	%		0.0005	N.D.
Total PBBs (Polybrominated biphenyls)/Sum of above	%		-	N.D.
Monobromobiphenyl ether	%	With reference to USEPA3540C or USEPA3550C. Analysis was performed by HPLC/DAD, LC/MS or GC/MS. (prohibited by 2002/95/EC (RoHS), 83/264/EEC, and 76/769/EEC)	0.0005	N.D.
Dibromobiphenyl ether	%		0.0005	N.D.
Tribromobiphenyl ether	%		0.0005	N.D.
Tetrabromobiphenyl ether	%		0.0005	N.D.
Pentabromobiphenyl ether	%		0.0005	N.D.
Hexabromobiphenyl ether	%		0.0005	N.D.
Heptabromobiphenyl ether	%		0.0005	N.D.
Octabromobiphenyl ether	%		0.0005	N.D.
Nonabromobiphenyl ether	%		0.0005	N.D.
Decabromobiphenyl ether	%		0.0005	N.D.
Total PBBEs(PBDEs) (Polybrominated biphenyl ethers)/Sum of above	%		-	N.D.
Total of Mono to Nona-brominated biphenyl ether. (Note 4)	%		-	N.D.

Test Report

GET-TEAM TECH CORPORATION
NO.122-8, CHUNG HUA RD., HSIN CHU INDUSTRIAL PARK, HSINCHU HSIEN, TAIWAN, R. O. C.

Report No. : CE/2005/B4965B
Date : 2005/11/29

Test Item (s):	Unit	Method	MDL	Result
				No.1
Chromium VI (Cr+6)	ppm	UV-VIS after reference to US EPA 3060A.	2	N.D.
Cadmium (Cd)	ppm	ICP-AES after reference to EN 1122, method B:2001 or other acid digestion.	2	N.D.
Mercury (Hg)	ppm	ICP-AES after reference to US EPA 3052 or other acid digestion.	2	N.D.
Lead (Pb)	ppm	ICP-AES after reference to US EPA 3050B or other acid digestion.	2	N.D.

NOTE: (1) N.D. = Not detected (<MDL)
(2) ppm = mg/kg
(3) MDL = Method Detection Limit
(4) Decabromodiphenyl ether (DecaBDE) in polymeric applications is exempted by Commission Decision of 13 Oct 2005 amending Directive 2002/95/EC notified under document 2005/717/EC.
(5) PBBEs=PBDEs=Polybrominated Diphenyl Ethers=PBDOs=PBBOs.
(6) " - " = Not Regulation

Test Report

GET-TEAM TECH CORPORATION
NO.122-8, CHUNG HUA RD., HSIN CHU INDUSTRIAL PARK, HSINCHU HSIEN, TAIWAN, R. O. C.

Report No. : CE/2005/B4965B
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