

Computer Organization HW04-1

$$1.1 \quad 180 \text{ ps} + 80 \text{ ps} = 260 \text{ ps} \#$$

$$1.2 \quad \text{SW} \Rightarrow \text{J-Mem} + \text{Ctrl. Unit} + \text{ALU-Ctrl.} + \text{ALU} + \text{Data-Mem} = 740 \text{ ps}$$

$$\text{beq} \Rightarrow \text{J-Mem} + \text{Ctrl. Unit} + \text{ALU-Ctrl.} + \text{ALU} + \text{AND} + \text{MUX} = 630 \text{ ps}$$

$$\text{add} \Rightarrow \text{J-Mem} + \text{Ctrl. Unit} + \text{ALU-Ctrl.} + \text{ALU} + \text{MUX} + \text{Regs. Access} = 670 \text{ ps}$$

$$\text{Max}(740, 630, 670) = 740 \text{ (ps)} \#$$

$$1.3 \quad 180 + 200 + 60 + 100 + 200 + 30 + 100 = 870 \text{ (ps)} \#$$

$$2.1 \quad \text{sign-extend: } 0000 \ 0000 \ 0000 \ 0000 \ 0101 \ 0000 \ 0010 \ 0010$$

$$\text{shift left: } 0101 \ 1010 \ 0101 \ 0100 \ 0000 \ 1000 \ 1000$$

$$2.2 \quad \text{instruction}[31:26] = 000000 \Rightarrow \text{R-format} \quad \text{OpCode}[1:0] = 10 \#, \quad \text{instruction}[5:0] = 100010 \#$$

$$2.3 \quad \text{PC} += 4, \quad \text{PC} \rightarrow \text{Add4} \rightarrow \text{branch MUX} \rightarrow \text{jump MUX} \#$$

$$2.4 \quad (1) \text{ RegDsc MUX: } 01010 \Rightarrow 10 \#$$

$$(2) \text{ ALUsrc MUX: } 3 \#$$

$$(3) \text{ PCsrc MUX: } \text{PC} + 4 \#$$

$$(4) \text{ MemtoReg MUX: } 1 \# \left(\frac{1}{r_s} - \frac{3}{r_c} \right)$$

$$2.5 \quad (1) \text{ ALU: } 4, 3 \#$$

$$(2) \text{ Add: } \text{PC}, 4 \#$$

$$(3) \text{ Add (ALU result): } \text{PC} + 4, \quad 0000 \ 0000 \ 0000 \ 0001 \ 0100 \ 0000 \ 1000 \ 1000 \#$$

$$2.6 \quad (1) \text{ Read Register 1: } 11 \#$$

$$(3) \text{ Write Register: } 10 \#$$

$$(5) \text{ Reg Write: } 1 \#$$

$$(2) \text{ Read Register 2: } 9 \#$$

$$(4) \text{ Write Data: } 1 \#$$

shift left 2 (x4)

3.1 ALUOp or ALUSrc, they need to be generated during Reg. Access (250ps).

In this way, ALUsrc can enable Read Data to pass through Mux (100ps) in the shortest time.

As for ALUOp, ALU control (100ps) signal can be generated in the shortest time.

keep the ALU input delay at 100ps.

3.2

$$R-Forward = I-Mem + RegDst + MUX + RegsAccess = 2250$$

$$LW = I-Mem + ALUOp + ALUctrl + ALU + Data-Mem + MUX + RegsAccess = 1950$$

$$SW = I-Mem + MemWrite + Data-Mem = 2000$$

$$Branch = I-Mem + Branch + AND + MUX = 1600$$

$$\text{MAX}(2250, 1950, 2000, 1600)$$

$$= 2250$$

not support

$$I-Mem + \text{MAX}(\text{MAX}(\text{MAX}(\text{MAX}(\text{RegsAccess}, \text{ALUSrc}), \text{ALUOp} + \text{ALUctrl}), \text{ALU}), \text{MemtoReg}), \text{RegWrite}, \text{RegDst} + \text{MUX})$$

$$I-Mem + \text{MAX}(\text{MAX}(\text{MAX}(\text{MAX}(\text{RegsAccess}, \text{ALUSrc}), \text{ALUOp} + \text{ALUctrl}), \text{ALU}), \text{MemRead}) + \text{Data-Mem}, \text{MemtoReg} + \text{MUX}$$

$$I-Mem + \text{MAX}(\text{MAX}(\text{MAX}(\text{RegsAccess}, \text{ALUSrc}), \text{MUX}), \text{ALUOp} + \text{ALUctrl}) + \text{ALU}, \text{MemWrite}) + \text{Data-Mem}$$

$$\text{MAX}(\text{ALU}, I-Mem + \text{MAX}(\text{RegsAccess}, \text{ALUSrc}) + \text{MUX}, \text{ALUOp} + \text{ALUctrl}) + \text{ALU}, \text{Branch})$$

4.1

$$I-Mem + \text{Registers} + \text{ALU} + \text{Data-Mem} + \text{MUX} + \text{Registers}$$

$$500 + 250 + 150 + 400 + 50 + 250 = 1600 \text{ ps}$$

$$500 + 250 + 450 + 400 + 50 + 250 = 1900 \text{ ps}$$

4.2

$$\frac{1600}{0.95 \times 1900} = 0.886$$

$$\frac{\text{cost}_1}{P_1} / \frac{\text{cost}_2}{P_2} = \frac{\text{cost}_1 / \text{cost}_2}{P_1 / P_2}$$

4.3

$$1100 + 2 \times 30 + 3 \times 20 + 80 + 200 + 1600 + 500 = 3600$$

$$\frac{3600 / 4100}{0.886} = 0.991$$

$$1100 + 60 + 60 + 580 + 200 + 1600 + 500 = 4100$$