Out: September 23rd, 2016
Due: October 7th, 2016

Goal

To perform low level tests on your CME 341 microprocessor. To design a test bench to exercise your RAM module using your CME 341 microprocessor.

Procedure

1. For Assignment #1, you created a test plan spreadsheet for your CME 341 microprocessor to outline the test(s) you would perform to exercise the low level i_pins and o_reg functionality. As part of this assignment you were to write some assembly language code to use in the ROM part of your microprocessor to perform the test(s).

   Before proceeding, please check your assembly code for the following common deficiencies and fix your code as needed:

   - "Ugly" assembly ☺ (i.e. long program without a loop).
   - Failing to test all possible cases. Each memory address should be tested with each possible value.

2. Leverage and update the SystemVerilog test bench environment from Lab 1/Assignment 1 to perform the above test(s). Note that you should have some way of synchronizing when you change the i_pin value such that your test(s) execute in the minimum amount of time. This minimum amount of time will depend on the assembly code you have written. Do NOT use hard coded delays (i.e., by counting clock cycles) in your test bench.

3. Now verify that the RAM module is working correctly (read/write all addresses). Develop a test plan spreadsheet and new assembly language source (create RAM_test.asm), then execute the test(s) using your CME 341 microprocessor running in the Questa simulation environment. This assumes that your microprocessor functioned correctly using the Altera megafunction for the RAM in the first place back in CME 341. If this wasn't the case, you have some work to do…

Deliverable

Waveform views of each of your complete test results, your RAM test plan spreadsheet, and RAM_test.asm. Package the required files in a zip archive that includes your name, NSID, and student number in the filename, and email to the course lab instructor Chandler Janzen (chandler.janzen@usask.ca) by midnight on October 7th.