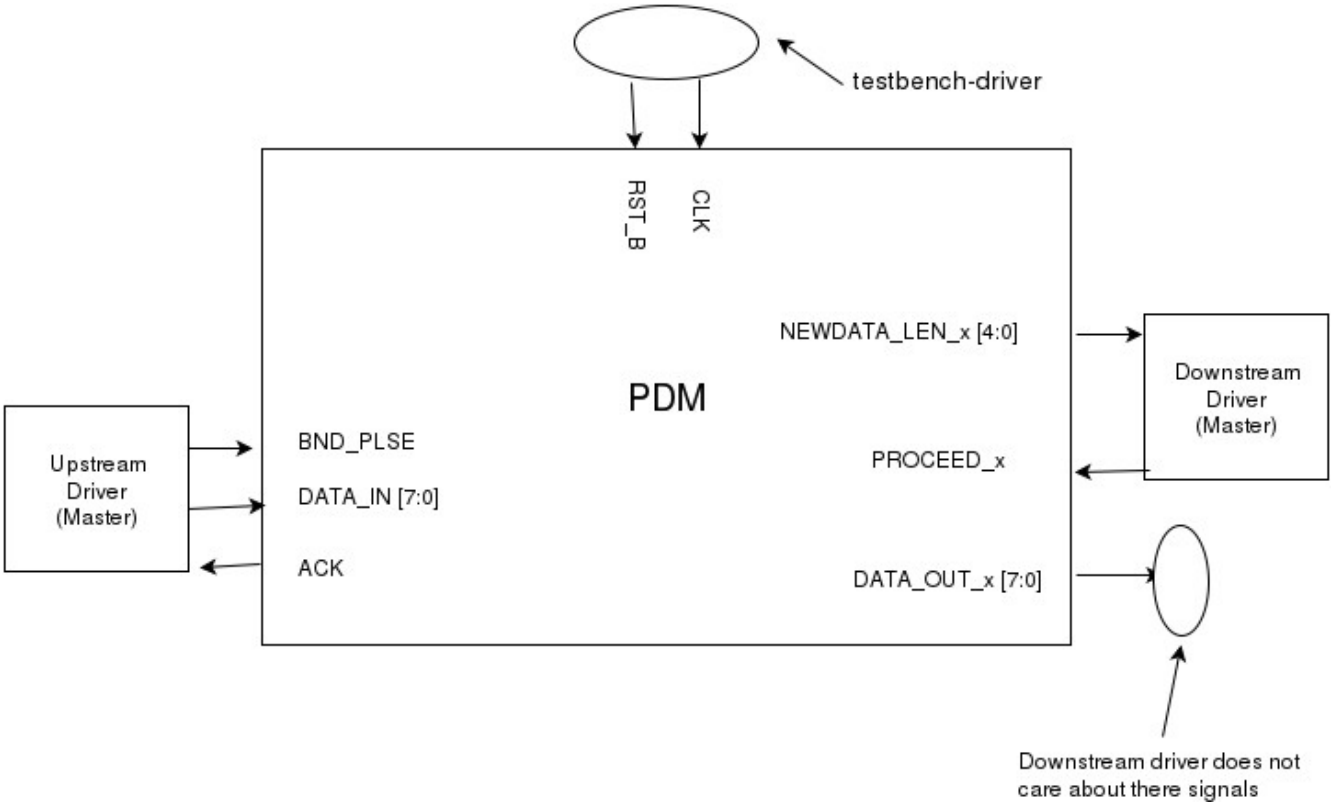
a. Block Diagram



b. Testbench Environment Requirement

- The device provide an 8-bit wide address/data bus.
- The clk has a nominal frequency of 50MHz.
- All interface packet transfer pins are synchronous to the rising edge of CLK.

c. Input Drive Requirement

- When the ACK is asserted,it shall be asserted for exactly 1 cycle.
- An external device connected to the PDM interface must not drive a new packet until at least 1 cycle after ACK is asserted.
- The PDM shall assert ACK within 1-4 cycles of the packet−terminating assertion of BND_PLSE.
- Packets received on the input interface are bounded by a single−cycle assertion of BND_PLSE coincident with both the first and last byte of each packet.

d. Input Drive Packet Protocol

- Wait for device reset deassertion.
- Assert BND_PLSE and first packet byte on DATA_IN.
- Commence driving a packet conforming the input interface protocol.
- Assert BND_PLSE and last packet byte on DATA_IN.
- ACK shall be asserted for a single cycle within 1-4 cycles of the packet-terminating assertion of BND_PLSE.

e. Output Drive Requirement

- NEWDATA_LEN_x, when asserted, shall be asserted for exactly 1 cycle.
- PROCEED_x must be asserted within 1-4 cycles of the assertion of NEWDATA_LEN_x.
- DATA_OUT_x shall be asserted exactly 1 cycle after the assertion of PROCEED_x.
- The first byte of each packet received on the input interface, which indicates the destination output port, is stripped off before the packet is forwarded to the appropriate output interface.

f. Output Drive Packet Protocol

- Wait for NEWDATA_LEN_x assertion.
- Wait for PROCEED_x assertion.
- On the next cycle after the PROCEED_x assertion, the PDM shall drive all packet payload bytes on the DATA_OUT_x bus without interruption and in the order received on the input interface until all payload bytes have been driven.