Out: September 29th, 2016
Due: October 6th, 2016

Goal

To use randomization and assertions to test your CME 341 Program Sequencer.

Procedure

Copy your CME 341 Program Sequencer Verilog file to a subdirectory of your CME_435 directory on your cabinet drive (i.e., H: drive).

Set up a directory structure identical to that used previously for your RAM and ROM modules. Reuse code from these exercises to save some of your development time.

It is expected that you will perform random tests on the Program Sequencer in order to verify its functionality. Appropriate test bench program coding will have to be done. This includes (but is not limited to):

- A class declaration for the random variable(s).
- Appropriate randomization constraints.
- The use of appropriate assertions to check error conditions (both in the test bench and for the Program Sequencer module operation).
- No output monitoring in the env is allowed. It must be done in the test program.

Create a test plan spreadsheet based on the CME_435_Testplan_Template.xls. Make sure that you have a test plan in place for the tests described before you attempt to do the actual verification using the Questa simulator on the Program Sequencer module. Note that running simulations in Questa is part of this assignment.

Deliverable

Completed test bench program (all source files) and test plan for this aspect of your CME 341 microprocessor.

Package the required files into a zip archive that includes your name, NSID, and student number in the filename, and email to the course marker Mehedi Hasan (mehedi.hasan@usask.ca) by midnight on October 6th.