

Packet DeMultiplexer (PDM)

Device Functional Specification, v1.0

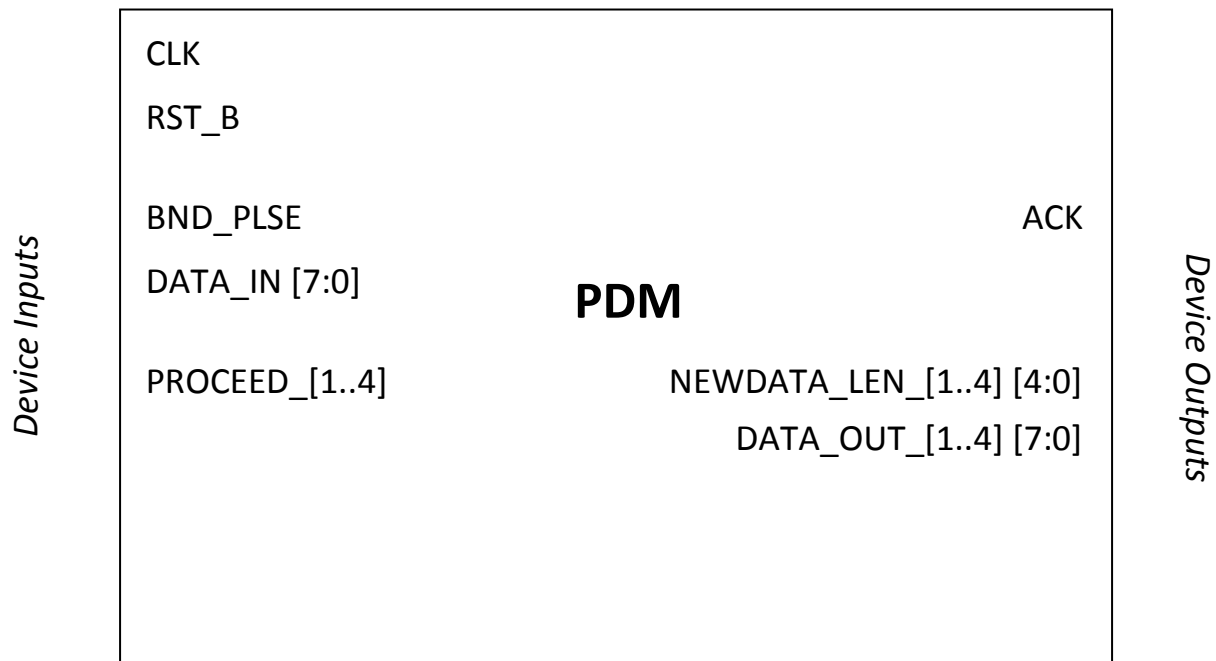
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1 Introduction

This document is the device functional specification for the Packet DeMultiplexer (PDM).

This device switches unidirectional unreliable packet traffic received by an external network interface to one of four output interfaces. The device provides an 8-bit wide address/data bus, limited end-to-end flow control, and parsing of packet payload sizes.

2 Block Diagram



3 Interfaces

3.1 Common

Name	Direction	Description
CLK	Input	Master clock. All interface packet transfer pins are synchronous to the rising edge of this clock.
RST_B	Input	Master reset. Active low. Asynchronous.

3.2 Input

The PDM accepts on its input interface packets that are to be routed to one of its output interfaces.

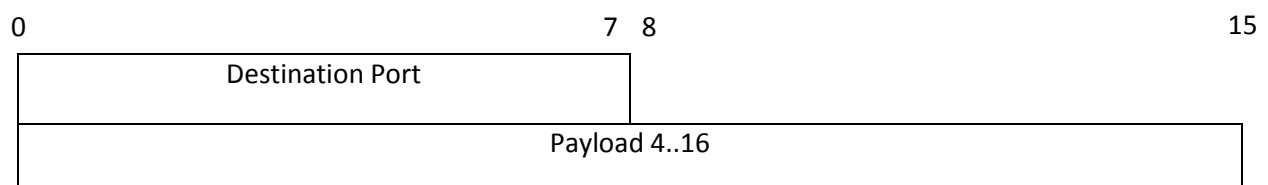
Name	Direction	Description
BND_PLSE	Input	Packet bounding indicator. Asserted high for a single cycle coincident with both the first and last byte of each packet.
DATA_IN [7:0]	Input	Packet data bus.
ACK	Output	Packet receipt acknowledgement. Shall assert for a single cycle within 1 to 4 cycles of the rising edge of each packet-terminating assertion of BND_PLSE.

3.3 Output

The PDM features four identical output interfaces to which packets received on the input interface may be routed.

Name	Direction	Description
NEWDATA_LEN_x [4:0]	Output	Conveys the payload size in bytes of the packet to be transmitted on the output interface. NOTE - payload size excludes destination port byte in the packet, which is stripped out before the packet is forwarded on the output interface. Shall assert for a single cycle within 1 to 4 cycles of the rising edge of the packet-terminating assertion of BND_PLSE.
PROCEED_x	Input	Output interface packet transmission grant. Must be asserted within 1 to 4 cycles of the transition to valid data on NEWDATA_LEN_x. Must assert for a single cycle only.
DATA_OUT_x [7:0]	Output	Packet data output bus. The first packet byte shall be driven precisely one cycle after the assertion of PROCEED_x, and the subsequent packet bytes shall be driven one per cycle without interruption until all packet bytes have been driven.

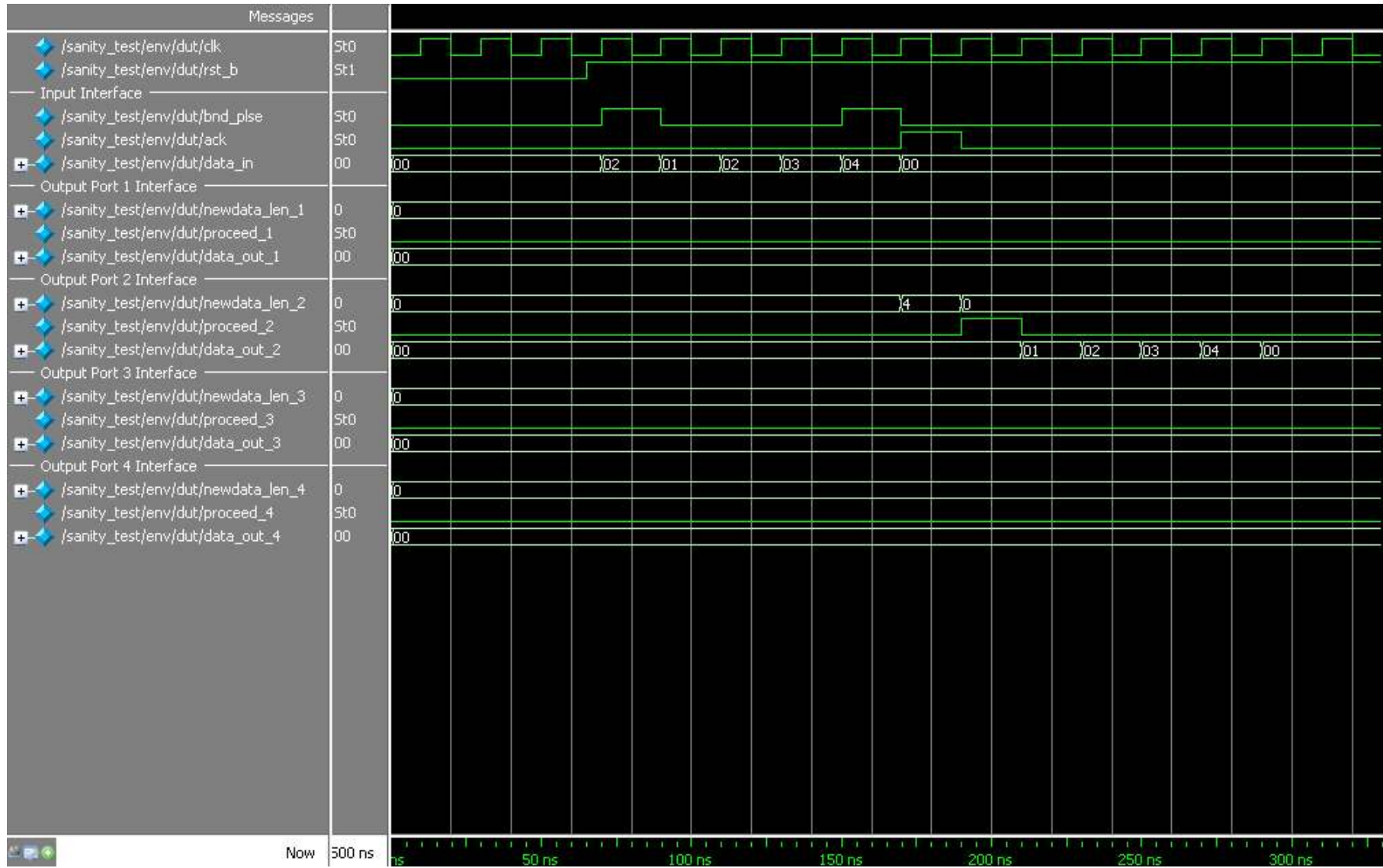
4 Packet Format



Destination Port – Specifies the output interface to which the packet should be routed. Ranges from 1-4.

Payload – Packet payload bytes. Ranges in size from 4 to 16 bytes in 4-byte increments. Individual payload bytes may range in value from 0-255.

5 Timing



6 Operation

6.1 Reset

To prepare the device for operation, the device must detect a low-to-high transition on the active-low RST_B signal. The device provides no explicit indication that it is out of reset.

Upon assertion of the RST_B signal, all device outputs shall immediately transition low. The internal data buffer is additionally cleared.

6.2 Clock

The device operates synchronously on a single clock signal, CLK, at a nominal frequency of 50MHz (20ns period).

6.3 Input Packet Transfer Protocol

At any time after the initial deassertion of RST_B, an external device may commence driving a packet conforming the input interface protocol. The external device must then wait for the assertion of ACK after this and each subsequent packet before commencing the driving of a new packet. ACK shall be asserted for a single cycle within 1-4 cycles of the packet-terminating assertion of BND_PLSE.

6.4 Packet Translation

The first byte of each packet received on the input interface, which indicates the destination output port, is stripped off before the packet is forwarded to the appropriate output interface.

6.5 Output Packet Transfer Protocol

Within 1-4 cycles of the packet-terminating assertion of BND_PLSE on the input interface, the packet payload size (which excludes the destination port byte) shall be asserted for a single cycle on the NEWDATA_LEN_x bus. Within a further 1-4 cycles of this packet payload size assertion, an external device connected to the PDM output interface must assert PROCEED_x. On the next cycle after the PROCEED_x assertion, the PDM shall drive all packet payload bytes on the DATA_OUT_x bus without interruption and in the order received on the input interface until all payload bytes have been driven.

Revision History

Version	Date	Changes
1.0	2012.10.27	Document created.