
ELECENG 2EI4: Electronic Devices and Circuits

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Project 2

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Date of Submission: March 3, 2025

As a future member of the engineering profession, the student is responsible for performing the required work in an honest manner, without plagiarism and cheating. Submitting this work with my name and student number is a statement and understanding that this work is my own and adheres to the Academic Integrity Policy of McMaster University and the Code of Conduct of the Professional Engineers of Ontario.

Test Plan

This test plan is designed to assess the performance of two switch types by analyzing key non-idealities such as ON resistance (R_{ON}), leakage current (I_{OFF}), and voltage behavior under controlled conditions. The evaluation will be conducted using a constant 5V DC power supply, a control signal in the form of a 100Hz square waveform oscillating between 0V and 5V (with an amplitude of 2.5V and an offset of 2.5V), and measurement tools including the AD2 and a $10k\Omega$ resistor for current calculations.

Switch Type 1

The voltage control will be configured to alternate between 0V and 5V using a square waveform. The supply voltage will be maintained at 5V DC, while V_1 is also set to 5V to ensure proper switch operation. The switching behavior will be examined by applying the control voltage and monitoring the corresponding voltage and current values.

When the control voltage is 0V, the switch is expected to be in the ON state, ideally resulting in $V_1=V_2=5V$. However, due to real-world imperfections, a minor voltage drop across the switch may occur, slightly reducing V_2 . Both V_1 and V_2 will be measured, and the current (I_{ON}) flowing through the switch will be recorded. Conversely, when the control voltage is set to 5V, the switch should transition to the OFF state, meaning no current should flow and both V_1 and V_2 should be 0V. Any observed nonzero voltage at V_2 will indicate leakage current (I_{OFF}), which will be calculated using the measured voltage across a $10k\Omega$ resistor.

To determine R_{ON} , Ohm's law will be applied using the measured voltage and current values when the switch is in the ON state. Similarly, leakage current (I_{OFF}) will be computed based on the voltage drop when the switch is OFF.

Switch Type 2

The test setup will remain the same as for Switch Type 1. The supply voltage will be held at 5V DC, and V_1 will be set to 3V to ensure proper switch operation. The control voltage will continue to oscillate between 0V and 5V using a square waveform with an amplitude of 2.5V and an offset of 2.5V.

When the control voltage is 0V, the switch should be in the ON state, ideally resulting in $V_1=V_A=3V$ though a slight voltage drop may still be present. The voltage at V_A and the corresponding current (I_{ON}) will be recorded. When the control voltage is 5V, the switch should transition to the OFF state, meaning $V_1=V_B=0V$. Any deviation from this expected result would indicate leakage current, which will be calculated based on the voltage across the $10k\Omega$ resistor. The ON resistance will be determined using Ohm's law.

The AD2 will be used to capture multiple voltage and current measurements to provide a thorough evaluation of switch performance. The focus remains on direct readings, ensuring a reliable assessment of efficiency and circuit isolation.

Switch 1:

Circuit Schematic:

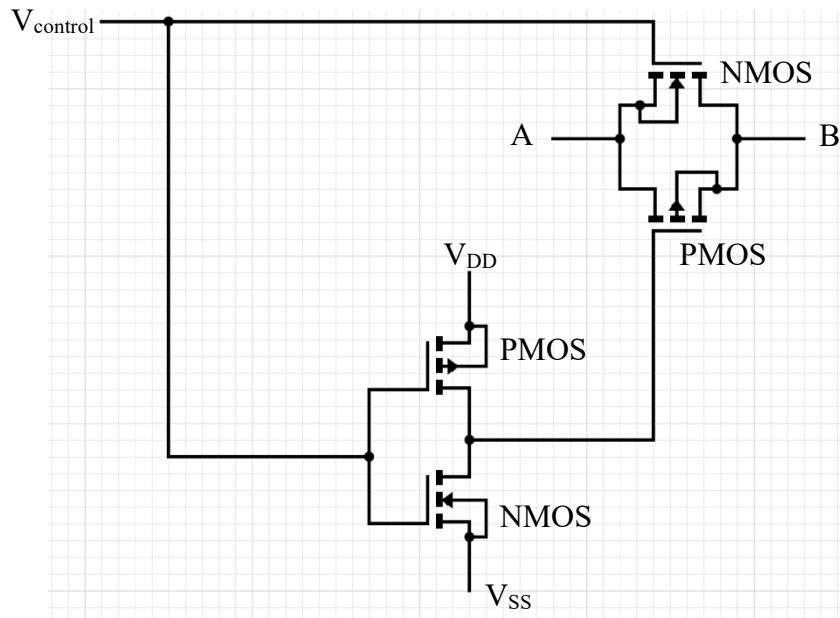


Figure 1: Schematic of Switch Type 1

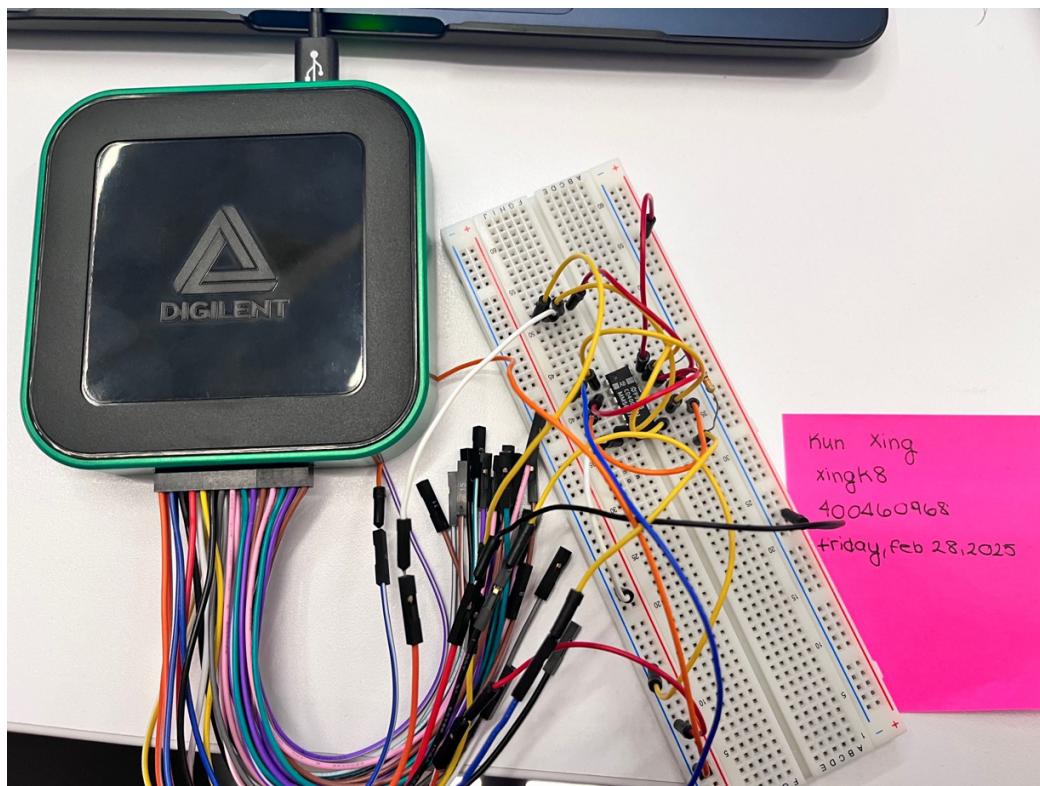


Figure 2: Physical Circuit of Switch Type 1

Measurements:

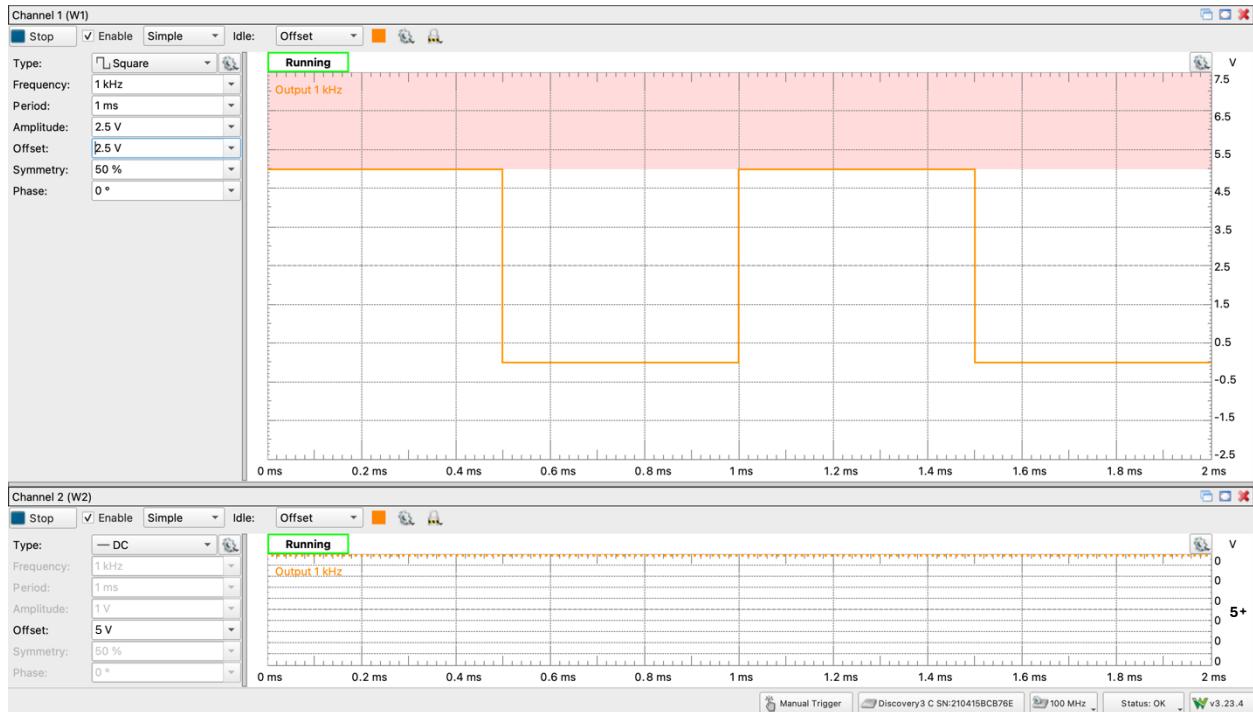


Figure 3: Waveform of $V_{control}$ and V_A

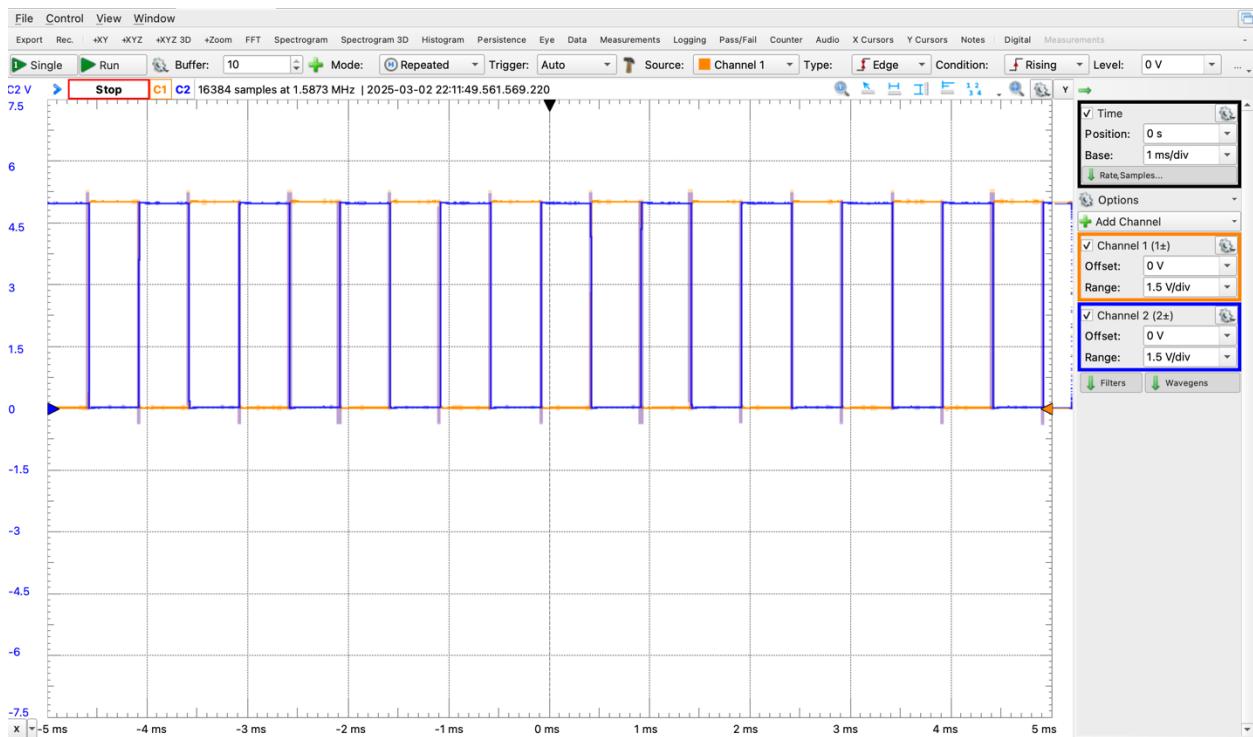


Figure 4: Waveform of $V_{control}$ (blue) and V_B (orange)

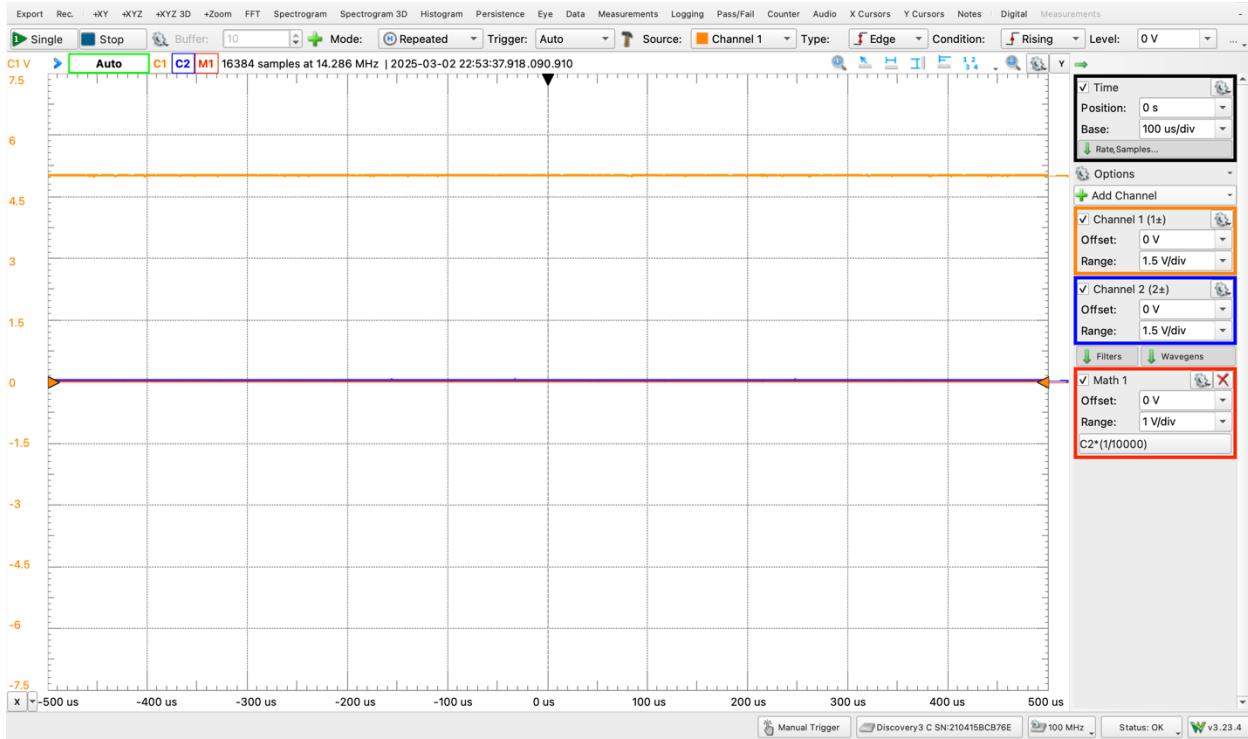


Figure 5: Waveform of $V_{control}$ as a DC 5V (orange), current at V_B (red) and V_B (blue)

$$I_1 = \frac{V_1}{R} = \frac{5.0684}{10k\Omega} = 0.50684 \text{ mA}$$

$$I_2 = \frac{V_2}{R} = \frac{5.0902}{10k\Omega} = 0.50902 \text{ mA}$$

$$R_{ON} = \frac{V_1 - V_2}{I_1 - I_2} = \frac{5.0684 - 5.0902}{0.50684 - 0.50902} = 10\Omega$$

Figure 6: Calculations for R_{ON}

Theoretical Explanation:

The observed results from the AD3 align with the expected theoretical behavior of a transmission gate, which consists of complementary NMOS and PMOS transistors. The circuit also includes an inverter, ensuring that only one transistor is ON at a time, thereby preventing both MOSFETs from conducting simultaneously. The transmission gate functions as a bidirectional switch, controlled by $V_{control}$, allowing or blocking signal transmission between V_A and V_B .

When $V_{control}$ is 0V, the PMOS transistor is ON, enabling conduction, while the NMOS transistor is OFF. This effectively connects V_A and V_B , ensuring $V_A = V_B$ ideally. The oscilloscope readings, as shown in Figure 4, confirm this behavior—when $V_{control}$ (Channel 1) is 0V, V_B (Channel 2) reads 5V, which matches the input voltage V_A (a constant DC voltage of 5V), as seen in Figure 3. This verifies that the switch is successfully conducting in the ON state.

When $V_{control}$ is 5V, the PMOS transistor turns OFF, while the NMOS transistor turns ON. However, since the NMOS's source is disconnected, no conduction occurs, and the transmission gate acts as an open switch, fully isolating V_A from V_B . This behavior is confirmed in Figure 4, where when $V_{control}$ (Channel 1) is held at 5V, causing V_B (Channel 2) to drop to 0V, indicating that V_A and V_B are no longer connected. This is also confirmed in Figure 5, where when a DC supply of 5V is applied ($V_{control}$), the calculated current through the $10k\Omega$ resistor is around 0A, implying the switch is open.

Because of the design, there is a small amount of leakage current when the switch is closed, as no MOSFET is entirely ideal. Additionally, the ON resistance (R_{ON}) of the transmission gate is not exactly zero, leading to minor voltage drops between V_A and V_B when the switch is conducting. Similarly, in the OFF state, while the transmission gate successfully isolates the circuit, the OFF resistance is not infinite, meaning some minimal leakage current may still be present due to the MOSFET junction capacitances. These deviations from ideal behaviour are expected and are a result of component limitations and fabrication constraints. Despite these minor non-idealities, the experimental results confirm that the transmission gate operates as intended, switching between ON and OFF states effectively, while maintaining acceptable performance within expected tolerances.

Design Trade-Offs:

Several design trade-offs were made to balance circuit complexity, power consumption, and switching performance in the transmission gate design. These trade-offs impacted the number of transistors used, switching speed, power efficiency, and voltage handling capabilities, ensuring that the circuit met requirements while maintaining efficiency.

Instead of using a single MOSFET, four transistors (two NMOS and two PMOS) were used to achieve bidirectional operation. While this approach increases circuit complexity, it significantly enhances the transmission gate's versatility for application. A single MOSFET would introduce voltage threshold limitations, preventing proper signal transmission in both directions. By using a complementary NMOS-PMOS pair, the gate can pass both high and low signals efficiently, reducing signal distortion.

The choice of MOSFET size also influences switching speed and power consumption. Smaller MOSFETs allow for faster switching speeds which reduces switching delays. This is beneficial in high-speed digital applications where fast transitions are required. However, smaller MOSFETs also introduce higher ON resistance (R_{ON}) and may limit the amount of current or voltage the switch can handle. A larger MOSFET could be used to reduce ON resistance (R_{ON}) and allow for higher current flow, but this would increase power consumption and switching delay. To balance these factors, a moderate MOSFET size was chosen.

Power efficiency was prioritized by selecting a simpler circuit design that effectively manages voltage and current levels without unnecessary complexity. The transmission gate's MOSFET threshold voltage was chosen to ensure proper switching behaviour while minimizing leakage current in the OFF state. These trade-offs allowed the circuit to achieve reliable signal

transmission with low power consumption, making it suitable for digital logic and switching applications.

Switch 2:

Circuit Schematic:

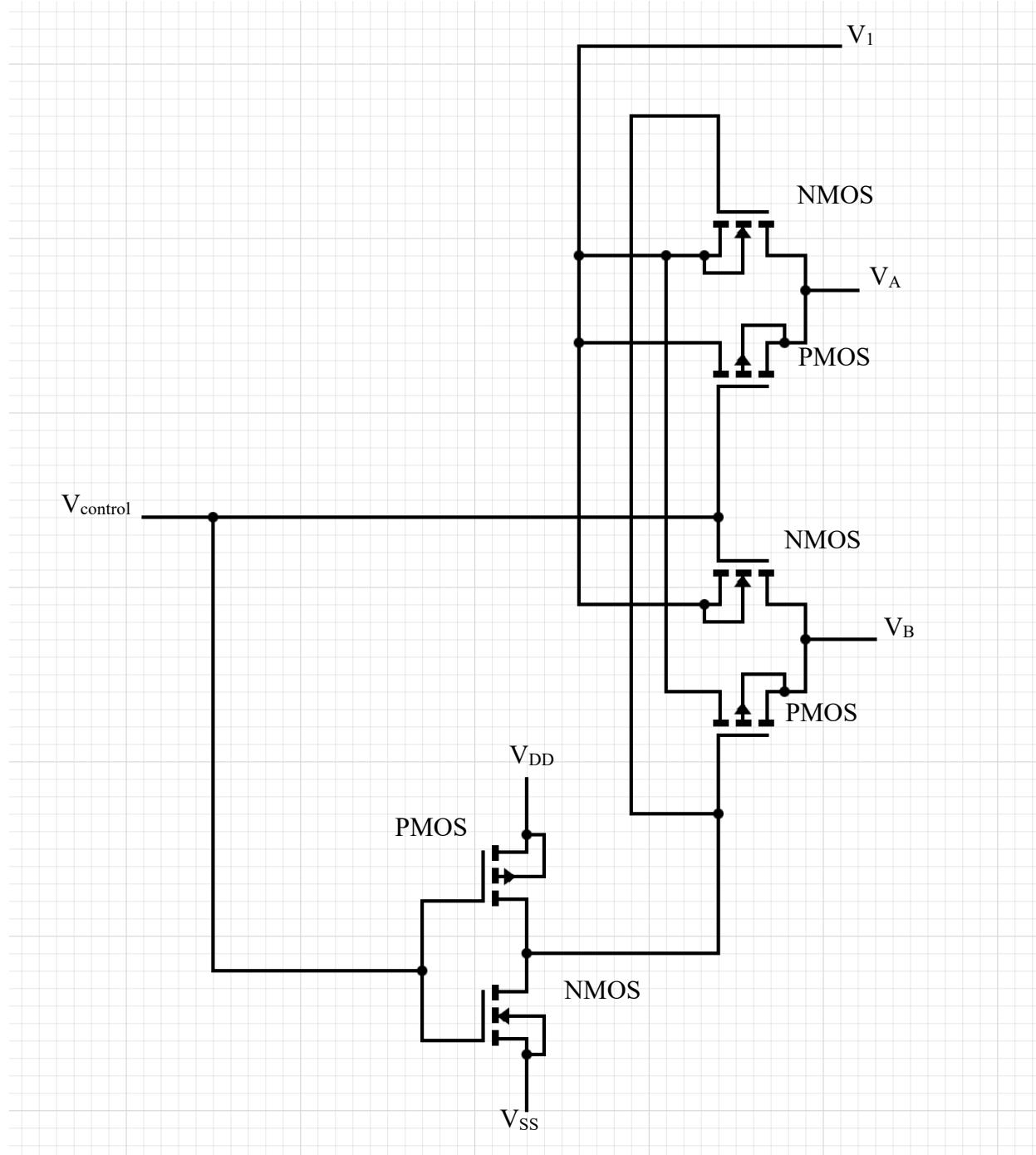


Figure 5: Schematic of Switch Type 2

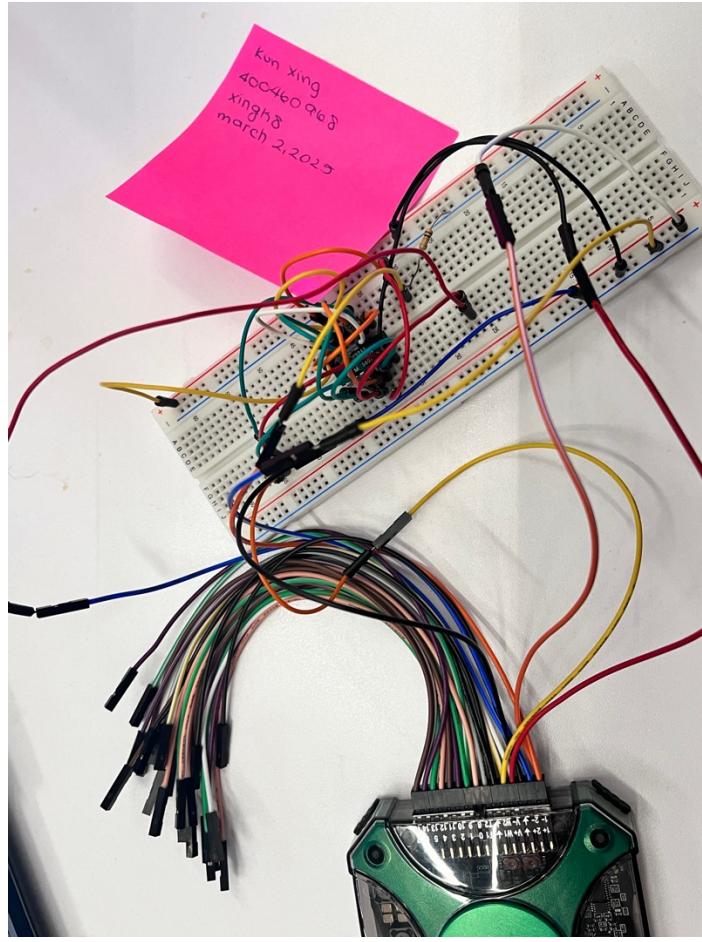


Figure 6: Physical Circuit of Switch Type 2

Measurements:



Figure 7: Waveform of $V_{control}$ (orange) and V_A (blue)

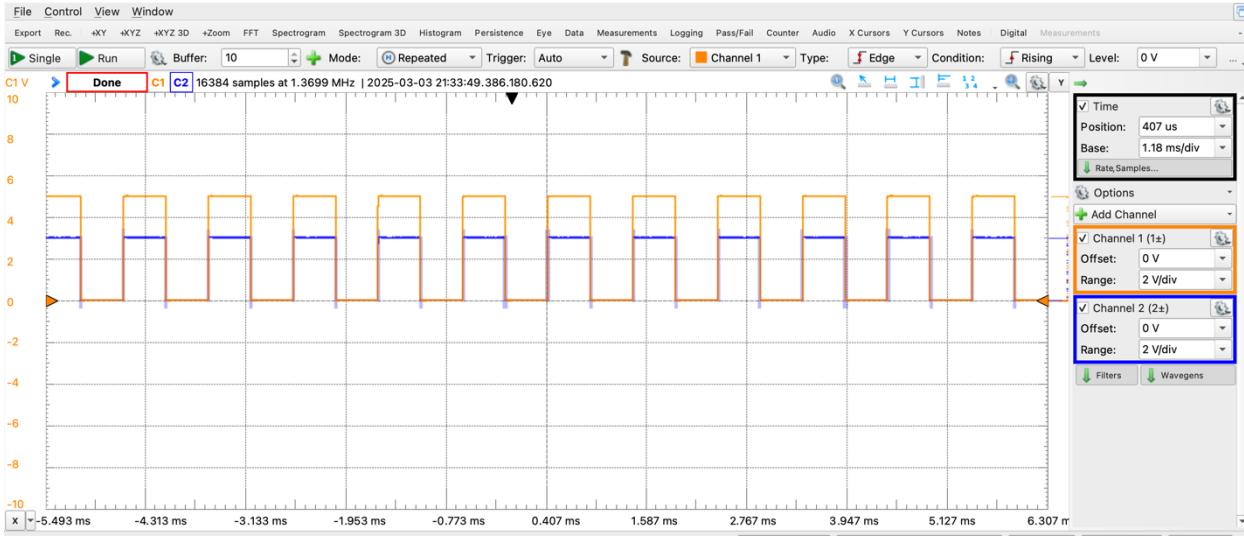


Figure 10: Waveform of V_{control} (orange) and V_B (blue)

$$I_1 = \frac{V_A}{R} = \frac{3.0698}{10k\Omega} = 0.30698 \text{ mA}$$

$$I_2 = \frac{V_B}{R} = \frac{3.07561}{10k\Omega} = 0.307561 \text{ mA}$$

$$R_{ON} = \frac{V_A - V_1}{I_1} \text{ or } \frac{V_B - V_1}{I_2}$$

$$R_{ON} = \frac{3.07561 - 3}{0.307561} = 0.2458\Omega$$

Figure 12: Calculations for R_{ON}

Theoretical Explanation:

According to the test plan, when the control signal V_{control} (orange) is set to 0V and V_1 is set to a constant 3V DC supply, V_1 should be connected to V_A , meaning V_A should ideally match V_1 where V_1 is a DC input of 2V. In this state, the NMOS transistor is conducting, while the PMOS transistor remains OFF. The oscilloscope confirms this behavior, with the measured output voltages showing $V_1=V_A=2V$ (V_A is blue in Figure 8) and $V_B=0V$ (V_B is blue in Figure 9), which corresponds to the expected behaviour.

When the control signal is raised to 5V, the switch transitions so that V_B is now linked to V_1 , meaning V_B should ideally be equal to V_1 where V_1 is a DC input of 2V . Here, the PMOS transistor turns ON while the NMOS transistor is in the OFF state. The oscilloscope readings confirm this expected behavior, with $V_1=V_B=2V$ and $V_A=0V$, while the control voltage remains at 5V. These results align with the expected switching operation and have been validated using the AD2 measurements.

As with Switch Type 1, a small amount of leakage current is present when the switch is in the closed state due to the transmission gate having a finite ON resistance. Additionally, when the switch is open, the gate does not act as a perfect insulator, allowing for a slight leakage current. These effects result from inherent component limitations, design compromises, and manufacturing tolerances.

Design Trade-Offs:

In designing Switch Type 2, several trade-offs were considered to balance performance, complexity, and cost. The primary focus was on optimizing switching speed and minimizing power consumption while ensuring bidirectional operation. Achieving low ON resistance was a key objective, as it directly impacts efficiency and voltage drop across the switch. However, this came at the cost of increased circuit complexity and a larger number of MOSFETs.

One of the main compromises involved increasing the number of MOSFETs to six to achieve a sufficiently low ON resistance while maintaining appropriate switching speeds and meeting the voltage requirements. A simpler design with fewer transistors would have been easier to implement and more cost-effective, but it would have resulted in a higher ON resistance, reducing overall performance. By expanding the design with additional MOSFETs, the circuit ensures better conductivity when ON while still switching effectively within the required voltage range.

Another factor considered was the trade-off between switch size and efficiency. A physically smaller switch would have been easier to integrate, but it would have led to greater resistance, impacting power loss and voltage regulation. By maintaining bidirectionality in the design, the switch is capable of handling signals more efficiently while keeping power consumption low.

Ultimately, the decision to prioritize performance and reliability over cost and simplicity resulted in a more complex design. However, this approach allows the switch to operate efficiently under the given constraints, making it a suitable choice for applications where low resistance and high-speed switching are critical.