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# **ELECENG 2EI4: Electronic Devices and Circuits**

## **I**

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### **Project 3**

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As a future member of the engineering profession, the student is responsible for performing the required work in an honest manner, without plagiarism and cheating. Submitting this work with my name and student number is a statement and understanding that this work is my own and adheres to the Academic Integrity Policy of McMaster University and the Code of Conduct of the Professional Engineers of Ontario.

## **1: Circuit Schematic**

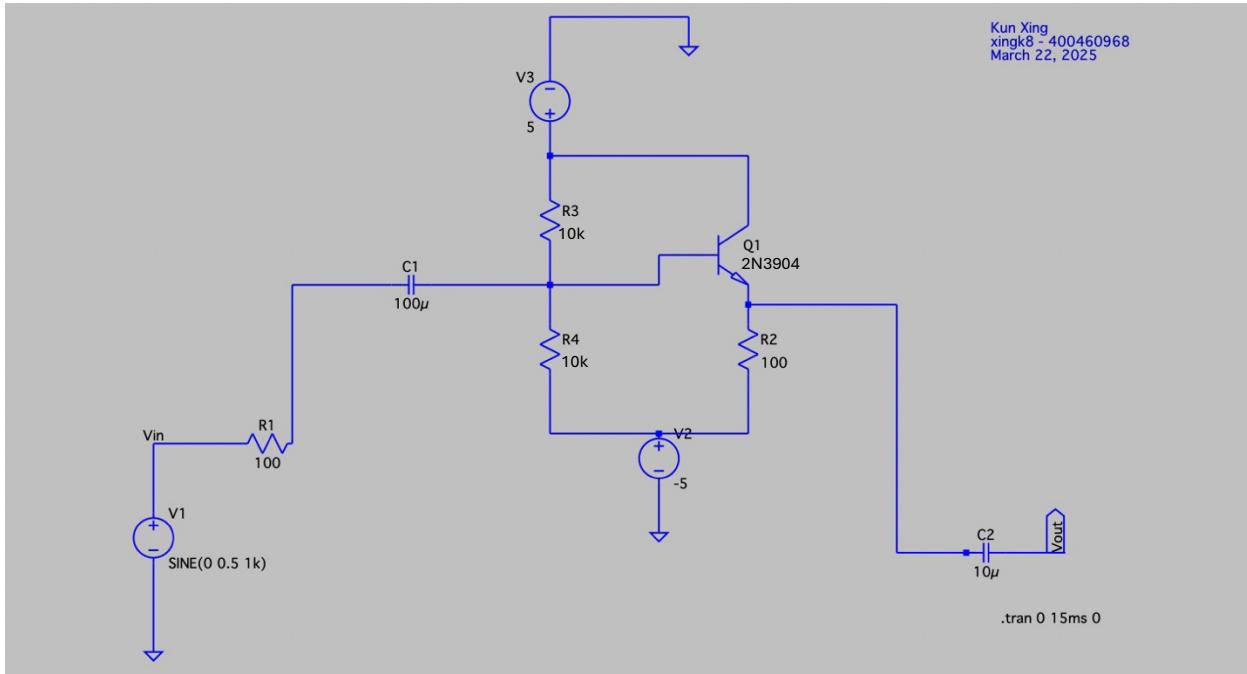


Figure 1: Circuit schematic

### a) What type of transistor did you choose (MOSFET/BJT)? Why?

A BJT was chosen over a MOSFET for this circuit as it better suits the requirement of a linear buffer. First, BJTs generally provide a higher  $g_m$  value than MOSFETS, meaning a small change in input voltage results in a larger change in output current as seen by BJT equation given in *Figure 2*. This leads to better voltage gain in the linear operating region, which is essential for maintaining consistent and predictable amplification. Additionally, BJTs have lower input capacitance at the base compared to the gate of a MOSFET. This reduces the time it takes for the transistor to respond to changes in put, resulting in a faster response time and better performance with signals that change quickly. Another factor is signal fidelity, where BJTs tend to produce cleaner, more accurate analog output when operated in their linear region, which is crucial in applications like buffering where the output should closely follow the input. While MOSFETs offer higher input resistance, they can introduce more distortion in linear analog circuits.

$$g_m = \frac{I_c}{V_T}$$

Figure 2: BJT  $g_m$  equation

**b) What amplifier topology (CE/CS/CD/etc.) did you choose? Why?**

A common collector (CC) amplifier topology was used. The configuration is ideal for buffer applications because it provides a voltage gain close to 1 as seen in *Figure 3*, meaning the output voltage will closely follow the input voltage with minimal attenuation. The design specification required less than 10% signal attenuation, which corresponds with a minimum gain of 0.9. The common collector satisfies this requirement, as its gain is slightly less than one but still very close. The output is taken from the emitter, and the emitter voltage “follows” the base voltage minus a small voltage drop. Additionally, this topology offers a high input resistance and low output resistance, which makes it well-suited to achieve the small gain desired. It also allows for a large voltage swing at the output, which improves signal handling. Overall, the common collector topology matches the linearity, gain, and impedance characteristics required by the project, making it a practical and efficient choice.

$$\frac{g_m R_L}{1 + g_m R_L} \cdot \frac{R_{in}}{R_{in} + R_s} \approx 1$$

*Figure 3: CC gain equation*

**c) What calculations did you use to determine the required component values?**

Given:

$$|v_{in}| = 0.5V \text{ (since } v_{in} \text{ is a sine wave with amplitude } 0.5V)$$

Allowed input signal range from formulas:

$$0.2V_T(1 + g_m R_L) \geq 0.5 \text{ where } V_T = 25 \text{ mV and } R_L = 100\Omega$$

$$0.2(25 \times 10^{-3})(1 + g_m(100)) \geq 0.5$$

$$(5 \times 10^{-3} + 5 \times 10^{-1} \times g_m) \geq 0.5$$

$$0.5g_m \geq 0.495$$

$$g_m \geq 0.099 = 990 \text{ mS}$$

$A_v$  from formulas:

$$A_v = \left[ \frac{g_m R_L}{1 + g_m R_L} \right] \left[ \frac{R_{in}}{R_{in} + R_s} \right] \text{ where } R_s = 100\Omega, R_L = 100\Omega, g_m = 990 \text{ mS and } A_v > 0.9$$

$$0.9 \leq \left[ \frac{(990m)(100)}{1 + (990m)(100)} \right] \left[ \frac{R_{in}}{R_{in} + 100} \right]$$

$$0.9 \leq \left[ \frac{99}{100} \right] \left[ \frac{R_{in}}{R_{in} + 100} \right]$$

$$\frac{90}{99} \leq \left[ \frac{R_{in}}{R_{in} + 100} \right]$$

$$\frac{90}{99} R_{in} + \frac{9000}{99} \leq R_{in}$$

$$\frac{9000}{99} \leq \frac{9}{99} R_{in}$$

$$R_{in} \geq 1000\Omega = 1k\Omega$$

$R_{in}$  from formulas:

$R_{in} = r_\pi(1 + g_m R_L)$  but  $R_1$  and  $R_2$  are in parallel so  $R_{in}$  changes as seen below

$R_{in} = R_1 || R_2 || r_\pi(1 + g_m R_L)$  where  $r_\pi = \beta/g_m$  and  $\beta = 100$  for the 2N3904 BJT

$$R_{in} = R_1 || R_2 || \left(\frac{100}{900m}\right)(1 + (990m)(100))$$

$$R_{in} = R_1 || R_2 || \left(\frac{1}{9} + 10000\right) = R_1 || R_2 || 10.11k$$

Choose  $R_1$  and  $R_2$  values to satisfy  $R_{in} > 1000\Omega$ , if  $R_1 = R_2 = 10k\Omega$  then:

$$R_{in} = \frac{1}{\frac{1}{10k} + \frac{1}{10k} + \frac{1}{10.11k}} = 3.34547k\Omega \text{ which satisfies } R_{in} > 1000\Omega = 1k\Omega$$

## 2: Simulation Results

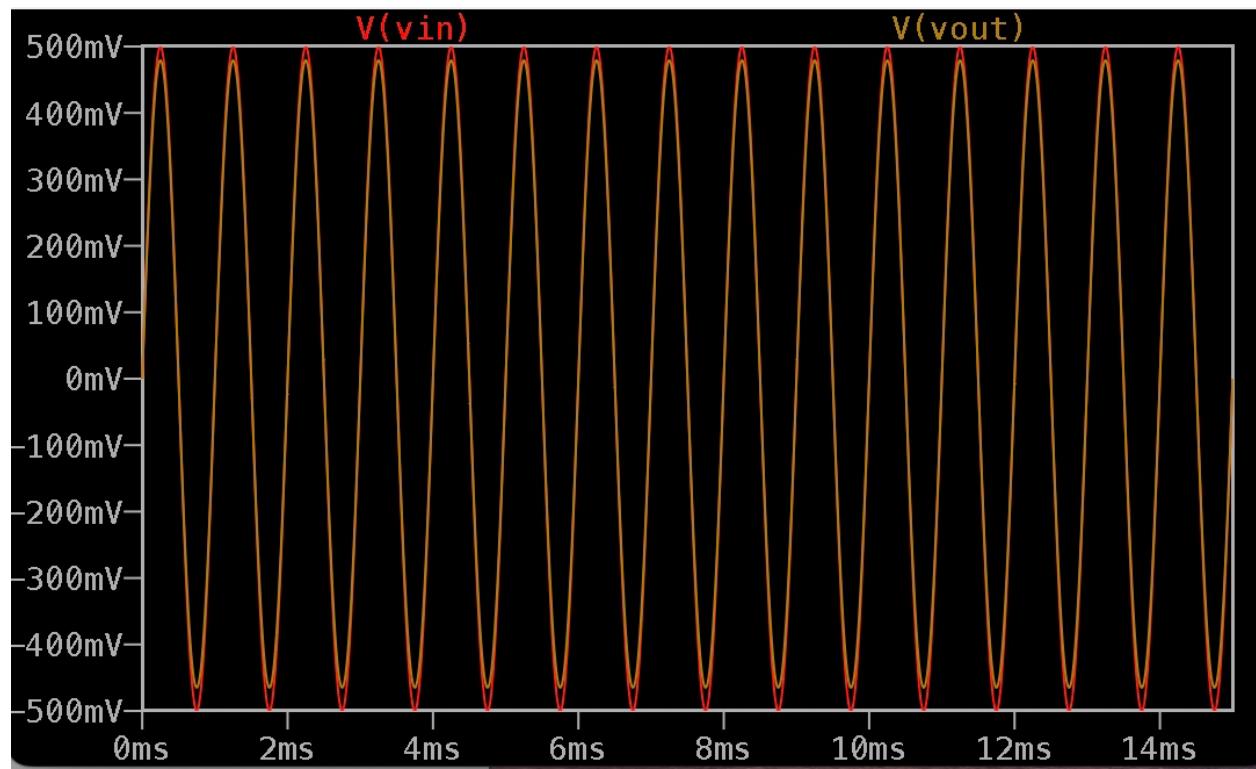


Figure 4: LTSpice simulation graph

**a) How did you model the transistor in the simulator you used?**

As seen in Figure 1, the transistor used was a 2N3904 BJT. The specifications for the 2N3904 BJT was obtained through the component search in LTSpice. The input voltage included sinusoid with an amplitude of 0.5V and frequency of 1kHz, applied through a  $100\Omega$  source resistor. The signal passes through a  $100 \mu F$  capacitor (C1), blocking any DC component and only allows only the AC signal to reach the transistors base. The base is biased using a voltage divider formed by two  $10k\Omega$  resistors (R3 and R4) connected between +5V and -5V. The transistor is configured in a common collector topology, with the collector connected to +5V and the emitter connected to ground through a  $100\Omega$  resistor (R2/RL) then to -5V. The output is taken from the emitter and passed through a  $10 \mu F$  capacitor (C2) to remove any DC offset.

**b) What setting did you use for each simulation (transient/dc sweep/frequency sweep/etc.)?**

A transient analysis was performed with a simulation stop time 15 ms was used, which allowed for several full cycles of the 1kHz input waveform to be analyzed. Both  $V_{in}$  and  $V_{out}$  were plotted with red and orange with  $V_{in}$  being the sinusoid mentioned in part (a), respectively. Through visual inspection, the lines mostly overlapped in both amplitude and phase. This overlap indicates that the amplifier circuit operates with a gain of  $\approx 1$ , consistent with the behaviour of a common collector buffer circuit.

**c) The overall gain determined form the simulations.**

By taking two sample points of values  $V_{in} = 498.36V$  and  $V_{out} = 484.33V$ , the resulting gain ( $V_{out}/V_{in}$ ) is around 0.97185, meeting the project requirements of 0.9.

**d) Other performance parameters determined from the simulations.**

Another performance parameter determined from the simulation is  $R_{in}$ . To calculate  $R_{in}$ , Ohm's law would be used to result in the equation shown in Figure 5. Using values from the simulation of  $V_{in} \approx 0.5V$  and  $I_{in} \approx 120 \mu A$  results in a  $R_{in}$  of approximately  $4.17 k\Omega$ , satisfying the requirement that  $R_{in} > 1k\Omega$ .

$$R_{in} = \frac{V_{in}}{I_{in}}$$

Figure 5:  $R_{in}$  equation using Ohm's law

### 3: Physical Circuit

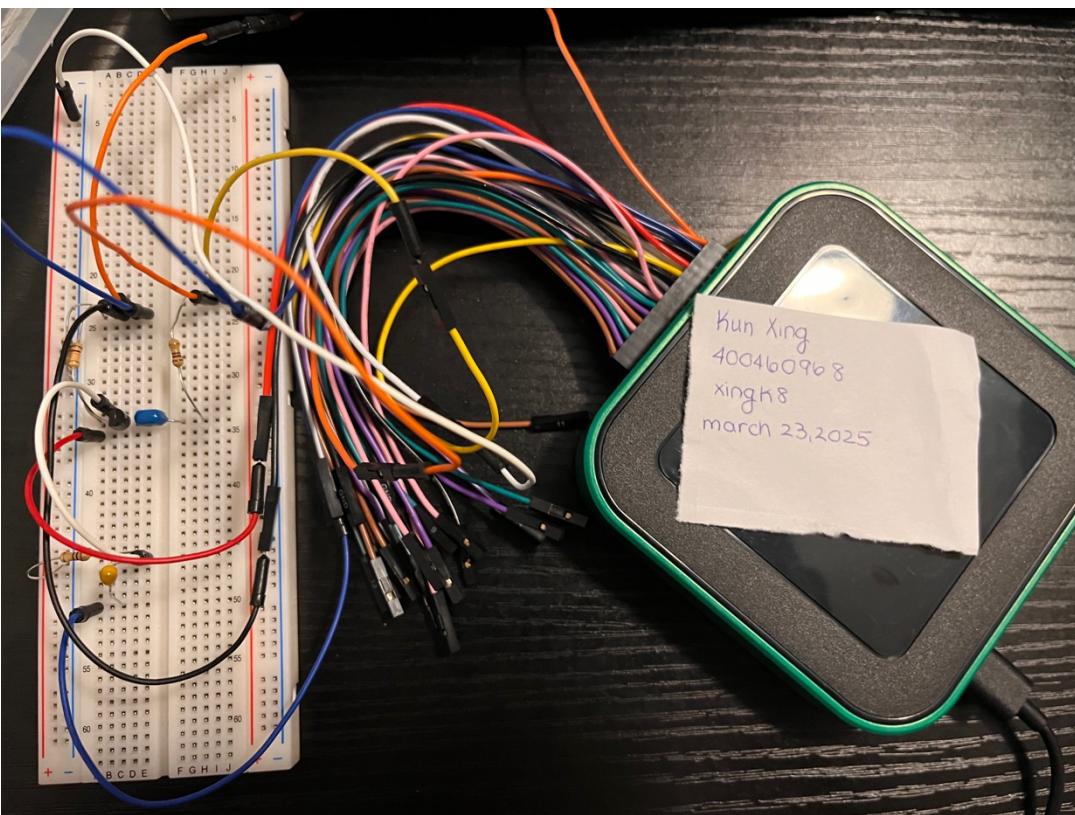


Figure 6: Physical circuit

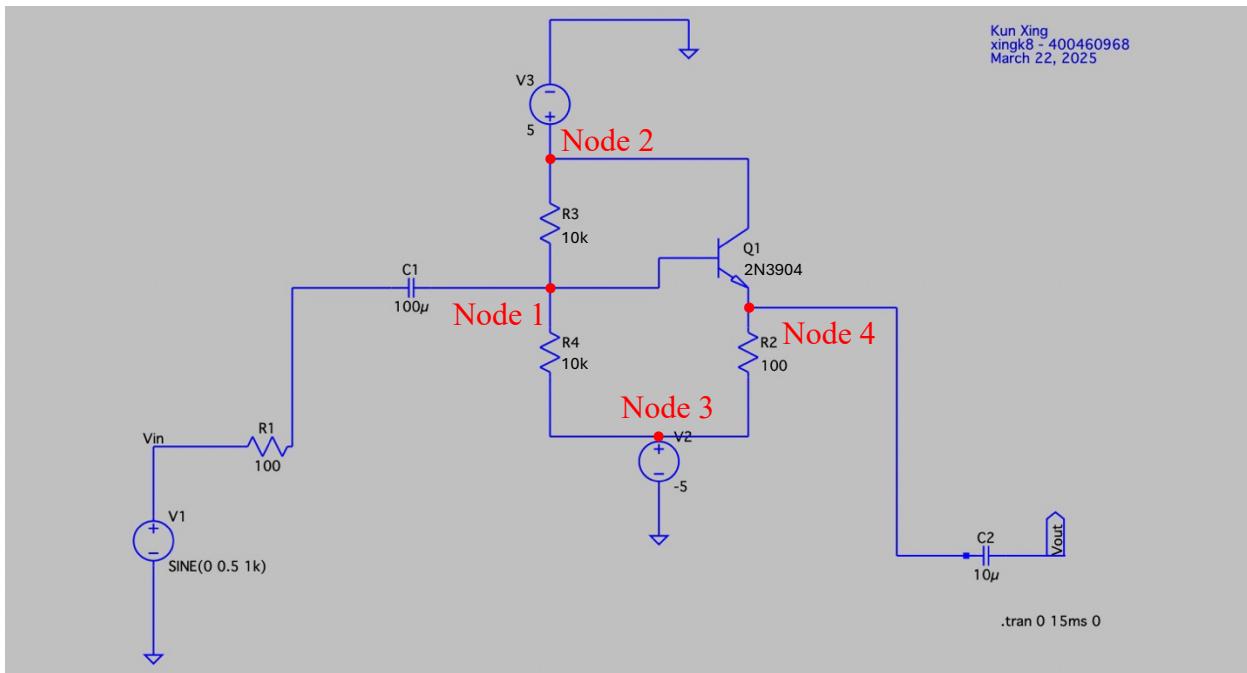


Figure 7: LTSpice circuit schematic with corresponding nodes labeled on physical circuit in Figure 9

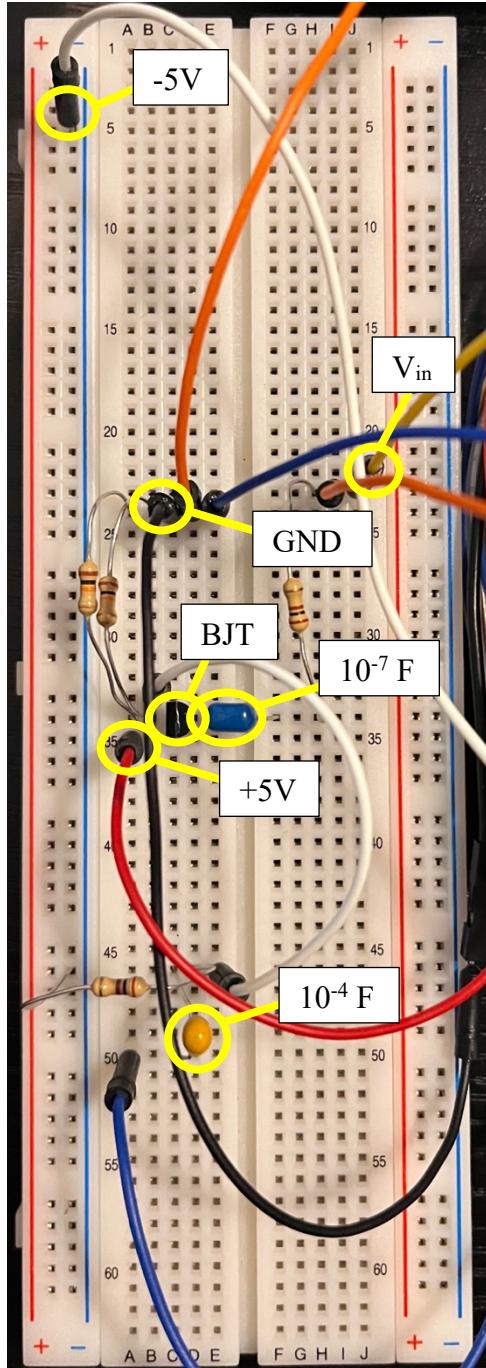


Figure 8: Physical circuit components

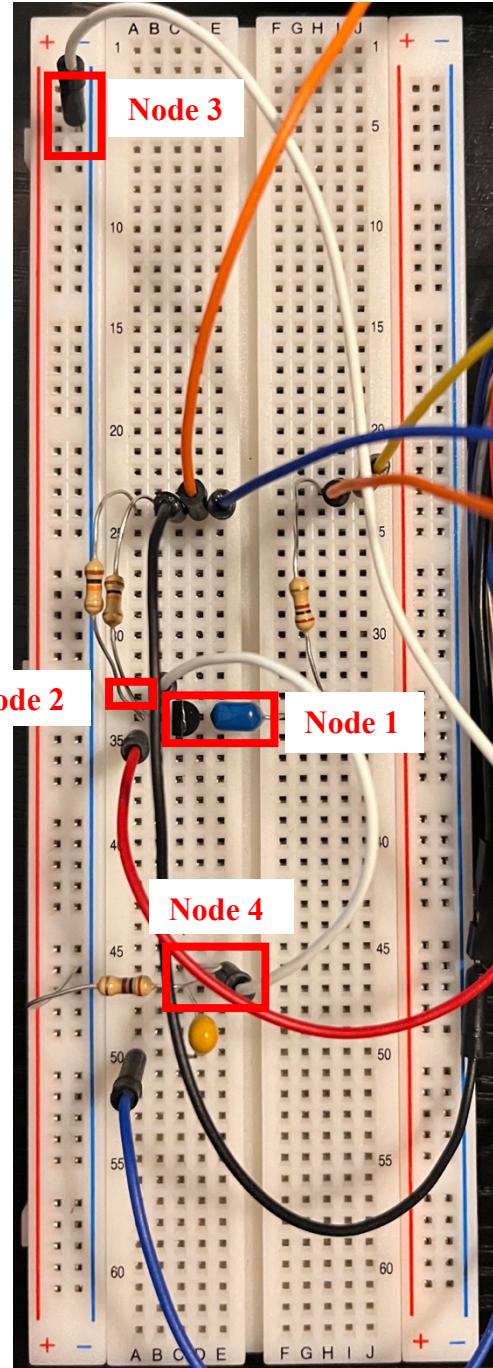


Figure 9: Physical circuit nodes

## 4: Waveform Results

- a) What measurements did you do? (E.g. waveforms as functions of time, XY plot, network analyzer, etc. You decide which measurements are beneficial and explain why you used them.)

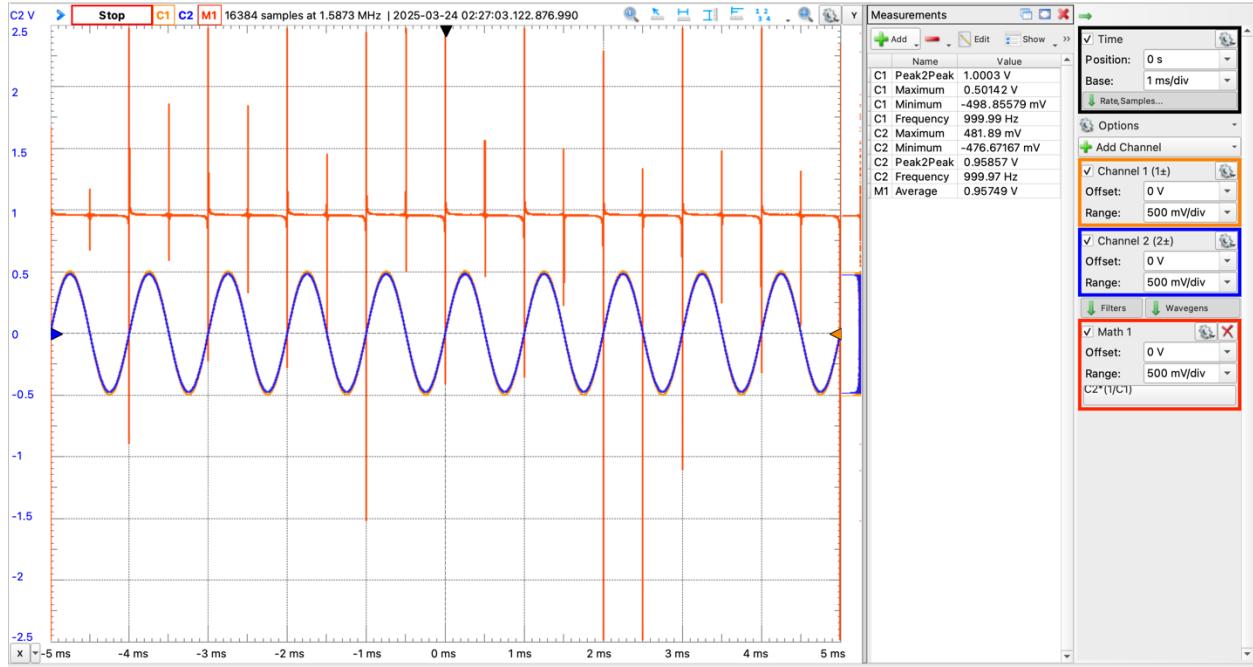


Figure 10: Waveform simulation with  $V_{in}$ ,  $V_{out}$ , and gain

To evaluate the performance of the amplifier circuit, both the input and output waveforms were captured using an oscilloscope. As shown in Figure 10, Channel 1 (orange) represents the input signal, while Channel 2 (blue) represents the output signal. The input waveform is a sinusoidal signal with a peak-to-peak value of approximately 1V and a frequency of 999.99 Hz, which aligns with the expected 1 kHz signal. The output waveform closely follows the input in shape and timing, with a slightly lower peak-to-peak value of approximately 954.57 mV. Additionally, through visual inspection, the output waveform closely follows the input, as expected from a buffer. The observations through visual and numerical inspection confirms that the amplifier a voltage gain of around one, which is consistent with the behaviour of a common collector buffer. The measurements confirm a gain of roughly 0.96 as seen by the average, which satisfies the project requirement of maintaining at least 0.9 gain. The waveforms are well-aligned in phase and frequency, and no significant distortion is visible, indicating good linearity and signal fidelity.

- b) How did you determine the midband gain for your amplifier? What value did you obtain? Compare your value with what was expected from calculations and simulations.**

In the waveform graph, the Math 1 Channel (red) is defined by the ratio of the output voltage (C2) to the input voltage (C1) (calculating  $V_{out}/V_{in}$ ) as seen in Figure 10. The average value of this ratio over the waveform duration represents the average voltage gain of the amplifier during steady state, also known as the midband gain. In this case the average shown for the Math 1 Channel is approximately 0.9574, meaning that on average the output is about 96% of the input voltage which is above the required 90%. Comparing the measured gain to the theoretical gain, there is a percentage difference of 1.49% (0.95749 vs. 0.97185) which may be attributed to tolerance in component values or parasitic elements in the simulated circuit.

- c) Demonstrate linearity at an input amplitude of 0.5V.**

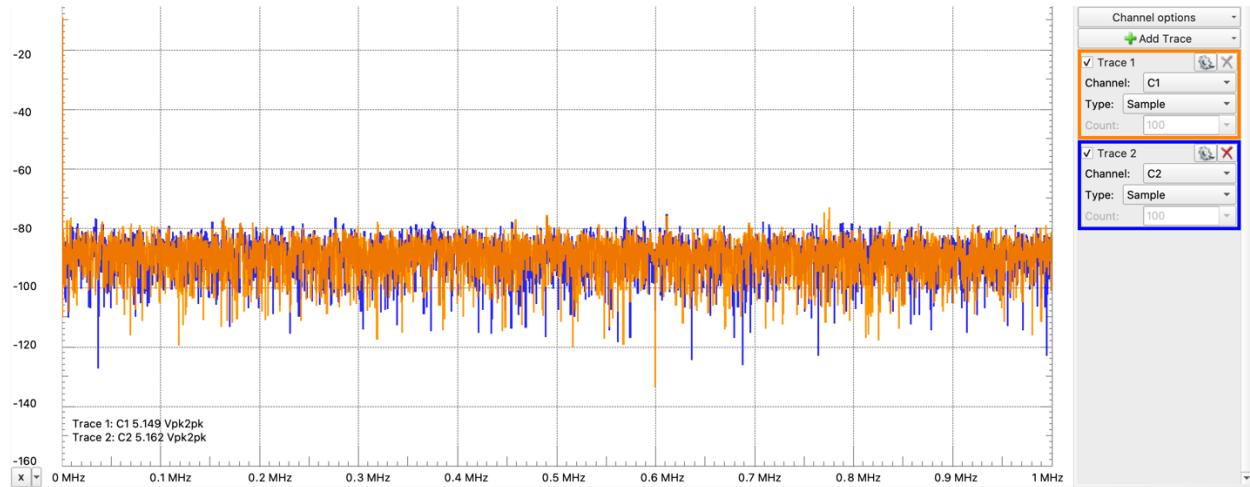


Figure 11: Waveform spectrum graph of  $V_{in}$  and  $V_{out}$

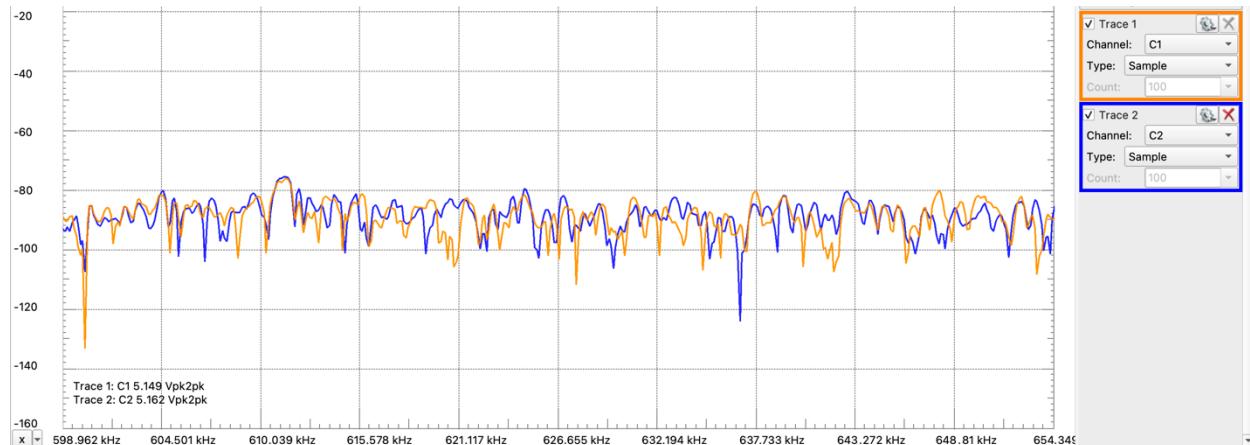


Figure 12: Zoomed-in waveform spectrum graph of  $V_{in}$  and  $V_{out}$

To assess the linearity of the amplifier, the spectrum analyzer was used as shown in Figure 11 and Figure 12. In both cases, Channel 1 (orange) represents the input signal and Channel 2 (blue) represents the output signal. Linearity within an amplifier means that it reproduces the input signal without introducing distortions. In the frequency domain, this would appear as the output having similar frequency components as the input. In the first graph, which is a broad frequency sweep up to 1 MHz, both signals remain relatively flat and overlap similarly without significant distortions or random peaks, indicating minimal distortion. The second graph provides a zoomed-in view around the 600-650 kHz region, where the input and output again both are very similar in shape and amplitude. This similarity confirms that the amplifier is not adding any non-linear components or unwanted frequencies to the output signal. Since both input and output signals maintain similar peak levels and follow the same frequency implies that the amplifier is behaving linearly across the tested frequency range.

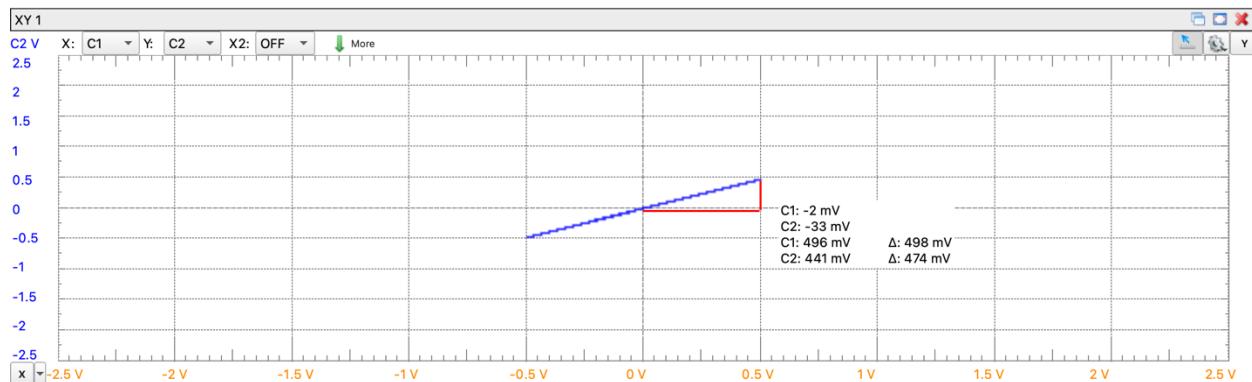


Figure 13: Waveform graph of  $V_{in}$  versus  $V_{out}$

The linearity can also be demonstrated by plotting  $V_{in}$  versus  $V_{out}$  using an XY plot as shown in Figure 13. In a linear amplifier, the output should be directly proportional to the input, resulting in a straight line when  $V_{out}$  is plotted against  $V_{in}$ . As shown in Figure 13, the plot forms a clean, diagonal straight line, which confirms a linear relation between input and output signals. This indicates that the amplifier maintains a constant over the full range of the input signal without introducing distortion. The slope represents the gain, which is close to 1 (0.96 with measured values), which is expected from a common collector configuration and matches with the waveform gain from Figure 10. This measurement supports the conclusion from the spectrum analysis that the amplifier operates in a linear behaviour.