
ELECENG 2EI4: Electronic Devices and Circuits I

Project 1

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Problem Summary

The objective of this project is to design and build a DC power supply capable of delivering $3V \pm 0.1V$ at 10 mA from an AC input of 120 V RMS at 1kHz. The design must incorporate power supply components, including a transformer, rectifier, filter and an optional voltage regulator to ensure a stable DC output.

2.1) Since the circuit requires a $3V \pm 0.1V$ DC output at 10 mA from a 120V RMS, 1 kHz AC source, a transformer is required for voltage step-down before rectification. A full-wave bridge rectifier introduces a voltage drop of 1.4 V (0.7 V per diode), which in addition to the desired DC voltage of 3.1 V results in an expected output voltage of 4.5 V. Additionally, since transformers operate on peak voltage, the peak of the input voltage is used. From this, the calculated turn ratio for the transformer is 10000:265 (primary: secondary) with calculations shown in *Figure 1*.

$$\text{Root Mean Square formula: } VRMS = \frac{V_{peak}}{\sqrt{2}}$$

$$V_p = V_{in, peak} \quad V_s = V_{out}$$

$$V_{in, peak} = V_{in, RMS} \times \sqrt{2}$$

$$\text{Turn Ratio} = \frac{V_p}{V_s} = \frac{120 \times \sqrt{2}}{4.5} = 37.71$$

$$V_{in, peak} = 120 \times \sqrt{2}$$

$$\text{Turn Ratio} = 37.71 : 1 = 10000 : 265$$

$$V_{out} = 2V_{On} + V_{DC} = 2(0.7) + 3.1 = 4.5 V$$

Figure 1: Turn Ratio Calculations

2.2) The rectifier topology used was a full-wave bridge rectifier. A full-wave bridge rectifier consists of four diodes where two diodes conduct on each half-cycle of the AC input depending on the input voltage polarity. During positive AC input, the top of terminal of the transformer secondary winding is positive and the bottoms terminal is negative allowing diodes D1 and D4 to conduct and vice versa as shown in *Figure 2*.

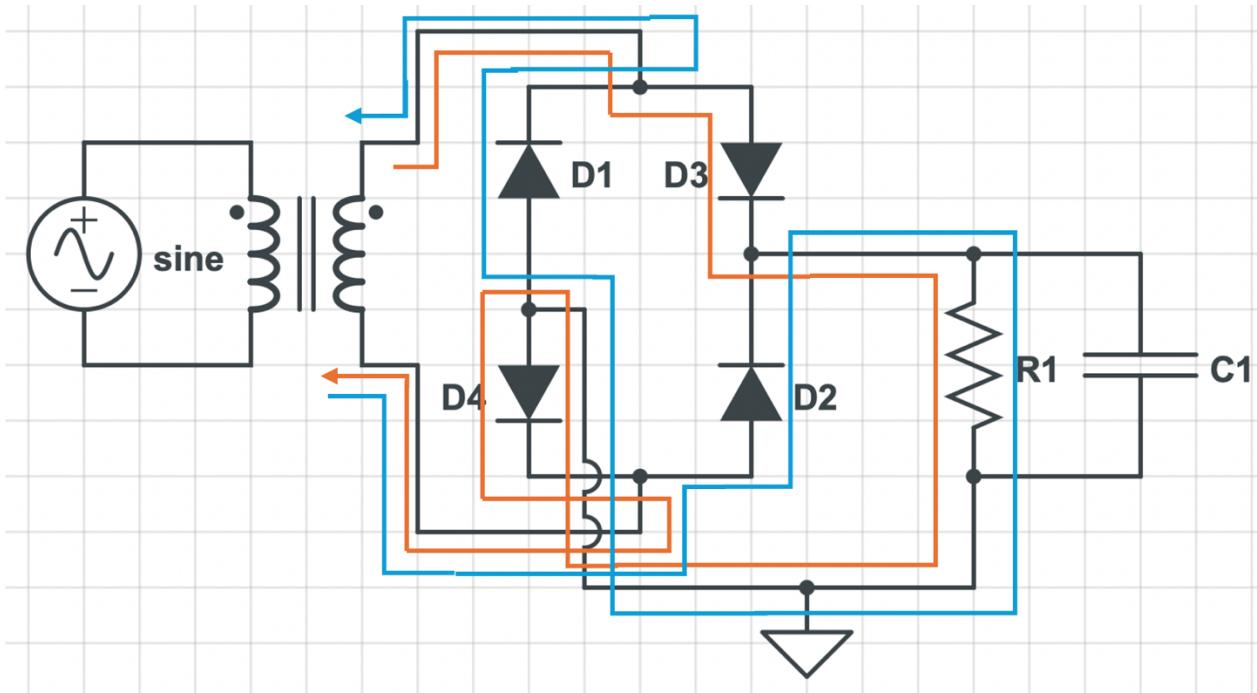


Figure 2: Current direction where blue is when the AC input is negative, and orange is when the AC input is positive

The diodes used were 1N4148 silicon diodes where they had properties of a breakdown voltage of 100 V ($V_{BR} = 100$ V) and a forward voltage of 0.7 V ($V_f = 0.7$ V). These properties were useful in the calculations in addition to the diodes' maximum forward current of 300 mA which is above the projects 10mA requirement.

2.3) From the provided values, V_{ripple} is given as ± 0.1 V, I_{in} as 10 mA, and f_{in} as 1 kHz. Using the ripple voltage equation for a capacitor-filtered rectifier and formulas for period and frequency, a value of 25 μ F for the capacitor is calculated as shown in *Figure 3*. A polarized capacitor is used as it allows for higher capacitance values (which is required for this circuit) for filtering rectified DC voltage.

$$\text{Ripple voltage equation: } V_{ripple} = \frac{I_{in}(T_{out})}{C}$$

$$\text{Frequency - period equation: } T_{out} = \frac{1}{2f_{in}}$$

$$\text{Given: } V_{ripple} = \pm 0.1 \text{ (0.2)V}, I_{in} = 10 \text{ mA}, f_{in} = 10 \text{ kHz}$$

$$C = \frac{I_{in}\left(\frac{1}{2f_{in}}\right)}{V_{ripple}} = \frac{(10 \times 10^{-3})\left(\frac{1}{2(1 \times 10^3)}\right)}{0.2} = 2.5 \times 10^{-5} \text{ C} = 25 \mu\text{F}$$

Figure 3: Calculations to obtain capacitor value

2.4) For the corresponding circuit a regulator was not used. However, if a voltage regulator were used, a Zener diode would be connected in parallel to the load resistor and capacitor. When the voltage across the Zener diode surpasses the breakdown voltage (V_B), the diode conducts in the reverse direction. In breakdown, the Zener diode sets the voltage across the load so that the load voltage remains under the V_B value, ensuring that the load voltage has minimal deviations even with input fluctuations.

2.5)

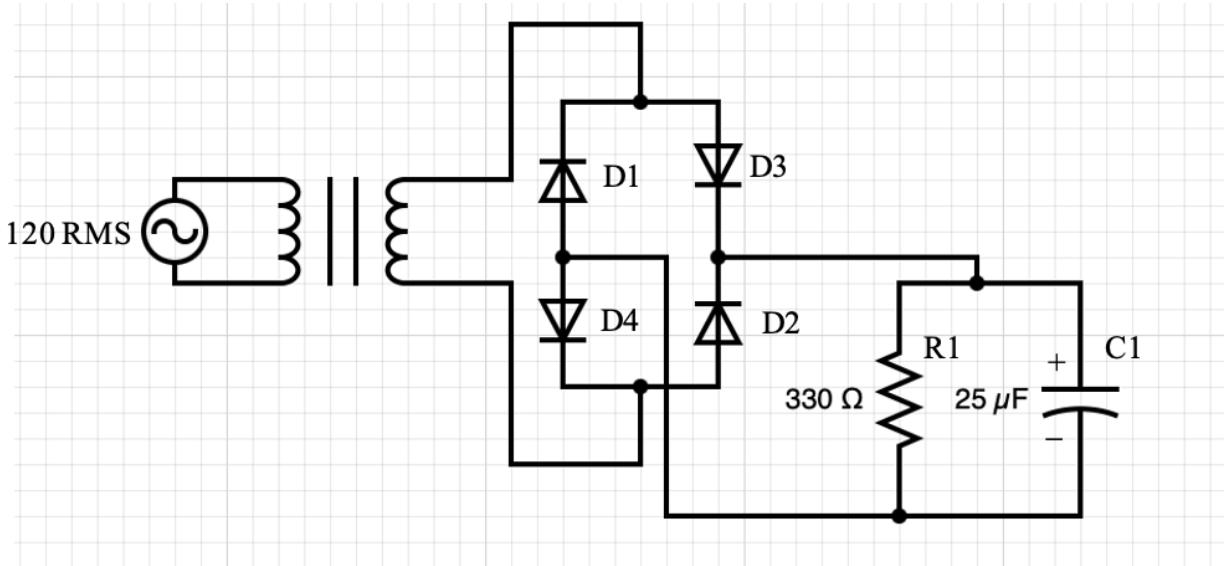


Figure 4: Complete circuit schematic

2.6)

Calculations for Transformer Turn Ratio:

$$\text{Transformer equation: } \frac{V_{in}}{V_{out}} = \frac{N_p}{N_s} \rightarrow V_{out} = \frac{N_s}{N_p} (V_{in})$$

$$V_{in, peak} = 120\sqrt{2} \text{ from the root mean square equation} \rightarrow V_{out} = \frac{N_s}{N_p} (120\sqrt{2})$$

When AC input is positive: KVL through D3, D4, and R1: $0.7 + Vl + 0.7 = Vout$

$$4.5 = \frac{Ns}{Np} (120\sqrt{2})$$

$$\frac{Ns}{Np} = \frac{4.5}{120\sqrt{2}} \approx 0.0265 = \frac{265}{10000}$$

Calculations for Capacitor as Filter in Figure 3

Calculations for Load Resistor:

$$V = IR$$

$$3V = 10mA(R)$$

$$R = \frac{3V}{10mA} = 300\Omega$$

Figure 5: Calculations for load resistor value

The theoretical calculated resistor value is 300Ω , however a 330Ω resistor was used instead as shown in the physical circuit due to component quantity limitations.

2.7) Looking at the previous theoretical calculations, the AD2 is expected to supply a sinusoidal input voltage with amplitude 4.5V and frequency of 1 kHz. For each half-wave of the input voltage two diodes will be ON, resulting in a 1.4V drop. In addition to the desired 3.1 V across the load resistor, this results in the final of 4.5V supplied by the AD2. The purpose of the capacitor is to limit the load (output) voltage within the desired range of a 0.2V peak-to-peak. The theoretical value for the capacitor is 25 uF, which means that for any capacitor that is at least 25 uF the load voltage is expected to fall within the desired range of 0.2V (2.9V to 3.1V).

2.8)

Design Trade-offs

Rectifier

A full-wave bridge rectifier was used over a center-tapped full-wave rectifier and half-wave rectifier as it provides higher efficiency, better voltage utilization, and simpler transformer conditions. A diagram of the full-wave bridge rectifier is shown in Figure 2.

A half-wave rectifier only utilizes half of the AC cycle as it only includes one diode, and this diode only conducts during the positive AC input. This would result in a lower average DC voltage as half of the input voltage is unused. In contrast, a full-wave rectifier uses both halves of the AC cycle, doubling the output frequency and in turn results in improved efficiency.

A center-tapped full-wave rectifier would require the secondary winding to be center tapped and provide twice the voltage, making the transformer more complex, bulky, and expensive.

Capacitor

A polarized capacitor was chosen over a non-polarized capacitor due to the capacitance values they offer and their typical use. Polarized capacitors offer much higher capacitance values in comparison to non-polarized capacitors, making polarized capacitors the better components to use.

Additionally, polarized capacitors are typically used for DC applications whereas non-polarized capacitors are typically used in AC applications.

Design Margins

Design margins are essential in ensuring circuits perform reliably in real-world conditions. Components must be selected with tolerances in mind to avoid failure from unexpected behaviour.

Diode

The 1N4148 diodes used in the full-wave bridge rectifier have a maximum forward current of 300 mA and a breakdown voltage of 100V, which are well over the values of 10 mA and rectified voltage of 4.5V, respectively. Additional design margins for the 1N4148 diodes can be found within the datasheet where maximum and minimum tolerances are provided to prevent failure. Another design margin is the diode operation temperature which should be considered for this circuit and especially high-power circuits to ensure that diodes can operate without fail.

Capacitor

Ideally, a 25 uF polarized capacitor would be used to ensure that the output voltage fell into the desired range. However, due to component limitations, three 10 uF polarized capacitors in parallel had to be used instead, resulting in a capacitor of 30 uF.

Components Ratings and Safety

To ensure safe and reliable circuit operation, all components were selected with appropriate voltage, current, and power ratings to avoid exceeding their maximum limits. Relevant values for diodes are provided in the above section labeled Design Margins. The calculations for the power dissipated in the 330 Ω resistor is presented in *Figure 6*. To ensure that the resistor behaves as expected, a resistor with a power rating greater than the calculated power dissipated value was used to ensure safety.

$$P = \frac{V^2}{R} = \frac{3^2}{330} = 27.3 \text{ mW}$$

Figure 6: Power dissipated in resistor

3) The physical circuit is shown in *Figure 7*. The full-bridge rectifier is shown with four 1N4148 diodes and the rest of the circuit consists of a $330\ \Omega$ load resistor was used, and three 10 uF polarized capacitors were placed in parallel to the load, resulting in a total capacitance of 30 uF, 5 uF over the calculated value.

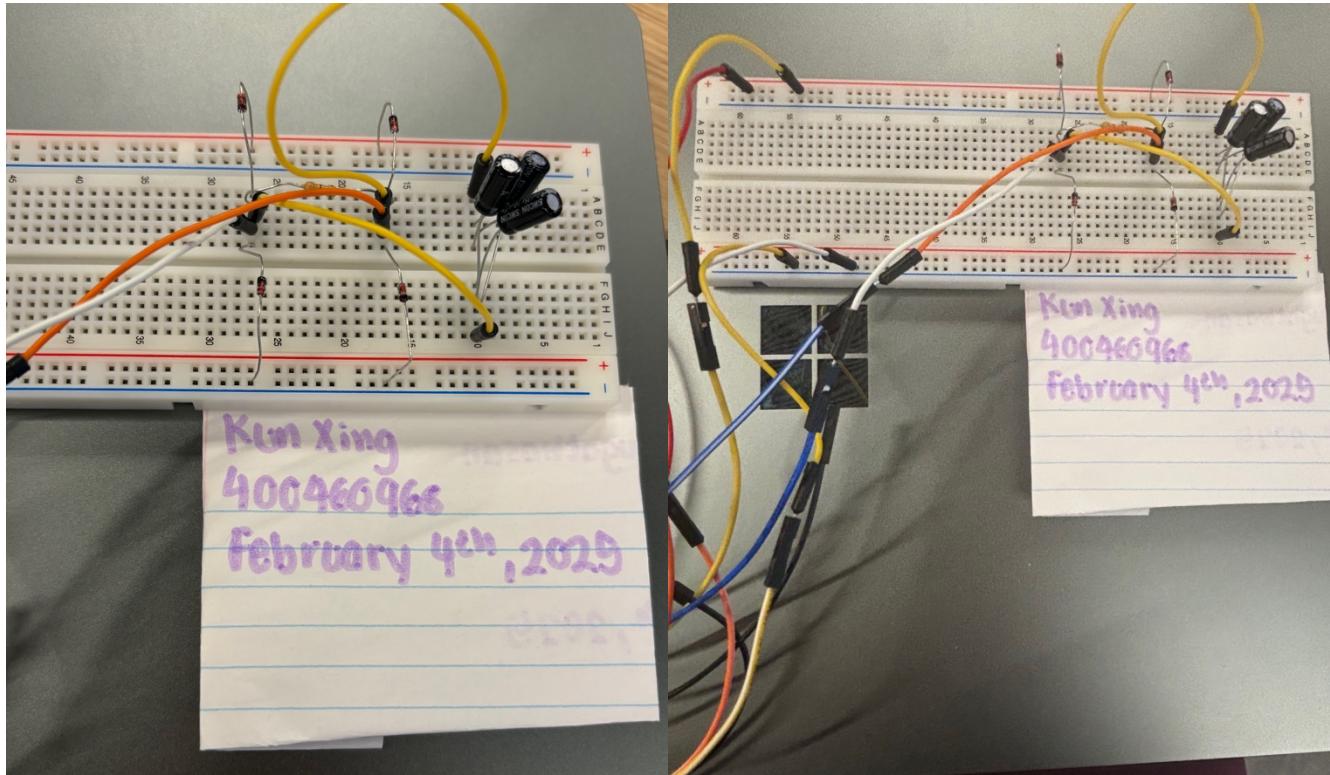


Figure 7: Images of physical circuit

The measurement procedure is listed as follows:

- 1) Created physical circuit and provided input AC signal.
- 2) Measured voltage values at the input and voltage drop across the load resistor.

Figure 8 shows the output from the transformer. The top graph displays the positive AC signal with a frequency of 1 kHz and a 4V amplitude from the secondary winding of the transformer, while the bottom graph shows the negative AC signal with a 1 kHz frequency and a 1V amplitude form the opposite side of the secondary winding. These two AC signals are the outputs from the transformer before they are processed through the full-wave rectifier, converting them into pulsating DC. Since the transformer outputs two signals with different amplitudes and polarity, the resulting signal is a $4 + 1 = 5$ V amplitude AC signal with 1 kHz frequency.

Figure 9 depicts the output voltage across the load resistor and the current through the load resistor. Channel 1 (orange) represents voltage across the secondary winding, Channel 2 (blue) represents the voltage across the load, and Math 1 (red) represents the current through the load. From the given load voltage, the corresponding voltage range is $2.9 \leq V_L \leq 3.1$. The same figure displays the DC output (blue) for an AC input of 5V (light orange). To simplify circuit setup, a $330\ \Omega$ resistor was used in place of $300\ \Omega$. Additionally, three capacitors were placed in parallel to achieve 30 uF, which is above the theoretical value but makes little impact on the output. The output through the load resistor is within the 2.9 – 3.07V range, falling into the 2.9 – 3.1V tolerance. A detail to highlight in *Figure 9* is the clipping of the AC

source measured by Channel 1. During the positive cycle of the AC signal, the capacitor charges to input signal. During the negative cycle of the AC signal, the capacitor discharges to supply the load. Clipping occurs when the capacitor is unable to charge fully or discharge enough to maintain the desired voltage, likely causing the clipping seen in *Figure 9*. This is referred to as “capacitor saturation”.

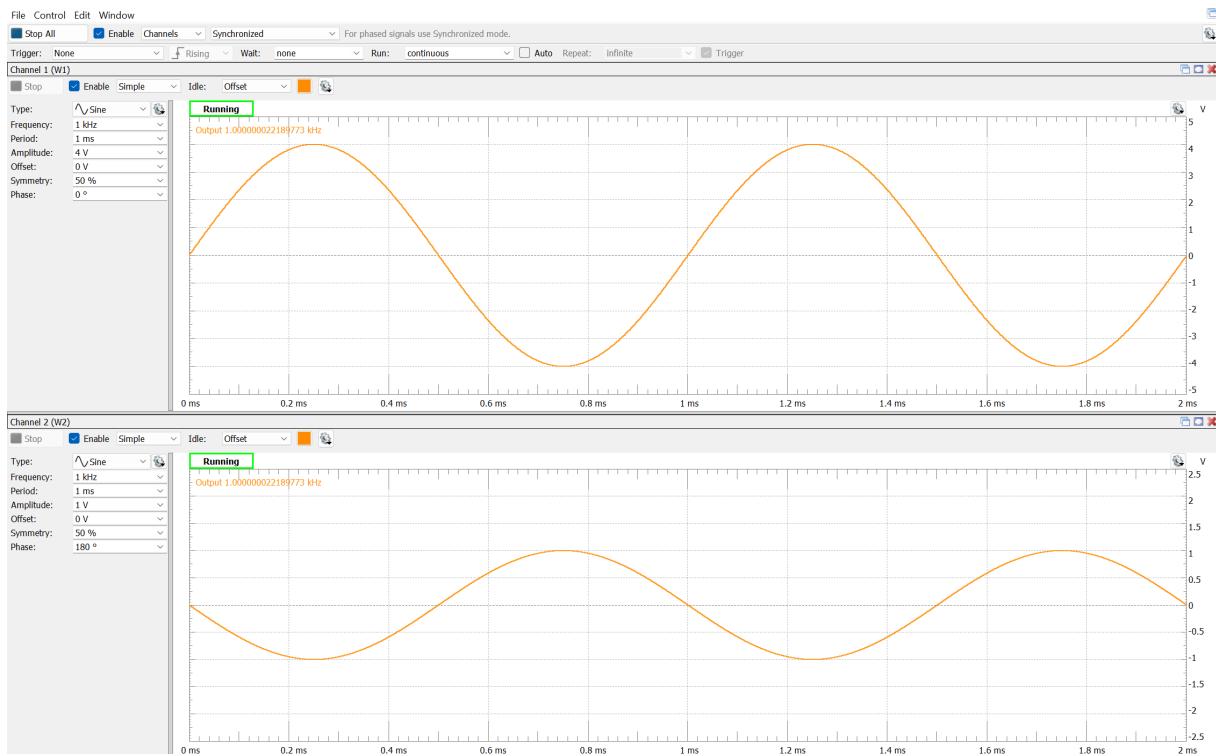


Figure 8: Graph of input AC signal produced by AD2 through the Wavegen application

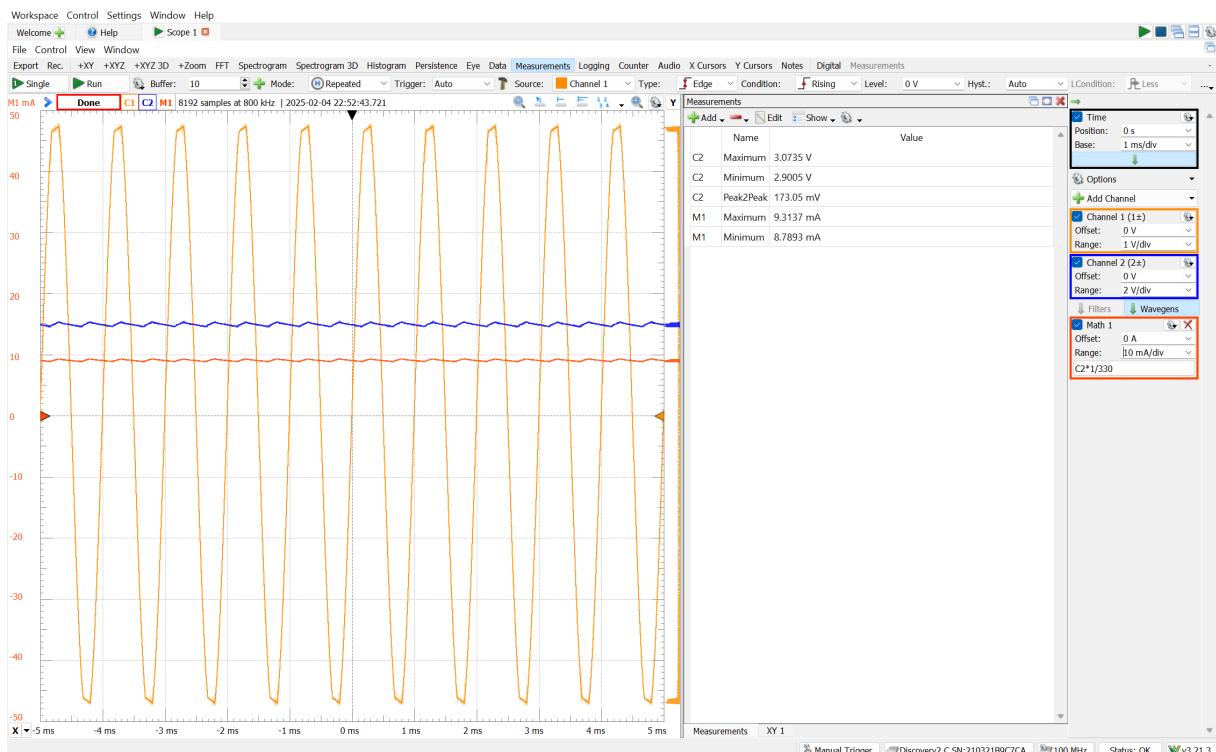
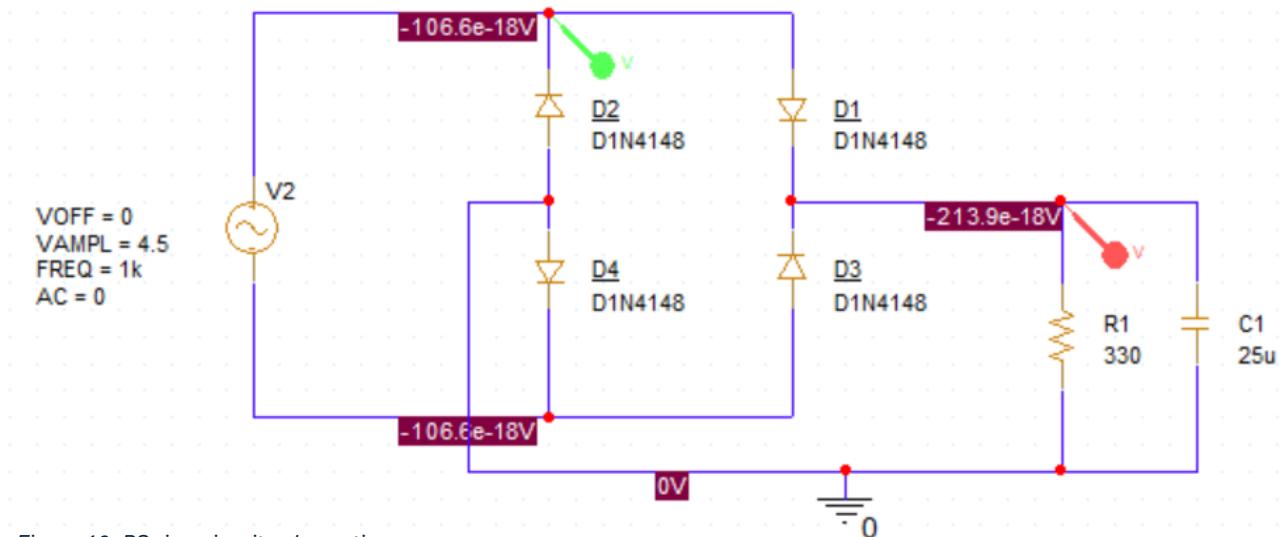


Figure 9: Graph of resulting output voltage (blue) and current (red) measured through the AD2 and Wavegen application

4)



```
31
32 **** INCLUDING SCHEMATIC1.net ****
33 * source PROJECT_1_PSPICE
34 D_D3    N00310 N00330 D1N4148_1
35 D_D2    0 N00298 D1N4148_1
36 D_D1    N00298 N00330 D1N4148_1
37 D_D4    0 N00310 D1N4148_1
38 R_R1    0 N00330 330 TC=0,0
39 C_C1    0 N00330 25u TC=0,0
40 V_V2    N00298 N00310 AC 0
41 +SIN 0 4.5 1k 0 0 0
42
```

Figure 11: PSpice circuit netlist

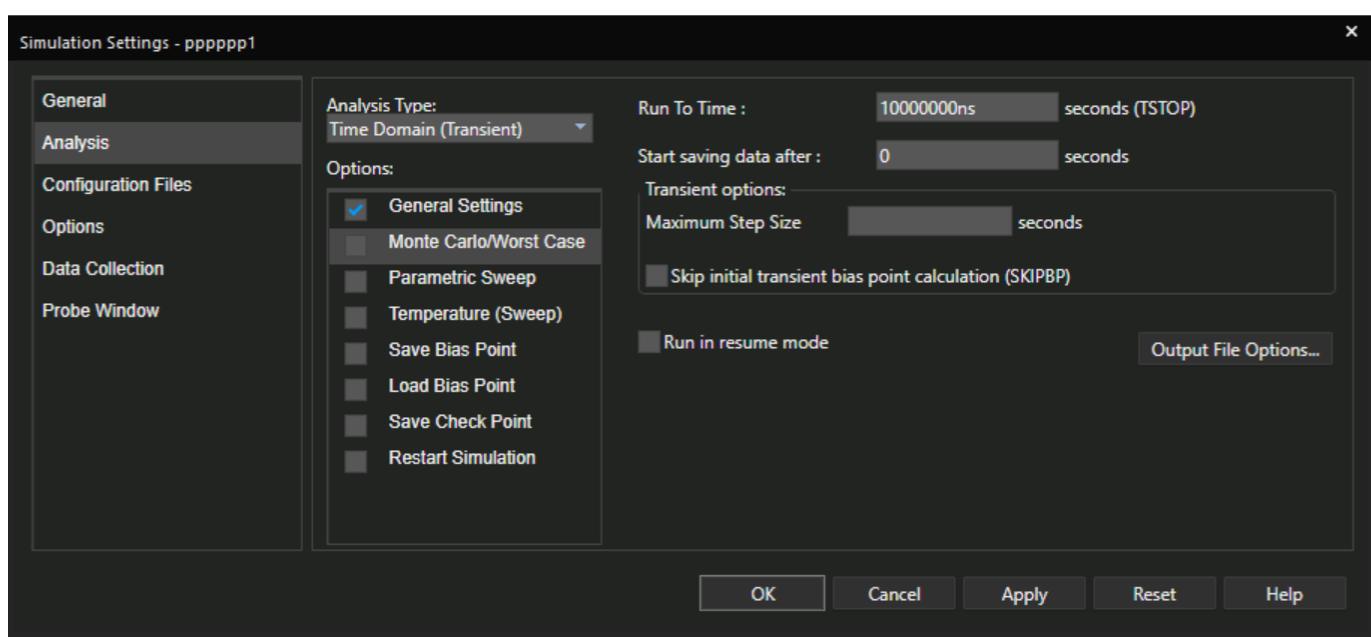


Figure 12: PSpice circuit simulation settings

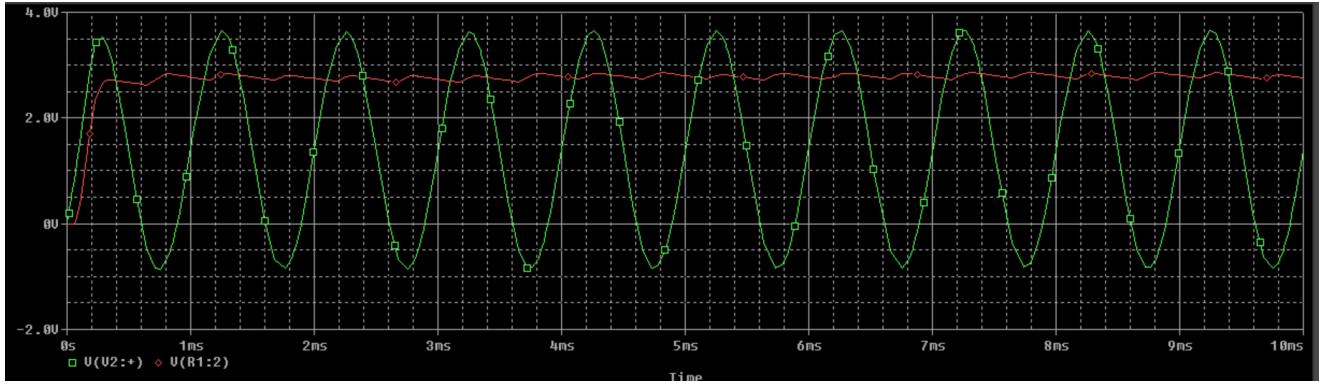


Figure 13: PSpice simulation graph

5) Comparing the AD2 with the theoretical calculations for voltage, while the AD2 provided a sufficient range of $2.9 \leq V_L \leq 3.07$, which was slightly lower than the calculated output of $2.9 \leq V_L \leq 3.1$, resulting in a percent error of 0.97%. Theoretical calculations predicted the V_L value with a resistor value of 300Ω , a capacitor value of $25 \mu F$, and an input of $4.5V$ AC. Discrepancies between the theoretical and AD2 may have been caused by using a value of 330Ω for the resistor and a value of $30 \mu F$ for the capacitor which would filter better due to component availability. Additionally, this could have been caused by error in the AD2 into the circuit where hardware tolerances may affect the supplied signal, internal resistance produced by using additional wiring, and theoretical calculations assuming an exact 0.7 V drop across diodes where real-world value may slightly fluctuate. As deviations in component values and real-world voltage drops were uncontrollable variables, the troubleshooting done in the physical circuit was using a minimal number of wires to prevent slight internal resistances while simplifying the appearance of the circuit. Maintaining the desired DC voltage was also an issue as using the expected $4.5V$ input did not output the desired DC voltage. To troubleshoot, changing the input to $5 V$ instead of $4.5V$ caused the load resistor voltage to remain within the theoretical range.

With the design using a full-wave rectifier using four diodes increases the complexity and cost of the circuit in comparison to using the half-wave rectifier. A setback in this design was using a resistor value of 330Ω instead of the theoretical 300Ω value to generate a 10 mA current. The outcome is demonstrated in *Figure 9* where the current reached of value of around 9.3137 mA instead of the desired 10 mA . The AD2 missing an ammeter may also be limitations to measurement errors.