
ELECENG 2EI4: Electronic Devices and Circuits

I

Project 4

Kun Xing, xingk8, 400460968

Instructor: Dr. Haddara

Date of Submission: April 7, 2025

As a future member of the engineering profession, the student is responsible for performing the required work in an honest manner, without plagiarism and cheating. Submitting this work with my name and student number is a statement and understanding that this work is my own and adheres to the Academic Integrity Policy of McMaster University and the Code of Conduct of the Professional Engineers of Ontario.

Part 1:

- a) The circuit's truth table for a logic XOR gate is shown in Figure 1. As illustrated, when inputs A and B are the same, the output is a logic low; when the inputs differ, the output is a logic high. Figure 2 presents the Boolean expression for the XOR gate based on this truth table. By applying different Boolean algebra simplification techniques, a final expression more suitable for CMOS implementation is derived and shown at the end of Figure 2.

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

Figure 1: Truth table for XOR gate

$$\begin{aligned}
 & A\bar{B} + \bar{A}B \\
 = & \overline{(A\bar{B} + \bar{A}B)} \quad \text{<< DeMorgan's Law } \overline{A + B} = \bar{A}\bar{B} \text{ >>} \\
 = & \overline{\overline{(A\bar{B})}(\overline{\bar{A}B})} \quad \text{<< DeMorgan's Law } \overline{AB} = \bar{A} + \bar{B} \text{ >>} \\
 = & \overline{(\bar{A} + B)(A + \bar{B})} \quad \text{<< Distributive Law } A(B+C) = AB + AC, \text{ Inverse Law } A\bar{A} = 0 \text{ >>} \\
 = & \overline{AB} + \bar{A}\bar{B}
 \end{aligned}$$

Figure 2: Boolean expression for XOR gate and Boolean expression used for CMOS circuit

The derived Boolean expression shown in Figure 2 can be implemented in the PDN (pull-down network) shown in Figure 3 using NMOS transistors where NMOS transistors. In this network, NMOS transistors in series represent AND operations while transistors in parallel represent OR operations. The complimentary signals \bar{A} and \bar{B} are generated using CMOS inverters consisting of a PMOS and NMOS transistors, as shown in Figure 4 for \bar{A} . By constructing the dual of the PDN in the PUN (pull-up network) using PMOS transistors shown in Figure 3, the corresponding XOR gate CMOS circuit will be completed. Additionally, since CMOS is negative logic, the overbar in the Boolean expression is accounted for through the structure of the PUN and PDN.

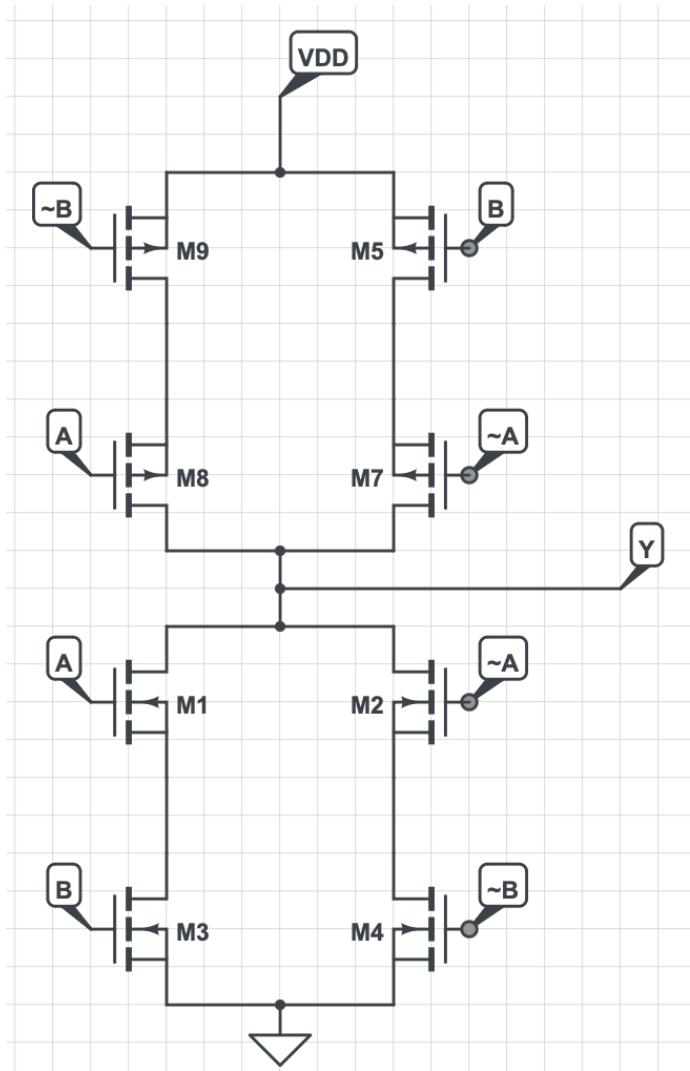


Figure 3: PDN and PUN for XOR gate

The final CMOS circuit, shown in Figure 5, is implemented using a total of 12 transistors, distributed across two CD4007CN ICs, with each containing 6 transistors. As detailed in Figure 3, the PDN utilizes 4 NMOS transistors and the PUN utilizes 4 PMOS transistors. To generate complementary inputs \bar{A} and \bar{B} , two CMOS inverters are required, each consisting of 1 NMOS and 1 PMOS transistors. Therefore, as shown in Figure 4, generating both complements uses 2 NMOS and 2 PMOS transistors. Altogether, the complete CMOS XOR implementation uses 6 NMOS and 6 PMOS transistors, totaling 12 transistors, which exactly fits in two CD4007CN IC packages.

Figure 5 illustrates the final circuit schematic of the CMOS XOR gate.

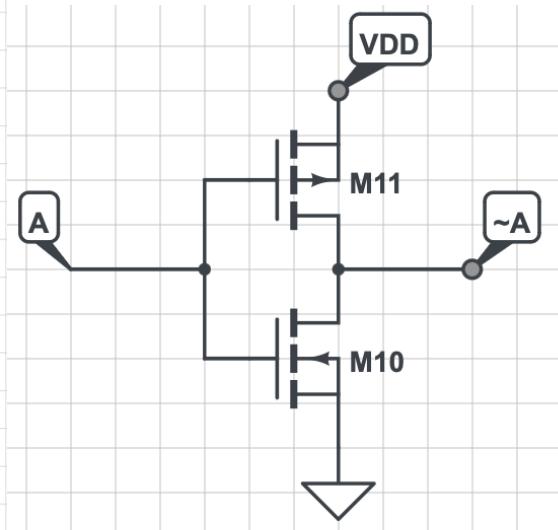


Figure 4: CMOS inverter gate

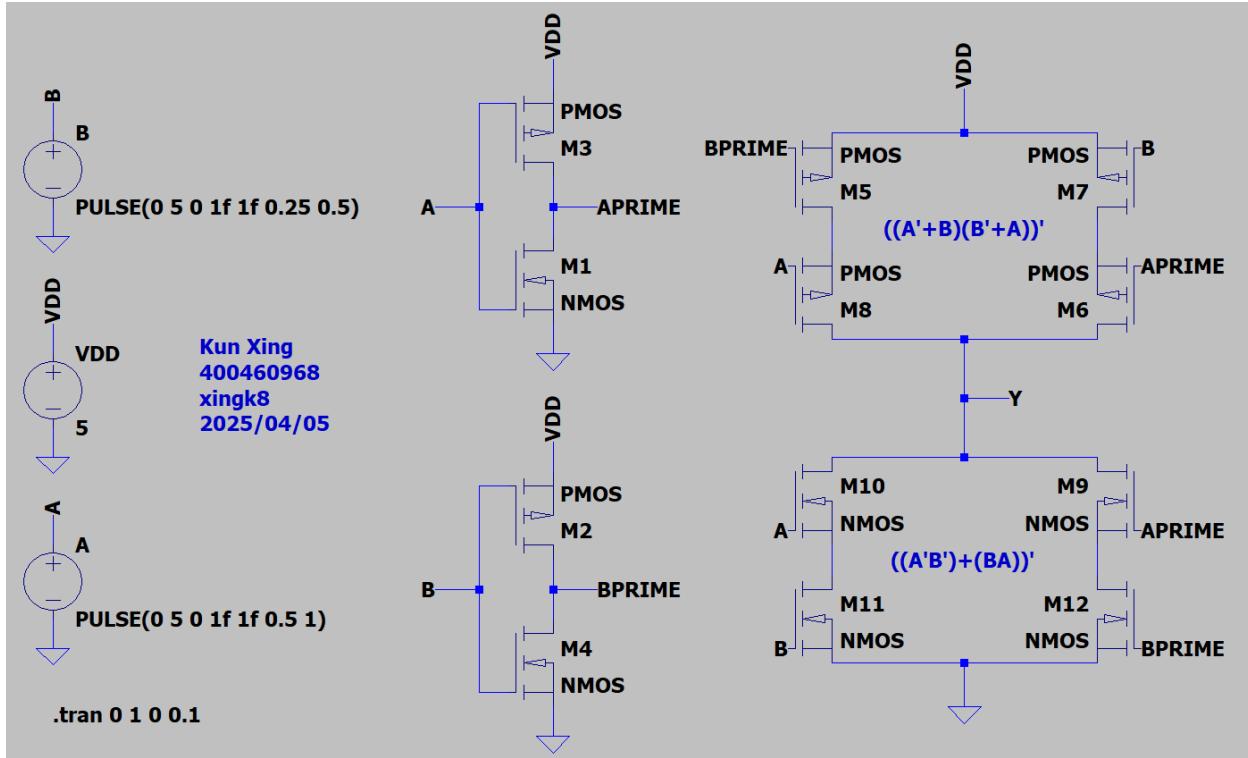


Figure 5: CMOS XOR gate implementation using LTSpice

- b) When designing the CMOS circuit, careful consideration is given to the sizing of PMOS and NMOS transistors to ensure balanced switching behaviour. Due to the lower mobility of holes in PMOS devices compared to electrons in NMOS, PMOS transistors inherently conduct more slowly. To compensate for this difference and match the drive strength of the NMOS transistors, PMOS devices are typically sized larger. In this design, it is assumed that the average sizing is $(W/L)_P = 5:1$ for PMOS and $(W/P)_N = 2:1$ for NMOS, reflecting an effective mobility compensation ratio of approximately 2.5. Analyzing the critical paths in the circuit, the longest path in both the pull-up and pull-down networks consists of two series-connected transistors. This results in equivalent resistance of $2RP$ and $2RN$, respectively. To ensure symmetrical rise and fall times, these resistances must be matched, and because resistance inversely proportional to the width-to-length ratio, the sizing ratio $\frac{2(W/L)_P}{2(W/L)_N} = \frac{5}{2} = 2.5$ (5: 2) is ideal. This balanced sizing improves the overall performance of the CMOS circuit by providing consistent transition delays and maintaining signal integrity.
- c) Given the above discussion, it is important to note that ideal transistor sizing cannot directly be implemented in our hardware design because the values of width (W) and length (L) of the transistors are fixed physical parameters predefined during IC fabrication. These characteristics are set by the manufacturer and cannot be modified by the user of the device. As a result, the circuit may not achieve theoretical propagation delay, due to the built-in sizing of the transistors constraints. However, because all

transistors within the IC are fabricated with consistent manufacturing processes, it is reasonable to assume that the same PMOS-to-NMOS sizing ratio applies across all devices. This allows us to consider that the ideal ratio is effectively achieved uniformly throughout the circuit, even if not numerically perfect. Although we cannot determine the exact time delay deviation without knowing internal sizing details, it is expected that the gate will perform slightly slower than the ideal case. However, if the MOSFETs on the chip are well matched, the gate is likely to behave symmetrically, with balanced rise and fall times. This demonstrate the importance of consistent transistor matching in CMOS logic design and reinforces how real-world constraints must be considered alongside ideal theoretical models.

Part 2:

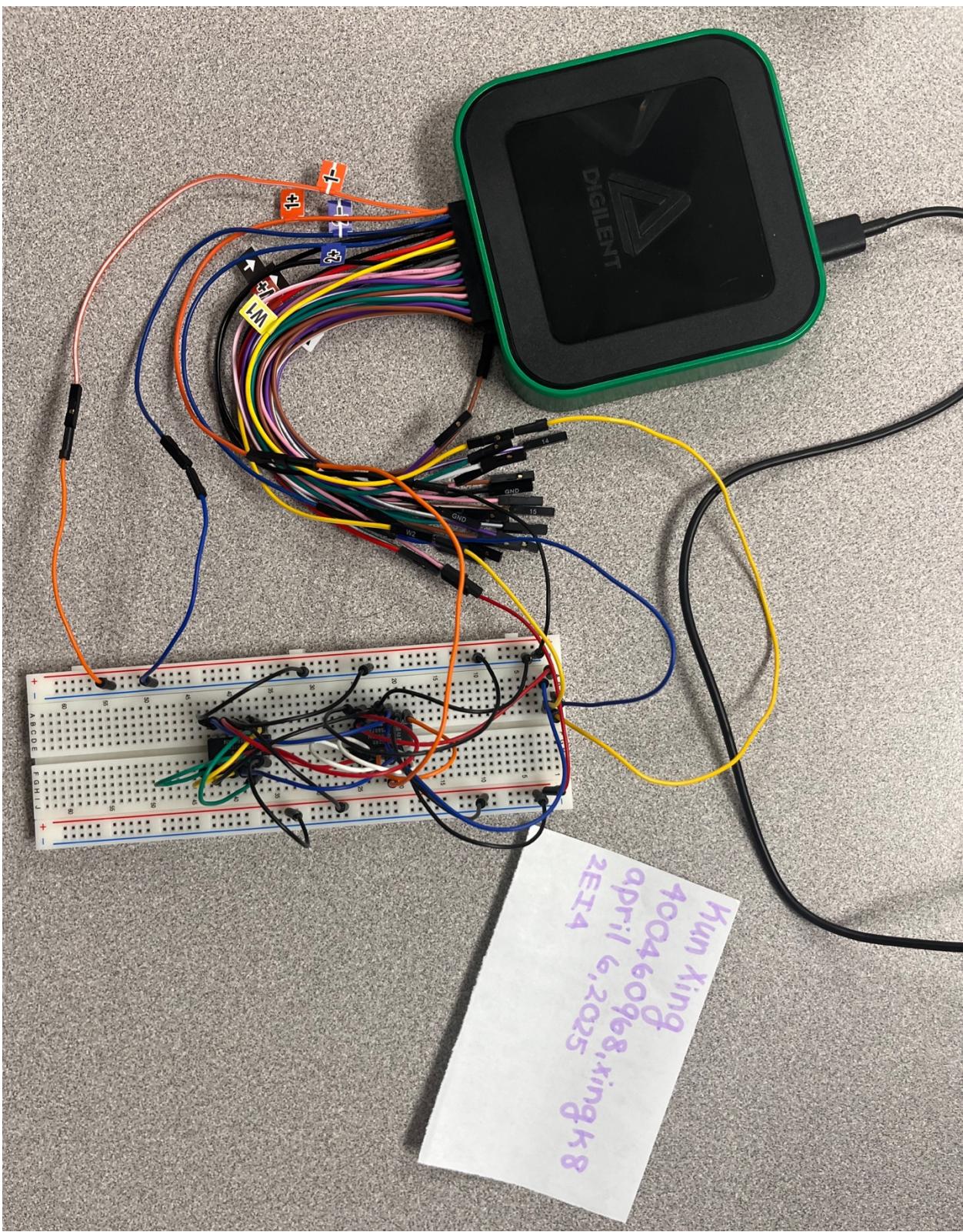


Figure 6: Physical circuit

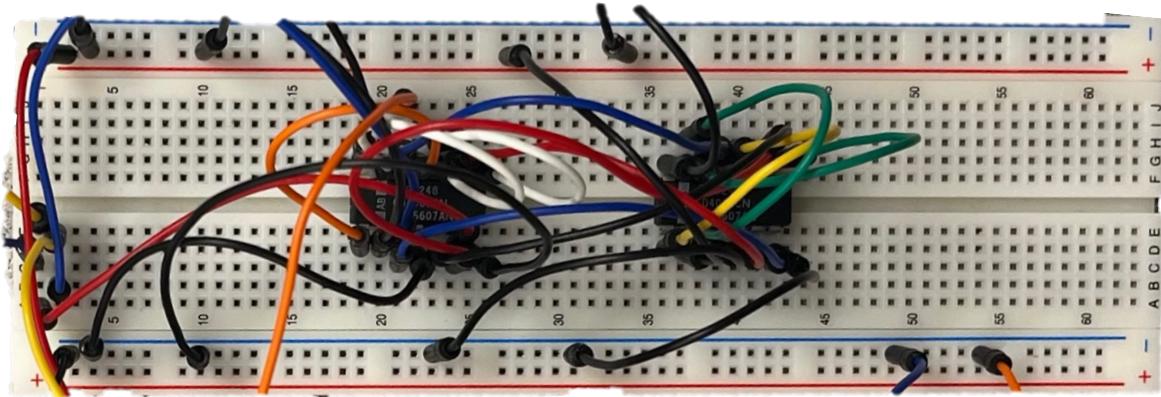


Figure 7: Physical circuit connections

- a) Figure 8 displays the functional testing of the XOR logic circuit. In this setup, DIO 1 (green) and DIO 2 (purple) measured the inputs A and B, respectively, while DIO 0 (pink) measured the output Y, where $Y = A \oplus B$. The first input (DIO 1 and input A) is a square wave with amplitude of 2.5V, an offset of 2.5V and a frequency of 500 Hz. The second input (DIO 2 and input B) share the same amplitude and offset but operates at a higher frequency of 1 kHz. This frequency difference creates varying logic conditions at the inputs, allowing the correct XOR behaviour to be observed in the output waveform on DIO 0.

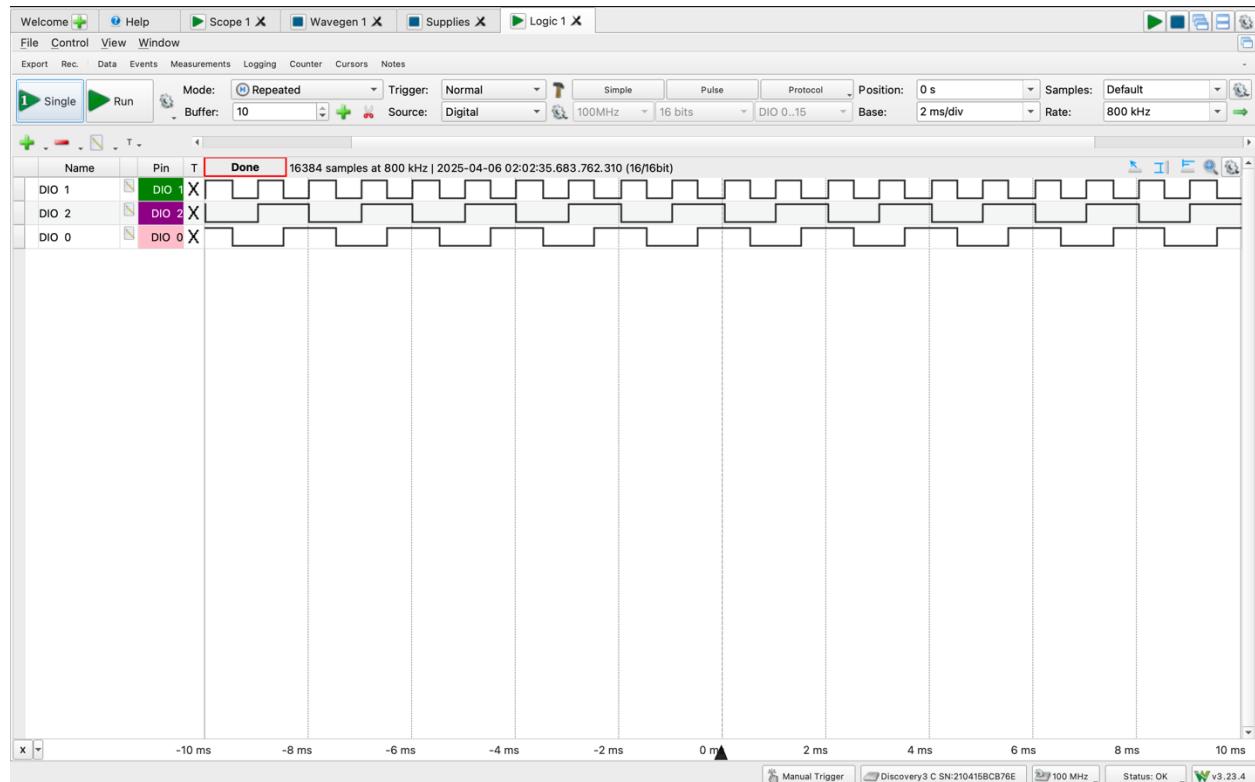


Figure 8: Logic simulation on AD3 (DIO 1 = input A, DIO 2 = inputs B, DIO 0 = output Y)

Looking at Figure 8, the output on DIO 0 exhibits the behaviour according to the XOR truth table shown in Figure 1. The logic waveform confirms that the output is logic high (5V) only when the inputs on DIO 1 and DIO 2 differ, for instance, when DIO 1 is high (5V) and DIO 2 is low (0V), or vice versa. Conversely, the output remains low (0V) when both inputs are either high (5V) or low (0V). This observed output pattern confirms correct XOR functionality, demonstrating that the circuit responds accurately to all combinations of A and B inputs.

- b) In the first test where input A was held at a logic high (5 V) while input B was set as a square wave toggling between 0 V and 5 V. As shown in Figure 9, the measured high output voltage was $V_H = 5.0208$ V, and the low output voltage was $V_L = -2.74548$ mV. In the second test, the inputs were swapped – input B was held at 5 V while input A toggled between 0 V and 5 V. The corresponding measurements were $V_H = 5.0213$ V and $V_L = -7.14982$ mV as seen in Figure 10. Upon inspection, both measurements produced nearly identical results, with a very small percentage of 0.00996% between V_H values, confirming consistent circuit behaviour. The low output values (V_L) exhibited a larger percentage error of 89.02%, but this discrepancy is not significant. Since the values being compared are in the mV range, a small absolute difference can lead to high percentage error. However, these deviations are minor in the context of 5 V logic levels and likely result from noise, measurement resolution, or minor wire connection issues. Overall, the results the expected XOR functionality with symmetrical behaviour when inputs are swapped.

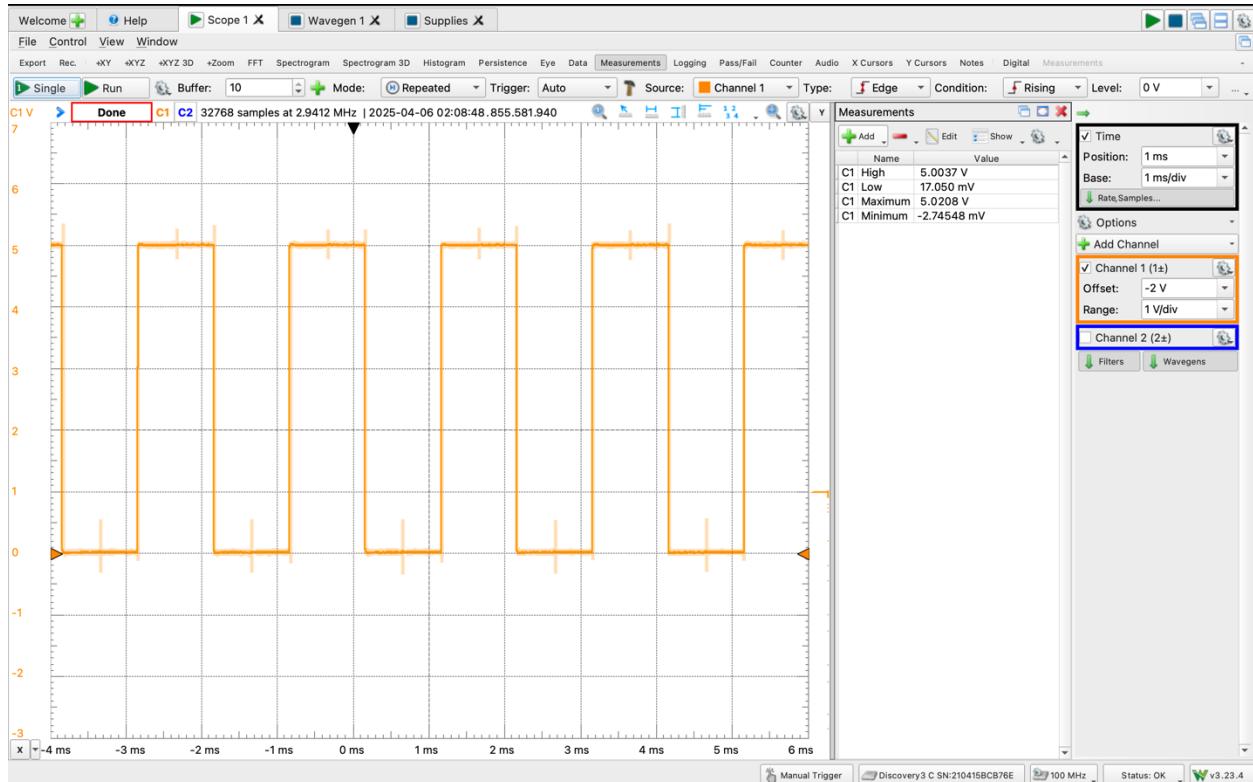


Figure 9: Static level testing (input A constant 5V, input B square wave toggling between 0V and 5V)

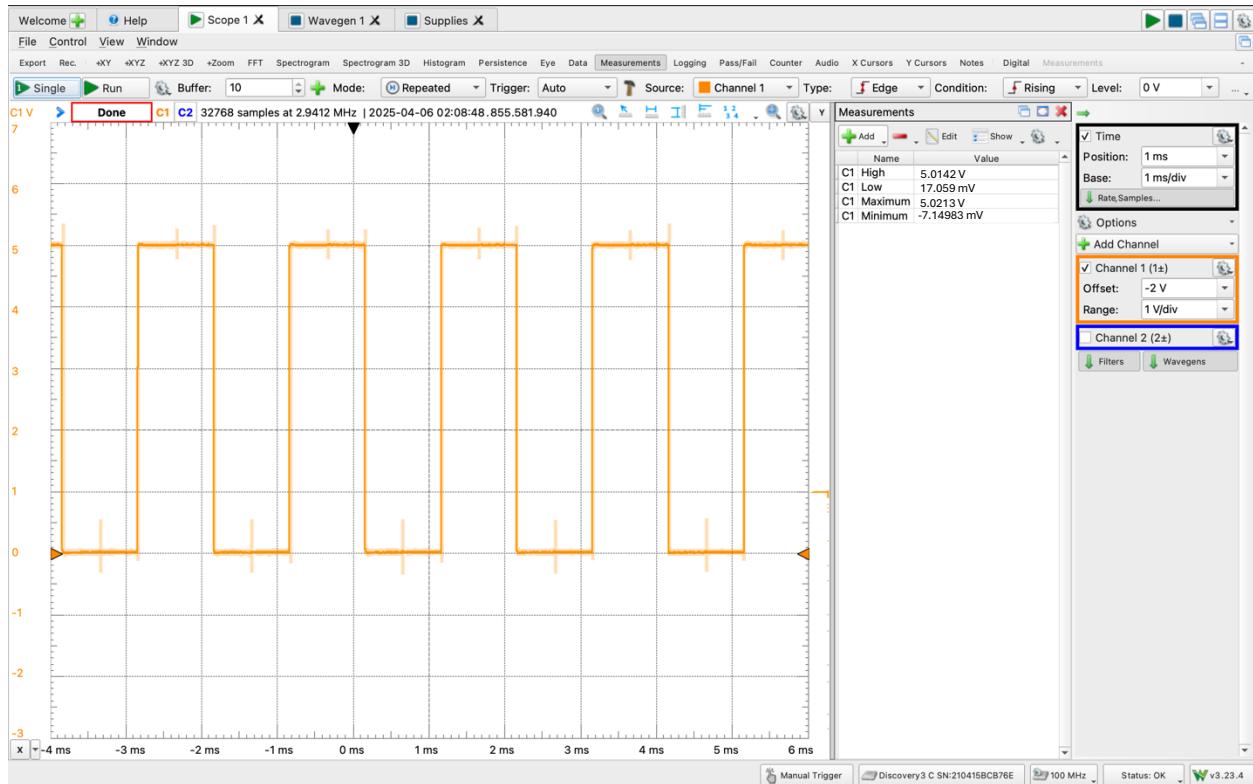


Figure 10: Static level testing (input A square wave toggling between 0V and 5V, input B constant 5V)

Part 3:

- a) To evaluate the timing characteristics of the CMOS XOR gate, one input was held at a constant logic high level (5 V), while the other input was driven by a square wave toggling between 0 V and 5 V with a frequency of 500 Hz. A 100 nF (labeled as 104) capacitor was connected at the output to simulate a capacitive load, exaggerating the transition delays for illustration. From the resulting waveform shown in Figure 11, the rise time (t_{rise}) was determined to be 323.29 μ s and the fall time (t_{fall}) to be 284.92 μ s.

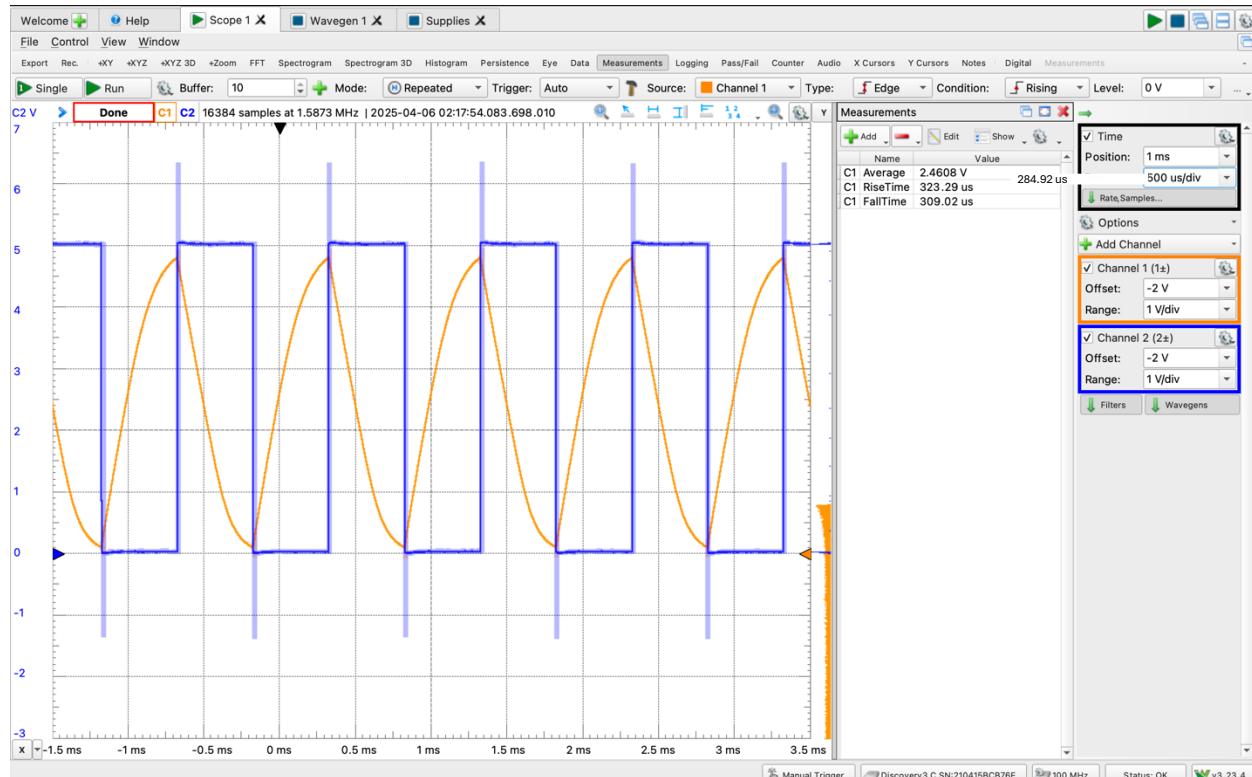


Figure 11: AD3 waveform for timing analysis

- b) To determine τ_{PLH} , τ_{PHL} , and τ_P , τ_{ref} was calculated first:

$$\tau_{ref} = 4.39(100n) = 4.39 \times 10^{-7} s$$

Using the τ_{ref} value, τ_{PLH} and τ_{PHL} values were calculated:

$$\tau_{PLH} = R_N \times C_L = \frac{2}{5} \times \tau_{ref} = 0.1756 \mu s$$

$$\tau_{PHL} = R_P \times C_L = \tau_{ref} = 0.439 \mu s$$

From the calculated τ_{PLH} and τ_{PHL} values, calculate τ_P :

$$\tau_P = \frac{\tau_{PLH} + \tau_{PHL}}{2} = \frac{0.1756\mu + 0.439\mu}{2} = 0.3073 \mu s$$

Part 5 (Bonus):

- a) Like Part 2 (a), the functional behaviour of the XOR gate was further verified for the bonus circuit using the AD3 tool, as illustrated in Figure 14. In this test, DIO 1 and DIO 2 were configured to serve as digital inputs A and B, respectively, while DIO 0 was used to observe the resulting output signal Y, where $Y = A \oplus B$. The waveform captured on DIO 0 consistently followed the expected behaviour dictated by the XOR truth table – outputting a logic high only when inputs differ, and a logic low when they are the same. This confirms that responds correctly to all four combinations of binary input, validating the logic gate's implementation. Additionally, the logic levels match that in Figure 8 (Part 2 (a)).

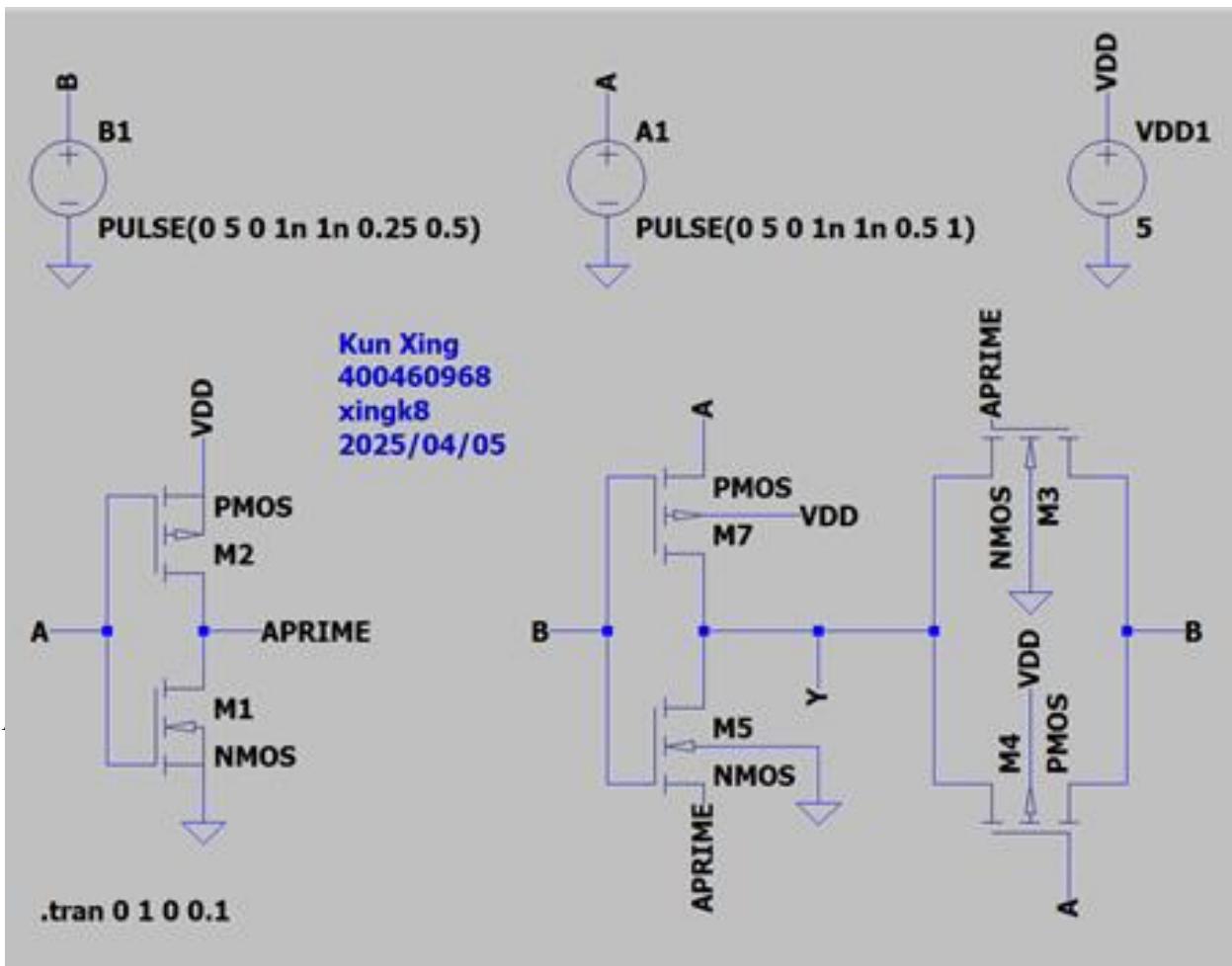


Figure 12: Bonus circuit schematic

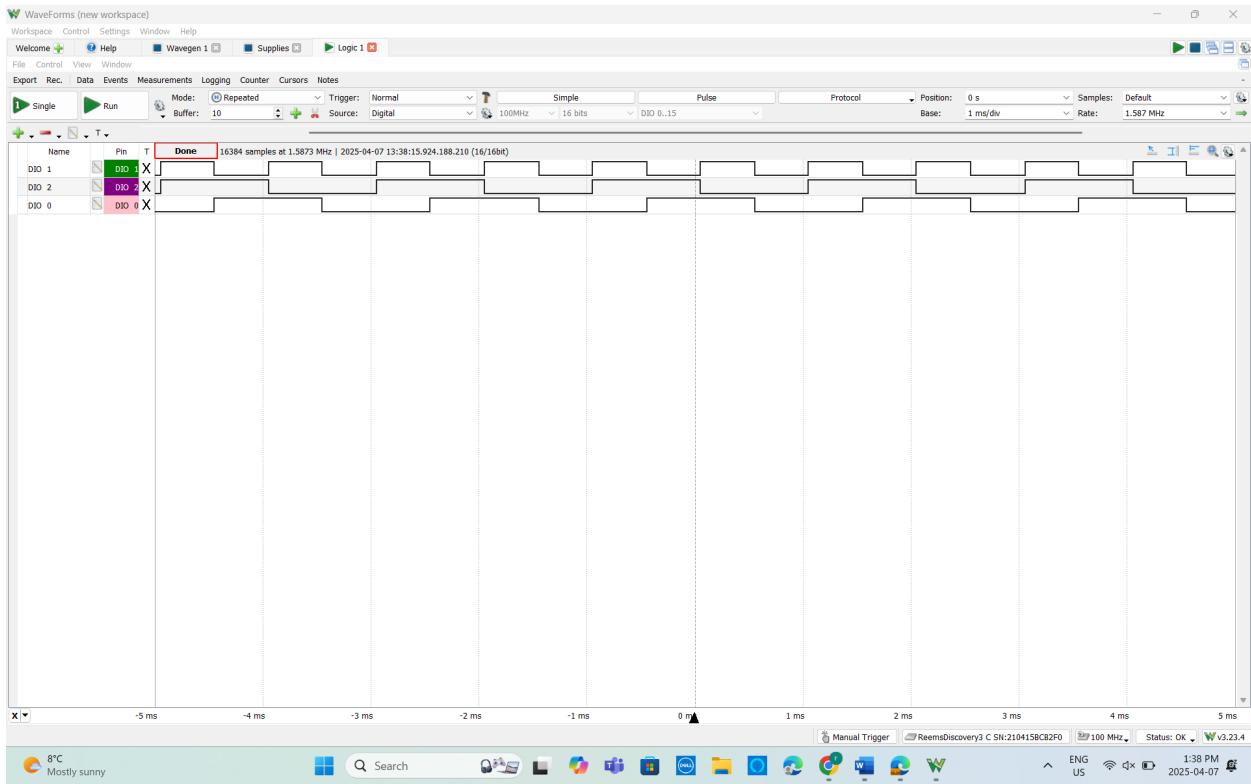


Figure 13: Bonus functional testing

b)

	Conventional Design	Bonus Design	Percent Difference
V_H	5.0208V	5.1591V	2.72%
V_L	-7.14983mV	29.097mV	330.31%

The measured values from the conventional XOR design yielded a high-level voltage (V_H) of 5.0208V and a low-level voltage (V_L) of -7.14983mV. In comparison, the bonus design produced a V_H of 5.1591V and a V_L of 29.097mV, shown in Figure 15. These measurements result in percent differences of 2.72% for the high state and 330.31% for the low state. The relatively small difference in the high output voltage can be attributed to minor variations internal resistance. However, the large percentage error in the low output voltage stems primarily from the fact that the initial low value was very close to 0 (-7mV), and the new value, though still small in magnitude, was positive. Because the average of the two small numbers near zero is small, this would result in a disproportionately large precent error. Despite the high relative error, both V_L values remain within a reasonable range to be interpreted as a logical low.

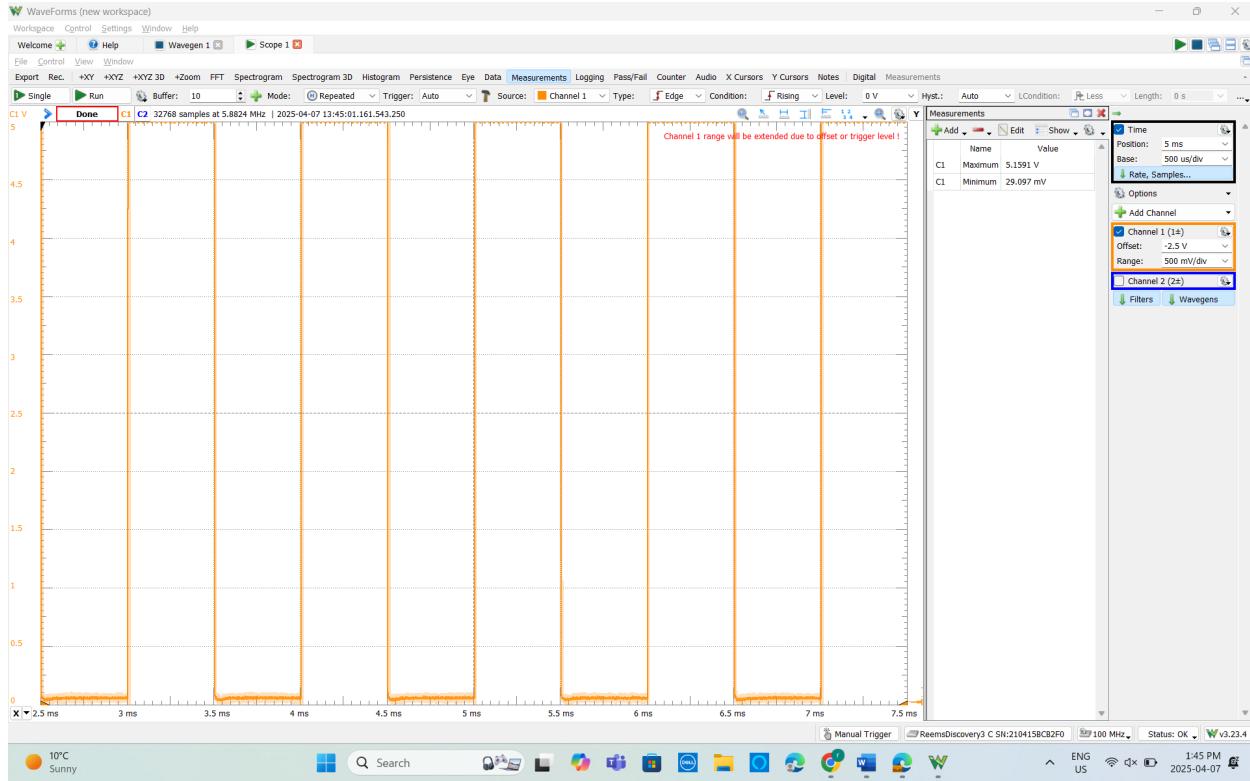


Figure 14: Bonus static level testing (input A constant 5V, input B toggling between 0V and 5V)

- c) From the waveform displayed in Figure 16, the rise time (τ_{rise}) is $161.12 \mu\text{s}$, while the fall time (τ_{fall}) is $307.31 \mu\text{s}$. Using these values, the reference delay (τ_{ref}) was calculated as $\tau_{ref} = 4.15(100nF) = 4.15 \times 10^{-7} \text{ s}$. Based on this, estimated propagation delays were found to be $\tau_{PHL} = 0.1660 \mu\text{s}$ and $\tau_{PLH} = 0.416 \mu\text{s}$, resulting in an average propagation delay of $\tau_p = 0.2905 \mu\text{s}$, as shown in Figure 15 calculations. The percent error of τ_p comparing the conventional design to the bonus design is calculated to be 5.47% which may be due to wiring connections as mentioned previously.

To determine τ_{PLH} , τ_{PHL} , and τ_p , τ_{ref} was calculated first:

$$\tau_{ref} = 4.15(100n) = 4.15 \times 10^{-7} \text{ s}$$

Using the τ_{ref} value, τ_{PLH} and τ_{PHL} values were calculated:

$$\tau_{PLH} = R_N \times C_L = \frac{2}{5} \times \tau_{ref} = 0.1660 \mu\text{s}$$

$$\tau_{PHL} = R_P \times C_L = \tau_{ref} = 0.415 \mu\text{s}$$

From the calculated τ_{PLH} and τ_{PHL} values, calculate τ_p value:

$$\tau_p = \frac{\tau_{PLH} + \tau_{PHL}}{2} = \frac{0.1756 \mu\text{s} + 0.439 \mu\text{s}}{2} = 0.2905 \mu\text{s}$$

Figure 15: Calculations for τ_p for the bonus design

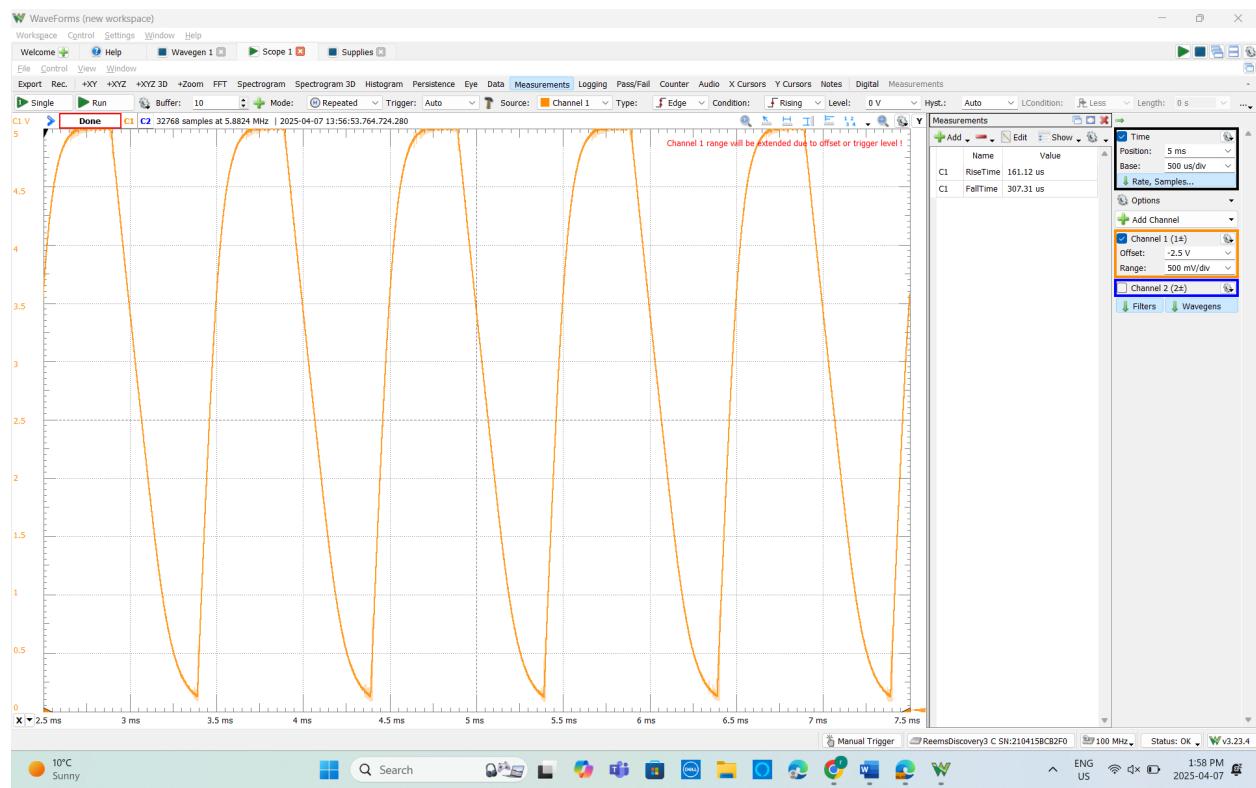


Figure 16: Bonus AD3 waveform for timing analysis