NOVATEK
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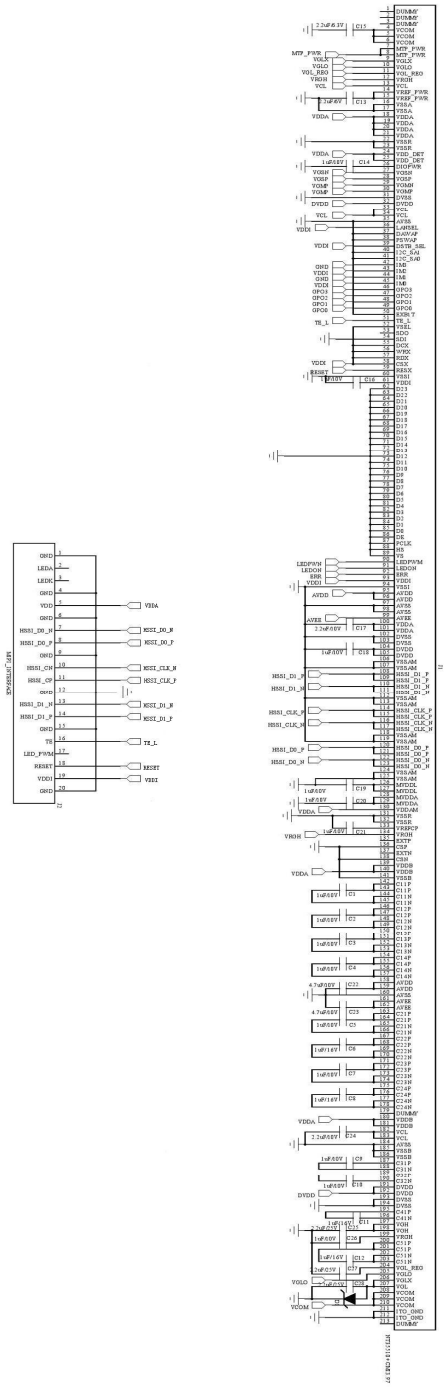
Data Sheet

NT35510 Application Notes
<< CMI IPS 4.02”>>

06/12,2012
Version 0.1

History				
Version	Date	Notes	Prepared By	Checked By
V 0.1	2012-06-12	New Release	Sam_Wu	Kevin_Su

1.1 FPC Reference Circuit for MIPI I/F:



Note：VGLO可以选择接VGLX或者是VGL_REG

1.2 Initial Code for MIPI I/F:

1.2.1 Display-on Sequence

- Step 1: VDDI On;
- Step 2: VDD On;
- Step 3: RESX = L;
- Step 4: Delay 10u Sec;
- Step 5: RESX = H;
- Step 6: Delay 5 mSec;

1.2.2 Software Setting

```
Void LCD_Initial(Void)
{
  HWRST 10

  DELAY 120

  #LV2 Page 1 enable
  REGW 0xF0,0x55,0xAA,0x52,0x08,0x01

  #AVDD Set AVDD 5.2V
  REGW 0xB0,0x0D,0x0D,0x0D

  #AVDD ratio
  REGW 0xB6,0x34,0x34,0x34

  #AVEE   -5.2V
  REGW 0xB1,0x0D,0x0D,0x0D

  #AVEE ratio
  REGW 0xB7,0x35,0x35,0x35

  #VCL   -2.5V
  REGW 0xB2,0x00,0x00,0x00

  #VCL ratio
  REGW 0xB8,0x24,0x24,0x24

  #VGH 15V
  REGW 0xBF,0x01
  REGW 0xB3,0x08,0x08,0x08

  #VGH ratio
  REGW 0xB9,0x34,0x34,0x34

  #VGLX ratio
```

```
REGW 0xBA,0x24,0x24,0x24

#VGMP/VGSP 4.7V/0V
REGW 0xBC,0x00,0x88,0x00

#VGMN/VGSN -4.7V/0V
REGW 0xBD,0x00,0x88,0x00

#VCOM -2.0375V
REGW 0xBE,0x00,0xA3

#Gamma Setting
REGW 0xD1,0x00,0x05,0x00,0x40,0x00,0x6D,0x00,0x90,0x00,0x99,0x00,0xBB,0x00,0xDC,0x01,0x04,
0x01,0x25,0x01,0x59,0x01,0x82,0x01,0xC6,0x02,0x01,0x02,0x02,0x02,0x39,0x02,0x79,0x02,0xA1,
0x02,0xD9,0x03,0x00,0x03,0x38,0x03,0x67,0x03,0x8F,0x03,0xCD,0x03,0xFD,0x03,0xFE,0x03,0xFF

REGW 0xD2,0x00,0x05,0x00,0x40,0x00,0x6D,0x00,0x90,0x00,0x99,0x00,0xBB,0x00,0xDC,0x01,0x04,
0x01,0x25,0x01,0x59,0x01,0x82,0x01,0xC6,0x02,0x01,0x02,0x02,0x02,0x39,0x02,0x79,0x02,0xA1,
0x02,0xD9,0x03,0x00,0x03,0x38,0x03,0x67,0x03,0x8F,0x03,0xCD,0x03,0xFD,0x03,0xFE,0x03,0xFF

REGW 0xD3,0x00,0x05,0x00,0x40,0x00,0x6D,0x00,0x90,0x00,0x99,0x00,0xBB,0x00,0xDC,0x01,0x04,
0x01,0x25,0x01,0x59,0x01,0x82,0x01,0xC6,0x02,0x01,0x02,0x02,0x02,0x39,0x02,0x79,0x02,0xA1,
0x02,0xD9,0x03,0x00,0x03,0x38,0x03,0x67,0x03,0x8F,0x03,0xCD,0x03,0xFD,0x03,0xFE,0x03,0xFF

REGW 0xD4,0x00,0x05,0x00,0x40,0x00,0x6D,0x00,0x90,0x00,0x99,0x00,0xBB,0x00,0xDC,0x01,0x04,
0x01,0x25,0x01,0x59,0x01,0x82,0x01,0xC6,0x02,0x01,0x02,0x02,0x02,0x39,0x02,0x79,0x02,0xA1,
0x02,0xD9,0x03,0x00,0x03,0x38,0x03,0x67,0x03,0x8F,0x03,0xCD,0x03,0xFD,0x03,0xFE,0x03,0xFF

REGW 0xD5,0x00,0x05,0x00,0x40,0x00,0x6D,0x00,0x90,0x00,0x99,0x00,0xBB,0x00,0xDC,0x01,0x04,
0x01,0x25,0x01,0x59,0x01,0x82,0x01,0xC6,0x02,0x01,0x02,0x02,0x02,0x39,0x02,0x79,0x02,0xA1,
0x02,0xD9,0x03,0x00,0x03,0x38,0x03,0x67,0x03,0x8F,0x03,0xCD,0x03,0xFD,0x03,0xFE,0x03,0xFF

REGW 0xD6,0x00,0x05,0x00,0x40,0x00,0x6D,0x00,0x90,0x00,0x99,0x00,0xBB,0x00,0xDC,0x01,0x04,
0x01,0x25,0x01,0x59,0x01,0x82,0x01,0xC6,0x02,0x01,0x02,0x02,0x02,0x39,0x02,0x79,0x02,0xA1,
0x02,0xD9,0x03,0x00,0x03,0x38,0x03,0x67,0x03,0x8F,0x03,0xCD,0x03,0xFD,0x03,0xFE,0x03,0xFF

#LV2 Page 0 enable
REGW 0xF0,0x55,0xAA,0x52,0x08,0x00

#Display control
REGW 0xB1,0xFC,0x00

#480x854
REGW 0xB5, 0x6B

#Source hold time
REGW 0xB6,0x05

#Gate EQ control
REGW 0xB7,0x70,0x70

#Source EQ control (Mode 2)
REGW 0xB8,0x01,0x05,0x05,0x05
```

#Inversion mode (Column)
REGW 0xBC,0x00,0x00,0x00

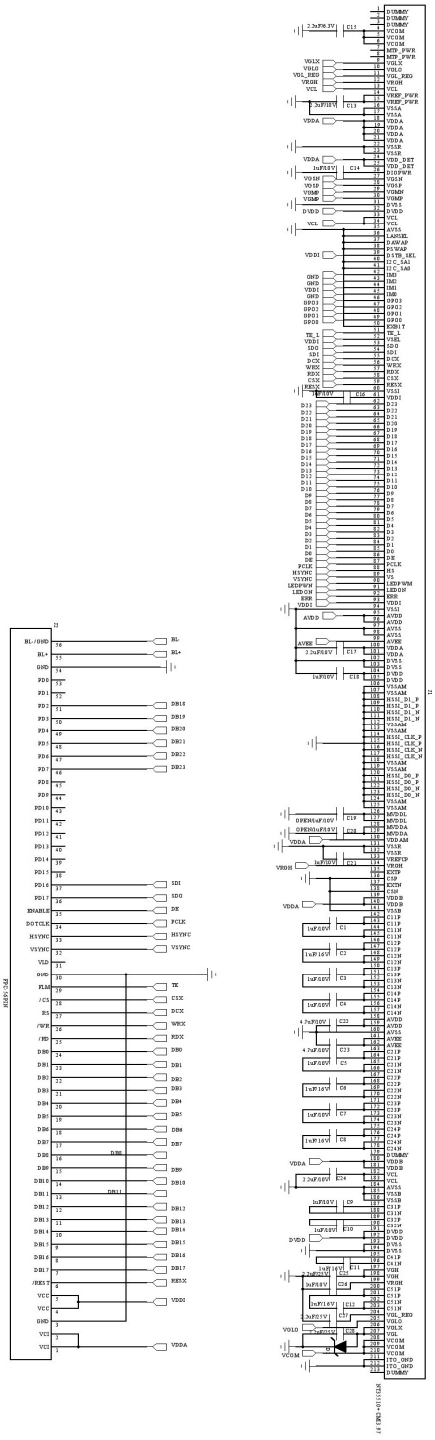
#Timing control 8phase dual side/4H/4delay/RST_EN
REGW 0xC9,0xD0,0x82,0x50,0x50,0x50

REGW 0x11

Delay 120

REGW 0x29

2.1 FPC Reference Circuit for RGB I/F:



Note：VGLO可以选择接VGLX或者是VGL_REG

2.2 Initial Code for RGB I/F:

2.2.1 Display-on Sequenc

- Step 1: VDDI On;
- Step 2: VDD On;
- Step 3: RESX = L;
- Step 4: Delay 10u Sec;
- Step 5: RESX = H;
- Step 6: Delay 5 mSec;

2.2.2 Software Setting

```
   Void LCD_Initial(Void)
{

  HWRST 10

  DELAY 120

  #LV2 Page 1 enable
  REGW 0xF000,0x55
  REGW 0xF001,0xAA
  REGW 0xF002,0x52
  REGW 0xF003,0x08
  REGW 0xF004,0x01

  #AVDD Set AVDD 5.2V
  REGW 0xB000,0x0D
  REGW 0xB001,0x0D
  REGW 0xB002,0x0D

  #AVDD ratio
  REGW 0xB600,0x34
  REGW 0xB601,0x34
  REGW 0xB602,0x34

  #AVEE   -5.2V
  REGW 0xB100,0x0D
  REGW 0xB101,0x0D
  REGW 0xB102,0x0D

  #AVEE ratio
  REGW 0xB700,0x35
  REGW 0xB701,0x35
  REGW 0xB702,0x35

  #VCL   -2.5V
```

```
REGW 0xB200,0x00

REGW 0xB201,0x00
REGW 0xB202,0x00

#VCL ratio
REGW 0xB800,0x24
REGW 0xB801,0x24
REGW 0xB802,0x24

#VGH 15V
REGW 0xBF00,0x01
REGW 0xB300,0x08
REGW 0xB301,0x08
REGW 0xB302,0x08

#VGH ratio
REGW 0xB900,0x34
REGW 0xB901,0x34
REGW 0xB902,0x34

#VGLX ratio
REGW 0xBA00,0x24
REGW 0xBA01,0x24
REGW 0xBA02,0x24

#VGMP/VGSP 4.7V/0V
REGW 0xBC00,0x00
REGW 0xBC01,0x88
REGW 0xBC02,0x00

#VGMN/VGSN -4.7V/0V
REGW 0xBD00,0x00
REGW 0xBD01,0x88
REGW 0xBD02,0x00

#VCOM -2.0375V
REGW 0xBE00,0x00
REGW 0xBE01,0xA3

#Gamma Setting
REGW 0xD100,0x00
REGW 0xD101,0x05
REGW 0xD102,0x00
REGW 0xD103,0x40
REGW 0xD104,0x00
REGW 0xD105,0x6D
REGW 0xD106,0x00
REGW 0xD107,0x90
REGW 0xD108,0x00
REGW 0xD109,0x99
REGW 0xD10A,0x00
REGW 0xD10B,0xBB
```

```
REGW 0xD10C,0x00
REGW 0xD10D,0xDC

REGW 0xD10E,0x01
REGW 0xD10F,0x04
REGW 0xD110,0x01
REGW 0xD111,0x25
REGW 0xD112,0x01
REGW 0xD113,0x59
REGW 0xD114,0x01
REGW 0xD115,0x82
REGW 0xD116,0x01
REGW 0xD117,0xC6
REGW 0xD118,0x02
REGW 0xD119,0x01
REGW 0xD11A,0x02
REGW 0xD11B,0x02
REGW 0xD11C,0x02
REGW 0xD11D,0x39
REGW 0xD11E,0x02
REGW 0xD11F,0x79
REGW 0xD120,0x02
REGW 0xD121,0xA1
REGW 0xD122,0x02
REGW 0xD123,0xD9
REGW 0xD124,0x03
REGW 0xD125,0x00
REGW 0xD126,0x03
REGW 0xD127,0x38
REGW 0xD128,0x03
REGW 0xD129,0x67
REGW 0xD12A,0x03
REGW 0xD12B,0x8F
REGW 0xD12C,0x03
REGW 0xD12D,0xCD
REGW 0xD12E,0x03
REGW 0xD12F,0xFD
REGW 0xD130,0x03
REGW 0xD131,0xFE
REGW 0xD132,0x03
REGW 0xD133,0xFF

REGW 0xD200,0x00
REGW 0xD201,0x05
REGW 0xD202,0x00
REGW 0xD203,0x40
REGW 0xD204,0x00
REGW 0xD205,0x6D
REGW 0xD206,0x00
REGW 0xD207,0x90
REGW 0xD208,0x00
REGW 0xD209,0x99
REGW 0xD20A,0x00
```

```
REGW 0xD20B,0xBB
REGW 0xD20C,0x00
REGW 0xD20D,0xDC

REGW 0xD20E,0x01
REGW 0xD20F,0x04
REGW 0xD210,0x01
REGW 0xD211,0x25
REGW 0xD212,0x01
REGW 0xD213,0x59
REGW 0xD214,0x01
REGW 0xD215,0x82
REGW 0xD216,0x01
REGW 0xD217,0xC6
REGW 0xD218,0x02
REGW 0xD219,0x01
REGW 0xD21A,0x02
REGW 0xD21B,0x02
REGW 0xD21C,0x02
REGW 0xD21D,0x39
REGW 0xD21E,0x02
REGW 0xD21F,0x79
REGW 0xD220,0x02
REGW 0xD221,0xA1
REGW 0xD222,0x02
REGW 0xD223,0xD9
REGW 0xD224,0x03
REGW 0xD225,0x00
REGW 0xD226,0x03
REGW 0xD227,0x38
REGW 0xD228,0x03
REGW 0xD229,0x67
REGW 0xD22A,0x03
REGW 0xD22B,0x8F
REGW 0xD22C,0x03
REGW 0xD22D,0xCD
REGW 0xD22E,0x03
REGW 0xD22F,0xFD
REGW 0xD230,0x03
REGW 0xD231,0xFE
REGW 0xD232,0x03
REGW 0xD233,0xFF

REGW 0xD300,0x00
REGW 0xD301,0x05
REGW 0xD302,0x00
REGW 0xD303,0x40
REGW 0xD304,0x00
REGW 0xD305,0x6D
REGW 0xD306,0x00
REGW 0xD307,0x90
REGW 0xD308,0x00
REGW 0xD309,0x99
```

```
REGW 0xD30A,0x00
REGW 0xD30B,0xBB
REGW 0xD30C,0x00
REGW 0xD30D,0xDC

REGW 0xD30E,0x01
REGW 0xD30F,0x04
REGW 0xD310,0x01
REGW 0xD311,0x25
REGW 0xD312,0x01
REGW 0xD313,0x59
REGW 0xD314,0x01
REGW 0xD315,0x82
REGW 0xD316,0x01
REGW 0xD317,0xC6
REGW 0xD318,0x02
REGW 0xD319,0x01
REGW 0xD31A,0x02
REGW 0xD31B,0x02
REGW 0xD31C,0x02
REGW 0xD31D,0x39
REGW 0xD31E,0x02
REGW 0xD31F,0x79
REGW 0xD320,0x02
REGW 0xD321,0xA1
REGW 0xD322,0x02
REGW 0xD323,0xD9
REGW 0xD324,0x03
REGW 0xD325,0x00
REGW 0xD326,0x03
REGW 0xD327,0x38
REGW 0xD328,0x03
REGW 0xD329,0x67
REGW 0xD32A,0x03
REGW 0xD32B,0x8F
REGW 0xD32C,0x03
REGW 0xD32D,0xCD
REGW 0xD32E,0x03
REGW 0xD32F,0xFD
REGW 0xD330,0x03
REGW 0xD331,0xFE
REGW 0xD332,0x03
REGW 0xD333,0xFF

REGW 0xD400,0x00
REGW 0xD401,0x05
REGW 0xD402,0x00
REGW 0xD403,0x40
REGW 0xD404,0x00
REGW 0xD405,0x6D
REGW 0xD406,0x00
REGW 0xD407,0x90
REGW 0xD408,0x00
```

```
REGW 0xD409,0x99
REGW 0xD40A,0x00
REGW 0xD40B,0xBB
REGW 0xD40C,0x00
REGW 0xD40D,0xDC

REGW 0xD40E,0x01
REGW 0xD40F,0x04
REGW 0xD410,0x01
REGW 0xD411,0x25
REGW 0xD412,0x01
REGW 0xD413,0x59
REGW 0xD414,0x01
REGW 0xD415,0x82
REGW 0xD416,0x01
REGW 0xD417,0xC6
REGW 0xD418,0x02
REGW 0xD419,0x01
REGW 0xD41A,0x02
REGW 0xD41B,0x02
REGW 0xD41C,0x02
REGW 0xD41D,0x39
REGW 0xD41E,0x02
REGW 0xD41F,0x79
REGW 0xD420,0x02
REGW 0xD421,0xA1
REGW 0xD422,0x02
REGW 0xD423,0xD9
REGW 0xD424,0x03
REGW 0xD425,0x00
REGW 0xD426,0x03
REGW 0xD427,0x38
REGW 0xD428,0x03
REGW 0xD429,0x67
REGW 0xD42A,0x03
REGW 0xD42B,0x8F
REGW 0xD42C,0x03
REGW 0xD42D,0xCD
REGW 0xD42E,0x03
REGW 0xD42F,0xFD
REGW 0xD430,0x03
REGW 0xD431,0xFE
REGW 0xD432,0x03
REGW 0xD433,0xFF

REGW 0xD500,0x00
REGW 0xD501,0x05
REGW 0xD502,0x00
REGW 0xD503,0x40
REGW 0xD504,0x00
REGW 0xD505,0x6D
REGW 0xD506,0x00
REGW 0xD507,0x90
```

```
REGW 0xD508,0x00
REGW 0xD509,0x99
REGW 0xD50A,0x00
REGW 0xD50B,0xBB
REGW 0xD50C,0x00
REGW 0xD50D,0xDC

REGW 0xD50E,0x01
REGW 0xD50F,0x04
REGW 0xD510,0x01
REGW 0xD511,0x25
REGW 0xD512,0x01
REGW 0xD513,0x59
REGW 0xD514,0x01
REGW 0xD515,0x82
REGW 0xD516,0x01
REGW 0xD517,0xC6
REGW 0xD518,0x02
REGW 0xD519,0x01
REGW 0xD51A,0x02
REGW 0xD51B,0x02
REGW 0xD51C,0x02
REGW 0xD51D,0x39
REGW 0xD51E,0x02
REGW 0xD51F,0x79
REGW 0xD520,0x02
REGW 0xD521,0xA1
REGW 0xD522,0x02
REGW 0xD523,0xD9
REGW 0xD524,0x03
REGW 0xD525,0x00
REGW 0xD526,0x03
REGW 0xD527,0x38
REGW 0xD528,0x03
REGW 0xD529,0x67
REGW 0xD52A,0x03
REGW 0xD52B,0x8F
REGW 0xD52C,0x03
REGW 0xD52D,0xCD
REGW 0xD52E,0x03
REGW 0xD52F,0xFD
REGW 0xD530,0x03
REGW 0xD531,0xFE
REGW 0xD532,0x03
REGW 0xD533,0xFF

REGW 0xD600,0x00
REGW 0xD601,0x05
REGW 0xD602,0x00
REGW 0xD603,0x40
REGW 0xD604,0x00
REGW 0xD605,0x6D
REGW 0xD606,0x00
```

```
REGW 0xD607,0x90
REGW 0xD608,0x00
REGW 0xD609,0x99
REGW 0xD60A,0x00
REGW 0xD60B,0xBB
REGW 0xD60C,0x00
REGW 0xD60D,0xDC

REGW 0xD60E,0x01
REGW 0xD60F,0x04
REGW 0xD610,0x01
REGW 0xD611,0x25
REGW 0xD612,0x01
REGW 0xD613,0x59
REGW 0xD614,0x01
REGW 0xD615,0x82
REGW 0xD616,0x01
REGW 0xD617,0xC6
REGW 0xD618,0x02
REGW 0xD619,0x01
REGW 0xD61A,0x02
REGW 0xD61B,0x02
REGW 0xD61C,0x02
REGW 0xD61D,0x39
REGW 0xD61E,0x02
REGW 0xD61F,0x79
REGW 0xD620,0x02
REGW 0xD621,0xA1
REGW 0xD622,0x02
REGW 0xD623,0xD9
REGW 0xD624,0x03
REGW 0xD625,0x00
REGW 0xD626,0x03
REGW 0xD627,0x38
REGW 0xD628,0x03
REGW 0xD629,0x67
REGW 0xD62A,0x03
REGW 0xD62B,0x8F
REGW 0xD62C,0x03
REGW 0xD62D,0xCD
REGW 0xD62E,0x03
REGW 0xD62F,0xFD
REGW 0xD630,0x03
REGW 0xD631,0xFE
REGW 0xD632,0x03
REGW 0xD633,0xFF

#LV2 Page 0 enable
REGW 0xF000,0x55
REGW 0xF001,0xAA
REGW 0xF002,0x52
REGW 0xF003,0x08
REGW 0xF004,0x00
```

#Display control
REGW 0xB100,0xFC
REGW 0xB101,0x00

#480x854
REGW 0xB500, 0x6B

#Source hold time
REGW 0xB600,0x05

#Gate EQ control
REGW 0xB700,0x70
REGW 0xB701,0x70

#Source EQ control (Mode 2)
REGW 0xB800,0x01
REGW 0xB801,0x05
REGW 0xB802,0x05
REGW 0xB803,0x05

#Inversion mode (Column)
REGW 0xBC00,0x00
REGW 0xBC01,0x00
REGW 0xBC02,0x00

#Timing control 8phase dual side/4H/4delay/RST_EN
REGW 0xC900,0xD0
REGW 0xC901,0x82
REGW 0xC902,0x50
REGW 0xC903,0x50
REGW 0xC904,0x50

REGW 0x1100

Delay 120

REGW 0x2900