

Migrating from AT89C51/C52 to AT89S51/S52

New Features

- Hardware Watchdog Timer
- Dual Data Pointer
- Power-off Flag
- Interrupt Recovery from Power-down Mode
- Flexible ISP Programming (Byte and Page Modes)
- 42-pin PDIP Package Option for Reduced EMI Emission

Introduction

The purpose of this application note is to help users convert existing designs from AT89C51/C52 to AT89S51/S52. The given information will also help users migrate from AT89LV51/LV52 to AT89LS51/LS52. This application note describes AT89S51/S52 memory sizes, features, and SFR mapping. More detailed information can be found in the AT89S51/S52 datasheets.

Memory Sizes

The following tables show a comparison of the individual memories.

Memory	AT89C51	AT89C52	AT89S51	AT89S52
Flash	4K Bytes	8K Bytes	4K Bytes	8K Bytes
RAM	128 Bytes	256 Bytes	128 Bytes	256 Bytes

Memory	AT89LV51	AT89LV52	AT89LS51	AT89LS52
Flash	4K Bytes	8K Bytes	4K Bytes	8K Bytes
RAM	128 Bytes	256 Bytes	128 Bytes	256 Bytes

Watchdog Timer

The hardware watchdog timer allows control of the microcontroller to be regained in situations where the CPU may be subjected to software upsets. The watchdog timer is enabled by software and resets the microcontroller after a specified period, unless the firmware intervenes and services the watchdog before its timeout.

Dual Data Pointer

Two banks of 16-bit Data Pointer Registers (DPTRs) are provided to facilitate access to internal and external data memory. Please refer to DPTR application note on Atmel Web site: www.atmel.com. Select Products > Microcontroller > 8051-Architecture > Documentation > Application Notes > AT89S8252 Primer



Flash Microcontrollers

Application Note



Power Off Flag

The Power Off Flag is in the PCON register in the SFR map and is set to “1” during power up. The Power Off Flag is not affected by reset and can be used to indicate that the microcontroller has been powered down.

Interrupt Recovery from Power-down Mode

An enabled external interrupt (through $\overline{\text{INT0}}$ or $\overline{\text{INT1}}$) can be used to exit from the power-down mode. In the older derivatives, the only way to recover from the power-down mode was to perform a hardware reset.

Flexible ISP Programming (Byte and Page Modes)

The program memory can be programmed using the serial ISP interface while RST is strapped to V_{CC} . Program memory can be programmed in page mode (1 code page = 256 bytes) or byte mode.

Operational V_{CC} Voltage Range

While the low-voltage versions AT89LV51/LV52 are offered in an extended operational V_{CC} voltage range of 2.7V to 6.0V, the low-voltage versions AT89LS51/LS52 are offered in a V_{CC} voltage range of 2.7V to 4.0V. If the application requires a V_{CC} voltage within a range of 4.0V to 5.5V, the user should select the AT89S51/S52.

42-pin PDIP Package Option for Reduced EMI Emission

The 42-pin package has extra pins PWRVDD and PWRGND to reduce EMI Emission. PWRVDD must be connected to the application board supply voltage. PWRGND must be connected to the application board GND.

SFRs Mapping

The highlighted SFR locations in the following table are the new registers for the AT89S51/S52 devices.

0F8H									0FFH
0F0H	B								0F7H
0E8H									0EFH
0E0H	ACC								0E7H
0D8H									0DFH
0D0H	PSW								0D7H
0C8H	T2CON*	T2MOD*	RCAP2L*	RCAP2H*	TL2*	TH2*			0CFH
0C0H									0C7H
0B8H	IP								0BFH
0B0H	P3								0B7H
0A8H	IE								0AFH
0A0H	P2		AUXR1				WDTRST		0A7H
98H	SCON	SBUF							9FH
90H	P1								97H
88H	TCON	TMOD	TL0	TL1	TH0	TH1	AUXR		8FH
80H	P0	SP	DP0L	DP0H	DP1L	DP1H		PCON	87H

Note: 1. *Only AT89LV52, AT89C52, AT89LS52, and AT89S52 have Timer 2 registers T2CON, T2MOD, RCAP2L, RCAP2H, TL2, and TH2



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