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- **Output Swing includes Both Supply Rails**
- Low Noise . . . 12 nV/ $\sqrt{\text{Hz}}$  Typ at f = 1 kHz
- Low Input Bias Current . . . 1 pA Typ
- Fully Specified for Both Single-Supply and **Split-Supply Operation**
- Low Power . . . 500 μA Max
- Common-Mode Input Voltage Range **Includes Negative Rail**

#### description

The TLC2262 and TLC2264 are dual and quadruple operational amplifiers from Texas Instruments. Both devices exhibit rail-to-rail output performance for increased dynamic range in single- or split-supply applications. The TLC226x family offers a compromise between the micropower TLC225x and the ac performance of the TLC227x. It has low supply current for battery-powered applications, while still having adequate ac performance for applications that demand it. The noise performance has been dramatically improved over previous generations of CMOS amplifiers. Figure 1 depicts the low level of noise voltage for this CMOS amplifier, which has only 200 µA (typ) of supply current per amplifier.

The TLC226x, exhibiting high input impedance and low noise, are excellent for small-signal conditioning for high-impedance sources, such as piezoelectric transducers. Because of the micropower dissipation levels, these devices work well in hand-held monitoring and remote-sensing

**Low Input Offset Voltage** 950  $\mu$ V Max at T<sub>A</sub> = 25°C (TLC2262A)

- Macromodel Included
- Performance Upgrade for the TS27M2/M4 and TLC27M2/M4
- **Available in Q-Temp Automotive HighRel Automotive Applications Configuration Control/Print Support Qualification to Automotive Standards**

### **EQUIVALENT INPUT NOISE VOLTAGE** VS

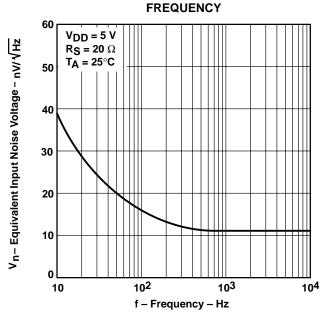


Figure 1

applications. In addition, the rail-to-rail output feature with single or split supplies makes this family a great choice when interfacing with analog-to-digital converters (ADCs). For precision applications, the TLC226xA family is available and has a maximum input offset voltage of 950 μV. This family is fully characterized at 5 V and ±5 V.

The TLC2262/4 also makes great upgrades to the TLC27M2/L4 or TS27M2/L4 in standard designs. They offer increased output dynamic range, lower noise voltage and lower input offset voltage. This enhanced feature set allows them to be used in a wider range of applications. For applications that require higher output drive and wider input voltage range, see the TLV2432 and TLV2442. If your design requires single amplifiers, please see the TLV2211/21/31 family. These devices are single rail-to-rail operational amplifiers in the SOT-23 package. Their small size and low power consumption, make them ideal for high density, battery-powered equipment.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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#### **TLC2262 AVAILABLE OPTIONS**

			PACKAGED DEVICES							
T <sub>A</sub>	V <sub>IO</sub> max AT 25°C	SMALL OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (JG)	PLASTIC DIP (P)	TSSOP (PW)	CERAMIC FLATPACK (U)			
0°C to 70°C	2.5 mV	TLC2262CD		_	TLC2262CP	TLC2262CPW	_			
-40°C to 125°C	950 μV 2.5 mV	TLC2262AID TLC2262ID		_ _	TLC2262AIP TLC2262IP	TLC2262AIPW —				
-40°C to 125°C	950 μV 2.5 mV	TLC2262AQD TLC2262QD	_ _	_ _	_					
−55°C to 125°C	950 μV 2.5 mV		TLC2262AMFK TLC2262MFK	TLC2262AMJG TLC2262MJG	_ _		TLC2262AMU TLC2262MU			

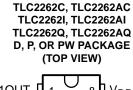
The D packages are available taped and reeled. Add R suffix to device type (e.g., TLC2262CDR). The PW package is available only left-end taped and reeled. Chips are tested at 25°C.

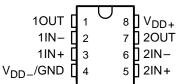
#### **TLC2264 AVAILABLE OPTIONS**

				PACKAGE	D DEVICES		
TA	V <sub>IO</sub> max AT 25°C	SMALL OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (J)	PLASTIC DIP (N)	TSSOP (PW)	CERAMIC FLATPACK (W)
0°C to 70°C	2.5 mV	TLC2264CD		_	TLC2264CN	TLC2264CPW	_
-40°C to 125°C	950 μV 2.5 mV	TLC2264AID TLC2264ID			TLC2264AIN TLC2264IN	TLC2264AIPW —	
-40°C to 125°C	950 μV 2.5 mV	TLC2264AQD TLC2264QD	_		_ _	_	_
−55°C to 125°C	950 μV 2.5 mV	_ _	TLC2264AMFK TLC2264MFK	TLC2264AMJ TLC2264MJ	_ _	_ _	TLC2264AMW TLC2264MW

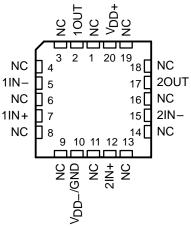
The D packages are available taped and reeled. Add R suffix to device type (e.g., TLC2264CDR). The PW package is available only left-end taped and reeled. Chips are tested at 25°C.





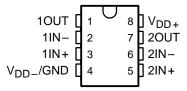


## TLC2262M, TLC2262AM . . . FK PACKAGE (TOP VIEW)

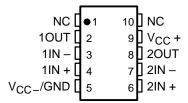


NC - No internal connection

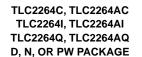
## TLC2262M, TLC2262AM . . . JG PACKAGE (TOP VIEW)



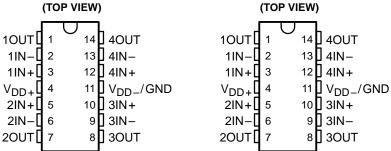
## TLC2262M, TLC2262AM . . . U PACKAGE (TOP VIEW)



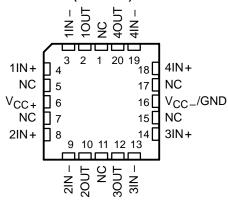
NC - No internal connection



## TLC2264M, TLC2264AM . . . J OR W PACKAGE (TOP VIEW)



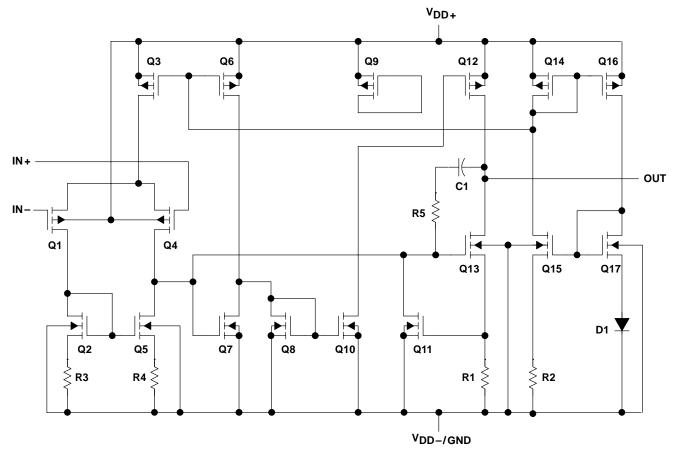
## TLC2264M, TLC2264AM . . . FK PACKAGE (TOP VIEW)



NC - No internal connection



## equivalent schematic (each amplifier)



ACTUAL DEVI	CE COMPONENT	COUNT <sup>†</sup>							
COMPONENT TLC2262 TLC2264									
Transistors	38	76							
Resistors	28	56							
Diodes	9	18							
Capacitors	3	6							

<sup>†</sup> Includes both amplifiers and all ESD, bias, and trim circuitry

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#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V <sub>DD+</sub> (see Note 1)		
Supply voltage, V <sub>DD</sub> (see Note 1)		
Differential input voltage, V <sub>ID</sub> (see Note 2)	)	
Input voltage, V <sub>I</sub> (any input, see Note 1)		$V_{DD-} - 0.3 \text{ V to } V_{DD+}$
		±5 mA
		±50 mA
Total current into V <sub>DD+</sub>		±50 mA
Total current out of V <sub>DD</sub>		±50 mA
Duration of short-circuit current at (or belo	ow) 25°C (see Note 3)	unlimited
Continuous total dissipation		See Dissipation Rating Table
Operating free-air temperature range, T <sub>A</sub> :	C suffix	0°C to 70°C
	I suffix	–40°C to 125°C
	Q suffix	–40°C to 125°C
	M suffix	
Storage temperature range, T <sub>stq</sub>		–65°C to 150°C
		D, N, P, and PW packages 260°C
		J, JG, U, and W packages 300°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. All voltage values, except differential voltages, are with respect to the midpoint between V<sub>DD+</sub> and V<sub>DD-</sub>.
  - 2. Differential voltages are at IN+ with respect to IN-. Excessive current flows if input is brought below  $V_{DD} = 0.3 \text{ V}$ .
  - 3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

#### **DISSIPATION RATING TABLE**

PACKAGE	T <sub>A</sub> ≤ 25°C POWER RATING	DERATING FACTOR ABOVE T <sub>A</sub> = 25°C	T <sub>A</sub> = 70°C POWER RATING	T <sub>A</sub> = 85°C POWER RATING	T <sub>A</sub> = 125°C POWER RATING
D-8	725 mW	5.8 mW/°C	464 mW	377 mW	145 mW
D-14	950 mW	7.6 mW/°C	608 mW	494 mW	190 mW
FK	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
J	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
JG	1050 mW	8.4 mW/°C	672 mW	546 mW	210 mW
N	1150 mW	9.2 mW/°C	736 mW	598 mW	230 mW
Р	1000 mW	8.0 mW/°C	640 mW	520 mW	200 mW
PW-8	525 mW	4.2 mW/°C	336 mW	273 mW	105 mW
PW-14	700 mW	5.6 mW/°C	448 mW	364 mW	140 mW
U	700 mW	5.5 mW/°C	452 mW	370 mW	150 mW
W	700 mW	5.5 mW/°C	452 mW	370 mW	150 mW

#### recommended operating conditions

	С	SUFFIX	I SUFFIX		Q SUFFIX		M SUFFIX		UNIT
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
Supply voltage, V <sub>DD±</sub>	±2.2	±8	±2.2	±8	±2.2	±8	±2.2	±8	V
Input voltage range, V <sub>I</sub>	$V_{DD-}$	V <sub>DD+</sub> -1.5	V						
Common-mode input voltage, V <sub>IC</sub>	$V_{DD-}$	V <sub>DD+</sub> -1.5	V						
Operating free-air temperature, TA	0	70	-40	125	-40	125	-55	125	°C



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# TLC2262C electrical characteristics at specified free-air temperature, $V_{DD} = 5 \text{ V}$ (unless otherwise noted)

PARAMETER		TEST CO	NOITIONS	- +	TI	_C22620	;	
	PARAMETER	TEST CO	NDITIONS	T <sub>A</sub> †	MIN	TYP	MAX	UNIT
VIO	Input offset voltage			25°C		300	2500	μV
V10	input onset voltage	]		Full range			3000	μν
ανιο	Temperature coefficient of input offset voltage			25°C to 70°C		2		μV/°C
	Input offset voltage long-term drift (see Note 4)	V <sub>IC</sub> = 0, V <sub>O</sub> = 0,	$V_{DD} \pm = \pm 2.5 \text{ V},$ RS = 50 \Omega	25°C		0.003		μV/mo
	lanut offeet current	1	_	25°C		0.5		<b>~</b> ^
ΙO	Input offset current			Full range			100	pА
lup.	Input bias current	]		25°C		1		pА
lВ	input bias current			Full range			100	PΛ
VICR	Common-mode input voltage range	R <sub>S</sub> = 50 Ω,	V <sub>IO</sub>   ≤ 5 mV	25°C	0 -0.3 to to 4 4.2	<b>&gt;</b>		
				Full range	0 to 3.5			
		$I_{OH} = -20  \mu A$		25°C		4.99		
		I <sub>OH</sub> = -100 μA		25°C	4.85	4.94		
∨он	High-level output voltage	ΙΟΗ = – 100 μΑ		Full range	4.82			V
		I <sub>OH</sub> = -400 μA		25°C	4.70	4.85		
		ΙΟΗ = -400 μΑ		Full range	4.60			
		$V_{IC} = 2.5 V$ ,	I <sub>OL</sub> = 50 μA	25°C		0.01		
		V <sub>IC</sub> = 2.5 V,	I <sub>OL</sub> = 500 μA	25°C		0.09	0.15	
		V <sub>1</sub> C = 2.5 V,	10[ = 300 μΑ	Full range			0.15	
VOL	Low-level output voltage	V <sub>IC</sub> = 2.5 V,	I <sub>OL</sub> = 1 mA	25°C		0.2	0.3	V
		V <sub>1</sub> C = 2.5 V,	IOL = TINA	Full range			0.3	
		V <sub>IC</sub> = 2.5 V,	I <sub>OL</sub> = 4 mA	25°C		0.7	1	
		V <sub>1</sub> C = 2.5 V,	IOL = 4 IIIA	Full range			1.2	
		.,	$R_L = 50 \text{ k}\Omega^{\ddagger}$	25°C	80	170		
$A_{VD}$	Large-signal differential voltage amplification	$V_{IC} = 2.5 \text{ V},$ $V_{O} = 1 \text{ V to 4 V}$	K[ = 50 K22+	Full range	55			V/mV
			$R_L = 1 M\Omega^{\ddagger}$	25°C		550		
r <sub>i(d)</sub>	Differential input resistance			25°C		1012		Ω
r <sub>i(c)</sub>	Common-mode input resistance			25°C		1012		Ω
Ci(c)	Common-mode input capacitance	f = 10 kHz,	P package	25°C		8		pF
z <sub>0</sub>	Closed-loop output impedance	f = 100 kHz,	A <sub>V</sub> = 10	25°C		240		Ω
	Opposed and animatics and	$V_{IC} = 0 \text{ to } 2.7 \text{ V},$	V <sub>O</sub> = 2.5 V,	25°C	70	83		10
CMRR	Common-mode rejection ratio	$R_S = 50 \Omega$	<i>,</i>	Full range	70			dB
l	Cumply voltage rejection and (AVI = /AVI )	$V_{DD} = 4.4 \text{ V to } 1$	16 V,	25°C	80	95		4D
ksvr	Supply-voltage rejection ratio (ΔV <sub>DD</sub> /ΔV <sub>IO</sub> )	$V_{IC} = V_{DD}/2$ ,	No load	Full range	80			dB
Inc	Supply current	Vo = 2.5.V	No load	25°C		400	500	^
IDD	Supply current	$V_0 = 2.5 V$ ,	No load	Full range			500	μΑ

<sup>†</sup> Full range is 0°C to 70°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at  $T_A = 150^{\circ}C$  extrapolated to  $T_A = 25^{\circ}C$  using the Arrhenius equation and assuming an activation energy of 0.96 eV.



<sup>‡</sup>Referenced to 2.5 V

## TLC2262C operating characteristics at specified free-air temperature, $V_{DD} = 5 \text{ V}$

PARAMETER		TEST CONDI	TIONS	<b>+</b> +	TLC2262C			UNIT
	PARAMETER	TEST CONDI	HONS	T <sub>A</sub> †	MIN	TYP	MAX	UNII
SR	Slew rate at unity gain	$V_0 = 1.5 \text{ V to } 3.5 \text{ V},$	$R_L = 50 \text{ k}\Omega^{\ddagger}$ ,	25°C	0.35	0.55		V/μs
SK	Siew rate at unity gain	$C_L = 100 \text{ pF}^{\ddagger}$		Full range	0.3			ν/μ3
V.	Equivalent input noise voltage	f = 10 Hz		25°C		40		nV/√Hz
V <sub>n</sub>	Equivalent input hoise voltage	f = 1 kHz		25°C		12		IIV/∀⊓Z
\/\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\	Peak-to-peak equivalent input noise	f = 0.1 Hz to 1 Hz		25°C 0.7			μV	
V <sub>N(PP)</sub>	voltage	f = 0.1 Hz to 10 Hz		25°C		1.3		μν
In	Equivalent input noise current			25°C		0.6		fA√Hz
THD + N	Total harmonic distortion plus noise	$V_O = 0.5 \text{ V to } 2.5 \text{ V},$ f = 20 kHz,	A <sub>V</sub> = 1	25°C	(	0.017%		
THE TH	Total Harmonic distortion plus hoise	$R_L = 50 \text{ k}\Omega^{\ddagger}$	A <sub>V</sub> = 10	25 0		0.03%		
	Gain-bandwidth product	f = 10 kHz, C <sub>L</sub> = 100 pF <sup>‡</sup>	$R_L = 50 \text{ k}\Omega^{\ddagger}$ ,	25°C		0.71		MHz
ВОМ	Maximum output-swing bandwidth	$V_{O(PP)} = 2 \text{ V},$ $R_{L} = 50 \text{ k}\Omega^{\ddagger},$	$A_V = 1,$ $C_L = 100 \text{ pF}^{\ddagger}$	25°C		185		kHz
t <sub>S</sub>	Settling time	$A_V = -1$ , Step = 0.5 V to 2.5 V,	To 0.1%	25°C		6.4		μs
'S		$R_L = 50 \text{ k}\Omega^{\ddagger},$ $C_L = 100 \text{ pF}^{\ddagger}$	To 0.01%	200		14.1		μο
φm	Phase margin at unity gain	$R_L = 50 \text{ k}\Omega^{\ddagger,}$	C <sub>I</sub> = 100 pF <sup>‡</sup>	25°C		56°		
	Gain margin	7 IVE = 20 K22+,	OL = 100 pi-+	25°C		11		dB

<sup>†</sup> Full range is 0°C to 70°C. ‡ Referenced to 2.5 V



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# TLC2262C electrical characteristics at specified free-air temperature, $V_{DD\pm}$ = $\pm 5$ V (unless otherwise specified)

	PARAMETER I TEST CONDITIONS I TAT I—————		LC22620	;				
	PARAMETER	TEST CO	ONDITIONS	'A'	MIN	TYP	MAX	UNIT
VIO	Input offset voltage			25°C		300	2500	μV
VIO	input onset voltage			Full range			3000	μν
αΛΙΟ	Temperature coefficient of input offset voltage			25°C to 70°C		2		μV/°C
	Input offset voltage long-term drift (see Note 4)	$V_{IC} = 0,$ $R_S = 50 \Omega$	$V_{O} = 0$ ,	25°C		0.003		μV/mo
li a	Innut offeet current	KS = 50 12		25°C		0.5		~^
IIO	Input offset current			Full range			100	pΑ
lin.	Input bias current			25°C		1		pА
ΙΒ	input bias current			Full range			100	pΑ
VICR	Common-mode input voltage range	V <sub> O</sub>  ≤5 mV,	Rs = 50 Ω	25°C	-5 to 4	-5.3 to 4.2		٧
· ICR	Common-mode input voltage range	V O  ≥3 IIIV,	NS = 30 22	Full range	-5 to 3.5			V
		$I_0 = -20 \mu\text{A}$		25°C		4.99		
		$I_{O} = -100  \mu$ A		25°C	4.85	4.94		
V <sub>OM+</sub>	Maximum positive peak output voltage	10 = -100 με	<b>\</b>	Full range	4.82			V
		$I_{O} = -400  \mu$ A		25°C	4.7	4.85		
		10 = 400 μι	•	Full range	4.6			
		$V_{IC} = 0$ ,	I <sub>O</sub> = 50 μA	25°C		-4.99		
		$V_{IC} = 0$ ,	ΙΟ = 500 μΑ	25°C	-4.85	-4.91		V
		10 3,		Full range	-4.85	_		
VOM-	Maximum negative peak output voltage	V <sub>IC</sub> = 0,	$I_O = 1 \text{ mA}$	25°C	-4.7	-4.8		
		10 3,		Full range	-4.7			
		$V_{IC} = 0$ ,	$I_O = 4 \text{ mA}$	25°C	-4	-4.3		
		10 17	•	Full range	-3.8			
			$R_L = 50 \text{ k}\Omega$	25°C	80	200		
AVD	Large-signal differential voltage amplification	$V_O = \pm 4 V$		Full range	55			V/mV
			$R_L = 1 M\Omega$	25°C		1000		
<sup>r</sup> i(d)	Differential input resistance			25°C		1012		Ω
ri(c)	Common-mode input resistance			25°C		1012		Ω
<sup>C</sup> i(c)	Common-mode input capacitance	f = 10 kHz,	P package	25°C		8		pF
z <sub>0</sub>	Closed-loop output impedance	f = 100 kHz,	A <sub>V</sub> = 10	25°C		220		Ω
CMRR	Common-mode rejection ratio	$V_{IC} = -5 \text{ V to}$		25°C	75	88		dB
	•	V <sub>O</sub> = 0 V,	$R_S = 50 \Omega$	Full range	75			
ksvr	Supply-voltage rejection ratio (ΔV <sub>DD+</sub> /ΔV <sub>IO</sub> )	$V_{DD\pm} = 2.2$		25°C	80	95		dB
		V <sub>IC</sub> = 0,	No load	Full range	80	405	500	
IDD	Supply current	$V_{O} = 0 V$	No load	25°C		425	500	μΑ
				Full range			500	

<sup>†</sup>Full range is 0°C to 70°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at  $T_A = 150$ °C extrapolated to  $T_A = 25$ °C using the Arrhenius equation and assuming an activation energy of 0.96 eV.



## TLC2262C operating characteristics at specified free-air temperature, $\rm V_{DD\pm}$ = $\pm 5~V$

	DADAMETED	TEST CONDIT	TONG	- +	Т	LINUT		
	PARAMETER	TEST CONDIT	IONS	T <sub>A</sub> †	MIN	TYP	MAX	UNIT
		V- 140V	D: 501-0	25°C	0.35	0.55		
SR	Slew rate at unity gain	$V_O = \pm 1.9 \text{ V},$ $C_L = 100 \text{ pF}$	$R_L = 50 \text{ k}\Omega$	Full range	0.3			V/μs
	Facilitate at increase values	f = 10 Hz		25°C		43		\ // <del>                                   </del>
V <sub>n</sub>	Equivalent input noise voltage	f = 1 kHz		25°C		12		nV/√Hz
\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\	Peak-to-peak equivalent input noise	f = 0.1 Hz to 1 Hz		25°C		0.8		μV
VN(PP)	voltage	f = 0.1 Hz to 10 Hz		25°C		1.3		μν
In	Equivalent input noise current			25°C		0.6		fA√Hz
THD + N	Total harmonic distortion pulse duration	$V_0 = \pm 2.3 \text{ V},$ f = 20 kHz,	A <sub>V</sub> = 1	25°C		0.014%		
I I I I I I I I I I I I I I I I I I I	rotal narmonic distortion pulse duration	$R_L = 50 \text{ k}\Omega$	A <sub>V</sub> = 10	25 C		0.024%		
	Gain-bandwidth product	f = 10 kHz, C <sub>L</sub> = 100 pF	$R_L = 50 \text{ k}\Omega$	25°C		0.73		MHz
ВОМ	Maximum output-swing bandwidth	$V_{O(PP)} = 4.6 \text{ V},$ $R_{L} = 50 \text{ k}\Omega,$	A <sub>V</sub> = 1, C <sub>L</sub> = 100 pF	25°C		85		kHz
	Settling time	$A_V = -1$ , Step = -2.3 V to 2.3 V,	To 0.1%	25°C		7.1		116
t <sub>S</sub>	Jetung tille	$R_L = 50 \text{ k}\Omega$ , $C_L = 100 \text{ pF}$	To 0.01%	20 0		16.5		μs
φm	Phase margin at unity gain	$R_1 = 50 \text{ k}\Omega$	C <sub>I</sub> = 100 pF	25°C		57°		
	Gain margin	] INL = 30 K22,	CL = 100 pr	25°C		11		dB

<sup>†</sup> Full range is 0°C to 70°C.

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# TLC2264C electrical characteristics at specified free-air temperature, $V_{DD} = 5 \text{ V}$ (unless otherwise noted)

	DADAMETED	TEST 00	NDITIONS	- +	Τl	C22640	;		
	PARAMETER	TEST CO	NDITIONS	T <sub>A</sub> †	MIN	TYP	MAX	UNIT	
۷ <sub>IO</sub>	Input offset voltage			25°C		300	2500	μV	
VIO	input onset voltage			Full range			3000	μν	
αVIO	Temperature coefficient of input offset voltage			25°C to 70°C		2		μV/°C	
	Input offset voltage long-term drift (see Note 4)	$V_{IC} = 0,$ $V_{O} = 0,$	$V_{DD\pm} = \pm 2.5 \text{ V},$ Rs = 50 \Omega	25°C		0.003		μV/mo	
	lanut offeet europe	1	_	25°C		0.5		- A	
ΙO	Input offset current			Full range			100	pА	
	Input bigg ourrent	1		25°C		1		n^	
ΙΒ	Input bias current			Full range			100	pΑ	
VICR	Common-mode input voltage range	$R_S = 50 \Omega$ ,	V <sub>IO</sub>   ≤ 5 mV	25°C	0 to 4	-0.3 to 4.2		V	
ICIX	, and the second of the second	<b>3</b> ••• ,	1101	Full range	0 to 3.5				
		$I_{OH} = -20 \mu A$		25°C		4.99			
		I <sub>OH</sub> = -100 μA		25°C	4.85	4.94			
Vон	High-level output voltage	ΙΟΗ = - 100 μΑ		Full range	4.82			V	
		I <sub>OH</sub> = -400 μA		25°C	4.70	4.85			
		ΙΟΗ = -400 μΑ		Full range	4.60				
		$V_{IC} = 2.5 V$ ,	$I_{OL} = 50 \mu A$	25°C		0.01			
		V <sub>IC</sub> = 2.5 V,	I <sub>OL</sub> = 500 μA	25°C		0.09	0.15		
		VIC = 2.5 V,	10L = 300 μΑ	Full range			0.15		
VOL	Low-level output voltage	V <sub>IC</sub> = 2.5 V,	I <sub>OL</sub> = 1 mA	25°C		0.2	0.3	V	
		VIC = 2.5 V,	IOL = 1 IIIA	Full range			0.3		
		V <sub>IC</sub> = 2.5 V,	I <sub>OL</sub> = 4 mA	25°C		0.7	1		
		VIC = 2.5 V,	IOL = 4 IIIA	Full range			1.2		
		.,	$R_L = 50 \text{ k}\Omega^{\ddagger}$	25°C	80	170			
$A_{VD}$	Large-signal differential voltage amplification	$V_{IC} = 2.5 \text{ V},$ $V_{O} = 1 \text{ V to 4 V}$	K[ = 50 K22+	Full range	55			V/mV	
			$R_L = 1 M\Omega^{\ddagger}$	25°C		550			
r <sub>i(d)</sub>	Differential input resistance			25°C		1012		Ω	
r <sub>i(c)</sub>	Common-mode input resistance			25°C		1012		Ω	
Ci(c)	Common-mode input capacitance	f = 10 kHz,	N package	25°C		8		pF	
z <sub>o</sub>	Closed-loop output impedance	f = 100 kHz,	A <sub>V</sub> = 10	25°C		240		Ω	
	Common mode unication water	V <sub>IC</sub> = 0 to 2.7 V.	o 2.7 V, V <sub>O</sub> = 2.5 V, 25°C		70	83		10	
CMRR	Common-mode rejection ratio	$R_S = 50 \Omega$	<i>,</i>	Full range	70			dB	
leas :=	Cumply voltage rejection and (AVI = IAVI )	$V_{DD} = 4.4 \text{ V to } 1$	6 V,	25°C	80	95		40	
ksvr	Supply-voltage rejection ratio (ΔV <sub>DD</sub> /ΔV <sub>IO</sub> )	$V_{IC} = V_{DD}/2$ ,	No load	Full range	80			dB	
Inc	Supply current (four amplifiers)	Vo = 2.5.V	No load	25°C		0.8	1	mΛ	
IDD	Supply current (four amplifiers)	$V_0 = 2.5 V$ ,	INU IUAU	Full range			1	mA	

<sup>†</sup> Full range is 0°C to 70°C.

NOTE 4. Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at  $T_A = 150$ °C extrapolated to  $T_A = 25$ °C using the Arrhenius equation and assuming an activation energy of 0.96 eV.



<sup>‡</sup>Referenced to 2.5 V

## TLC2264C operating characteristics at specified free-air temperature, $V_{DD} = 5 \text{ V}$

	PARAMETER	TEST CONDI	TIONS	_ +	TLC2264C			UNIT
	PARAMETER	TEST CONDI	TIONS	T <sub>A</sub> †	MIN	TYP	MAX	UNII
		V 4.4V/+= 0.6V/	$R_1 = 50 \text{ k}\Omega^{\ddagger}$	25°C	0.35	0.55		
SR	Slew rate at unity gain	$V_{O}$ = 1.4 V to 2.6 V, $R_{L}$ = 50 k $\Omega^{\ddagger}$ , $C_{L}$ = 100 pF $^{\ddagger}$		Full range	0.3			V/μs
\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \	Fault plant input poins voltage	f = 10 Hz		25°C		40		->4/15
Vn	Equivalent input noise voltage	f = 1 kHz		25°C		12		nV/√Hz
\/\.\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\	Peak-to-peak equivalent input noise	f = 0.1 Hz to 1 Hz		25°C		0.7		μV
VN(PP)	voltage	f = 0.1 Hz to 10 Hz		25°C		1.3		μν
In	Equivalent input noise current			25°C		0.6		fA/√Hz
THD + N	Total harmonic distortion plus noise	$V_O = 0.5 \text{ V to } 2.5 \text{ V},$ f = 20 kHz.	A <sub>V</sub> = 1	25°C		0.017%		
THEFN	Total Harmonic distortion plus hoise	$R_L = 50 \text{ k}\Omega^{\ddagger}$	A <sub>V</sub> = 10	25 C		0.03%		
	Gain-bandwidth product	f = 10 kHz, C <sub>L</sub> = 100 pF <sup>‡</sup>	$R_L = 50 \text{ k}\Omega^{\ddagger}$ ,	25°C		0.71		MHz
Вом	Maximum output-swing bandwidth	$V_{O(PP)} = 2 \text{ V},$ $R_{L} = 50 \text{ k}\Omega^{\ddagger},$	$A_V = 1,$ $C_L = 100 \text{ pF}^{\ddagger}$	25°C		185		kHz
t-	Settling time	$A_V = -1$ , Step = 0.5 V to 2.5 V,	To 0.1%	25°C		6.4		μs
t <sub>S</sub>	Columny units	$R_L = 50 \text{ k}\Omega^{\ddagger},$ $C_L = 100 \text{ pF}^{\ddagger}$	To 0.01%	20 0		14.1		μο
φm	Phase margin at unity gain	$R_L = 50 \text{ k}\Omega^{\ddagger}$	C <sub>L</sub> = 100 pF <sup>‡</sup>	25°C		56°	·	
	Gain margin	- 00	OL = 100 pl +	25°C		11		dB

<sup>†</sup> Full range is 0°C to 70°C. ‡ Referenced to 2.5 V



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# TLC2264C electrical characteristics at specified free-air temperature, $V_{DD\pm}$ = $\pm 5$ V (unless otherwise specified)

	DADAMETED	TEST COL	IDITIONS	- +	Т	LC22640	;	LINUT
	PARAMETER	TEST CON	SMOITIUMS	T <sub>A</sub> †	MIN	TYP	MAX	UNIT
VIO	Input offset voltage			25°C		300	2500	μV
VIO	input onset voltage			Full range			3000	μν
αVIO	Temperature coefficient of input offset voltage			25°C to 70°C		2		μV/°C
	Input offset voltage long-term drift (see Note 4)	$V_{IC} = 0$ , R <sub>S</sub> = 50 $\Omega$	$V_{O} = 0$ ,	25°C		0.003		μV/mo
1	Input offset current	KS = 50 12		25°C		0.5		
liO	input onset current			Full range			100	pА
lin	Input bias current	]		25°C		1		pА
ΙΒ	input bias current			Full range			100	pΑ
Vion	Common-mode input voltage range	V <sub>1O</sub>   ≤5 mV,	Rs = 50 Ω	25°C	-5 to 4	-5.3 to 4.2		<
VICR	Common-mode input voltage range	V  O   23 IIIV,	1/5 = 30 22	Full range	-5 to 3.5			V
		$I_{O} = -20 \mu\text{A}$		25°C		4.99		
		I <sub>O</sub> = -100 μA		25°C	4.85	4.94		
VOM+	Maximum positive peak output voltage	10 = 100 μΑ		Full range	4.82			V
		I <sub>O</sub> = -400 μA		25°C	4.7	4.85		
		ισ 100 μπ		Full range	4.6			
		V <sub>IC</sub> = 0,	$I_O = 50 \mu A$	25°C		-4.99		
		V <sub>IC</sub> = 0,	I <sub>O</sub> = 500 μA	25°C	-4.85	-4.91		
		-10 -3,		Full range	-4.85			
VOM-	Maximum negative peak output voltage	V <sub>IC</sub> = 0,	I <sub>O</sub> = 1 mA	25°C	-4.7	-4.8		V
				Full range	-4.7			
		V <sub>IC</sub> = 0,	I <sub>O</sub> = 4 mA	25°C	-4	-4.3		
		, ,		Full range	-3.8			
			$R_L = 50 \text{ k}\Omega$	25°C	80	200		
$A_{VD}$	Large-signal differential voltage amplification	$V_O = \pm 4 V$		Full range	55			V/mV
			$R_L = 1 M\Omega$	25°C		1000		
r <sub>i(d)</sub>	Differential input resistance			25°C		10 <sup>12</sup>		Ω
r <sub>i(c)</sub>	Common-mode input resistance			25°C		1012		Ω
<sup>C</sup> i(c)	Common-mode input capacitance	f = 10 kHz,	N package	25°C		8		pF
z <sub>O</sub>	Closed-loop output impedance	f = 100 kHz,	$A_{V} = 10$	25°C		220		Ω
CMPP	Common-mode rejection ratio	$V_{IC} = -5 \text{ V to 2}.$	7 V,	25°C	75	88		dB
CIVICK	Common-mode rejection ratio	$V_0 = 0,$	$R_S = 50 \Omega$	Full range	75			ub
ksvr	Supply-voltage rejection ratio (ΔV <sub>DD+</sub> /ΔV <sub>IO</sub> )	$V_{DD\pm} = \pm 2.2 \text{ V}$	to ±8 V,	25°C	80	95		dB
"SVK	Cappi, voltage rejection ratio (AvDD±/AvIO)	V <sub>IC</sub> = 0,	No load	Full range	80			GD.
IDD	Supply current (four amplifiers)	V <sub>O</sub> = 0,	No load	25°C Full range		0.85	1	mA
‡ F. II	i- 000 t- 7000	L	-				•	

<sup>†</sup> Full range is 0°C to 70°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at  $T_A = 150$ °C extrapolated to  $T_A = 25$ °C using the Arrhenius equation and assuming an activation energy of 0.96 eV.



## TLC2264C operating characteristics at specified free-air temperature, $\rm V_{DD\pm}$ = $\pm 5~V$

	DADAMETED	TEST CONDIT	IONE	_ +	Т	LC2264C		UNIT
	PARAMETER	TEST CONDIT	IONS	T <sub>A</sub> †	MIN	TYP	MAX	UNII
		V- +4.0 V	D: 501-0	25°C	0.35	0.55		
SR	Slew rate at unity gain	$V_O = \pm 1.9 \text{ V},$ $C_L = 100 \text{ pF}$	$R_L = 50 \text{ k}\Omega$ ,	Full range	0.3			V/μs
V	Equivalent input poice voltage	f = 10 Hz		25°C		43		->///\/\ <del>-</del>
۷ <sub>n</sub>	Equivalent input noise voltage	f = 1 kHz		25°C		12		nV/√Hz
\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\	Peak-to-peak equivalent input noise	f = 0.1 Hz to 1 Hz		25°C		0.8		μV
VN(PP)	voltage	f = 0.1 Hz to 10 Hz		25°C		1.3		μν
In	Equivalent input noise current			25°C		0.6		fA/√Hz
THD + N	Total harmonic distortion plus noise	$V_0 = \pm 2.3 \text{ V},$ f = 20  kHz,	A <sub>V</sub> = 1	25°C		0.014%		
THE TIV	Total Harmonic distortion plus hoise	$R_L = 50 \text{ k}\Omega$	A <sub>V</sub> = 10	20 0		0.024%		
	Gain-bandwidth product	f = 10 kHz, C <sub>L</sub> = 100 pF	$R_L = 50 \text{ k}\Omega$ ,	25°C		0.73		MHz
ВОМ	Maximum output-swing bandwidth	$V_{O(PP)} = 4.6 \text{ V},$ $R_{L} = 50 \text{ k}\Omega,$	A <sub>V</sub> = 1, C <sub>L</sub> = 100 pF	25°C		70		kHz
	Settling time	$A_V = -1$ , Step = -2.3 V to 2.3 V,	To 0.1%	25°C		7.1		μs
t <sub>S</sub>	Columny affic	$R_L = 50 \text{ k}\Omega$ , $C_L = 100 \text{ pF}$	To 0.01%	23 0		16.5		μο
φm	Phase margin at unity gain	$R_L = 50 \text{ k}\Omega$	C <sub>I</sub> = 100 pF	25°C		57°		
	Gain margin	T IN L = 50 K22,	CL = 100 <b>p</b> F	25°C		11		dB

<sup>†</sup>Full range is 0°C to 70°C.

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# TLC2262I electrical characteristics at specified free-air temperature, $V_{DD}$ = 5 V (unless otherwise noted)

	DADAMETED	TEST CON	IDITIONS	- +	Т	LC2262	<u>!</u>	TL	.C2262	ΑI	
	PARAMETER	TEST CON	IDITIONS	T <sub>A</sub> †	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
VIO	Input offset voltage			25°C		300	2500		300	950	μV
V10	Input onset voltage			Full range			3000			1500	μν
αVIO	Temperature coefficient of input offset voltage			25°C to 85°C		2			2		μV/°C
	Input offset voltage long-term drift (see Note 4)	$V_{DD\pm} = \pm 2.5 \text{ V},$ $V_{O} = 0,$	$V_{IC} = 0$ , RS = 50 $\Omega$	25°C		0.003			0.003		μV/mo
		]		25°C		0.5			0.5		nΛ
lιO	Input offset current			85°C			150			150	pА
				Full range			800			800	pА
		1		25°C		1			1		pА
lΒ	Input bias current			85°C			150			150	pА
				Full range			800			800	pА
VICR	Common-mode input	$R_S = 50 \Omega$ ,	V <sub> O</sub>   ≤5 mV	25°C	0 to 4	-0.3 to 4.2		0 to 4	-0.3 to 4.2		٧
FIGIC	voltage range		11101=0	Full range	0 to 3.5			0 to 3.5			
		$I_{OH} = -20  \mu A$		25°C		4.99			4.99		
	High-level output	I <sub>OH</sub> = -100 μA		25°C	4.85	4.94		4.85	4.94		
VOH	voltage	- 100 μ/τ		Full range	4.82			4.82			V
	· ·	I <sub>OH</sub> = -400 μA		25°C	4.7	4.85		4.7	4.85		
				Full range	4.5			4.5			
		$V_{IC} = 2.5 V,$	I <sub>OL</sub> = 50 μA	25°C		0.01			0.01		
	Low-level output	V <sub>IC</sub> = 2.5 V,	I <sub>OL</sub> = 500 μA	25°C		0.09	0.15		0.09	0.15	
VOL	voltage	10 - ,	<u> </u>	Full range	ļ		0.15			0.15	V
		V <sub>IC</sub> = 2.5 V,	IOL = 4 mA	25°C		0.8	1		0.7	1	
		10 - ,	,	Full range	ļ	-	1.2			1.2	
	Large-signal	V <sub>IC</sub> = 2.5 V,	$R_L = 50 \text{ k}\Omega^{\ddagger}$	25°C	80	100		80	170		
AVD	differential	$V_0 = 1 \text{ V to 4 V}$		Full range	50			50			V/mV
	voltage amplification		$R_L = 1 M\Omega^{\ddagger}$	25°C		550			550		
<sup>r</sup> i(d)	Differential input resistance			25°C		1012			1012		Ω
r <sub>i(c)</sub>	Common-mode input resistance			25°C		1012			1012		Ω
<sup>C</sup> i(c)	Common-mode input capacitance	f = 10 kHz,	P package	25°C		8			8		pF
z <sub>O</sub>	Closed-loop output impedance	f = 100 kHz,	A <sub>V</sub> = 10	25°C		240			240		Ω
CMPP	Common-mode	$V_{IC} = 0 \text{ to } 2.7 \text{ V},$	V <sub>O</sub> = 2.5 V,	25°C	70	83		70	83		40
CMRR	rejection ratio	$R_S = 50 \Omega$		Full range	70			70			dB

<sup>†</sup> Full range is – 40°C to 125°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at  $T_A = 150$ °C extrapolated to  $T_A = 25$ °C using the Arrhenius equation and assuming an activation energy of 0.96 eV.



<sup>‡</sup>Referenced to 2.5 V

## TLC2262I operating characteristics at specified free-air temperature, $V_{DD} = 5 \text{ V}$

	ADAMETED	TEST CONDI	TIONS	- +		TLC2262	ı	1	LC2262	AI .	UNIT
P	ARAMETER	TEST CONDI	IIONS	T <sub>A</sub> †	MIN	TYP	MAX	MIN	TYP	MAX	UNII
	Supply-voltage re-	V <sub>DD</sub> = 4.4 V to 16 V,		25°C	80	95		80	95		
k <sub>SVR</sub>	jection ratio $(\Delta V_{DD}/\Delta V_{IO})$	$V_{IC} = V_{DD}/2$ ,	No load	Full range	80			80			dB
				25°C		400	500		400	500	
I <sub>DD</sub>	Supply current	$V_0 = 2.5 V,$	No load	Full range			500			500	μΑ
	Clow rate at unity	V <sub>O</sub> = 1.5 V to 3.5 V,	D. FOROT	25°C	0.35	0.55		0.35	0.55		
SR	Slew rate at unity gain	$C_L = 100 \text{ pF}^{\ddagger}$	$R_L = 50 \text{ k}\Omega^{\ddagger}$ ,	Full range	0.25			0.25			V/μs
V	Equivalent input	f = 10 Hz		25°C		40			40		nV/√ <del>Hz</del>
V <sub>n</sub>	noise voltage	f = 1 kHz		25°C		12			12		nv/√Hz
M	Peak-to-peak	f = 0.1 Hz to 1 Hz		25°C		0.7			0.7		\/
V <sub>N(PP)</sub>	equivalent input noise voltage	f = 0.1 Hz to 10 Hz		25°C		1.3			1.3		μV
In	Equivalent input noise current			25°C		0.6			0.6		fA√Hz
THD + N	Total harmonic	$V_O = 0.5 \text{ V to } 2.5 \text{ V},$ f = 20 kHz.	A <sub>V</sub> = 1	25°C		0.017%			0.017%		
I I D + N	distortion plus noise	$R_L = 50 \text{ k}\Omega^{\ddagger}$	A <sub>V</sub> = 10	25 C		0.03%			0.03%		
	Gain-bandwidth product	f = 50  kHz, $C_L = 100 \text{ pF}^{\ddagger}$	$R_L = 50 \text{ k}\Omega^{\ddagger}$ ,	25°C		0.82			0.82		MHz
ВОМ	Maximum output- swing bandwidth	$V_{O(PP)} = 2 \text{ V},$ $R_{L} = 50 \text{ k}\Omega^{\ddagger},$	$A_V = 1,$ $C_L = 100 \text{ pF}^{\ddagger}$	25°C		185			185		kHz
t <sub>S</sub>	Settling time	$A_V = -1$ , Step = 0.5 V to 2.5 V,	To 0.1%	25°C		6.4			6.4		μs
'S	Octuing title	$R_L = 50 \text{ k}\Omega^{\ddagger},$ $C_L = 100 \text{ pF}^{\ddagger}$	To 0.01%	200		14.1			14.1		μδ
φm	Phase margin at unity gain	R <sub>L</sub> = 50 kΩ <sup>‡</sup> ,	C <sub>L</sub> = 100 pF <sup>‡</sup>	25°C		56°			56°		
	Gain margin		-	25°C		11			11		dB

<sup>†</sup> Full range is – 40°C to 125°C.

<sup>‡</sup>Referenced to 2.5 V

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# TLC2262I electrical characteristics at specified free-air temperature, $V_{DD\pm}$ = $\pm 5$ V (unless otherwise noted)

	PARAMETER	TEST C	ONDITIONS	T. †	1	LC2262		T	LC2262A	NI	
	PARAMETER	IESI C	SNOTTIONS	T <sub>A</sub> †	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
\/	Input offeet voltage			25°C		300	2500		300	950	μV
VIO	Input offset voltage			Full range			3000			1500	μν
αΛΙΟ	Temperature coefficient of input offset voltage			25°C to 85°C		2			2		μV/°C
	Input offset voltage long-term drift (see Note 4)		V <sub>O</sub> = 0	25°C		0.003			0.003		μV/mo
		$R_S = 50 \Omega$		25°C		0.5			0.5		pА
lιO	Input offset current			85°C			150			150	pА
				Full range			800			800	pА
		1		25°C		1			1		pА
lΒ	Input bias current			85°C			150			150	pА
				Full range			800			800	pА
V:	Common-mode input	D- 50.0	1\/: =1 < F m) /	25°C	-5 to 4	-5.3 to 4.2		-5 to 4	-5.3 to 4.2		V
VICR	voltage range	KS = 50 12,	V <sub>IO</sub>   ≤5 mV	Full range	-5 to 3.5			-5 to 3.5			V
		$I_{O} = -20  \mu A$		25°C		4.99			4.99		
		1- 400	Δ.	25°C	4.85	4.94		4.85	4.94		
V <sub>OM+</sub>	Maximum positive peak output voltage	$I_{O} = -100 \mu$	A	Full range	4.82			4.82			٧
	output voltage	1 400	Δ.	25°C	4.7	4.85		4.7	4.85		
		$I_{O} = -400 \mu$	A	Full range	4.5			4.5			
		V <sub>IC</sub> = 0,	I <sub>O</sub> = 50 μA	25°C		-4.99			-4.99		
		V 0	I- 500 ·· A	25°C	-4.85	-4.91		-4.85	-4.91		
V <sub>OM</sub> -	Maximum negative peak output voltage	$V_{IC} = 0$ ,	$I_{O} = 500  \mu A$	Full range	-4.85			-4.85			V
	output voltage	\/ O	1- 4	25°C	-4	-4.3		-4	-4.3		
		VIC = 0,	$I_O = 4 \text{ mA}$	Full range	-3.8			-3.8			
			D. 50 kg	25°C	80	200		80	200		
$A_{VD}$	Large-signal differential voltage amplification	V <sub>O</sub> = ±4 V	$R_L = 50 \text{ k}\Omega$	Full range	50			50			V/mV
	voltago amplinoation		$R_L = 1 M\Omega$	25°C		1000			1000		
r <sub>i(d)</sub>	Differential input resistance			25°C		1012			1012		Ω
r <sub>i(c)</sub>	Common-mode input resistance			25°C		10 <sup>12</sup>			10 <sup>12</sup>		Ω
<sup>C</sup> i(c)	Common-mode input capacitance	f = 10 kHz,	P package	25°C		8			8		pF
z <sub>o</sub>	Closed-loop output impedance	f = 100 kHz,	A <sub>V</sub> = 10	25°C		220			220		Ω
CMRR	Common-mode	V <sub>IC</sub> = −5 V t	o 2.7 V,	25°C	75	88		75	88		٩D
CIVIKK	rejection ratio	$V_{O} = 0,$	$R_S = 50 \Omega$	Full range	75			75			dB
ka. :-	Supply-voltage rejection	V <sub>DD</sub> = 4.4 V	to 16 V,	25°C	80	95		80	95		40
ksvr	ratio (ΔV <sub>DD±</sub> /ΔV <sub>IO</sub> )	VIC = V <sub>DD</sub> /2		Full range	80			80			dB

<sup>†</sup> Full range is – 40°C to 125°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at  $T_A = 150^{\circ}C$  extrapolated to  $T_A = 25^{\circ}C$  using the Arrhenius equation and assuming an activation energy of 0.96 eV.



## TLC2262I operating characteristics at specified free-air temperature, $\rm V_{DD\pm}$ = $\pm 5~V$

	A D A METED	TEST SONDITI	IONO	- +		TLC2262	I	Т	LC2262	AI .	
1	ARAMETER	TEST CONDITI	IONS	T <sub>A</sub> †	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
				25°C		425	500		425	500	
I <sub>DD</sub>	Supply Current	$V_0 = 2.5 V,$	No load	Full range			500			500	
	Class rate at units	V- 14.0 V	D: 5010	25°C	0.35	0.55		0.35	0.55		
SR	Slew rate at unity gain	$V_O = \pm 1.9 \text{ V},$ $C_L = 100 \text{ pF}$	$R_L = 50 \text{ k}\Omega$ ,	Full range	0.25			0.25			V/μs
V	Equivalent input	f = 10 Hz		25°C		43			43		->4/10=
Vn	noise voltage	f = 1 kHz		25°C		12			12		nV/√Hz
V <sub>N(PP)</sub>	Peak-to-peak equivalent input	f = 0.1 Hz to 1 Hz		25°C		0.8			0.8		μV
VN(PP)	noise voltage	f = 0.1 Hz to 10 Hz		25°C		1.3			1.3		μν
In	Equivalent input noise current			25°C		0.6			0.6		fA√Hz
THD + N	Total harmonic	$V_0 = \pm 2.3 \text{ V},$	A <sub>V</sub> = 1	25°C		0.014%			0.014%		
I I D + N	distortion plus noise	$R_L = 50 \text{ k}\Omega,$ f = 20 kHz	A <sub>V</sub> = 10	25 C		0.024%			0.024%		
	Gain-bandwidth product	f =10 kHz, C <sub>L</sub> = 100 pF	$R_L = 50 \text{ k}\Omega$ ,	25°C		0.73			0.73		MHz
ВОМ	Maximum output-swing bandwidth	V <sub>O</sub> (PP) = 4.6 V, R <sub>L</sub> = 50 kΩ,	A <sub>V</sub> = 1, C <sub>L</sub> = 100 pF	25°C		85			85		kHz
+_	Settling time	$A_V = -1$ , Step = -2.3 V to 2.3 V,	To 0.1%	25°C		7.1			7.1		116
t <sub>S</sub>	Octaining time	$R_L$ = 50 kΩ, $C_L$ = 100 pF	To 0.01%	23 0		16.5			16.5		μ\$
φm	Phase margin at unity gain	$R_L = 50 \text{ k}\Omega$ ,	C <sub>L</sub> = 100 pF	25°C		57°			57°		
	Gain margin			25°C		11			11		dB

<sup>†</sup> Full range is –40°C to 125°C.

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# TLC2264I electrical characteristics at specified free-air temperature, $V_{DD} = 5 \text{ V}$ (unless otherwise noted)

	PARAMETER	TEST CON	DITIONS		Т	LC2264	H	TL	.C2264	ΑI	UNIT
	TANAMETER	1E31 CON	DITIONS	T <sub>A</sub> †	MIN	TYP	MAX	MIN	TYP	MAX	UNII
VIO	Input offset voltage			25°C		300	2500		300	950	μV
10				Full range			3000			1500	μ
αΛΙΟ	Temperature coefficient of input offset voltage			25°C to 125°C		2			2		μV/°C
	Input offset voltage long-term drift (see Note 4)	V <sub>DD±</sub> =±2.5 V,	V10 = 0	25°C		0.003			0.003		μV/mo
		$V_0 = 0$ ,	$R_S = 50 \Omega$	25°C		0.5			0.5		
lio	Input offset current		_	85°C			150			150	pА
				Full range			800			800	
		1		25°C		1			1		
lΒ	Input bias current			85°C			150			150	pА
				Full range			800			800	
					0	-0.3		0	-0.3		
				25°C	to 4	to		to 4	to		
VICR	Common-mode input voltage range	$R_S = 50 \Omega$ ,	$ V_{IO}  \le 5 \text{ mV}$		0	4.2			4.2		V
	voltage range			Full range	to			0 to			
				i un rungo	3.5			3.5			
		I <sub>OH</sub> = -20 μA		25°C		4.99			4.99		
				25°C	4.85	4.94		4.85	4.94		
Vон	High-level output	IOH = -100 μA		Full range	4.82			4.82	,		V
	voltage	400 4		25°C	4.7	4.85		4.7	4.85		
		ΙΟΗ = -400 μΑ		Full range	4.5			4.5			
		V <sub>IC</sub> = 2.5 V,	I <sub>OL</sub> = 50 μA	25°C		0.01			0.01		
		V 0.5.V	I 500 ·· A	25°C		0.09	0.15		0.09	0.15	
VOL	Low-level output voltage	$V_{IC} = 2.5 \text{ V},$	$I_{OL} = 500 \mu\text{A}$	Full range			0.15			0.15	V
	voltage	V 2.5.V	Ισ. 4 m Λ	25°C		0.8	1		0.7	1	
		V <sub>IC</sub> = 2.5 V,	IOL = 4 mA	Full range			1.2			1.2	
	Lorge signal differential	V 2.5.V	$R_L = 50 \text{ k}\Omega^{\ddagger}$	25°C	80	100		80	170		
$A_{VD}$	Large-signal differential voltage amplification	$V_{IC} = 2.5 \text{ V},$ $V_{O} = 1 \text{ V to 4 V}$	K[ = 50 K22+	Full range	50			50			V/mV
			$R_L = 1 M\Omega^{\ddagger}$	25°C		550			550		
r <sub>i(d)</sub>	Differential input resistance			25°C		10 <sup>12</sup>			10 <sup>12</sup>		Ω
r <sub>i(c)</sub>	Common-mode input resistance			25°C		1012			1012		Ω
<sup>C</sup> i(c)	Common-mode input capacitance	f = 10 kHz,	N package	25°C		8			8		pF
z <sub>O</sub>	Closed-loop output impedance	f = 100 kHz,	A <sub>V</sub> = 10	25°C		240			240		Ω
OMES	Common-mode	$V_{IC} = 0 \text{ to } 2.7 \text{ V},$	V <sub>O</sub> = 2.5 V,	25°C	70	83		70	83		<u>.</u>
CMRR	rejection ratio	$R_S = 50 \Omega$	,	Full range	70			70			dB
keve	Supply-voltage rejection ratio	V <sub>DD</sub> = 4.4 V to 16	6 V,	25°C	80	95		80	95		dB
ksvr	$(\Delta V_{DD}/\Delta V_{IO})$	$V_{IC} = V_{DD}/2$ ,	No load	Full range	80			80			ub

<sup>†</sup> Full range is – 40°C to 125°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at  $T_A = 150$ °C extrapolated to  $T_A = 25$ °C using the Arrhenius equation and assuming an activation energy of 0.96 eV.



<sup>‡</sup>Referenced to 2.5 V

## TLC2264I operating characteristics at specified free-air temperature, $V_{DD} = 5 \text{ V}$

	RAMETER	TECT CONDI	TIONS	_ +		TLC2264I		Τι	_C2264AI		UNIT
	RAMETER	TEST CONDI	IIONS	T <sub>A</sub> †	MIN	TYP	MAX	MIN	TYP	MAX	UNII
	Supply current			25°C		0.8	1		0.8	1	
I <sub>DD</sub>	(four amplifiers)	$V_0 = 2.5 V,$	No load	Full range			1			1	V/μs
	Class nata at smits	V 4.4.V.15.0.0.V	p solot	25°C	0.35	0.55		0.35	0.55		
SR	Slew rate at unity gain	$V_O = 1.4 \text{ V to } 2.6 \text{ V},$ $C_L = 100 \text{ pF}^{\ddagger}$	$R_L = 50 \text{ k}\Omega^{\ddagger}$ ,	Full range	0.25			0.25			V/μs
\ <u></u>	Equivalent input	f = 10 Hz		25°C		40			40		nV/√ <del>Hz</del>
V <sub>n</sub>	noise voltage	f = 1 kHz		25°C		12			12		nv/√HZ
V	Peak-to-peak	f = 0.1 Hz to 1 Hz		25°C		0.7			0.7		μV
V <sub>N(PP)</sub>	equivalent input noise voltage	f = 0.1 Hz to 10 Hz		25°C		1.3			1.3		μν
In	Equivalent input noise current			25°C		0.6			0.6		fA/√ <del>Hz</del>
TUD . N	Total harmonic	$V_0 = 0.5 \text{ V to } 2.5 \text{ V},$	A <sub>V</sub> = 1	0500		0.017%			0.017%		
THD + N	distortion plus noise	f = 20 kHz, R <sub>L</sub> = 50 kΩ <sup>‡</sup>	A <sub>V</sub> = 10	25°C		0.03%			0.03%		
	Gain-bandwidth product	f = 50 kHz, C <sub>L</sub> = 100 pF‡	$R_L = 50 \text{ k}\Omega^{\ddagger}$ ,	25°C		0.71			0.71		MHz
ВОМ	Maximum output- swing bandwidth	$V_{O(PP)} = 2 \text{ V},$ $R_{L} = 50 \text{ k}\Omega^{\ddagger},$	$A_V = 1$ , $C_L = 100 \text{ pF}^{\ddagger}$	25°C		185			185		kHz
t <sub>S</sub>	Settling time	$A_V = -1$ , Step = 0.5 V to 2.5 V,	To 0.1%	25°C		6.4			6.4		μs
's	Coming time	$R_L = 50 \text{ k}\Omega^{\ddagger}$ , $C_L = 100 \text{ pF}^{\ddagger}$	To 0.01%	20 0		14.1			14.1		μο
φm	Phase margin at unity gain	$R_L = 50 \text{ k}\Omega^{\ddagger}$ ,	C <sub>L</sub> = 100 pF‡	25°C		56°			56°		
	Gain margin			25°C		11			11		dB

<sup>†</sup> Full range is – 40°C to 125°C.

<sup>‡</sup>Referenced to 2.5 V

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# TLC2264I electrical characteristics at specified free-air temperature, $V_{DD\pm}$ = $\pm 5$ V (unless otherwise noted)

	PARAMETER	TEST OF	NDITIONS	T <sub>A</sub> †	T	LC2264		TI	_C2264A	d	UNIT
	PARAMETER	1231 00	PINDITIONS	'A'	MIN	TYP	MAX	MIN	TYP	MAX	UNII
\/10	Input offset voltage			25°C		300	2500		300	950	μV
VIO	input onset voltage			Full range			3000			1500	μν
αΛΙΟ	Temperature coefficient of input offset voltage			25°C to 125°C		2			2		μV/°C
	Input offset voltage long-term drift (see Note 4)	V <sub>IC</sub> = 0,	V <sub>O</sub> = 0,	25°C		0.003			0.003		μV/mo
		$R_S = 50 \Omega$		25°C		0.5			0.5		
lιο	Input offset current			85°C			150			150	pА
				Full range			800			800	
				25°C		1			1		pА
lΒ	Input bias current			85°C			150			150	pА
				Full range			800			800	pА
.,	Common-mode input	<b>D 50</b> 0	N/ 1.45 N/	25°C	-5 to 4	-5.3 to 4.2		-5 to 4	-5.3 to 4.2		.,
VICR	voltage range	$R_S = 50 \Omega$ ,	V <sub>IO</sub>   ≤5 mV	Full range	-5 to 3.5			-5 to 3.5			V
		$I_0 = -20  \mu A$		25°C		4.99			4.99		
	Mandanan a adda a a a ab	lo - 100 u/		25°C	4.85	4.94		4.85	4.94		
VOM+	Maximum positive peak output voltage	$I_{O} = -100 \mu$	`	Full range	4.82			4.82			V
	output voltago	$I_{O} = -400  \mu$ A	•	25°C	4.7	4.85		4.7	4.85		
		10 = -400 μ/	`	Full range	4.5			4.5			
		$V_{IC} = 0$ ,	$I_0 = 50  \mu A$	25°C		-4.99			-4.99		
	Maximum negative peak	V <sub>IC</sub> = 0,	I <sub>O</sub> = 500 μA	25°C	-4.85	-4.91		-4.85	-4.91		
VOM-	output voltage	VIC = 0,	10 = 000 μ/ (	Full range	-4.85			-4.85	_		V
		V <sub>IC</sub> = 0,	$I_O = 4 \text{ mA}$	25°C	-4	-4.3		-4	-4.3		
		10 0,	•	Full range	-3.8			-3.8			
	Large-signal differential		$R_L = 50 \text{ k}\Omega$	25°C	80	200		80	200		
AVD	voltage amplification	$V_O = \pm 4 V$		Full range	50			50			V/mV
			$R_L = 1 M\Omega$	25°C		1000			1000		
<sup>r</sup> i(d)	Differential input resistance			25°C		10 <sup>12</sup>			10 <sup>12</sup>		Ω
ri(c)	Common-mode input resistance			25°C		1012			1012		Ω
<sup>C</sup> i(c)	Common-mode input capacitance	f = 10 kHz,	N package	25°C		8			8		pF
z <sub>o</sub>	Closed-loop output impedance	f = 100 kHz,	A <sub>V</sub> = 10	25°C		220			220		Ω
CMDD	Common-mode	$V_{IC} = -5 \text{ V to}$	2.7 V,	25°C	75	88		75	88		٩D
CMRR	rejection ratio	$V_{O} = 0$ ,	$R_S = 50 \Omega$	Full range	75			75			dB
kove	Supply-voltage rejection	$V_{DD\pm} = \pm 2.2$	V to ±8 V,	25°C	80	95		80	95		٩D
ksvr	ratio ( $\Delta V_{DD\pm}/\Delta V_{IO}$ )	V <sub>IC</sub> =V <sub>DD</sub> /2,	No load	Full range	80			80			dB

<sup>†</sup> Full range is – 40°C to 125°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at  $T_A = 150$ °C extrapolated to  $T_A = 25$ °C using the Arrhenius equation and assuming an activation energy of 0.96 eV.



## TLC2264I operating characteristics at specified free-air temperature, $\rm V_{DD\pm}$ = $\pm 5~V$

	DAMETER	TEGT COMPLE	10110			TLC2264		Т	LC2264A	/I	
PA	ARAMETER	TEST CONDIT	IONS	T <sub>A</sub> †	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
	Cumply ourrant			25°C		0.85	1		0.85	1	
I <sub>DD</sub>	Supply current (four amplifiers)	$V_{O} = 0$ ,	No load	Full range			1			1	
	Olavi nata at imiti	V 14.0 V	D 501-0	25°C	0.35	0.55		0.35	0.55		
SR	Slew rate at unity gain	$V_O = \pm 1.9 \text{ V},$ $C_L = 100 \text{ pF}$	$R_L = 50 \text{ k}\Omega$ ,	Full range	0.25			0.25			V/μs
V	Equivalent input	f = 10 Hz		25°C		43			43		nV/√Hz
Vn	noise voltage	f = 1 kHz		25°C		12			12		nv/√HZ
V	Peak-to-peak	f = 0.1 Hz to 1 Hz		25°C		0.8			8.0		\/
VN(PP)	equivalent input noise voltage	f = 0.1 Hz to 10 Hz		25°C		1.3			1.3		μV
In	Equivalent input noise current			25°C		0.6			0.6		fA/√Hz
T. 10. A.	Total harmonic	$V_0 = \pm 2.3 \text{ V},$	A <sub>V</sub> = 1	0500		0.014%			0.014%		
THD + N	distortion plus noise	$R_L = 50 \text{ k}\Omega,$ f = 20 kHz	A <sub>V</sub> = 10	25°C		0.024%			0.024%		
	Gain-bandwidth product	f =10 kHz, C <sub>L</sub> = 100 pF	$R_L = 50 \text{ k}\Omega$ ,	25°C		0.73			0.73		MHz
ВОМ	Maximum output- swing bandwidth	$V_{O(PP)} = 4.6 \text{ V},$ $R_{L} = 50 \text{ k}\Omega,$	Ay = 1, C <sub>L</sub> = 100 pF	25°C		70			70		kHz
t <sub>s</sub>	Settling time	$A_V = -1$ , Step = -2.3 V to 2.3 V,	To 0.1%	25°C		7.1			7.1		μs
·S		$R_L = 50 \text{ k}\Omega$ , $C_L = 100 \text{ pF}$	To 0.01%	200		16.5			16.5		μο
φm	Phase margin at unity gain	$R_L = 50 \text{ k}\Omega$	C <sub>L</sub> = 100 pF	25°C		57°			57°		
	Gain margin	]		25°C		11			11		dB

<sup>†</sup>Full range is –40°C to 125°C.

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# TLC2262Q/M electrical characteristics at specified free-air temperature, $V_{DD}$ = 5 V (unless otherwise noted)

	PARAMETER	TEST CON	IDITIONS	T <sub>A</sub> †		LC22620 LC2262			C2262A .C2262A		UNIT
				^	MIN	TYP	MAX	MIN	TYP	MAX	
\/.a	Input offset voltage			25°C		300	2500		300	950	μV
VIO	input onset voltage	]		Full range			3000			1500	μν
αVIO	Temperature coefficient of input offset voltage			Full range		5			5		μV/°C
	Input offset voltage long-term drift (see Note 4)	$V_{DD\pm} = \pm 2.5 \text{ V},$ $V_{O} = 0,$	$V_{IC} = 0$ , RS = 50 $\Omega$	25°C		0.003			0.003		μV/mo
110	Input offset current			25°C		0.5			0.5		pА
.10	- Input onoct ourront			125°C			800			800	P''
I <sub>IB</sub>	Input bias current			25°C		1			1		pА
10				125°C			800			800	F
VICR	Common-mode input	$R_S = 50 \Omega$ ,	V <sub> O</sub>   ≤5 mV	25°C	0 to 4	-0.3 to 4.2		0 to 4	-0.3 to 4.2		V
VICK	voltage range	113 - 30 32,	V  O   = 3 111V	Full range	0 to 3.5			0 to 3.5			V
		I <sub>OH</sub> = -20 μA		25°C		4.99			4.99		
	I Pak Javal autaut	ΙΟΗ = -100 μΑ		25°C	4.85	4.94		4.85	4.94		
Vон	High-level output voltage	ΙΟΗ = – 100 μΑ		Full range	4.82			4.82			V
	voltage	I <sub>OH</sub> = -400 μA		25°C	4.7	4.85		4.7	4.85		
		ΙΟΗ = -400 μΑ		Full range	4.5			4.5			
		$V_{IC} = 2.5 V$ ,	I <sub>OL</sub> = 50 μA	25°C		0.01			0.01		
	Low-level output	V <sub>IC</sub> = 2.5 V,	I <sub>OL</sub> = 500 μA	25°C		0.09	0.15		0.09	0.15	
VOL	voltage	VIC - 2.0 V,	-10L = 000 μ/τ	Full range			0.15			0.15	V
	ŭ	V <sub>IC</sub> = 2.5 V,	$I_{OL} = 4 \text{ mA}$	25°C		8.0	1		0.7	1	
		10 =10 1,		Full range			1.2			1.2	
	Large-signal differential	V <sub>IC</sub> = 2.5 V,	$R_L = 50 \text{ k}\Omega^{\ddagger}$	25°C	80	100		80	170		
AVD	voltage amplification	$V_0 = 1 \text{ V to 4 V}$		Full range	50			50			V/mV
		Ŭ	$R_L = 1 M\Omega^{\ddagger}$	25°C		550			550		
<sup>r</sup> i(d)	Differential input resistance			25°C		10 <sup>12</sup>			10 <sup>12</sup>		Ω
r <sub>i(c)</sub>	Common-mode input resistance			25°C		10 <sup>12</sup>			10 <sup>12</sup>		Ω
c <sub>i(c)</sub>	Common-mode input capacitance	f = 10 kHz,	P package	25°C		8			8		pF
z <sub>O</sub>	Closed-loop output impedance	f = 100 kHz,	A <sub>V</sub> = 10	25°C		240			240		Ω
CMRR	Common-mode	$V_{IC} = 0 \text{ to } 2.7 \text{ V},$	V <sub>O</sub> = 2.5 V,	25°C	70	83		70	83		dB
CIVILLY	rejection ratio	$R_S = 50 \Omega$		Full range	70			70			ub
ksvr	Supply-voltage rejection	$V_{DD} = 4.4 \text{ V to 1}$		25°C	80	95		80	95		dB
"SVK	ratio (ΔV <sub>DD</sub> /ΔV <sub>IO</sub> )	$V_{IC} = V_{DD}/2$ ,	No load	Full range	80			80			
I <sub>DD</sub>	Supply current	V <sub>O</sub> = 2.5 V,	No load	25°C		400	500		400	500	μΑ
		] === .,		Full range			500			500	F

<sup>†</sup> Full range is –40°C to 125°C for Q suffix, – 55°C to 125°C for M suffix.

NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at  $T_A = 150$ °C extrapolated to  $T_A = 25$ °C using the Arrhenius equation and assuming an activation energy of 0.96 eV.



<sup>‡</sup>Referenced to 2.5 V

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### TLC2262Q/M operating characteristics at specified free-air temperature, $V_{DD} = 5 \text{ V}$

P.	ARAMETER	TEST CONDI	TIONS	T <sub>A</sub> †		LC22620 LC22621			.C2262A .C2262A		UNIT
				,	MIN	TYP	MAX	MIN	TYP	MAX	
	Claw rate at unity	$V_{O} = 0.5 \text{ V to } 3.5 \text{ V},$	$R_1 = 50 \text{ k}\Omega^{\ddagger}$	25°C	0.35	0.55		0.35	0.55		
SR	Slew rate at unity gain	$C_L = 100 \text{ pF}^{\ddagger}$	K[ = 50 K22+,	Full range	0.25			0.25			V/μs
	Equivalent input	f = 10 Hz		25°C		40			40		nV/√ <del>Hz</del>
٧ <sub>n</sub>	noise voltage	f = 1 kHz		25°C		12			12		IIV/√⊓Z
\\=\	Peak-to-peak	f = 0.1 Hz to 1 Hz		25°C		0.7			0.7		/
VN(PP)	equivalent input noise voltage	f = 0.1 Hz to 10 Hz		25°C		1.3			1.3		μV
In	Equivalent input noise current			25°C		0.6			0.6		fA√ <del>Hz</del>
THD + N	Total harmonic	$V_0 = 0.5 \text{ V to } 2.5 \text{ V},$	A <sub>V</sub> = 1	25°C		0.017%			0.017%		
I I HD + N	distortion plus noise	f = 20 kHz, R <sub>L</sub> = 50 kΩ <sup>‡</sup>	A <sub>V</sub> = 10	25°C		0.03%			0.03%		
	Gain-bandwidth product	f = 50 kHz, C <sub>L</sub> = 100 pF‡	$R_L = 50 \text{ k}\Omega^{\ddagger}$ ,	25°C		0.82			0.82		MHz
ВОМ	Maximum output- swing bandwidth	$V_{O(PP)} = 2 \text{ V},$ $R_L = 50 \text{ k}\Omega^{\ddagger},$	$A_V = 1,$ $C_L = 100 \text{ pF}^{\ddagger}$	25°C		185			185		kHz
t <sub>S</sub>	Settling time	$A_V = -1$ , Step = 0.5 V to 2.5 V,	To 0.1%	25°C		6.4			6.4		μs
.5		$R_L = 50 \text{ k}\Omega^{\ddagger}$ , $C_L = 100 \text{ pF}^{\ddagger}$	To 0.01%			14.1			14.1		μο
φm	Phase margin at unity gain	$R_L = 50 \text{ k}\Omega^{\ddagger}$ ,	C <sub>L</sub> = 100 pF‡	25°C		56°			56°		
	Gain margin			25°C		11			11		dB

<sup>†</sup> Full range is -40°C to 125°C for Q suffix, -55°C to 125°C for M suffix.

<sup>‡</sup>Referenced to 2.5 V

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# TLC2262Q/M electrical characteristics at specified free-air temperature, $V_{DD\pm}$ = $\pm 5$ V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T <sub>A</sub> †	TLC2262Q, TLC2262M			TLC2262AQ, TLC2262AM			UNIT		
					MIN	TYP	MAX	MIN	TYP	MAX			
VIO	Input offset voltage			25°C		300	2500		300	950	μV		
VIO	Input onset voltage	]		Full range			3000			1500	μν		
ανιο	Temperature coefficient of input offset voltage			Full range		5			5		μV/°C		
	Input offset voltage long- term drift (see Note 4)	V <sub>IC</sub> = 0, R <sub>S</sub> = 50 Ω	$V_{O} = 0$ ,	25°C		0.003			0.003		μV/mo		
IIO	Input offset current			25°C		0.5			0.5		pА		
10	input onset current			125°C			800			800	PΛ		
I <sub>IB</sub>	Input bias current			25°C		1			1		pА		
ΊΒ	mput biao ourrent			125°C			800			800	P/\		
VICR	Common-mode input	Rs = 50 Ω,	V <b> </b> O  ≤ 5 mV	25°C	-5 to 4	-5.3 to 4		-5 to 4	-5.3 to 4.2		V		
TICK	voltage range	115 = 00 22,	14101 = 0 1114	Full range	-5 to 3.5			-5 to 3.5			٧		
		$I_0 = -20 \mu\text{A}$		25°C		4.99			4.99				
	Maximum positivo pook	I <sub>O</sub> = -100 μA		25°C	4.85	4.94		4.85	4.94				
VOM+	Maximum positive peak output voltage	10 = -100 μΑ		Full range	4.82			4.82			V		
	output romago	I <sub>O</sub> = -400 μA		25°C	4.7	4.85		4.7	4.85				
		10 = -400 μΑ		Full range	4.5			4.5					
		$V_{IC} = 0$ ,	$I_0 = 50 \mu A$	25°C		-4.99			-4.99		V		
	Maximum negative peak	V <sub>IC</sub> = 0,	I <sub>O</sub> = 500 μA	25°C	-4.85	-4.91		-4.85	-4.91				
VOM-	output voltage	VIC = 0,	10 = σσσ μ.τ	Full range	-4.85			-4.85					
	, ,	V <sub>IC</sub> = 0,	Io = 4 mA	Io = 4 mA	$I_{C} = 0$ , $I_{O} = 4 \text{ mA}$	25°C	-4	-4.3		-4	-4.3		
		10 3,		Full range	-3.8	-		-3.8					
	Large-signal differential		R <sub>L</sub> = 50 kΩ	25°C	80	200		80	200				
AVD	voltage amplification	$V_O = \pm 4 V$		Full range	50			50			V/mV		
			$R_L = 1 M\Omega$	25°C		1000			1000				
<sup>r</sup> i(d)	Differential input resistance			25°C		1012			1012		Ω		
ri(c)	Common-mode input resistance			25°C		10 <sup>12</sup>			1012		Ω		
c <sub>i(c)</sub>	Common-mode input capacitance	f = 10 kHz,	P package	25°C		8			8		pF		
z <sub>O</sub>	Closed-loop output impedance	f = 100 kHz,	A <sub>V</sub> = 10	25°C		220			220		Ω		
OMBB	Common-mode	$V_{IC} = -5 \text{ V to}$		25°C	75	88		75	88		4D		
CMRR	rejection ratio	$V_{O} = 0$ ,	$R_S = 50 \Omega$	Full range	75			75	-		dB		
ka. :-	Supply-voltage rejection	V <sub>DD</sub> = 4.4 V t	o 16 V,	25°C	80	95		80	95		4D		
ksvr	ratio ( $\Delta V_{DD\pm}/\Delta V_{IO}$ )	$V_{IC} = V_{DD}/2$	No load	Full range	80			80			dB		
Inn	Supply current	Vo = 0	No load	25°C		425	500		425	500	0		
IDD	Supply current	V <sub>O</sub> = 0,	INU IUaU	Full range			500			500	μΑ		

<sup>†</sup> Full range is –40°C to 125°C for Q suffix, – 55°C to 125°C for M suffix.



NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at  $T_A = 150$ °C extrapolated to  $T_A = 25$ °C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

## TLC2262Q/M operating characteristics at specified free-air temperature, $\rm V_{DD\pm}$ = $\pm 5~V$

PARAMETER		TEST CONDITI	T <sub>A</sub> †	TLC2262Q, TLC2262M			TLC2262AQ, TLC2262AM			UNIT	
				,	MIN	TYP	MAX	MIN	TYP	MAX	
	Slew rate at unity	$V_{O} = \pm 2 V$	$R_1 = 50 \text{ k}\Omega$	25°C	0.35	0.55		0.35	0.55		
SR	gain	$C_L = 100 \text{ pF}$	K[ = 50 K22,	Full range	0.25			0.25			V/μs
٧ <sub>n</sub>	Equivalent input	f = 10 Hz	) Hz 2			43			43		nV/√Hz
٧n	noise voltage	f = 1 kHz		25°C		12			12		IIV/∀⊓Z
\/ = = .	Peak-to-peak	f = 0.1 Hz to 1 Hz		25°C		0.8			0.8		\/
V <sub>N(PP)</sub>	equivalent input noise voltage	f = 0.1 Hz to 10 Hz		25°C		1.3			1.3		μV
In	Equivalent input noise current			25°C		0.6			0.6		fA√Hz
THD + N	Total harmonic	$V_0 = \pm 2.3 \text{ V},$	A <sub>V</sub> = 1	25°C		0.014%			0.014%		
I HD + N	distortion plus noise	$R_L = 50 \text{ k}\Omega,$ f = 20  kHz	A <sub>V</sub> = 10	25°C		0.024%			0.024%		
	Gain-bandwidth product	f =10 kHz, C <sub>L</sub> = 100 pF	$R_L = 50 \text{ k}\Omega$ ,	25°C		0.73			0.73		MHz
ВОМ	Maximum output- swing bandwidth	$V_{O(PP)} = 4.6 \text{ V},$ $R_{L} = 50 \text{ k}\Omega,$	A <sub>V</sub> = 1, C <sub>L</sub> = 100 pF	25°C		85			85		kHz
t <sub>S</sub>	Settling time	$A_V = -1$ , Step = -2.3 V to 2.3 V,	To 0.1%	25°C		7.1			7.1		μs
'S	Octaing time	$R_L = 50 \text{ k}\Omega$ , $C_L = 100 \text{ pF}$	To 0.01%	23 0		16.5			16.5		μο
φm	Phase margin at unity gain	R <sub>L</sub> = 50 kΩ,	C <sub>L</sub> = 100 pF	25°C		57°			57°		
	Gain margin			25°C		11			11		dB

<sup>†</sup> Full range is –40°C to 125°C for Q suffix, – 55°C to 125°C for M suffix.

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# TLC2264Q/M electrical characteristics at specified free-air temperature, $V_{DD}$ = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T <sub>A</sub> †		TLC2264Q, TLC2264M		TLC2264AQ, TLC2264AM			UNIT		
					MIN	TYP	MAX	MIN	TYP	MAX			
VIO	Input offset voltage			25°C		300	2500		300	950	μV		
۷IO				Full range			3000			1500	μν		
αVIO	Temperature coefficient of input offset voltage			Full range		2			2		μV/°C		
	Input offset voltage long-term drift (see Note 4)	$V_{DD\pm} = \pm 2.5 \text{ V},$ $V_{O} = 0,$	$V_{IC} = 0$ , $R_S = 50 \Omega$	25°C		0.003			0.003		μV/mo		
110	Input offset current			25°C		0.5			0.5		pА		
10	input onoct outront			125°C		_	800			800	Ρ/ (		
I <sub>IB</sub>	Input bias current			25°C		1			1		pА		
п	mpat blad carront			125°C			800			800	Ρ, .		
,,	Common-mode input	D 500 W 145 mW	25°C	0 to 4	-0.3 to 4.2		0 to 4	-0.3 to 4.2					
VICR	voltage range	$R_S = 50 \Omega$ ,	V <sub>IO</sub>   ≤5 mV	Full range	0 to 3.5			0 to 3.5			V		
		$I_{OH} = -20  \mu A$		25°C		4.99			4.99				
Vон	High-level output voltage	Jan - 100 u A		25°C	4.85	4.94		4.85	4.94		V		
		I <sub>OH</sub> = -100 μA		Full range	4.82			4.82					
		ΙΟΗ = -400 μΑ		25°C	4.7	4.85		4.7	4.85				
				Full range	4.5			4.5					
		$V_{IC} = 2.5 \text{ V},$	I <sub>OL</sub> = 50 μA	25°C		0.01			0.01				
		V <sub>IC</sub> = 2.5 V,	I <sub>OL</sub> = 500 μA	25°C		0.09	0.15		0.09	0.15			
VOL	Low-level output voltage	V <sub>1</sub> C = 2.0 V, 1OL = 000 μ/			I <sub>OL</sub> = 4 mA	Full range			0.15			0.15	V
		V <sub>IC</sub> = 2.5 V,				25°C		0.8	1		0.7	1	
		V <sub>1</sub> C = 2.5 v,	10L = 4 111A	Full range			1.2			1.2			
	Lorgo signal differential	V: 2.5.V	$R_L = 50 \text{ k}\Omega^{\ddagger}$	25°C	80	100		80	170				
AVD	Large-signal differential voltage amplification	$V_{IC} = 2.5 \text{ V},$ $V_{O} = 1 \text{ V to 4 V}$	IVE = 30 K22+	Full range	50			50			V/mV		
	,	10	$R_L = 1 M\Omega^{\ddagger}$	25°C		550			550				
r <sub>i(d)</sub>	Differential input resistance			25°C		10 <sup>12</sup>			10 <sup>12</sup>		Ω		
r <sub>i(c)</sub>	Common-mode input resistance			25°C		1012			10 <sup>12</sup>		Ω		
c <sub>i(c)</sub>	Common-mode input capacitance	f = 10 kHz,	N package	25°C		8			8		pF		
z <sub>O</sub>	Closed-loop output impedance	f = 100 kHz,	A <sub>V</sub> = 10	25°C		240			240		Ω		
CMRR	Common-mode rejection ratio	$V_{IC} = 0 \text{ to } 2.7 \text{ V},$ RS = 50 $\Omega$	$V_0 = 2.5 \text{ V},$	25°C Full range	70 70	83		70 70	83		dB		
ksvr	Supply-voltage rejection ratio (ΔVDD/ΔVIO)	V <sub>DD</sub> = 4.4 V to 1	6 V,	25°C	80	95		80	95		dB		
<u>.                                    </u>	Supply current			25°C		0.8	1		0.8	1			
IDD	(four amplifiers)	$V_0 = 2.5 V$ ,	No load	Full range			1			1	mA		
		1											

<sup>†</sup> Full range is –40°C to 125°C for Q suffix, – 55°C to 125°C for M suffix.

NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at  $T_A = 150^{\circ}C$  extrapolated to  $T_A = 25^{\circ}C$  using the Arrhenius equation and assuming an activation energy of 0.96 eV.



<sup>‡</sup>Referenced to 2.5 V

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### TLC2264Q/M operating characteristics at specified free-air temperature, $V_{DD} = 5 \text{ V}$

PA	RAMETER	TEST CONDI	TIONS	T <sub>A</sub> †		LC2264Q LC2264N	<i>'</i>		C2264AC C2264AN	,	UNIT
				,,	MIN	TYP	MAX	MIN	TYP	MAX	
	Claus rata at units	V= 05 V to 25 V	n salat	25°C	0.35	0.55		0.35	0.55		
SR	Slew rate at unity gain	$V_O = 0.5 \text{ V to } 3.5 \text{ V},$ $C_L = 100 \text{ pF}^{\ddagger}$	$R_L = 50 \text{ k}\Omega^{\ddagger}$ ,	Full range	0.25			0.25			V/µs
V	Equivalent input	f = 10 Hz		25°C		40			40		nV/√Hz
V <sub>n</sub>	noise voltage	f = 1 kHz		25°C		12			12		110/ \\ \\ \
V	Peak-to-peak	f = 0.1 Hz to 1 Hz		25°C		0.7			0.7		μV
V <sub>N(PP)</sub>	equivalent input noise voltage	f = 0.1 Hz to 10 Hz		25°C		1.3			1.3		μν
In	Equivalent input noise current			25°C		0.6			0.6		fA/√ <del>Hz</del>
THD + N	Total harmonic	$V_O = 0.5 \text{ V to } 2.5 \text{ V},$ f = 20 kHz,	A <sub>V</sub> = 1	25°C		0.017%			0.017%		
I I I D + N	distortion plus noise	$R_L = 50 \text{ k}\Omega^{\ddagger}$	A <sub>V</sub> = 10	25 C		0.03%			0.03%		
	Gain-bandwidth product	f = 50 kHz, C <sub>L</sub> = 100 pF‡	$R_L = 50 \text{ k}\Omega^{\ddagger}$ ,	25°C		0.71			0.71		MHz
Вом	Maximum output- swing bandwidth	$V_{O(PP)} = 2 \text{ V},$ $R_{L} = 50 \text{ k}\Omega^{\ddagger},$	$A_V = 1,$ $C_L = 100 \text{ pF}^{\ddagger}$	25°C		185			185		kHz
t <sub>S</sub>	Settling time	$A_V = -1$ , Step = 0.5 V to 2.5 V,	To 0.1%	25°C		6.4			6.4		μs
		$R_L = 50 \text{ k}\Omega^{\ddagger}$ , $C_L = 100 \text{ pF}^{\ddagger}$	To 0.01%	20 0		14.1			14.1		μο
φm	Phase margin at unity gain	$R_L = 50 \text{ k}\Omega^{\ddagger}$ ,	C <sub>L</sub> = 100 pF <sup>‡</sup>	25°C		56°			56°		
	Gain margin		•	25°C		11			11		dB

<sup>†</sup> Full range is -40°C to 125°C for Q suffix, - 55°C to 125°C for M suffix. ‡ Referenced to 2.5 V

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# TLC2264Q/M electrical characteristics at specified free-air temperature, $V_{DD\pm}$ = $\pm 5$ V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T <sub>A</sub> †		C22640 C2264			C2264A C2264A		UNIT	
					MIN	TYP	MAX	MIN	TYP	MAX		
V:0	Input offset voltage			25°C		300	2500		300	950	\/	
VIO	Input offset voltage			Full range			3000			1500	μV	
αΛΙΟ	Temperature coefficient of input offset voltage			Full range		2			2		μV/°C	
	Input offset voltage long-term drift (see Note 4)	$V_{IC} = 0,$ R <sub>S</sub> = 50 $\Omega$	$V_{O} = 0$ ,	25°C		0.003			0.003		μV/mo	
	land offers and a summer to			25°C		0.5			0.5		- 4	
lio	Input offset current			125°C			800			800	pА	
	Lead Plan summed			25°C		1			1		0	
IB	Input bias current			125°C			800			800	pА	
\\.	Common-mode input	$R_S = 50 \Omega$ ,		25°C	-5 to 4	-5.3 to 4.2		-5 to 4	-5.3 to 4.2		V	
VICR	voltage range	V <sub>IO</sub>   ≤5 mV		Full range	-5 to 3.5			-5 to 3.5			V	
		$I_{O} = -20 \mu\text{A}$		25°C		4.99			4.99			
Maximum positive peak	In 100 ·· A		25°C	4.85	4.94		4.85	4.94				
	·	$I_O = -100 \mu\text{A}$		Full range	4.82			4.82			V	
	output voltage	ΙΟ = -400 μΑ		25°C	4.7	4.85		4.7	4.85			
				Full range	4.5			4.5				
		V <sub>IC</sub> = 0,	ΙΟ = 50 μΑ	25°C		-4.99			-4.99			
		V:0 - 0	I- 500 ·· A	25°C	-4.85	-4.91		-4.85	-4.91			
VOM-	Maximum negative peak output voltage	VIC = 0,	$I_{O} = 500 \mu\text{A}$	ΙΟ = 500 μΑ	Full range	-4.85			-4.85			V
	output voltago	V <sub>IC</sub> = 0,	I <sub>O</sub> = 4 mA	25°C	-4	-4.3		-4	-4.3			
		VIC = 0,	10 = 4 111A	Full range	-3.8			-3.8				
			R <sub>L</sub> = 50 kΩ	25°C	80	200		80	200			
$A_{VD}$	Large-signal differential voltage amplification	$V_O = \pm 4 V$	K[ = 50 K22	Full range	50			50			V/mV	
	ronage ampimoation		$R_L = 1 M\Omega$	25°C		1000			1000			
r <sub>i(d)</sub>	Differential input resistance			25°C		10 <sup>12</sup>			10 <sup>12</sup>		Ω	
r <sub>i(c)</sub>	Common-mode input resistance			25°C		1012			1012		Ω	
c <sub>i(c)</sub>	Common-mode input capacitance	f = 10 kHz,	N package	25°C		8			8		pF	
z <sub>o</sub>	Closed-loop output impedance	f = 100 kHz,	A <sub>V</sub> = 10	25°C		220			220		Ω	
CMRR	Common-mode	$V_{IC} = -5 \text{ V to } 2$	2.7 V,	25°C	75	88		75	88		dB	
CIVIRR	rejection ratio	V <sub>O</sub> = 0,	$R_S = 50 \Omega$	Full range	75			75			ub	
kovis	Supply-voltage rejection	$V_{DD\pm} = \pm 2.2 \text{ V}$	to ±8 V,	25°C	80	95		80	95		4D	
ksvr	ratio ( $\Delta V_{DD\pm}/\Delta V_{IO}$ )	$V_{IC} = V_{DD}/2$ ,	No load	Full range	80			80			dB	
Inc	Supply current	V <sub>O</sub> = 0,	No load	25°C		0.85	1		0.85	1	mA	
lDD	(four amplifiers)	VO = 0,	i vo ioau	Full range			1			1	111/	

<sup>†</sup> Full range is -40°C to 125°C for Q suffix, -55°C to 125°C for M suffix.

NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at  $T_A = 150^{\circ}C$  extrapolated to  $T_A = 25^{\circ}C$  using the Arrhenius equation and assuming an activation energy of 0.96 eV.



## TLC2264Q/M operating characteristics at specified free-air temperature, $V_{DD\pm}$ = $\pm5~V$

P#	ARAMETER	TEST CONDITI	IONS	T <sub>A</sub> †		LC22640 LC2264N	,		C2264A .C2264A	,	UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
	Slew rate at unity	$V_{O} = \pm 2 V$	$R_1 = 50 \text{ k}\Omega$	25°C	0.35	0.55		0.35	0.55		
SR	gain	C <sub>L</sub> = 100 pF	N_ = 50 K22,	Full range	0.25			0.25			V/μs
V <sub>n</sub>	Equivalent input	f = 10 Hz		25°C		43			43		nV/√Hz
٧n	noise voltage	f = 1 kHz		25°C		12			12		IIV/VIIZ
\\\.\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\	Peak-to-peak equivalent input	f = 0.1 Hz to 1 Hz		25°C		0.8			0.8		μV
V <sub>N(PP)</sub>	noise voltage	f = 0.1 Hz to 10 Hz		25°C		1.3			1.3		μν
In	Equivalent input noise current			25°C		0.6			0.6		fA/√Hz
THD + N	Total harmonic	$V_0 = \pm 2.3 \text{ V},$	A <sub>V</sub> = 1	25°C		0.014%			0.014%		
I HD + N	distortion plus noise	$R_L$ = 50 kΩ, f = 20 kHz	A <sub>V</sub> = 10	25°C		0.024%			0.024%		
	Gain-bandwidth product	f =10 kHz, C <sub>L</sub> = 100 pF	$R_L = 50 \text{ k}\Omega$ ,	25°C		0.73			0.73		MHz
ВОМ	Maximum output- swing bandwidth	$V_{O(PP)} = 4.6 \text{ V},$ $R_{L} = 50 \text{ k}\Omega,$	A <sub>V</sub> = 1, C <sub>L</sub> = 100 pF	25°C		70			70		kHz
t <sub>S</sub>	Settling time	$A_V = -1$ , Step = -2.3 V to 2.3 V,	To 0.1%	25°C		7.1			7.1		μs
<i>'</i> S		$R_L = 50 \text{ k}\Omega$ , $C_L = 100 \text{ pF}$	To 0.01%	200		16.5			16.5		μο
φm	Phase margin at unity gain	R <sub>L</sub> = 50 kΩ,	C <sub>L</sub> = 100 pF	25°C		57°			57°		
	Gain margin			25°C		11			11		dB

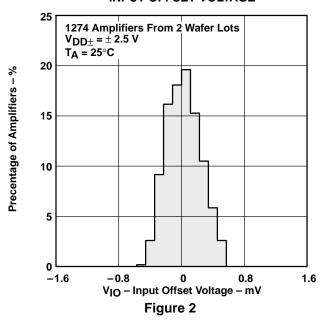
<sup>†</sup> Full range is –40°C to 125°C for Q suffix, –55°C to 125°C for M suffix.

### **Table of Graphs**

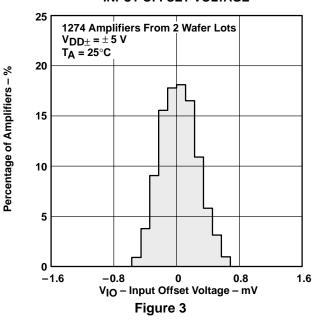
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V <sub>OM</sub> -	Maximum negative output voltage	vs Output current	19
VO(PP)	Maximum peak-to-peak output voltage	vs Frequency	20
los	Short-circuit output current	vs Supply voltage vs Free-air temperature	21 22
Vo	Output voltage	vs Differential input voltage	23, 24
	Differential gain	vs Load resistance	25
A <sub>VD</sub>	Large-signal differential voltage amplification	vs Frequency vs Free-air temperature	26, 27 28, 29
z <sub>O</sub>	Output impedance	vs Frequency	30, 31
CMRR	Common-mode rejection ratio	vs Frequency vs Free-air temperature	32 33
ksvr	Supply-voltage rejection ratio	vs Frequency vs Free-air temperature	34, 35 36
I <sub>DD</sub>	Supply current	vs Supply voltage vs Free-air temperature	37, 38 39, 40
SR	Slew rate	vs Load capacitance vs Free-air temperature	41 42
	Inverting large-signal pulse response		43, 44
	Voltage-follower large-signal pulse response		45, 46
VO	Inverting small-signal pulse response		47, 48
	Voltage-follower small-signal pulse response		49, 50
$V_n$	Equivalent input noise voltage	vs Frequency	51, 52
	Noise voltage (referred to input)	Over a 10-second period	53
	Integrated noise voltage	vs Frequency	54
THD + N	Total harmonic distortion plus noise	vs Frequency	55
	Gain-bandwidth product	vs Supply voltage vs Free-air temperature	56 57
φm	Phase margin	vs Frequency vs Load capacitance	26, 27 58
	Gain margin	vs Load capacitance	59
B <sub>1</sub>	Unity-gain bandwidth	vs Load capacitance	60
•	Overestimation of phase margin	vs Load capacitance	61



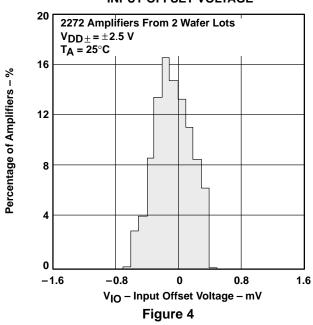
# DISTRIBUTION OF TLC2262 INPUT OFFSET VOLTAGE



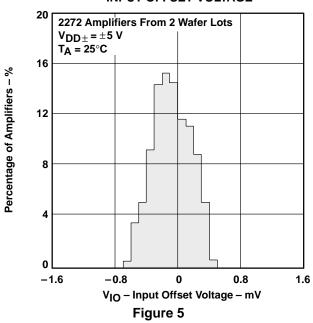
# DISTRIBUTION OF TLC2262 INPUT OFFSET VOLTAGE

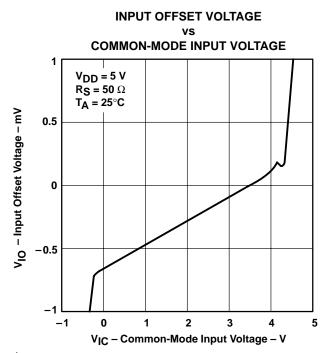


#### DISTRIBUTION OF TLC2264 INPUT OFFSET VOLTAGE



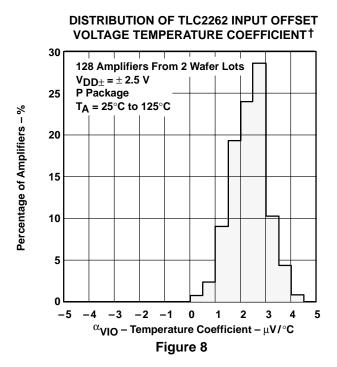
# DISTRIBUTION OF TLC2264 INPUT OFFSET VOLTAGE





 $\dagger$  For curves where  $V_{DD}$  = 5 V, all loads are referenced to 2.5 V.





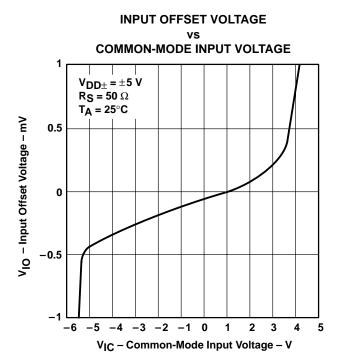
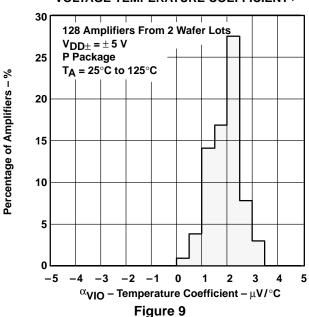


Figure 7

# DISTRIBUTION OF TLC2262 INPUT OFFSET VOLTAGE TEMPERATURE COEFFICIENT<sup>†</sup>



<sup>†</sup> Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.



**DISTRIBUTION OF TLC2264 INPUT OFFSET** 

**VOLTAGE TEMPERATURE COEFFICIENT**<sup>†</sup>

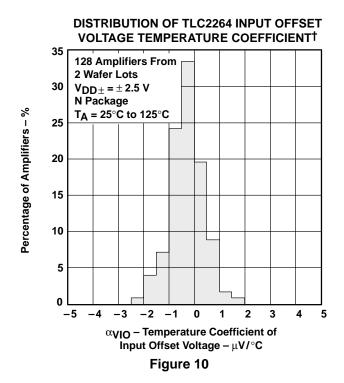
#### TYPICAL CHARACTERISTICS

35

10

5

-5 -4



### 2 Wafer Lots 30 $V_{DD\pm} = \pm 5 V$ N Package Percentage of Amplifiers – % $T_A = 25^{\circ}C$ 25 to 125°C 20 15

128 Amplifiers From

-2  $\alpha_{\mbox{VIO}}$  – Temperature Coefficient of Input Offset Voltage – μV/°C

Figure 11

#### INPUT BIAS AND INPUT OFFSET CURRENTS<sup>†</sup>

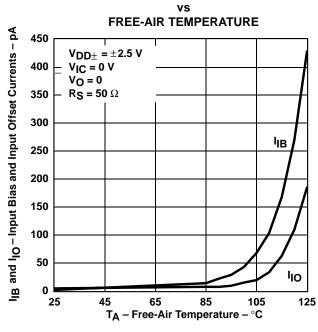


Figure 12

# **INPUT VOLTAGE RANGE**

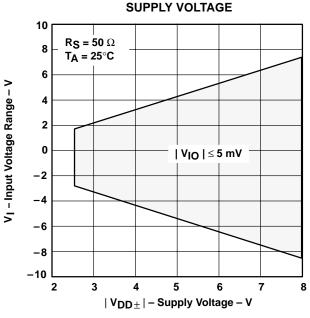
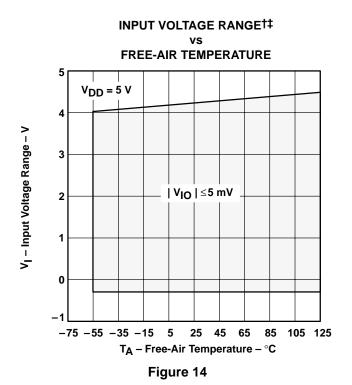
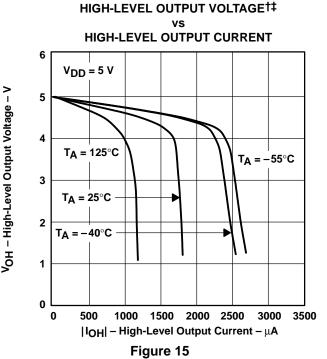


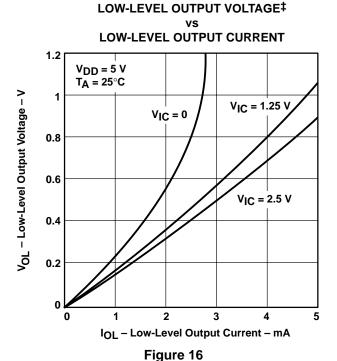
Figure 13

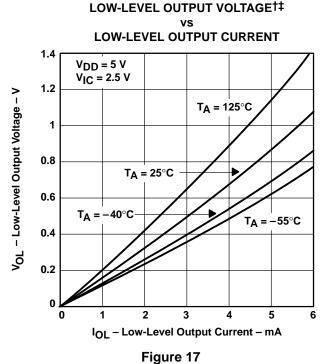
† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.







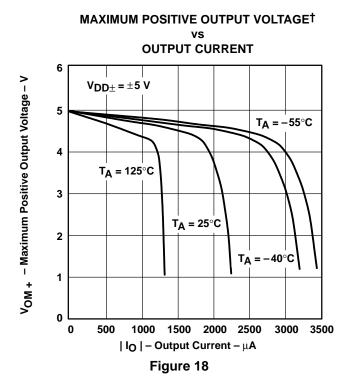


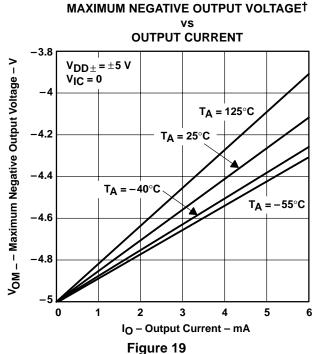


† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

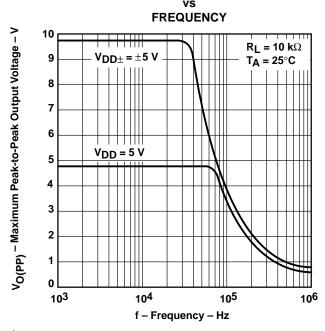
 $\ddagger$  For curves where  $V_{DD} = 5$  V, all loads are referenced to 2.5 V.

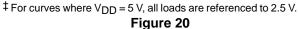






## MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE†‡





# SHORT-CIRCUIT OUTPUT CURRENT vs

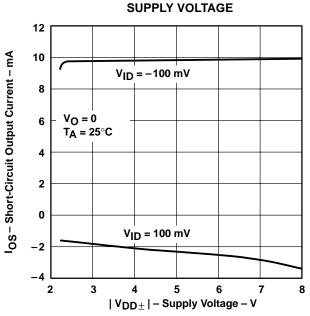
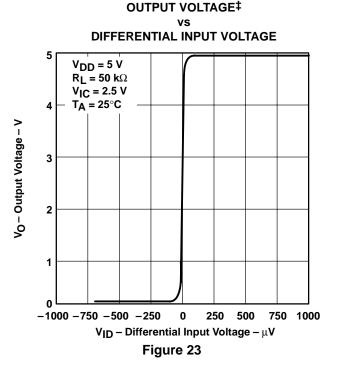


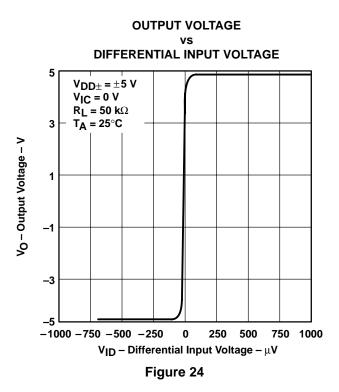
Figure 21

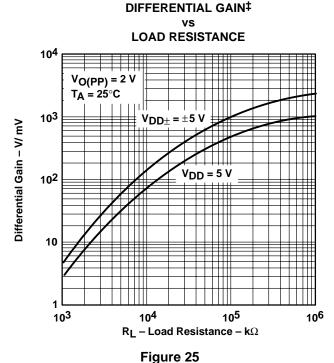
<sup>†</sup> Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.



#### SHORT-CIRCUIT OUTPUT CURRENT<sup>†</sup> FREE-AIR TEMPERATURE 13 $V_0 = 0$ 12 $V_{DD\pm}$ = ±5 VI<sub>OS</sub> - Short-Circuit Output Current - mA 11 10 $V_{ID} = -100 \text{ mV}$ 9 8 7 0 V<sub>ID</sub> = 100 mV -3 -75 -50 -25 25 50 100 75 125 TA - Free-Air Temperature - °C Figure 22







† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices. ‡ For curves where  $V_{DD} = 5 \text{ V}$ , all loads are referenced to 2.5 V.



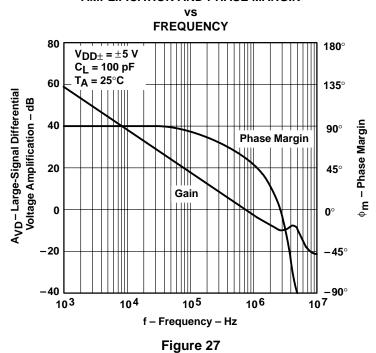
# LARGE-SIGNAL DIFFERENTIAL VOLTAGE<sup>†</sup> AMPLIFICATION AND PHASE MARGIN

#### **FREQUENCY** 80 180° $V_{DD} = 5 V$ C<sub>L</sub>= 100 pF T<sub>A</sub> = 25°C 60 135° A<sub>VD</sub>-Large-Signal Differential Voltage Amplification - dB 40 <sub>0</sub> – Phase Margin 90° Phase Margin 20 45° Gain 0 **0**° -20-45° -40 -90° 10<sup>3</sup> 104 105 106 107 f - Frequency - Hz

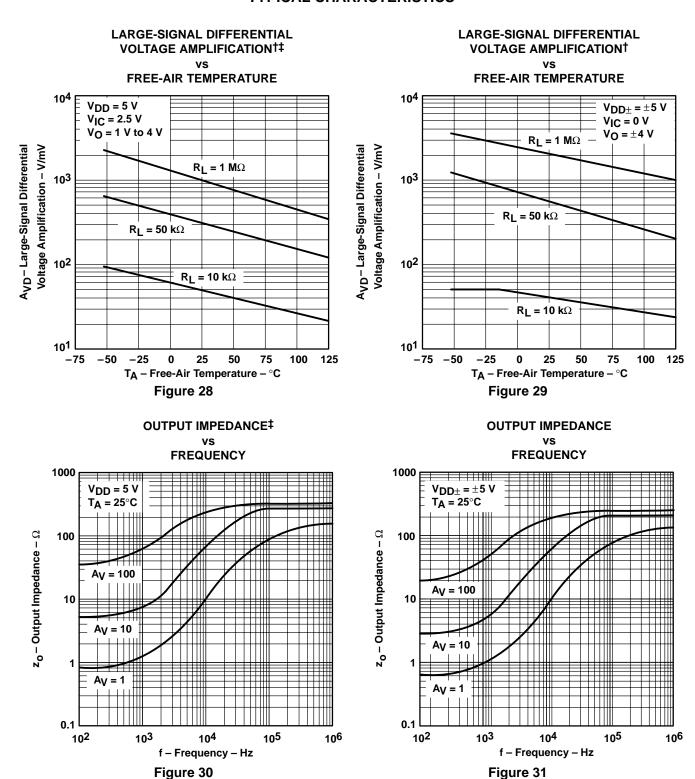
 $\dagger$  For curves where  $V_{DD}$  = 5 V, all loads are referenced to 2.5 V.

Figure 26

# LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE MARGIN







<sup>†</sup> Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

<sup>‡</sup> For curves where  $V_{DD} = 5 \text{ V}$ , all loads are referenced to 2.5 V.



# **COMMON-MODE REJECTION RATIO**† **FREQUENCY** 100 CMRR - Common-Mode Rejection Ratio - dB $V_{DD\pm} = \pm 5 V$ 80 V<sub>DD</sub> = 5 V 60 40 20 101 10<sup>2</sup> 103 104 105 10<sup>6</sup> f - Frequency - Hz

# COMMON-MODE REJECTION RATIO†‡ vs FREE-AIR TEMPERATURE

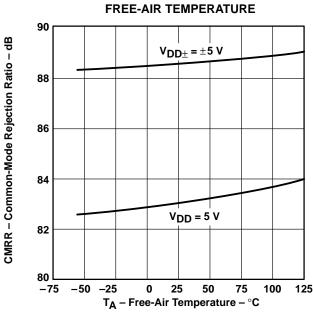
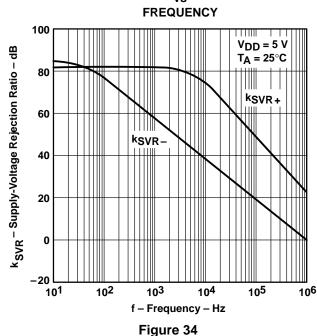


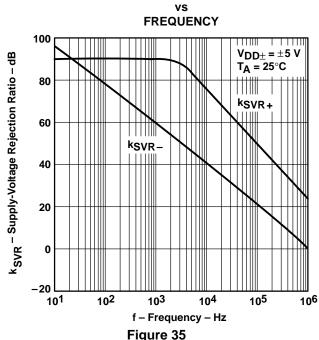
Figure 33



Figure 32



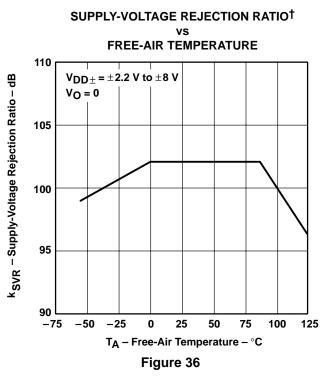
# SUPPLY-VOLTAGE REJECTION RATIO

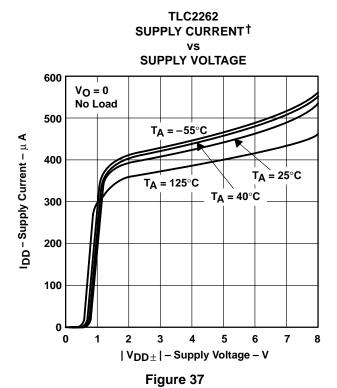


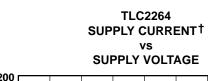
 $<sup>\</sup>dagger$  For curves where  $V_{DD}$  = 5 V, all loads are referenced to 2.5 V.

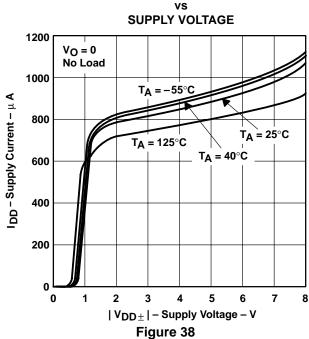
<sup>‡</sup> Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

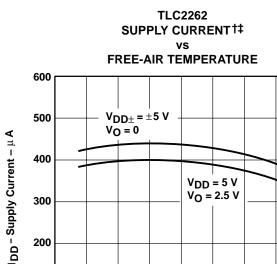


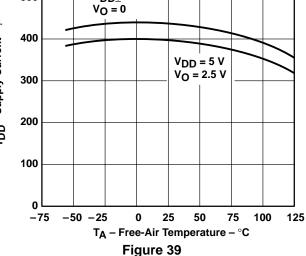








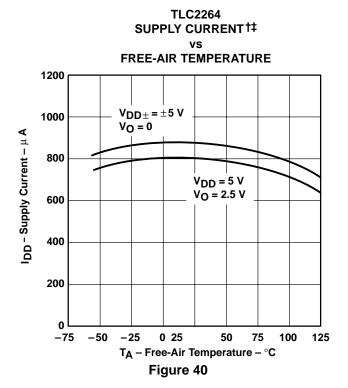


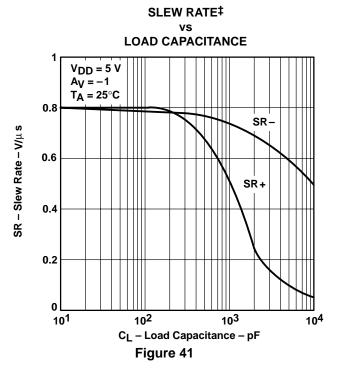


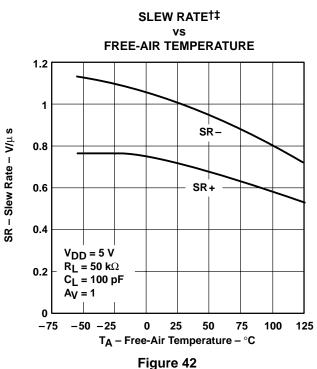
† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

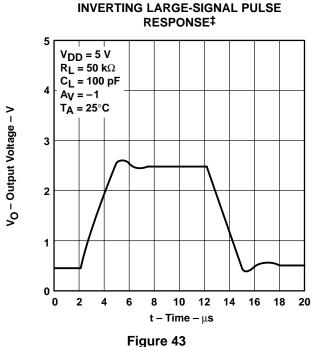
<sup>‡</sup> For curves where  $V_{DD} = 5 \text{ V}$ , all loads are referenced to 2.5 V.











† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

 $<sup>\</sup>ddagger$  For curves where  $V_{DD}$  = 5 V, all loads are referenced to 2.5 V.



V<sub>O</sub> - Output Voltage - V

# INVERTING LARGE-SIGNAL PULSE RESPONSE

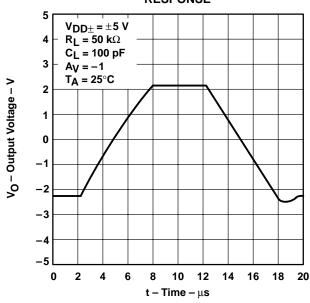


Figure 44

# VOLTAGE-FOLLOWER LARGE-SIGNAL PULSE RESPONSE<sup>†</sup>

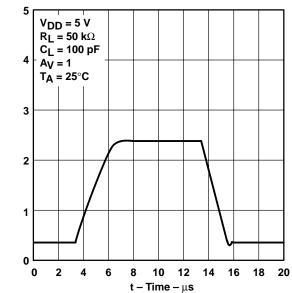


Figure 45

# VOLTAGE-FOLLOWER LARGE-SIGNAL PULSE RESPONSE

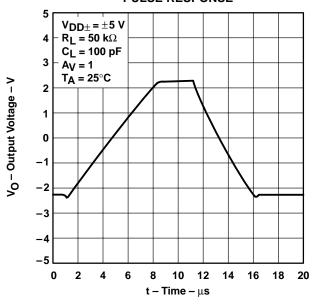


Figure 46

# INVERTING SMALL-SIGNAL

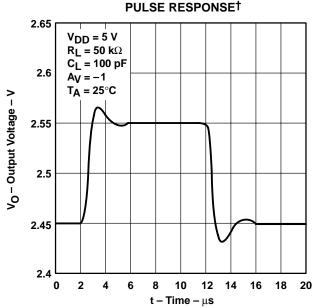


Figure 47

 $<sup>\</sup>dagger$  For curves where  $V_{DD}$  = 5 V, all loads are referenced to 2.5 V.



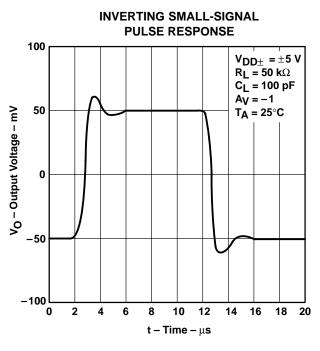


Figure 48

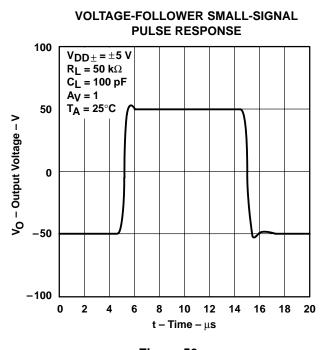


Figure 50

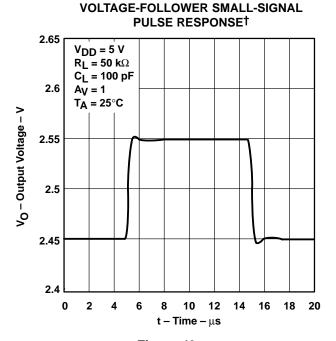


Figure 49

# EQUIVALENT INPUT NOISE VOLTAGE<sup>†</sup> vs FREQUENCY

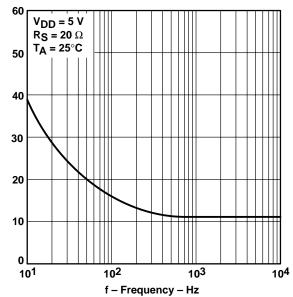


Figure 51

 $\dagger$  For curves where  $V_{DD}$  = 5 V, all loads are referenced to 2.5 V.



Vn – Equivalent Input Noise Voltage – nV/√Hz

## **EQUIVALENT INPUT NOISE VOLTAGE FREQUENCY** 60 Vn – Equivalent Input Noise Voltage – nV/√Hz $V_{DD\pm} = \pm 5 V$ $R_S = 20 \Omega$ $T_A = 25^{\circ}C$ 50 40 30 20 10 0 10<sup>1</sup> 10<sup>2</sup> 103 104 f - Frequency - Hz

Figure 52

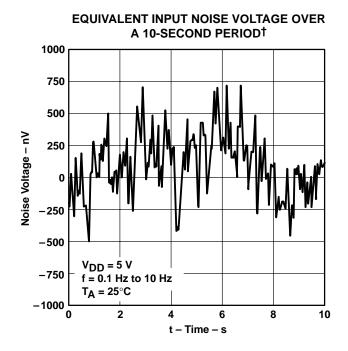
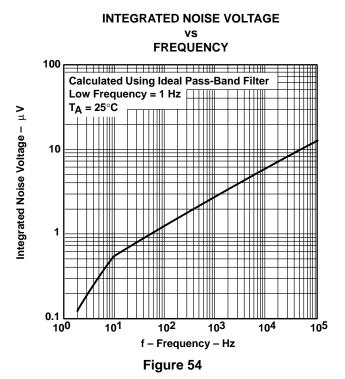


Figure 53



TOTAL HARMONIC DISTORTION PLUS NOISE<sup>†</sup>

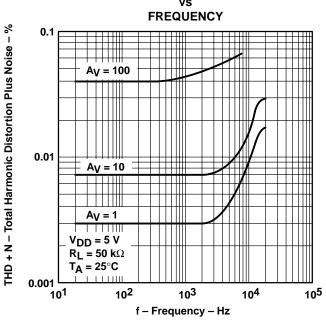
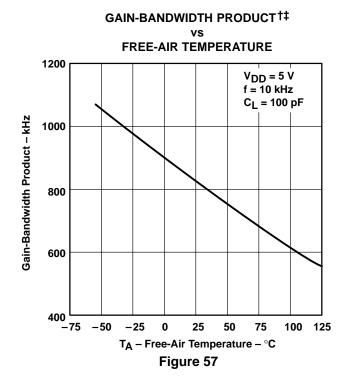


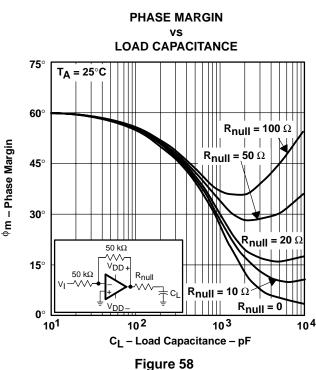
Figure 55

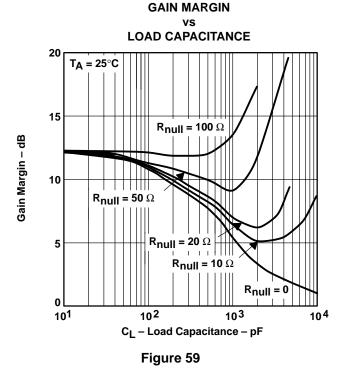
 $<sup>\</sup>dagger$  For curves where  $V_{DD}$  = 5 V, all loads are referenced to 2.5 V.



## **GAIN-BANDWIDTH PRODUCT SUPPLY VOLTAGE** 940 f = 10 kHz $R_L = 50 \text{ k}\Omega$ $C_{L} = 100 \text{ pF}$ $T_A = 25^{\circ}C$ 900 Gain-Bandwidth Product - kHz 860 820 780 740 0 1 2 6 7 | V<sub>DD ±</sub> | - Supply Voltage - V Figure 56



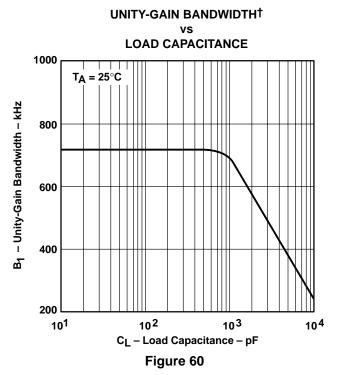


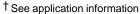


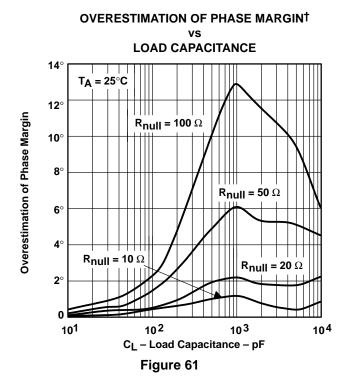
† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

 $<sup>\</sup>ddagger$  For curves where  $V_{DD}$  = 5 V, all loads are referenced to 2.5 V.











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#### **APPLICATION INFORMATION**

#### driving large capacitive loads

The TLC226x is designed to drive larger capacitive loads than most CMOS operational amplifiers. Figure 58 and Figure 59 illustrate its ability to drive loads greater than 400 pF while maintaining good gain and phase margins (R<sub>null</sub> = 0).

A smaller series resistor ( $R_{null}$ ) at the output of the device (see Figure 62) improves the gain and phase margins when driving large capacitive loads. Figure 58 and Figure 59 show the effects of adding series resistances of 10  $\Omega$ , 20  $\Omega$ , 50  $\Omega$ , and 100  $\Omega$ . The addition of this series resistor has two effects: the first is that it adds a zero to the transfer function and the second is that it reduces the frequency of the pole associated with the output load in the transfer function.

The zero introduced to the transfer function is equal to the series resistance times the load capacitance. To calculate the improvement in phase margin, equation 1 can be used.

$$\Delta\Theta_{\rm m1} = \tan^{-1} \left( 2 \times \pi \times \rm UGBW \times R_{\rm null} \times C_{\rm L} \right) \tag{1}$$

Where:

 $\Delta\Theta_{m1}$  = improvement in phase margin

UGBW = unity-gain bandwidth frequency

R<sub>null</sub> = output series resistance

C<sub>I</sub> = load capacitance

The unity-gain bandwidth (UGBW) frequency decreases as the capacitive load increases (see Figure 60). To use equation 1, UGBW must be approximated from Figure 60.

Using equation 1 alone overestimates the improvement in phase margin, as illustrated in Figure 61. The overestimation is caused by the decrease in the frequency of the pole associated with the load, thus providing additional phase shift and reducing the overall improvement in phase margin. The pole associated with the load is reduced by the factor calculated in equation 2.

$$F = \frac{1}{1 + g_{m} \times R_{null}}$$
 (2)

Where:

F = factor reducing frequency of pole

 $g_m = \text{small-signal output transconductance (typically } 4.83 \times 10^{-3} \text{ mhos)}$ 

R<sub>null</sub> = output series resistance

For the TLC226x, the pole associated with the load is typically 7 MHz with 100-pF load capacitance. This value varies inversely with  $C_I$ : at  $C_I = 10$  pF, use 70 MHz, at  $C_I = 1000$  pF, use 700 kHz, and so on.

Reducing the pole associated with the load introduces phase shift, thereby reducing phase margin. This results in an error in the increase in phase margin expected by considering the zero alone (equation 1). Equation 3 approximates the reduction in phase margin due to the movement of the pole associated with the load. The result of this equation can be subtracted from the result of the equation in equation 1 to better approximate the improvement in phase margin.



#### APPLICATION INFORMATION

#### driving large capacitive loads (continued)

$$\Delta\Theta_{\text{m2}} = \tan^{-1} \left[ \frac{\text{UGBW}}{\left( \text{F} \times \text{P}_2 \right)} \right] - \tan^{-1} \left( \frac{\text{UGBW}}{\text{P}_2} \right)$$
 (3)

Where:

 $\Delta\Theta_{m2}$  = reduction in phase margin

UGBW = unity-gain bandwidth frequency

F = factor from equation 2

P<sub>2</sub> = unadjusted pole (70 MHz@10 pF, 7 MHz@100 pF, etc.)

Using these equations with Figure 60 and Figure 61 enables the designer to choose the appropriate output series resistance to optimize the design of circuits driving large capacitive loads.

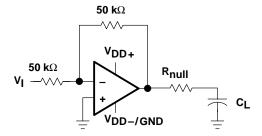


Figure 62. Series-Resistance Circuit



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#### APPLICATION INFORMATION

#### macromodel information

Macromodel information provided was derived using Microsim  $Parts^{TM}$ , the model generation software used with Microsim  $PSpice^{TM}$ . The Boyle macromodel (see Note 5) and subcircuit in Figure 63 are generated using the TLC226x typical electrical and operating characteristics at  $T_A = 25$ °C. Using this information, output simulations of the following key parameters can be generated to a tolerance of 20% (in most cases):

- Maximum positive output voltage swing
- Maximum negative output voltage swing
- Slew rate
- Quiescent power dissipation
- Input bias current
- Open-loop voltage amplification

- Unity-gain frequency
- Common-mode rejection ratio
- Phase margin
- DC output resistance
- AC output resistance
- Short-circuit output current limit

NOTE 5: G. R. Boyle, B. M. Cohn, D. O. Pederson, and J. E. Solomon, "Macromodeling of Integrated Circuit Operational Amplifiers," *IEEE Journal of Solid-State Circuits*, SC-9, 353 (1974).

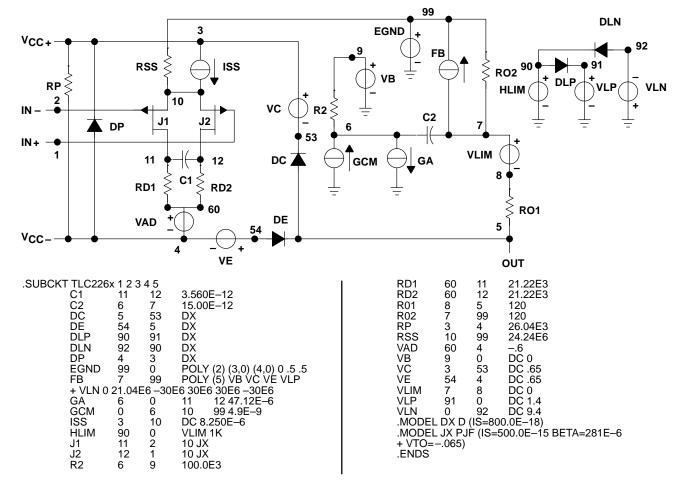


Figure 63. Boyle Macromodel and Subcircuit

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#### **PACKAGING INFORMATION**

Orderable Device	Status	Package Type	Package Drawing	Pins	Package Qty	Eco Plan	Lead finish/ Ball material	MSL Peak Temp	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9469201QHA	ACTIVE	CFP	U	10	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	9469201QHA TLC2262M	Samples
5962-9469203QPA	ACTIVE	CDIP	JG	8	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	9469203QPA TLC2262AM	Samples
5962-9469204Q2A	ACTIVE	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962- 9469204Q2A TLC2264 AMFKB	Samples
5962-9469204QCA	ACTIVE	CDIP	J	14	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9469204QC A TLC2264AMJB	Samples
TLC2262AID	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2262AI	Samples
TLC2262AIDG4	LIFEBUY	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2262AI	
TLC2262AIDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2262AI	Samples
TLC2262AIP	ACTIVE	PDIP	Р	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 125	TLC2262AI	Samples
TLC2262AIPW	ACTIVE	TSSOP	PW	8	150	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	Y2262A	Samples
TLC2262AIPWR	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	Y2262A	Samples
TLC2262AIPWRG4	LIFEBUY	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	Y2262A	
TLC2262AMJG	ACTIVE	CDIP	JG	8	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	TLC2262 AMJG	Samples
TLC2262AMJGB	ACTIVE	CDIP	JG	8	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	9469203QPA TLC2262AM	Samples
TLC2262AQD	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C2262A	Samples
TLC2262CD	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	2262C	Samples
TLC2262CDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	2262C	Samples
TLC2262CP	ACTIVE	PDIP	Р	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	TLC2262CP	Samples
TLC2262CPE4	LIFEBUY	PDIP	Р	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	TLC2262CP	



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Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp	Op Temp (°C)	<b>Device Marking</b> (4/5)	Samples
TLC2262CPW	ACTIVE	TSSOP	PW	8	150	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	P2262	Samples
TLC2262CPWR	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	P2262	Samples
TLC2262CPWRG4	LIFEBUY	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	P2262	
TLC2262ID	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM		22621	Samples
TLC2262IDG4	LIFEBUY	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM		22621	
TLC2262IDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM		22621	Samples
TLC2262IP	ACTIVE	PDIP	Р	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type		TLC2262IP	Samples
TLC2262MUB	ACTIVE	CFP	U	10	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	9469201QHA TLC2262M	Samples
TLC2262QD	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C2262Q	Samples
TLC2262QDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C2262Q	Samples
TLC2264AID	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2264AI	Samples
TLC2264AIDG4	LIFEBUY	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2264AI	
TLC2264AIDR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2264AI	Samples
TLC2264AIN	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 125	TLC2264AIN	Samples
TLC2264AIPW	ACTIVE	TSSOP	PW	14	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	Y2264A	Samples
TLC2264AIPWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	Y2264A	Samples
TLC2264AIPWRG4	LIFEBUY	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	Y2264A	
TLC2264AMFKB	ACTIVE	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962- 9469204Q2A TLC2264 AMFKB	Samples
TLC2264AMJB	ACTIVE	CDIP	J	14	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9469204QC A TLC2264AMJB	Samples
TLC2264AQD	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2264AQ	Samples

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Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan	Lead finish/ Ball material	MSL Peak Temp	Op Temp (°C)	Device Marking (4/5)	Samples
TLC2264AQDRG4	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM		PJ2264A	Samples
TLC2264CD	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TLC2264C	Samples
TLC2264CDR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TLC2264C	Samples
TLC2264CN	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	TLC2264CN	Samples
TLC2264CPW	ACTIVE	TSSOP	PW	14	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	P2264	Samples
TLC2264CPWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	P2264	Samples
TLC2264ID	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM		TLC2264I	Samples
TLC2264IDR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM		TLC2264I	Samples
TLC2264IN	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type		TLC2264IN	Samples

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) RoHS: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (CI) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

### PACKAGE OPTION ADDENDUM

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(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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#### OTHER QUALIFIED VERSIONS OF TLC2262, TLC2262A, TLC2262AM, TLC2264A, TLC2264AM:

Catalog: TLC2262A, TLC2262, TLC2264A

Automotive: TLC2264A-Q1, TLC2264A-Q1

Military: TLC2262M, TLC2262AM, TLC2264AM

NOTE: Qualified Version Definitions:

- Catalog TI's standard catalog product
- Automotive Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Military QML certified for Military and Defense Applications



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#### TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

#### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



#### \*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLC2262AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLC2262AIPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TLC2262CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLC2262CPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TLC2262IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLC2262QDR	SOIC	D	8	2500	330.0	12.5	6.4	5.2	2.1	8.0	12.0	Q1
TLC2264AIDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLC2264AIPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TLC2264AQDRG4	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLC2264CDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLC2264CPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TLC2264IDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1



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\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLC2262AIDR	SOIC	D	8	2500	340.5	336.1	25.0
TLC2262AIPWR	TSSOP	PW	8	2000	356.0	356.0	35.0
TLC2262CDR	SOIC	D	8	2500	340.5	336.1	25.0
TLC2262CPWR	TSSOP	PW	8	2000	356.0	356.0	35.0
TLC2262IDR	SOIC	D	8	2500	340.5	336.1	25.0
TLC2262QDR	SOIC	D	8	2500	340.5	336.1	25.0
TLC2264AIDR	SOIC	D	14	2500	340.5	336.1	32.0
TLC2264AIPWR	TSSOP	PW	14	2000	356.0	356.0	35.0
TLC2264AQDRG4	SOIC	D	14	2500	350.0	350.0	43.0
TLC2264CDR	SOIC	D	14	2500	340.5	336.1	32.0
TLC2264CPWR	TSSOP	PW	14	2000	356.0	356.0	35.0
TLC2264IDR	SOIC	D	14	2500	340.5	336.1	32.0



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#### **TUBE**



\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
5962-9469201QHA	U	CFP	10	1	506.98	26.16	6220	NA
5962-9469204Q2A	FK	LCCC	20	1	506.98	12.06	2030	NA
TLC2262AID	D	SOIC	8	75	505.46	6.76	3810	4
TLC2262AID	D	SOIC	8	75	507	8	3940	4.32
TLC2262AIDG4	D	SOIC	8	75	507	8	3940	4.32
TLC2262AIDG4	D	SOIC	8	75	505.46	6.76	3810	4
TLC2262AIP	Р	PDIP	8	50	506	13.97	11230	4.32
TLC2262AIPW	PW	TSSOP	8	150	530	10.2	3600	3.5
TLC2262AQD	D	SOIC	8	75	507	8	3940	4.32
TLC2262CD	D	SOIC	8	75	507	8	3940	4.32
TLC2262CP	Р	PDIP	8	50	506	13.97	11230	4.32
TLC2262CPE4	Р	PDIP	8	50	506	13.97	11230	4.32
TLC2262CPW	PW	TSSOP	8	150	530	10.2	3600	3.5
TLC2262ID	D	SOIC	8	75	507	8	3940	4.32
TLC2262IDG4	D	SOIC	8	75	507	8	3940	4.32
TLC2262IP	Р	PDIP	8	50	506	13.97	11230	4.32
TLC2262MUB	U	CFP	10	1	506.98	26.16	6220	NA
TLC2262QD	D	SOIC	8	75	507	8	3940	4.32
TLC2264AID	D	SOIC	14	50	507	8	3940	4.32
TLC2264AID	D	SOIC	14	50	505.46	6.76	3810	4
TLC2264AIDG4	D	SOIC	14	50	507	8	3940	4.32
TLC2264AIDG4	D	SOIC	14	50	505.46	6.76	3810	4
TLC2264AIN	N	PDIP	14	25	506	13.97	11230	4.32
TLC2264AIPW	PW	TSSOP	14	90	530	10.2	3600	3.5
TLC2264AMFKB	FK	LCCC	20	1	506.98	12.06	2030	NA
TLC2264AQD	D	SOIC	14	50	505.46	6.76	3810	4
TLC2264CD	D	SOIC	14	50	505.46	6.76	3810	4
TLC2264CD	D	SOIC	14	50	507	8	3940	4.32
TLC2264CN	N	PDIP	14	25	506	13.97	11230	4.32



# **PACKAGE MATERIALS INFORMATION**

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Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TLC2264CPW	PW	TSSOP	14	90	530	10.2	3600	3.5
TLC2264ID	D	SOIC	14	50	507	8	3940	4.32
TLC2264IN	N	PDIP	14	25	506	13.97	11230	4.32

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary. Refer to the product data sheet for package details.



**INSTRUMENTS** www.ti.com

CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary. Refer to the product data sheet for package details.

4040083-5/G





CERAMIC DUAL IN LINE PACKAGE



- 1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- 2. This drawing is subject to change without notice.
- 3. This package is hermitically sealed with a ceramic lid using glass frit.
- His package is remitted by sealed with a ceramic its using glass mit.
   Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
   Falls within MIL-STD-1835 and GDIP1-T14.



CERAMIC DUAL IN LINE PACKAGE



# D (R-PDSO-G14)

#### PLASTIC SMALL OUTLINE



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AB.



PW (R-PDSO-G14)

#### PLASTIC SMALL OUTLINE



- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M—1994.
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
- E. Falls within JEDEC MO-153





SMALL OUTLINE INTEGRATED CIRCUIT



- 1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
- 2. This drawing is subject to change without notice.
- 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
- 4. This dimension does not include interlead flash.
- 5. Reference JEDEC registration MS-012, variation AA.



SMALL OUTLINE INTEGRATED CIRCUIT



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SMALL OUTLINE INTEGRATED CIRCUIT



NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



#### JG (R-GDIP-T8)

#### **CERAMIC DUAL-IN-LINE**



NOTES: A. All linear dimensions are in inches (millimeters).

- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification.
- E. Falls within MIL STD 1835 GDIP1-T8

# P (R-PDIP-T8)

## PLASTIC DUAL-IN-LINE PACKAGE



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Falls within JEDEC MS-001 variation BA.



# N (R-PDIP-T\*\*)

## PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- The 20 pin end lead shoulder width is a vendor option, either half or full width.





SMALL OUTLINE PACKAGE



- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

  2. This drawing is subject to change without notice.

  3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- 5. Reference JEDEC registration MO-153, variation AA.



SMALL OUTLINE PACKAGE



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SMALL OUTLINE PACKAGE



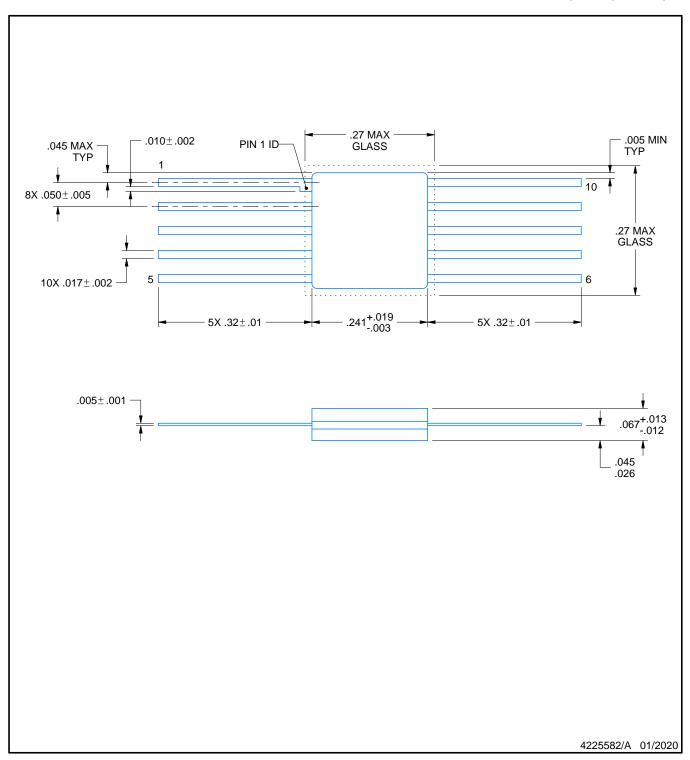
NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.





CERAMIC FLATPACK



- 1. All linear dimensions are in inches. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
  2. This drawing is subject to change without notice.



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