Project 3

Power System

Report

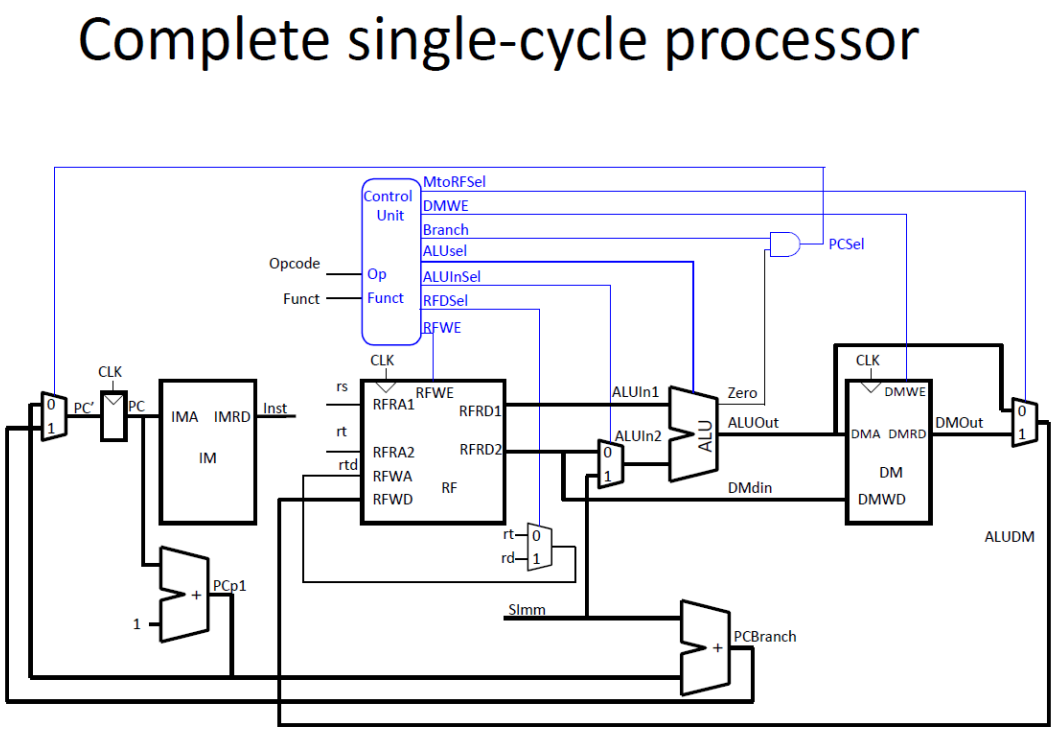
by Xinqiao Zhang

EE-670

May, 2018

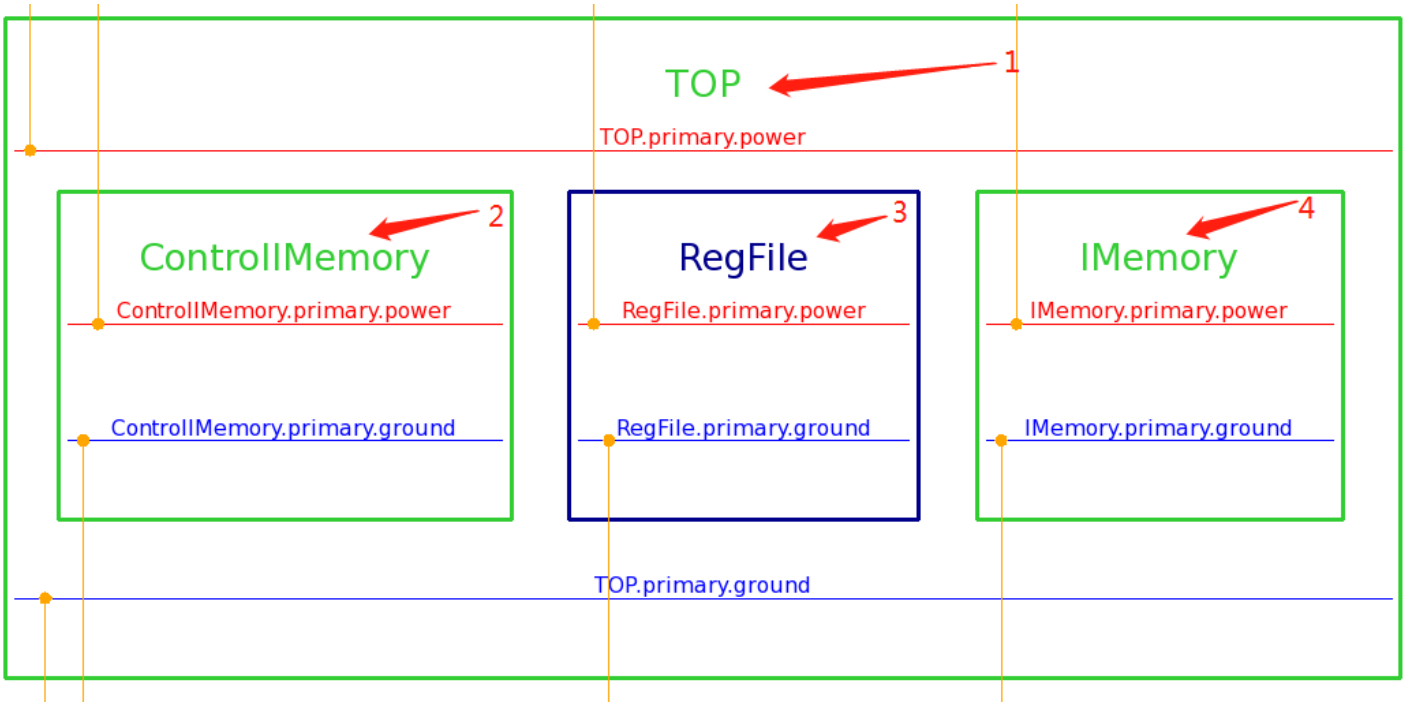
Content

1. Module mips

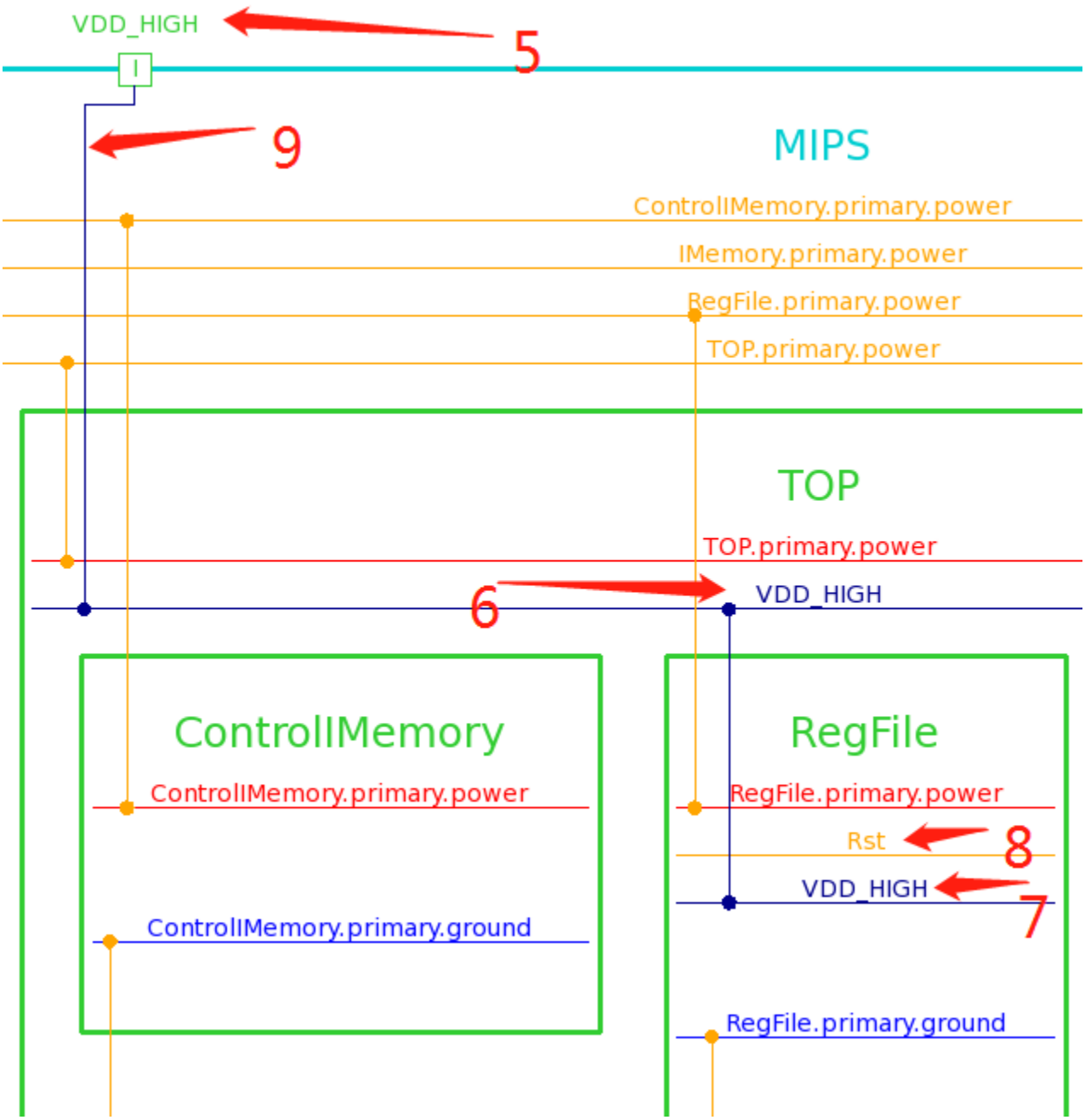


2. UPF file and Block diagram

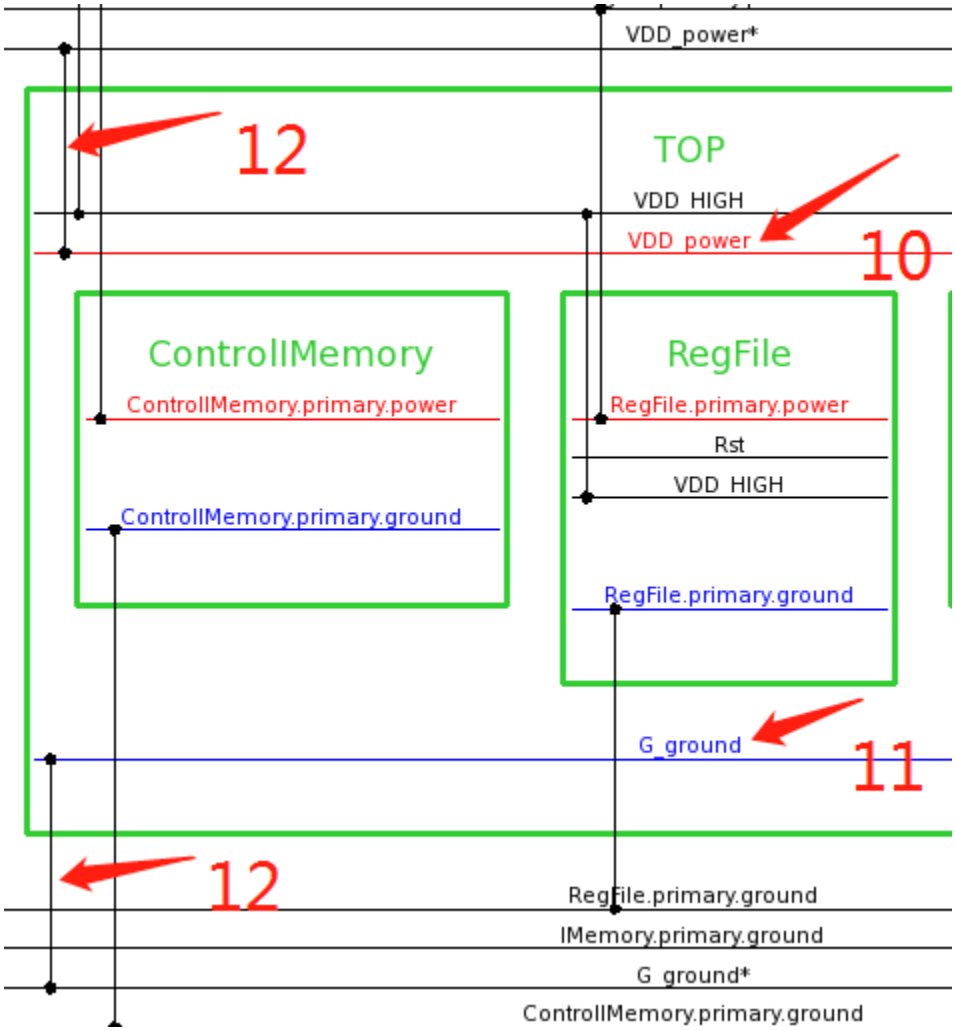
```
######## Create Power Domains ############

1.  create_power_domain TOP
2.  create_power_domain IMemory -elements InstructionMemory
3.  create_power_domain ControlIMemory -elements ControlInstructionMemory
4.  create_power_domain RegFile -elements RegisterFile
```



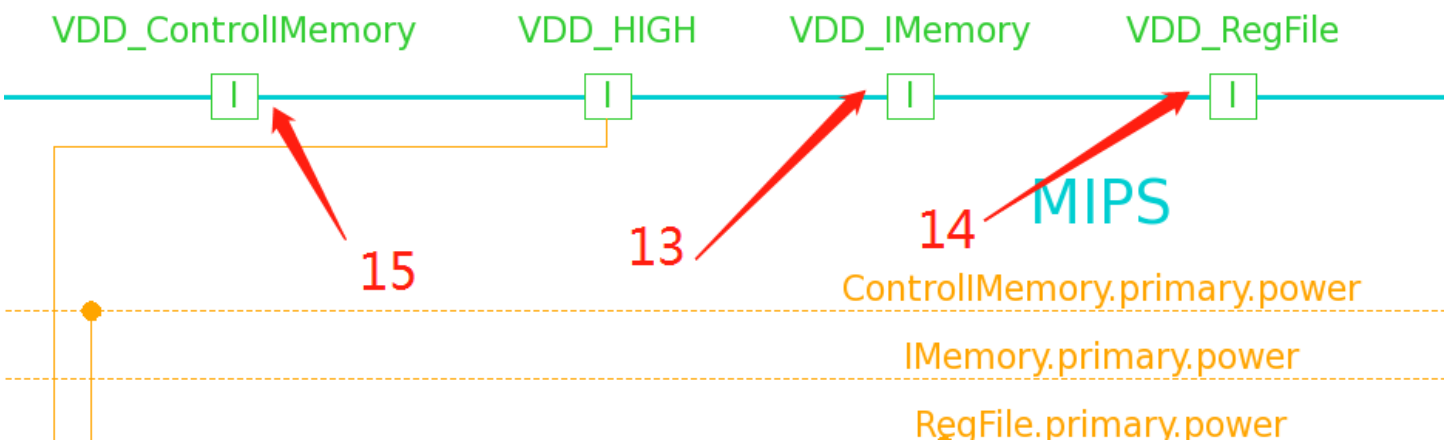
```
## Toplevel Connections ######
## Create supply port and net ######

5.  create_supply_port VDD_HIGH
6.  create_supply_net VDD_HIGH -domain TOP
7.  create_supply_net VDD_HIGH -domain RegFile -reuse
8.  create_supply_net Rst -domain RegFile
9.  connect_supply_net VDD_HIGH -ports VDD_HIGH
```



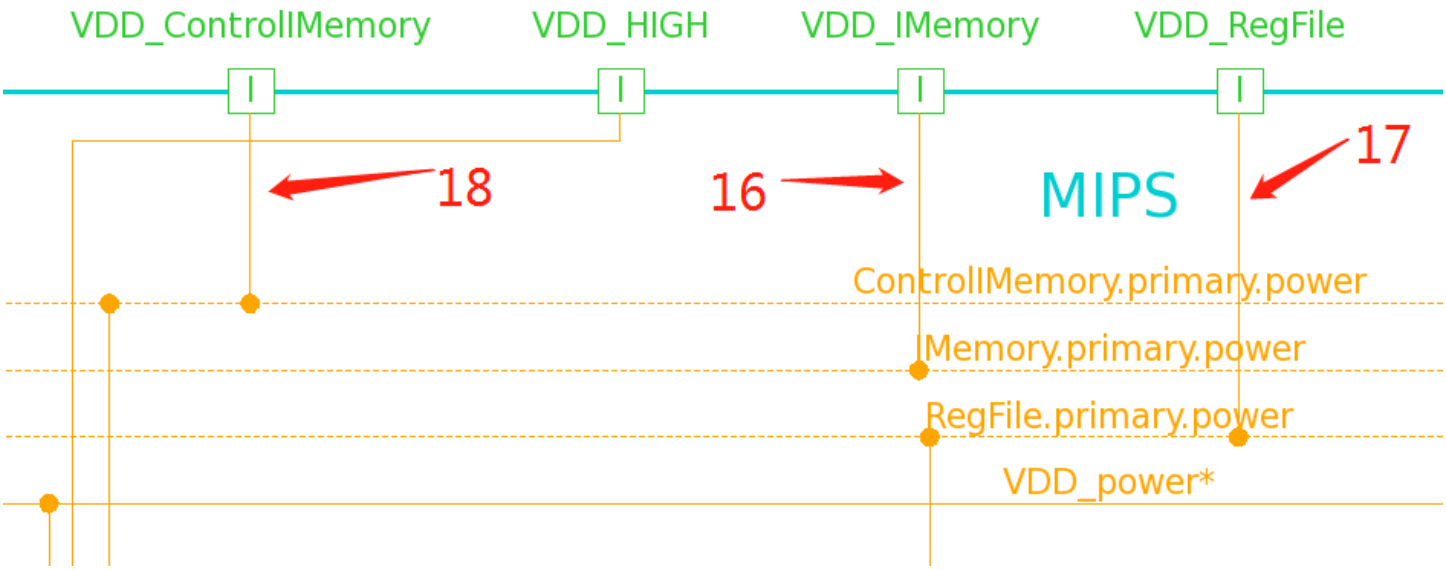
```
## Create supply net ######
10. create_supply_net VDD_power
11. create_supply_net G_ground
12. set_domain_supply_net TOP -primary_power_net VDD_power -primary_ground_net G_ground
```



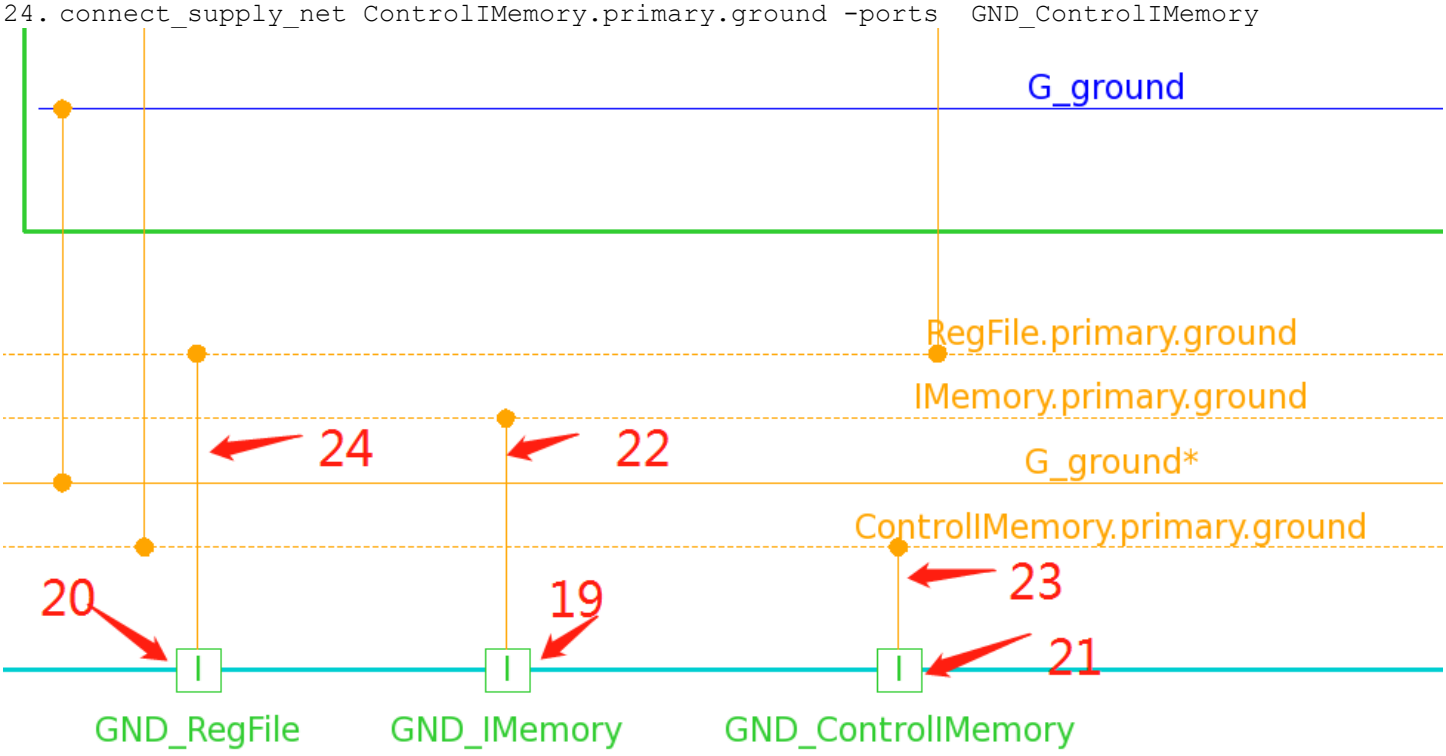

```
## Create supply port ######
13. create_supply_port VDD_IMemory
14. create_supply_port VDD_RegFile
15. create_supply_port VDD_ControlIMemory
```



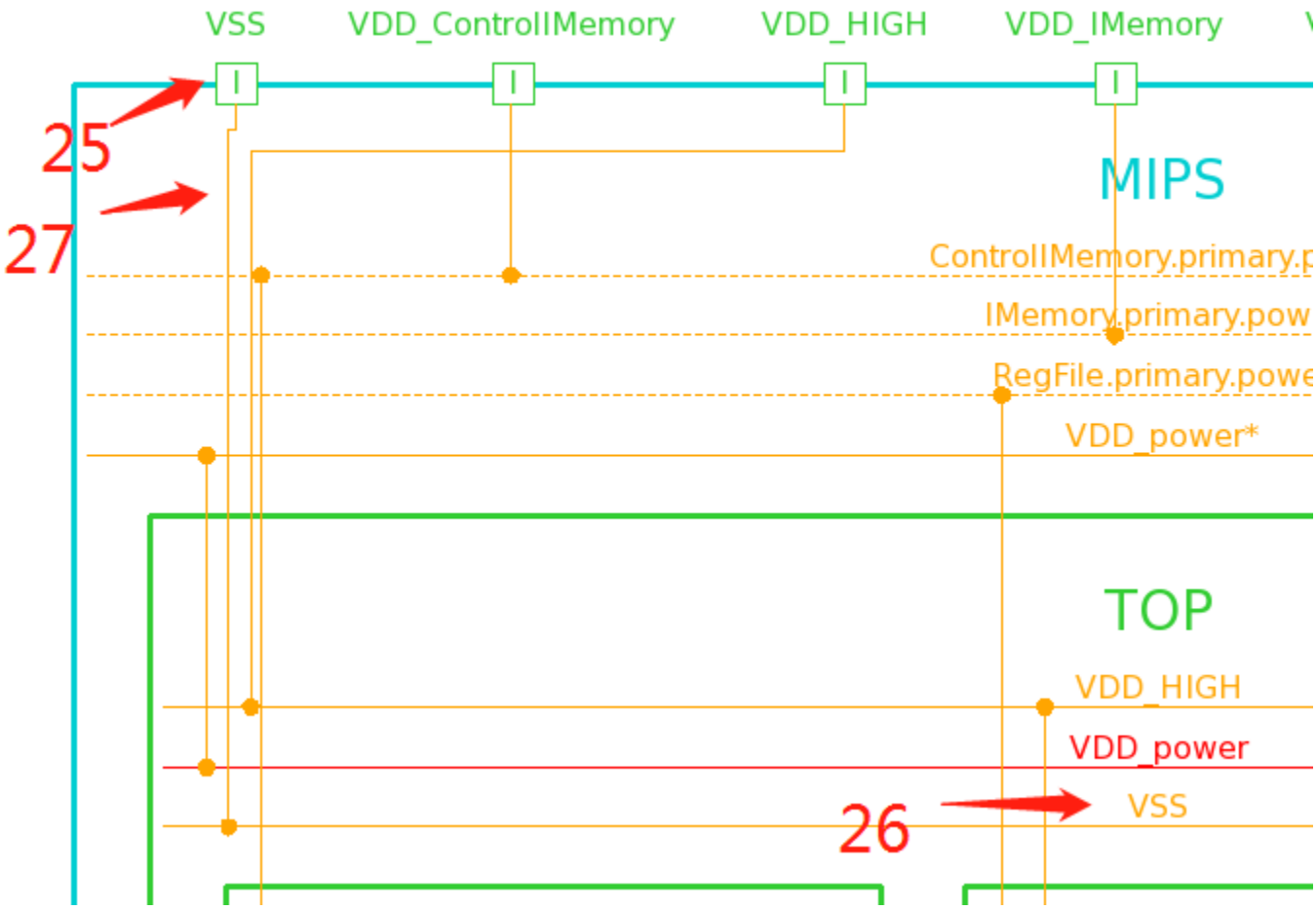
```
## Connect ports to nets ######
16. connect_supply_net IMemory.primary.power -ports VDD_IMemory
17. connect_supply_net RegFile.primary.power -ports VDD_RegFile
18. connect_supply_net ControlIMemory.primary.power -ports VDD_ControlIMemory
```




```
## create ports and connect nets ######
19. create_supply_port GND_IMemory
20. create_supply_port GND_RegFile
21. create_supply_port GND_ControlIMemory
22. connect_supply_net IMemory.primary.ground -ports  GND_IMemory
23. connect_supply_net RegFile.primary.ground -ports  GND_RegFile
24. connect_supply_net ControlIMemory.primary.ground -ports  GND_ControlIMemory
```

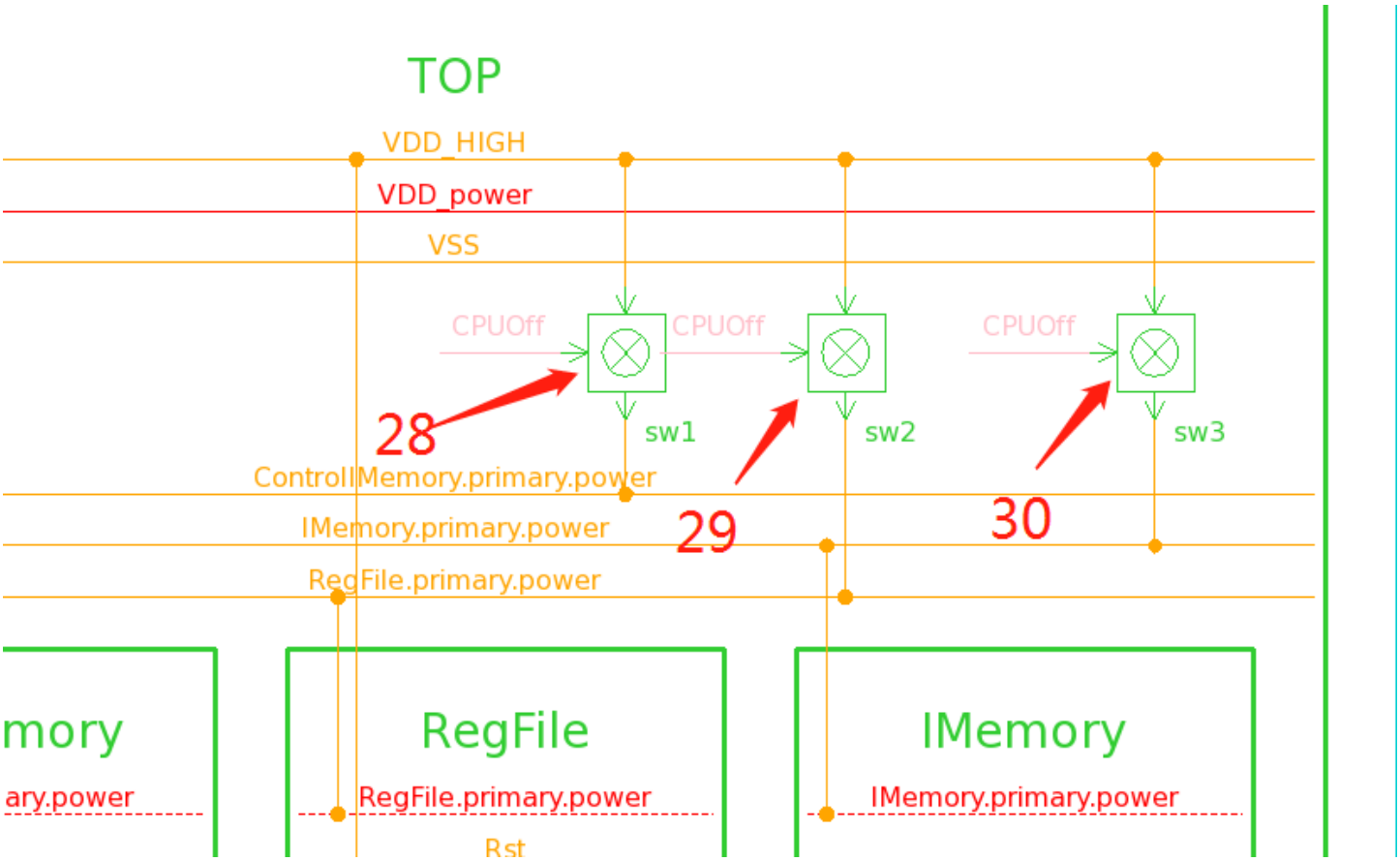


```
# create supply VSS
25. create_supply_port VSS
26. create_supply_net VSS -domain TOP
27. connect_supply_net VSS -ports VSS
```

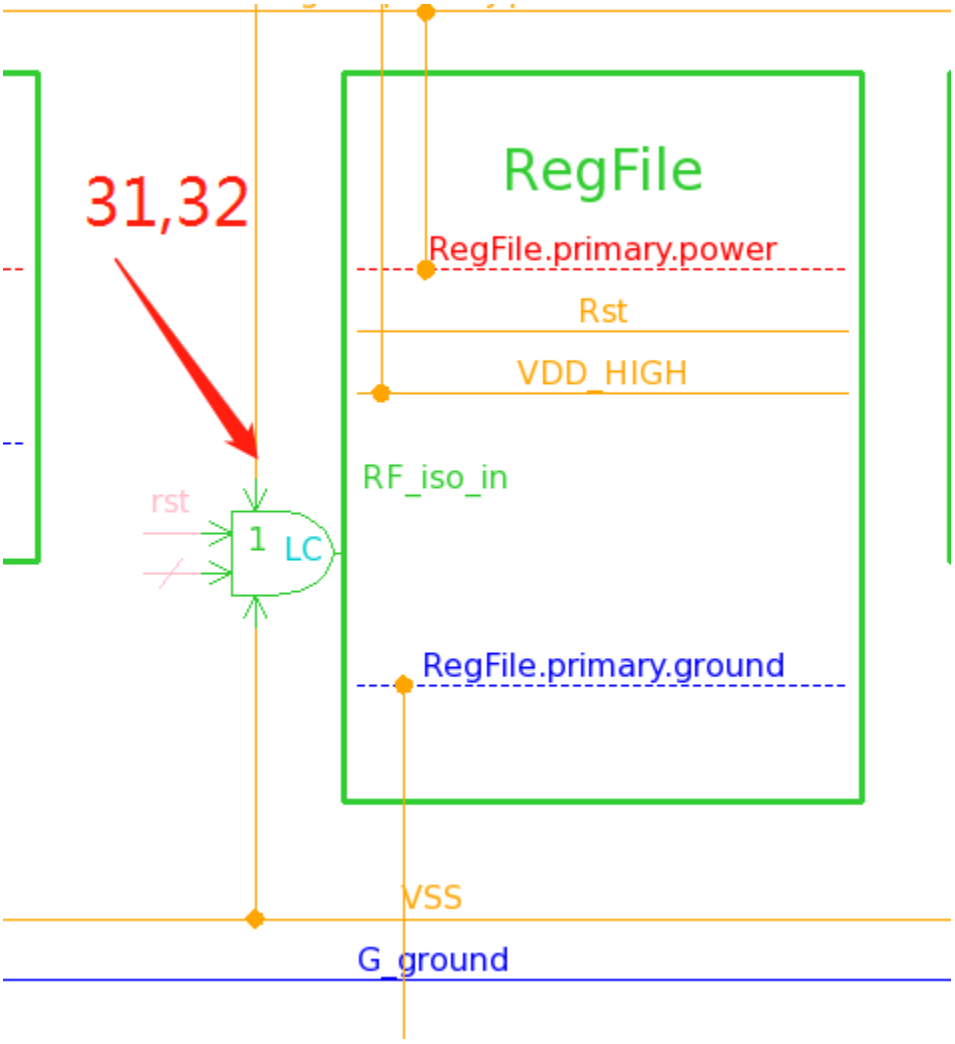



```
###set different voltage ###
set_voltage 1.1  -object_list Rst

set_voltage 1.1  -object_list VDD_HIGH
set_voltage 1.1  -object_list VDD_power

set_voltage 0  -object_list VSS
set_voltage 0  -object_list G_ground

set_voltage 1.1  -object_list TOP.primary.power
set_voltage 0  -object_list TOP.primary.ground

set_voltage 1.1  -object_list IMemory.primary.power
set_voltage 0  -object_list IMemory.primary.ground

set_voltage 1.1  -object_list RegFile.primary.power
set_voltage 0  -object_list RegFile.primary.ground

set_voltage 1.1  -object_list ControlIMemory.primary.power
set_voltage 0  -object_list ControlIMemory.primary.ground
```

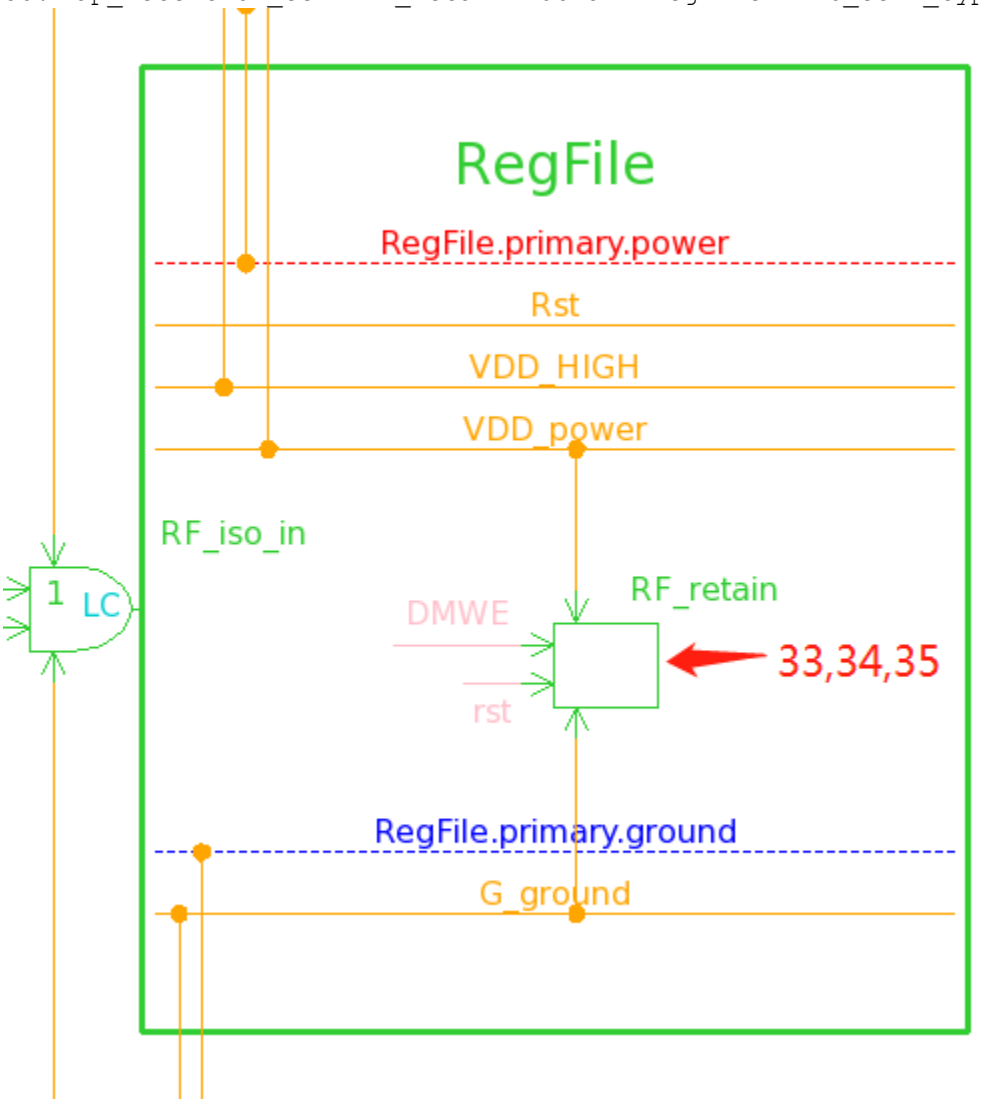
```
########## Create Shut-Down Logic #######

28. create_power_switch sw1 -domain TOP -input_supply_port {in1 VDD_HIGH} -
    output_supply_port {out1 ControlIMemory.primary.power} -control_port {cc CPUOff} -
    on_state {state2009 in1 {!cc}}


29. create_power_switch sw2 -domain TOP -input_supply_port {in1 VDD_HIGH} -
    output_supply_port {out1 RegFile.primary.power} -control_port {cc CPUOff} -on_state
    {state2009 in1 {!cc}}


30. create_power_switch sw3 -domain TOP -input_supply_port {in1 VDD_HIGH} -
    output_supply_port {out1 IMemory.primary.power} -control_port {cc CPUOff} -on_state
    {state2009 in1 {!cc}}
```



```
######### Isolation cell Settings for all #########

31. set_isolation RF_iso_in -domain RegFile -isolation_power_net VDD_HIGH -
    isolation_ground_net VSS -clamp_value 1 -applies_to inputs
32. set_isolation_control RF_iso_in -domain RegFile -isolation_signal rst -isolation_sense
    high -location parent
```

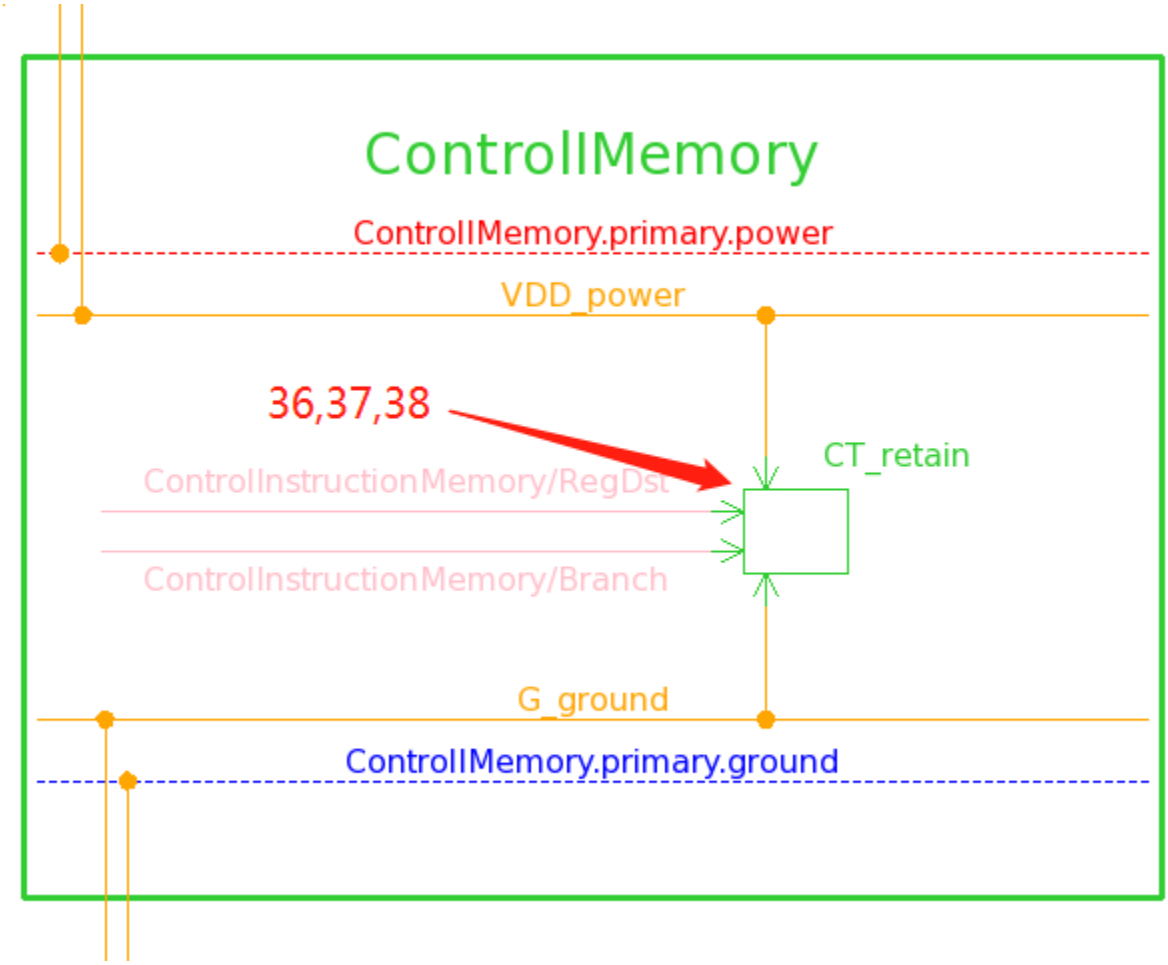


```
#### Retention Logic ##############

33. set_retention RF_retain -domain RegFile -retention_power_net VDD_power -
    retention_ground_net G_ground

34. set_retention_control RF_retain -domain RegFile -save_signal {DMWE high} -
    restore_signal {rst low}
35. map_retention_cell RF_retain -domain RegFile -lib_cell_type LIB_CELL_NAME
```



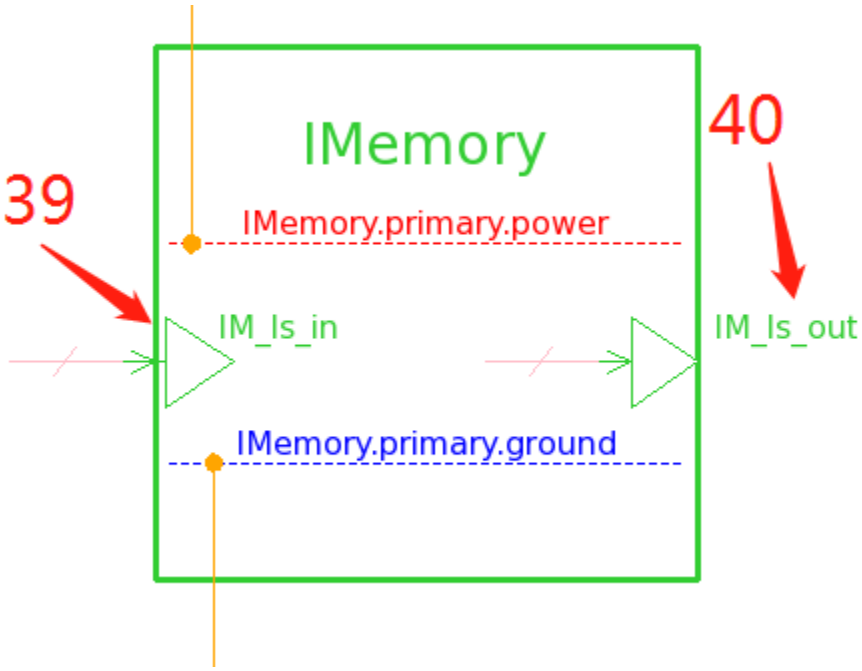
```
#### Retention Logic ##############
```

```
36. set_retention CT_retain -domain ControlIMemory -retention_power_net VDD_power -
    retention_ground_net G_ground
37. set_retention_control CT_retain -domain ControlIMemory -save_signal {RegDst high} -
    restore_signal {Branch high}
38. map_retention_cell CT_retain -domain ControlIMemory -lib_cell_type LIB_CELL_NAME
```



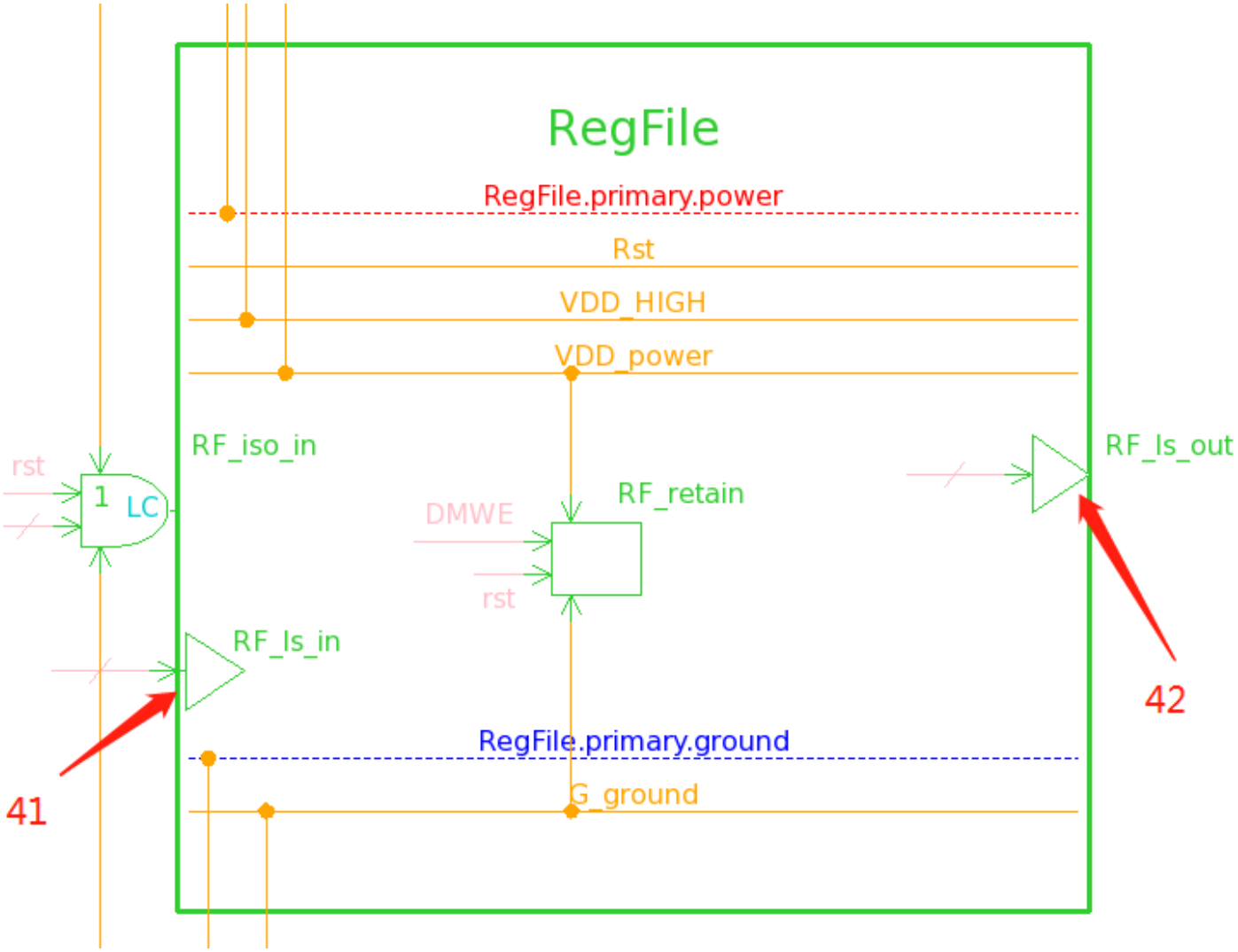
```
#### Level Shifter #################
```

```
39. set_level_shifter IM_ls_in  -domain IMemory -applies_to inputs -location self -rule
    both
40. set_level_shifter IM_ls_out -domain IMemory -applies_to outputs -location self -rule
    both
```

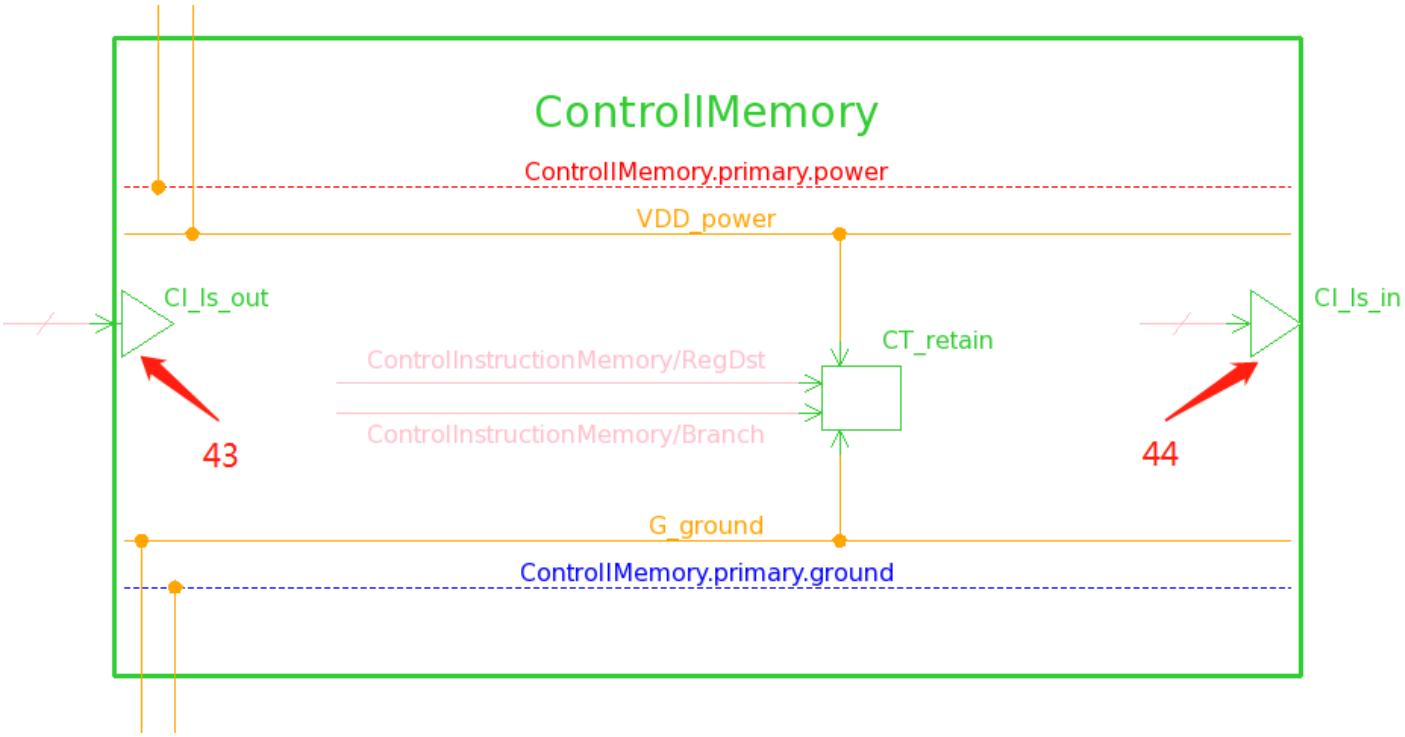


Level Shifter

41. set_level_shifter RF_ls_out -domain RegFile -applies_to outputs -location self -rule both
42. set_level_shifter RF_ls_in -domain RegFile -applies_to inputs -location self -rule both

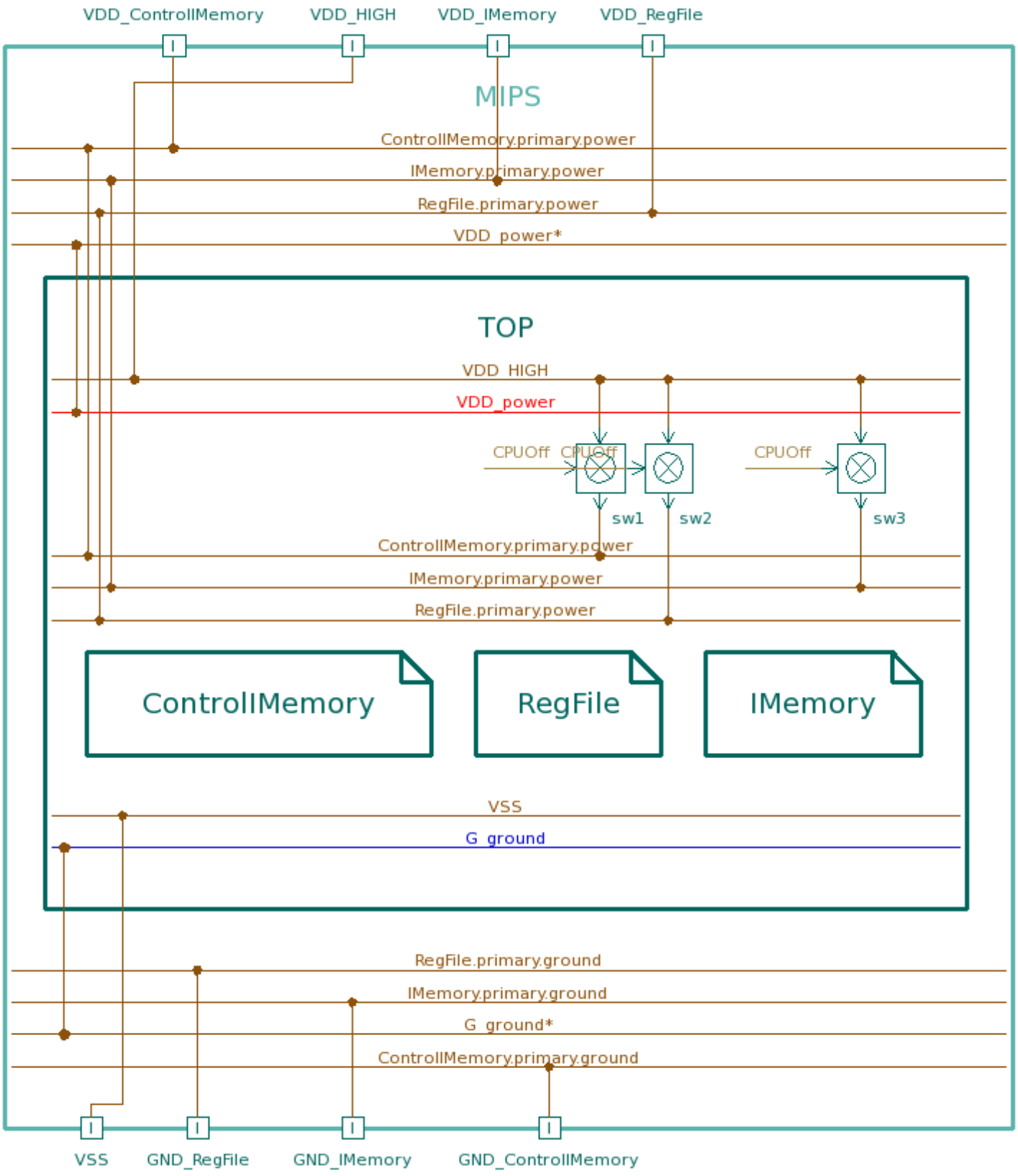


```
#### Level Shifter ####
43. set_level_shifter CI_ls_out -domain ControlIMemory -applies_to inputs -location self -
    rule both
44. set_level_shifter CI_ls_in -domain ControlIMemory -applies_to outputs -location self -
    rule both
```



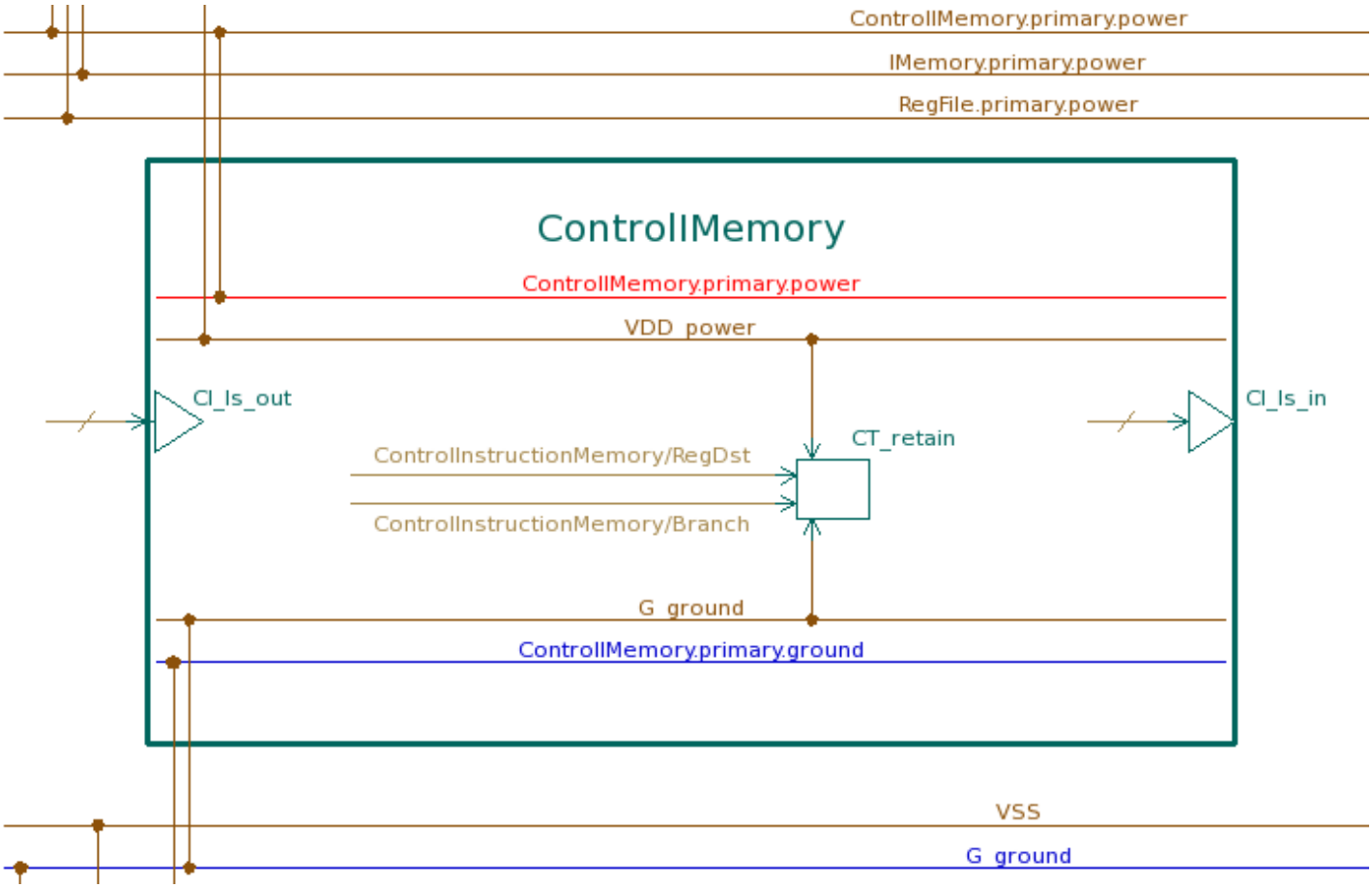

```
### Create Power State Table ###################

# NOT support for this tech file
```

3. UPF diagram (three domains collapsed)

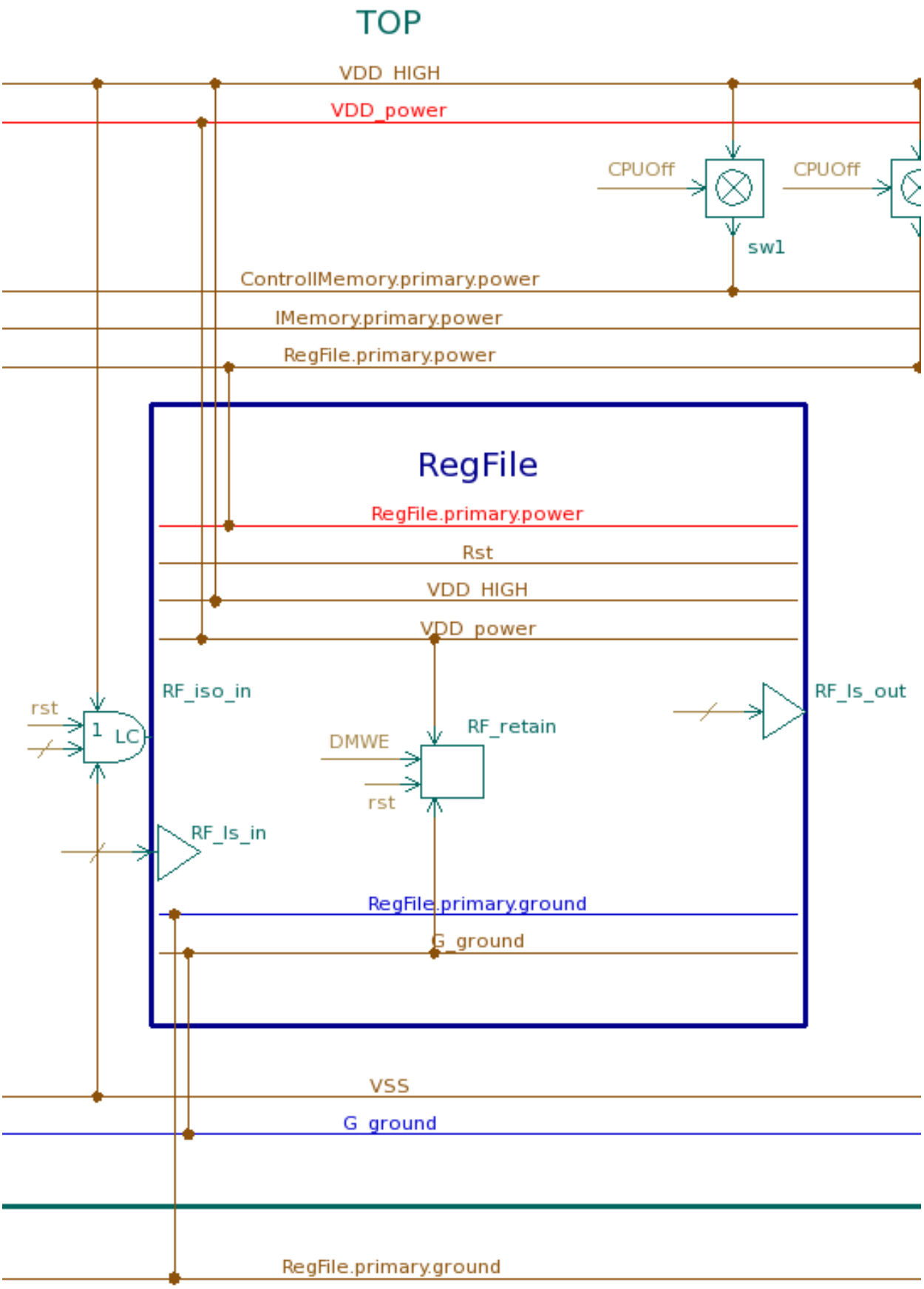


4. UPF diagram (three domains in detail)

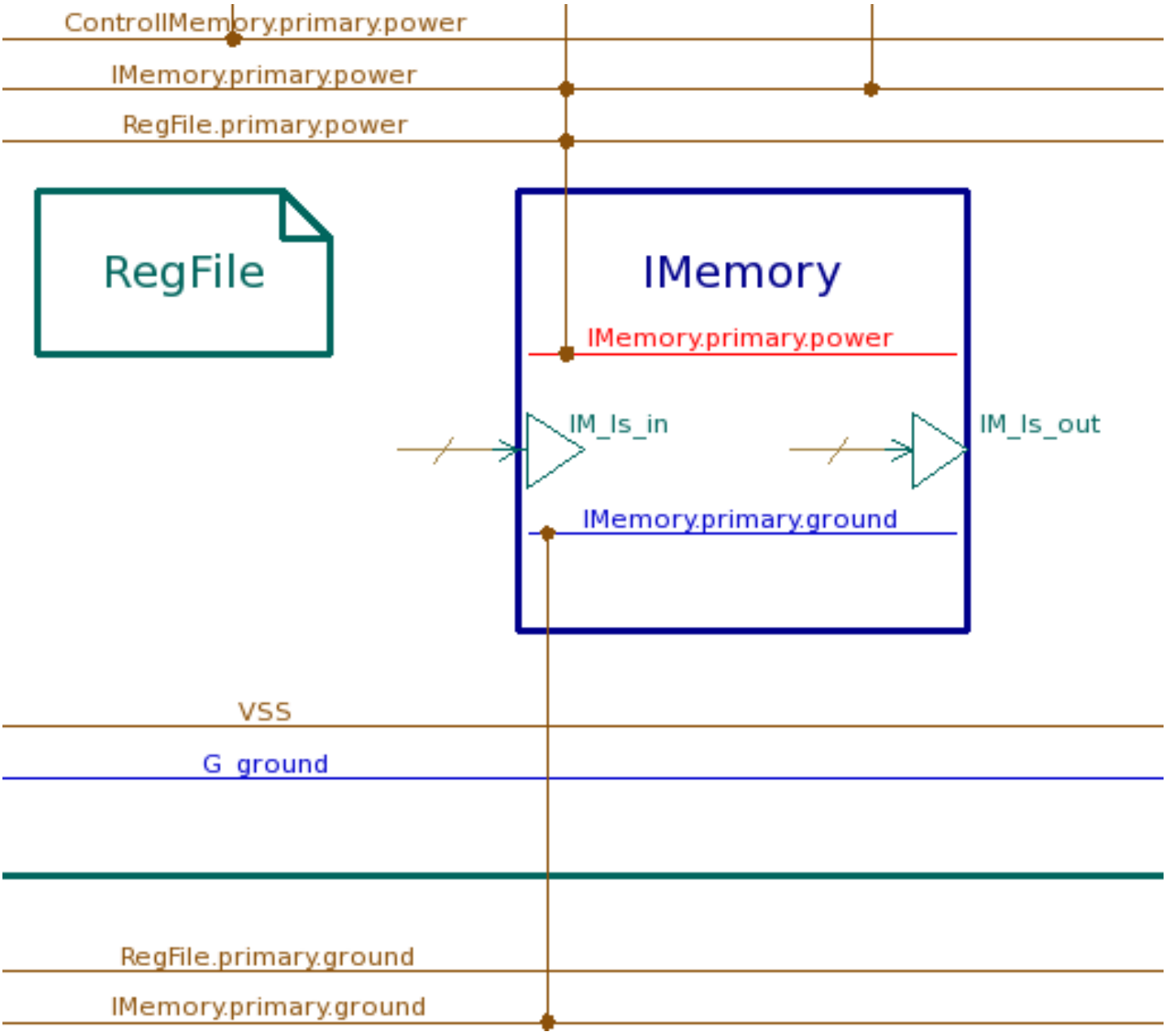
4.1 ControllMemory



4.2 RegFile


TOP
VDD_HIGH
VDD_power
CPUOff
CPUOff
sw1
ControlIMemory.primary.power
IMemory.primary.power
RegFile.primary.power
RegFile
RegFile.primary.power
Rst
VDD_HIGH
VDD_power
RF_iso_in
RF_Is_out
rst
1
LC
DMWE
RF_retain
rst
RF_Is_in
RegFile.primary.ground
G_ground
VSS
G_ground
RegFile.primary.ground

4.3 IMemory


ControlIMemory.primary.power
IMemory.primary.power
RegFile.primary.power
RegFile
IMemory
IMemory.primary.power
IM_Is_in
IM_Is_out
IMemory.primary.ground
VSS
G_ground
RegFile.primary.ground
IMemory.primary.ground

5. Power Report

5.1 Report result (Good)

```
****************************************
Report : power
        -analysis_effort low
Design : MIPS
Version: I-2013.12-SP5-11
Date   : Wed May 16 18:47:57 2018
****************************************


Library(s) Used:

    gscl45nm (File: /export/opt/FreePDK45/osu_soc/lib/files/gscl45nm.db)
    gtech (File: /export/opt/synopsys/I-2013.12-SP5-11/libraries/syn/gtech.db)


Global Operating Voltage = 1.1
Power-specific unit information :
    Voltage Units = 1V
    Capacitance Units = 1.000000pf
    Time Units = 1ns
    Dynamic Power Units = 1mW    (derived from V,C,T units)
    Leakage Power Units = 1nW


  Cell Internal Power  = 766.1342 uW     (0%)
  Net Switching Power  = 592.1776 mW   (100%)
                         ---------
Total Dynamic Power    = 592.9437 mW   (100%)

Cell Leakage Power     =  97.0047 uW


                 Internal         Switching           Leakage             Total
Power Group      Power            Power               Power               Power   (   %    )
--------------------------------------------------------------------------------------------
io_pad             0.0000           0.0000              0.0000             0.0000  (  0.00%)
memory             0.0000           0.0000              0.0000             0.0000  (  0.00%)
black_box          0.0000           0.0000              0.0000             0.0000  (  0.00%)
clock_network      0.0000         591.4296              0.0000           591.4296  ( 99.73%)
register           0.4638        9.5207e-03          1.7593e+03            0.4750  (  0.08%)
sequential     2.9194e-03        2.3088e-03             98.0132        5.3262e-03  (  0.00%)
combinational      0.2995           0.7362          9.5147e+04            1.1308  (  0.19%)
--------------------------------------------------------------------------------------------
Total              0.7661 mW       592.1776 mW      9.7005e+04 nW        593.0408 mW
```

5.2 Report result (Before)

```
****************************************
Report : power
        -analysis_effort low
Design : MIPS
Version: I-2013.12-SP5-11
Date   : Wed May 16 15:46:51 2018
****************************************


Library(s) Used:

    gscl45nm (File: /export/opt/FreePDK45/osu_soc/lib/files/gscl45nm.db)
    gtech (File: /export/opt/synopsys/I-2013.12-SP5-11/libraries/syn/gtech.db)


Global Operating Voltage = 1.1
Power-specific unit information :
    Voltage Units = 1V
    Capacitance Units = 1.000000pf
    Time Units = 1ns
    Dynamic Power Units = 1mW    (derived from V,C,T units)
    Leakage Power Units = 1nW

  Cell Internal Power  =   6.5876 uW    (0%)
  Net Switching Power  =   6.1926 mW   (100%)
                         ---------
Total Dynamic Power    =   6.1991 mW   (100%)

Cell Leakage Power     =  48.5175 uW

                 Internal         Switching           Leakage            Total
Power Group      Power            Power               Power              Power   (   %    )
------------------------------------------------------------------------------------------
io_pad             0.0000           0.0000              0.0000           0.0000  (   0.00%)
memory             0.0000           0.0000              0.0000           0.0000  (   0.00%)
black_box          0.0000           0.0000              0.0000           0.0000  (   0.00%)
clock_network      0.0000           6.1857              0.0000           6.1857  (  99.01%)
register       4.6434e-03       1.3678e-04       1.7593e+03       6.5394e-03  (   0.10%)
sequential     3.0520e-05       3.0716e-05          98.0132       1.5925e-04  (   0.00%)
combinational  1.9137e-03       6.6868e-03       4.6660e+04       5.5261e-02  (   0.88%)
------------------------------------------------------------------------------------------
Total          6.5876e-03 mW        6.1926 mW    4.8517e+04 nW        6.2477 mW
```

5.3 Report analyses

- **Why the power is about 6 mW before?**

  I have searched online for power consumption of mips, and I found a word "***If the CPU is a multi-core design, then each core will likely use between 600 to 750 milliwatts***."[(1)] .

  Here are some likely main reasons:

  - My clock period is 100us before, which is a very low frequency, according to $P = CVdd^2f$, the power consumption may be much less, **If I set my clock period to 1us, it will be about 600 milliwatts (shown in 5.1 good).**
  - My design can run limited instruction commands like "add, sub, or ,stl, jump"
  - The size of my Datamemory is 128 *32, which is not big enough

- **Why memory power is zero?**

  There are 7 predefined power groups

  - ** io_pad: cells defined as part of the pad_cell group in the library.*
  - ** memory: cells defined as part of the memory group in the library.*
  - ** black_box: cells with no functional description in the library.*
  - ** clock_network: cells in the clock_network excluding io_pad cells.*
  - ** register: latches and flip flops driven by the clock network excluding io_pads and black_boxes.*
  - ** combinational: non-sequential cells with a functional description.*
  - ** sequential: latches and flip flops clocked by signals other than those in the clock network.*

The reason why memory power is 0 is that library file (gscl45nm) did not group any module in 'memory' group when compiling.

- **What is the difference between Inverter and level-shifter?**
  - Inverter can be used when going from high to low (as long as you mantain reliability). We cannot use it when going from low to high because the pmos won't switch off.
  - level-shifter may be used in most cases.

- **Why clock power takes more than 99% while sequential and combinational takes less than 1%?**
  - In my instruction memory, I have only 12 instructions and the rest of the time, the processor do nothing but changing clock.
  - The clock power mainly used to change clock
  - The sequential or combinational power mainly used to run instructions.
- **In order to change the power from 0.02mW (presentation on May 16th) to 6.2mW, what did you modified in UPF file?**

  I found that most of the registers were removed during compiling, so I use another command to let complier does not touch it, the command is:

  set_dont_touch [get_designs Shifter_2]

5.4 Additional Report information

```
                                TOTAL
 ELAPSED              WORST NEG  SETUP    DESIGN
  TIME       AREA      SLACK     COST    RULE COST          ENDPOINT
--------- --------- --------- --------- --------- -------------------------
  0:03:35   19022.6      0.31     234.7      12.3
  0:03:35   19022.6      0.31     234.7      12.3
  0:03:35   19022.6      0.31     234.7      12.3
  0:03:35   19022.6      0.31     234.7      12.3
Re-synthesis Optimization (Phase 1)
Re-synthesis Optimization (Phase 2)
Global Optimization (Phase 1)
Global Optimization (Phase 2)
Global Optimization (Phase 3)
Global Optimization (Phase 4)
Global Optimization (Phase 5)
Global Optimization (Phase 6)
Global Optimization (Phase 7)
Global Optimization (Phase 8)
Global Optimization (Phase 9)
Global Optimization (Phase 10)
Global Optimization (Phase 11)
Global Optimization (Phase 12)
Global Optimization (Phase 13)
Global Optimization (Phase 14)
Global Optimization (Phase 15)
Global Optimization (Phase 16)
Global Optimization (Phase 17)
Global Optimization (Phase 18)
Global Optimization (Phase 19)
Global Optimization (Phase 20)
Global Optimization (Phase 21)
```

```
Global Optimization (Phase 22)
Global Optimization (Phase 23)
Global Optimization (Phase 24)
Global Optimization (Phase 25)
Global Optimization (Phase 26)
Global Optimization (Phase 27)
Global Optimization (Phase 28)
Global Optimization (Phase 29)
Global Optimization (Phase 30)
Mapping 'MIPS_DW01_add_4'
  0:04:46   16950.6      0.06      36.0      11.3


Beginning Delay Optimization Phase
----------------------------------

                                TOTAL
 ELAPSED            WORST NEG   SETUP    DESIGN
  TIME      AREA      SLACK     COST    RULE COST         ENDPOINT
--------- --------- --------- --------- --------- -------------------------
  0:04:46   16950.6      0.06      36.0      11.3
  0:04:49   17069.8      0.03      16.1      11.2
  0:04:51   17173.6      0.02       9.0      11.2
  0:04:53   17192.8      0.02       7.2      11.2
  0:04:54   17208.3      0.02       6.2      11.2
  0:04:58   17317.2      0.01       4.4      11.3
  0:04:59   17317.2      0.01       4.4      11.3
  0:04:59   17317.2      0.01       4.4      11.3
  0:04:59   17317.2      0.01       4.4      11.3
  0:05:01   17317.2      0.01       4.4      11.3
  0:05:01   17317.2      0.01       4.4      11.3
  0:05:11   17345.8      0.00       0.0      11.4
  0:05:11   17345.8      0.00       0.0      11.4
  0:05:11   17345.8      0.00       0.0      11.4

Beginning Delay Optimization
----------------------------
  0:05:11   17345.8      0.00       0.0      11.4
  0:05:11   17345.8      0.00       0.0      11.4
  0:05:11   17345.8      0.00       0.0      11.4
  0:05:11   17345.8      0.00       0.0      11.4
  0:05:11   17345.8      0.00       0.0      11.4
  0:05:11   17345.8      0.00       0.0      11.4
  0:05:11   17345.8      0.00       0.0      11.4
  0:05:11   17345.8      0.00       0.0      11.4


Beginning Design Rule Fixing  (max_capacitance)
----------------------------

                                TOTAL
 ELAPSED            WORST NEG   SETUP    DESIGN
  TIME      AREA      SLACK     COST    RULE COST         ENDPOINT
--------- --------- --------- --------- --------- -------------------------
  0:05:11   17345.8      0.00       0.0      11.4
Global Optimization (Phase 31)
Global Optimization (Phase 32)
Global Optimization (Phase 33)
  0:05:21   18115.0      0.03      11.8      10.3 RegisterFile/net237336
  0:05:22   19012.8      0.03      12.0       9.8 RegisterFile/net238095
  0:05:23   19567.0      0.03      11.9       9.6 RegisterFile/net237048
  0:05:24   20348.8      0.03      11.9       9.3 RegisterFile/net238543
```

0:05:25	22081.5	0.03	11.9	8.5	RegisterFile/net239697
0:05:27	23586.1	0.03	11.9	7.9	RegisterFile/net237265
0:05:28	24130.9	0.03	11.9	7.7	RegisterFile/net238607
0:05:28	24359.0	0.03	11.9	7.7	RegisterFile/net239640
0:05:29	24602.6	0.03	11.9	7.7	RegisterFile/net235095
0:05:30	25299.5	0.03	11.9	7.5	RegisterFile/net237366
0:05:31	25697.0	0.03	11.6	7.4	RegisterFile/net236733
0:05:32	25703.6	0.03	11.6	7.4	RegisterFile/net242085
0:05:32	25731.2	0.02	8.8	7.4	RegisterFile/net236436
0:05:34	25733.6	0.02	8.8	7.4	RegisterFile/net235243
0:05:35	26008.1	0.02	8.8	7.0	sub_x_7/net240880
0:05:37	26675.5	0.02	7.5	6.4	add_x_6/net240656
0:05:38	27287.9	0.02	7.1	6.2	add_x_6/net240618
0:05:40	27305.8	0.02	6.9	6.2	RegisterFile/net238215
0:05:41	27402.0	0.02	6.9	6.1	RegisterFile/net244147
0:05:42	27495.3	0.02	6.9	6.1	RegisterFile/net241355
0:05:43	27621.1	0.02	6.7	6.1	RegisterFile/net235780
0:05:44	27669.9	0.02	6.7	6.1	RegisterFile/net239355
0:05:45	27707.5	0.02	6.7	6.0	RegisterFile/net236406
0:05:46	27704.7	0.02	6.7	6.0	RegisterFile/net239216
0:05:48	27702.3	0.02	6.7	6.0	sub_x_7/net241009
0:05:49	27705.6	0.02	6.5	6.0	sub_x_7/net241004
0:05:52	27713.1	0.02	6.3	6.0	RegisterFile/reg30_reg[31]/next_state
0:05:54	27745.5	0.01	2.3	6.0	RegisterFile/reg30_reg[23]/next_state
0:05:55	27821.0	0.00	1.6	6.0	RegisterFile/reg30_reg[29]/next_state
0:05:57	27846.4	0.00	0.3	6.0	RegisterFile/reg30_reg[25]/next_state
0:06:00	27861.9	0.02	9.0	6.0	RegisterFile/net237996
0:06:04	28729.1	0.26	205.7	5.2	RegisterFile/net238359
0:06:08	29796.8	0.26	219.3	4.3	RegisterFile/net240122
0:06:11	30785.6	0.31	272.3	3.8	RegisterFile/net235922
0:06:12	31749.1	0.31	277.7	3.1	RegisterFile/net241214
0:06:17	32267.7	0.32	296.2	2.7	InstructionMemory/IMRD[23]
0:06:19	32331.5	0.33	299.7	2.7	RegisterFile/net235450
0:06:23	32939.7	0.46	402.1	2.1	sub_x_7/net241128
0:06:26	33052.8	0.42	370.0	2.0	RegisterFile/reg21_reg[22]/next_state
0:06:28	33042.9	0.37	332.0	2.0	RegisterFile/reg21_reg[29]/next_state
0:06:31	32995.5	0.35	316.5	2.0	RegisterFile/reg21_reg[22]/next_state
0:06:33	32967.4	0.33	302.5	2.0	RegisterFile/reg21_reg[22]/next_state
0:06:36	32939.7	0.32	288.9	2.0	RegisterFile/reg5_reg[25]/next_state
0:06:38	32944.9	0.31	282.4	2.0	RegisterFile/reg5_reg[29]/next_state
0:06:40	32917.6	0.30	276.1	2.0	RegisterFile/reg21_reg[27]/next_state
0:06:41	32913.9	0.30	275.0	2.0	RegisterFile/reg21_reg[27]/next_state
0:06:46	32928.0	0.34	300.1	2.0	RegisterFile/net237597
0:06:48	32926.1	0.34	300.1	1.9	net234896
0:06:50	32919.0	0.34	300.1	1.9	
0:06:54	29255.2	0.33	298.3	1.9	
0:06:54	29255.2	0.33	298.3	1.9	
0:06:56	29001.8	0.32	288.7	1.9	
0:06:57	27959.5	0.32	273.8	1.9	
0:06:58	27429.6	0.32	272.5	1.9	
0:06:59	26186.9	0.31	270.8	1.9	
0:07:00	25995.5	0.30	266.7	1.9	RegisterFile/reg17_reg[21]/next_state
0:07:01	26000.6	0.29	260.0	1.9	
0:09:07	23642.9	0.03	21.8	7.7	

ELAPSED TIME	AREA	WORST NEG SLACK	TOTAL SETUP COST	DESIGN RULE COST	ENDPOINT
0:09:08	23642.9	0.03	21.8	7.7	
0:09:08	23642.9	0.03	21.8	7.7	

Information: Total 0 level shifters are removed incrementally. (MV-238)

```
Information: Total 0 level shifters are inserted incrementally. (MV-239)
    0:09:12   23768.6      0.03      19.3       7.7


  Beginning Area-Recovery Phase  (max_area 0)
  ----------------------------

                                    TOTAL
   ELAPSED            WORST NEG     SETUP    DESIGN
     TIME      AREA      SLACK       COST    RULE COST          ENDPOINT
  --------- --------- --------- --------- --------- -------------------------
    0:09:12   23768.6      0.03      19.3       7.7
  Global Optimization (Phase 34)
  Global Optimization (Phase 35)
  Global Optimization (Phase 36)
  Global Optimization (Phase 37)
  Global Optimization (Phase 38)
  Global Optimization (Phase 39)
  Global Optimization (Phase 40)
  Global Optimization (Phase 41)
  Global Optimization (Phase 42)
  Global Optimization (Phase 43)
  Global Optimization (Phase 44)
  Global Optimization (Phase 45)
  Global Optimization (Phase 46)
  Global Optimization (Phase 47)
  Global Optimization (Phase 48)
  Global Optimization (Phase 49)
  Global Optimization (Phase 50)
  Global Optimization (Phase 51)
  Global Optimization (Phase 52)
  Global Optimization (Phase 53)
  Global Optimization (Phase 54)
  Global Optimization (Phase 55)
  Global Optimization (Phase 56)
  Global Optimization (Phase 57)
  Global Optimization (Phase 58)
  Global Optimization (Phase 59)
  Global Optimization (Phase 60)
  Global Optimization (Phase 61)
  Global Optimization (Phase 62)
  Global Optimization (Phase 63)
  Global Optimization (Phase 64)
  Global Optimization (Phase 65)
  Global Optimization (Phase 66)
    0:09:49   26689.1      0.48     404.3       2.0 RegisterFile/reg17_reg[31]/next_state
    0:09:49   26694.7      0.48     402.6       2.0
    0:11:29   24494.2      0.05      32.5       7.7
    0:11:32   24571.1      0.04      23.0       7.5
    0:11:34   24616.7      0.03      17.3       7.4
    0:11:35   24677.7      0.02      13.2       7.3
    0:11:37   24714.7      0.02      10.3       7.3
    0:11:38   24742.4      0.02       8.7       7.3
    0:11:39   24756.5      0.02       8.6       7.2
    0:11:39   24781.4      0.02       6.9       7.2
    0:11:40   24781.4      0.02       6.7       7.2
    0:11:49   24694.1      0.01       3.6       7.5
    0:11:49   24694.1      0.01       3.6       7.5
    0:11:49   24694.1      0.01       3.3       7.5
    0:11:49   24694.1      0.01       3.3       7.5
    0:11:57   24652.8      0.01       1.9       7.6
    0:11:57   24652.8      0.01       1.9       7.6
    0:12:03   24606.8      0.00       0.0       7.7
```

```
    0:12:03   24606.8      0.00       0.0       7.7
    0:12:03   24606.8      0.00       0.0       7.7
    0:12:03   24606.8      0.00       0.0       7.7
    0:12:03   24606.8      0.00       0.0       7.7
    0:12:03   24606.8      0.00       0.0       7.7
    0:12:03   24606.8      0.00       0.0       7.7
    0:12:03   24606.8      0.00       0.0       7.7
    0:12:03   24606.8      0.00       0.0       7.7
    0:12:03   24606.8      0.00       0.0       7.7
    0:12:03   24606.8      0.00       0.0       7.7
Loading db file '/export/opt/FreePDK45/osu_soc/lib/files/gscl45nm.db'

  Optimization Complete
  ---------------------
```

6. Reference

(1) https://www.androidauthority.com/arms-secret-recipe-for-power-efficient-processing-409850/