Project 2

Timing Analysis Report

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EE-670

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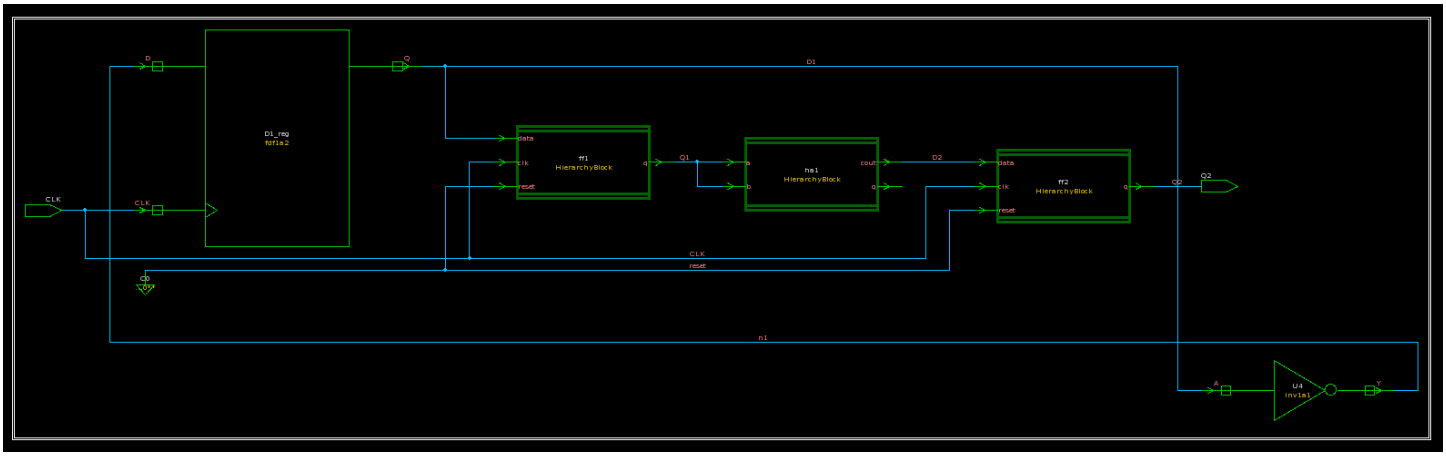
1. Positive flip-flop to Positive flip-flop

1.1. Module Figure



1.2. Module Verilog file

```
`timescale 1ns/1ns

module time_test (

output Q2 ,
input CLK
);

reg  D1;
wire Q1, D2;
reg reset;

dff ff1 (.data(D1), .clk(CLK), .q(Q1), .reset(reset));
dff ff2 (.data(D2), .clk(CLK), .q(Q2), .reset(reset));
halfadder      ha1 (.a(Q1), .b(Q1), .cout(D2));

initial D1 =1;
always @(posedge CLK)
 begin D1 <=  ~D1;
end


endmodule

module dff (
data    , // Data Input
clk     , // Clock Input
reset   , // Reset input
q         // Q output
```

```
);
//-----------Input Ports--------------
input data, clk, reset ;

//-----------Output Ports---------------
output q;

//------------Internal Variables--------
reg q;

//-------------Code Starts Here---------
always @ ( posedge clk)
if (~reset) begin
  q <= 1'b0;
end  else begin
  q <= data;
end

endmodule //End Of Module dff_sync_reset


module halfadder(
a ,
b ,
cout,
q
);
input a,b;
output cout,q;

assign cout = a ^ b;
assign q    = a & b;

endmodule
```

1.3. Module netlist file

```
module dff_0 ( data, clk, reset, q );
  input data, clk, reset;
  output q;
  wire   N3;

  fdf1a2 q_reg ( .D(N3), .CLK(clk), .Q(q) );
  and2a3 U3 ( .A(reset), .B(data), .Y(N3) );
endmodule


module halfadder ( a, b, cout, q );
  input a, b;
  output cout, q;


  and2a3 U1 ( .A(b), .B(a), .Y(q) );
  xor2a1 U2 ( .A(b), .B(a), .Y(cout) );
endmodule


module dff_1 ( data, clk, reset, q );
  input data, clk, reset;
  output q;
  wire   N3;

  fdf1a2 q_reg ( .D(N3), .CLK(clk), .Q(q) );
  and2a3 U3 ( .A(reset), .B(data), .Y(N3) );
endmodule


module time_test ( Q2, CLK );
  input CLK;
  output Q2;
  wire   D1, Q1, D2, n1;

  dff_0 ff1 ( .data(D1), .clk(CLK), .reset(1'b0), .q(Q1) );
  dff_1 ff2 ( .data(D2), .clk(CLK), .reset(1'b0), .q(Q2) );
  halfadder ha1 ( .a(Q1), .b(Q1), .cout(D2) );
  fdf1a2 D1_reg ( .D(n1), .CLK(CLK), .Q(D1) );
  inv1a1 U4 ( .A(D1), .Y(n1) );
endmodule
```

1.4. Library file

Link library /home/zhang/Asic/time/libs/core_typ.db

Target library /home/zhang/Asic/time/libs/core_typ.db

Symbol library /home/zhang/Asic/time/libs/core.sdb

1.5. Setup time check(met)

1.5.1. Setup time check script file

```
# Create user defined variables
set CLK_PORT [get_ports CLK]
set CLK_PERIOD 5.00
set CLK_SKEW 0.14

set INPUT_DELAY 0.1

set OUTPUT_DELAY 0.5

set MAX_AREA 380000

# Time Budget
create_clock -period $CLK_PERIOD -name my_clock $CLK_PORT
set_dont_touch_network my_clock

create_clock -period $CLK_PERIOD -name CLKP [get_ports CLK]

set_multicycle_path 2 -from [get_pins ff1/clk] -to [get_pins ff2/data]


set library_setup_time 0.04
set_clock_uncertainty -setup 0.4 $CLK_PORT

set_clock_latency 1.0 $CLK_PORT
set_clock_uncertainty -hold 0.54 $CLK_PORT

#set_input_delay $INPUT_DELAY -max -clock my_clock [remove_from_collection [all_inputs]
$CLK_PORT]
#set_output_delay $OUTPUT_DELAY -max -clock my_clock [all_outputs]

set library_hold_time 0.01
```

1.5.2. Setup time check result

```
Startpoint: D1_reg (rising edge-triggered flip-flop clocked by CLKP)
 Endpoint: D1_reg (rising edge-triggered flip-flop clocked by CLKP)
 Path Group: CLKP
 Path Type: max

 Des/Clust/Port     Wire Load Model       Library
 ------------------------------------------------
 time_test          5KGATES               ssc_core

 Point                                    Incr       Path
 ----------------------------------------------------------
 clock CLKP (rise edge)                   0.00       0.00
 clock network delay (ideal)              1.00       1.00
 D1_reg/CLK (fdf1a2)                      0.00       1.00 r
 D1_reg/Q (fdf1a2)                        0.62       1.62 f
 U4/Y (inv1a1)                            0.51       2.13 r
 D1_reg/D (fdf1a2)                        0.00       2.13 r
 data arrival time                                   2.13

 clock CLKP (rise edge)                   5.00       5.00
 clock network delay (ideal)              1.00       6.00
 clock uncertainty                       -0.40       5.60
 D1_reg/CLK (fdf1a2)                      0.00       5.60 r
 library setup time                      -0.17       5.43
 data required time                                  5.43
 ----------------------------------------------------------
 data required time                                  5.43
 data arrival time                                  -2.13
 ----------------------------------------------------------
 slack (MET)                                         3.31
```

1.6. Setup time check (violated)

1.6.1. Setup time check script file

```
# Create user defined variables
set CLK_PORT [get_ports CLK]
set CLK_PERIOD 1.00
set CLK_SKEW 0.14


set INPUT_DELAY 0.1

set OUTPUT_DELAY 0.5

set MAX_AREA 380000


# Time Budget
create_clock -period $CLK_PERIOD -name my_clock $CLK_PORT
set_dont_touch_network my_clock

create_clock -period $CLK_PERIOD -name CLKP [get_ports CLK]

set_multicycle_path 2 -from [get_pins ff1/clk] -to [get_pins ff2/data]


set library_setup_time 0.04
set_clock_uncertainty -setup 0.4 $CLK_PORT

set_clock_latency 1.0 $CLK_PORT
set_clock_uncertainty -hold 0.54 $CLK_PORT


set library_hold_time 0.01
```

1.6.2. Setup time check result

```
Startpoint: D1_reg (rising edge-triggered flip-flop clocked by CLKP)
 Endpoint: D1_reg (rising edge-triggered flip-flop clocked by CLKP)
 Path Group: CLKP
 Path Type: max

 Des/Clust/Port     Wire Load Model       Library
 ------------------------------------------------
 time_test          5KGATES               ssc_core

 Point                                    Incr       Path
 -----------------------------------------------------------
 clock CLKP (rise edge)                   0.00       0.00
 clock network delay (ideal)              1.00       1.00
 D1_reg/CLK (fdf1a2)                      0.00       1.00 r
 D1_reg/Q (fdf1a2)                        0.62       1.62 f
 U4/Y (inv1a1)                            0.51       2.13 r
 D1_reg/D (fdf1a2)                        0.00       2.13 r
 data arrival time                                   2.13

 clock CLKP (rise edge)                   1.00       1.00
 clock network delay (ideal)              1.00       2.00
 clock uncertainty                       -0.40       1.60
 D1_reg/CLK (fdf1a2)                      0.00       1.60 r
 library setup time                      -0.17       1.43
 data required time                                  1.43
 -----------------------------------------------------------
 data required time                                  1.43
 data arrival time                                  -2.13
 -----------------------------------------------------------
 slack (VIOLATED)                                   -0.69
```

1.7. Hold time check(met)

1.7.1. Hold time check script file

```
# Create user defined variables
set CLK_PORT [get_ports CLK]
set CLK_PERIOD 4.00
set CLK_SKEW 0.14


set INPUT_DELAY 2.0

set OUTPUT_DELAY 0.5

set MAX_AREA 380000


# Time Budget
create_clock -period $CLK_PERIOD -name my_clock $CLK_PORT
set_dont_touch_network my_clock
set_clock_uncertainty $CLK_SKEW [get_clocks my_clock]

set library_setup_time 0.04
set_clock_uncertainty -setup 0.4 $CLK_PORT

set_clock_latency 2.0 $CLK_PORT
set_clock_uncertainty -hold 0.14 $CLK_PORT

#set_input_delay $INPUT_DELAY -max -clock my_clock [remove_from_collection [all_inputs]
$CLK_PORT]
#set_output_delay $OUTPUT_DELAY -max -clock my_clock [all_outputs]

set library_hold_time 0.51
```

1.7.2. Hold time check result

```
Startpoint: D1_reg (rising edge-triggered flip-flop clocked by my_clock)
  Endpoint: D1_reg (rising edge-triggered flip-flop clocked by my_clock)
  Path Group: my_clock
  Path Type: min

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  time_test          5KGATES               ssc_core

  Point                                    Incr       Path
  -----------------------------------------------------------
  clock my_clock (rise edge)               0.00       0.00
  clock network delay (ideal)              2.00       2.00
  D1_reg/CLK (fdf1a2)                      0.00       2.00 r
  D1_reg/Q (fdf1a2)                        0.55       2.55 r
  U4/Y (inv1a1)                            0.37       2.92 f
  D1_reg/D (fdf1a2)                        0.00       2.92 f
  data arrival time                                   2.92

  clock my_clock (rise edge)               0.00       0.00
  clock network delay (ideal)              2.00       2.00
  clock uncertainty                        0.14       2.14
  D1_reg/CLK (fdf1a2)                      0.00       2.14 r
  library hold time                        0.32       2.46
  data required time                                  2.46
  -----------------------------------------------------------
  data required time                                  2.46
  data arrival time                                  -2.92
  -----------------------------------------------------------
  slack (MET)                                         0.46
```

1.8. Hold time check(violated)

1.8.1. Hold time check script file

```
# Create user defined variables
set CLK_PORT [get_ports CLK]
set CLK_PERIOD 4.00
set CLK_SKEW 0.14


set INPUT_DELAY 2.0

set OUTPUT_DELAY 0.5

set MAX_AREA 380000


# Time Budget
create_clock -period $CLK_PERIOD -name my_clock $CLK_PORT
set_dont_touch_network my_clock
set_clock_uncertainty $CLK_SKEW [get_clocks my_clock]

set library_setup_time 0.04
set_clock_uncertainty -setup 0.4 $CLK_PORT

set_clock_latency 3.0 $CLK_PORT
set_clock_uncertainty -hold 0.84 $CLK_PORT

#set_input_delay $INPUT_DELAY -max -clock my_clock [remove_from_collection [all_inputs]
$CLK_PORT]
#set_output_delay $OUTPUT_DELAY -max -clock my_clock [all_outputs]

set library_hold_time 1.51
```

1.8.2. Hold time check result

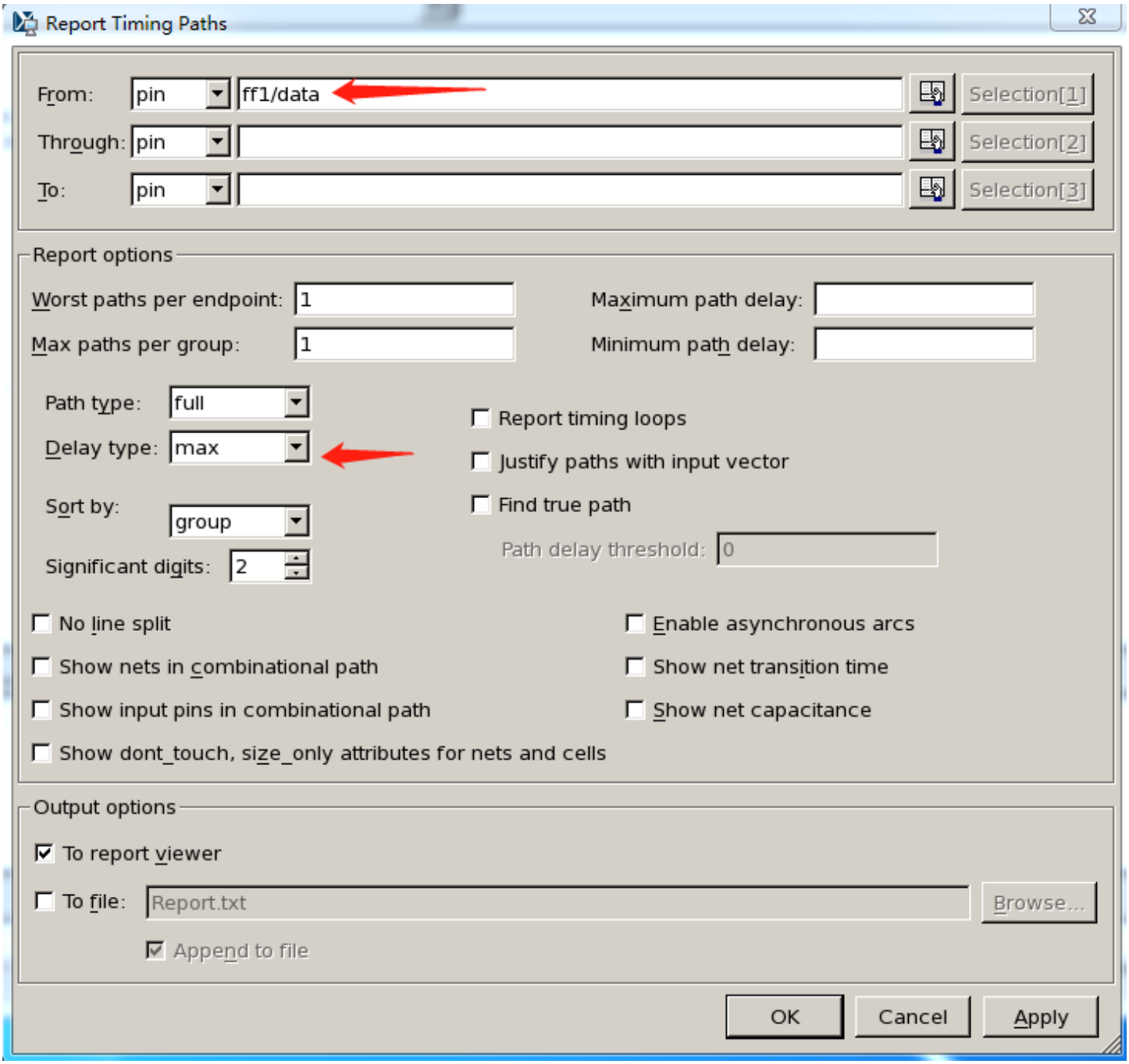
```
Startpoint: D1_reg (rising edge-triggered flip-flop clocked by my_clock)
  Endpoint: D1_reg (rising edge-triggered flip-flop clocked by my_clock)
  Path Group: my_clock
  Path Type: min

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  time_test          5KGATES               ssc_core

  Point                                    Incr       Path
  -----------------------------------------------------------
  clock my_clock (rise edge)               0.00       0.00
  clock network delay (ideal)              3.00       3.00
  D1_reg/CLK (fdf1a2)                      0.00       3.00 r
  D1_reg/Q (fdf1a2)                        0.55       3.55 r
  U4/Y (inv1a1)                            0.37       3.92 f
  D1_reg/D (fdf1a2)                        0.00       3.92 f
  data arrival time                                   3.92

  clock my_clock (rise edge)               0.00       0.00
  clock network delay (ideal)              3.00       3.00
  clock uncertainty                        0.84       3.84
  D1_reg/CLK (fdf1a2)                      0.00       3.84 r
  library hold time                        0.32       4.16
  data required time                                  4.16
  -----------------------------------------------------------
  data required time                                  4.16
  data arrival time                                  -3.92
  -----------------------------------------------------------
  slack (VIOLATED)                                   -0.24
```

1.9. Input delay(met)

1.9.1. Input delay script file

```
# Create user defined variables
set CLK_PORT [get_ports CLK]
set CLK_PERIOD 3.00
set CLK_SKEW 0.14

set_clock_uncertainty -setup 0.4 $CLK_PORT

set_clock_latency 1.0 $CLK_PORT
set_clock_uncertainty -hold 0.54 $CLK_PORT


create_clock -name theclk -period 20 [get_ports CLK]

set_input_delay -clock theclk -max 4 [get_ports  ff1/data]
set_input_delay -clock theclk -min 2 [get_ports  ff1/data]
```

1.9.2. Input delay settings



1.9.3. Input delay result

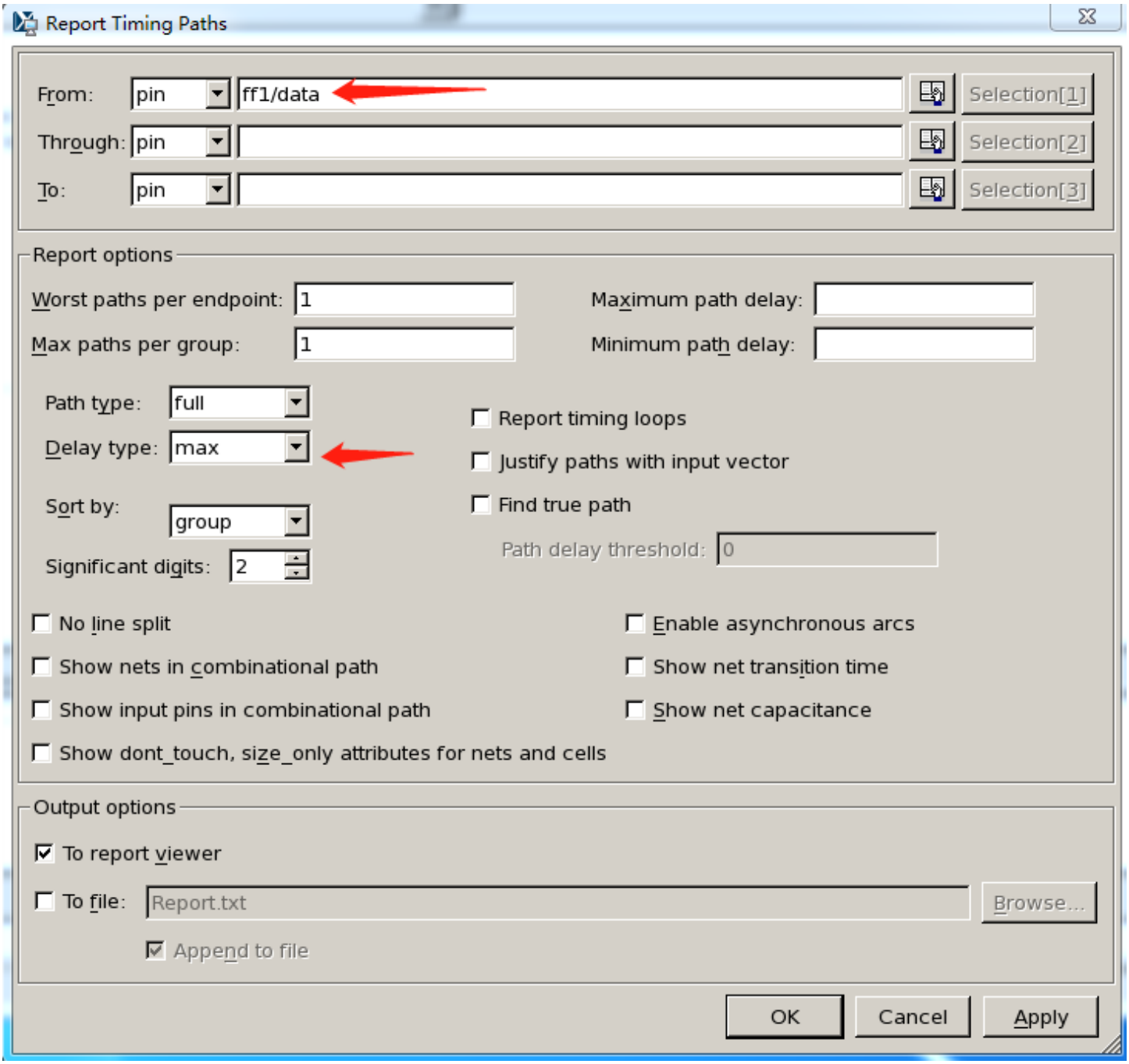
```
Startpoint: ff1/data (internal path startpoint clocked by theclk)
Endpoint: ff1/q_reg (rising edge-triggered flip-flop clocked by theclk)
Path Group: theclk
Path Type: max

Des/Clust/Port     Wire Load Model       Library
------------------------------------------------
time_test          5KGATES               ssc_core
dff                5KGATES               ssc_core

Point                                    Incr       Path
-----------------------------------------------------------
clock theclk (rise edge)                 0.00       0.00
clock network delay (ideal)              0.00       0.00
input external delay                     4.00       4.00 r
ff1/data (dff)                           0.00       4.00 r
ff1/C11/Z_0 (*SELECT_OP_2.1_2.1_1)       0.00       4.00 r
ff1/q_reg/next_state (**SEQGEN**)        0.00       4.00 r
data arrival time                                   4.00

clock theclk (rise edge)                20.00      20.00
clock network delay (ideal)              1.00      21.00
clock uncertainty                       -0.40      20.60
ff1/q_reg/clocked_on (**SEQGEN**)        0.00      20.60 r
library setup time                       0.00      20.60
data required time                                 20.60
-----------------------------------------------------------
data required time                                 20.60
data arrival time                                  -4.00
-----------------------------------------------------------
slack (MET)                                        16.60
```

1.10. Input delay(violated)

1.10.1. Input delay script file

```
# Create user defined variables
set CLK_PORT [get_ports CLK]
set CLK_PERIOD 3.00
set CLK_SKEW 0.14

set_clock_uncertainty -setup 0.4 $CLK_PORT

set_clock_latency 1.0 $CLK_PORT
set_clock_uncertainty -hold 0.54 $CLK_PORT


create_clock -name theclk -period 3 [get_ports CLK]

set_input_delay -clock theclk -max 4 [get_ports  ff1/data]
set_input_delay -clock theclk -min 2 [get_ports  ff1/data]
```

1.10.2. Input delay settings



1.10.3. Input delay result

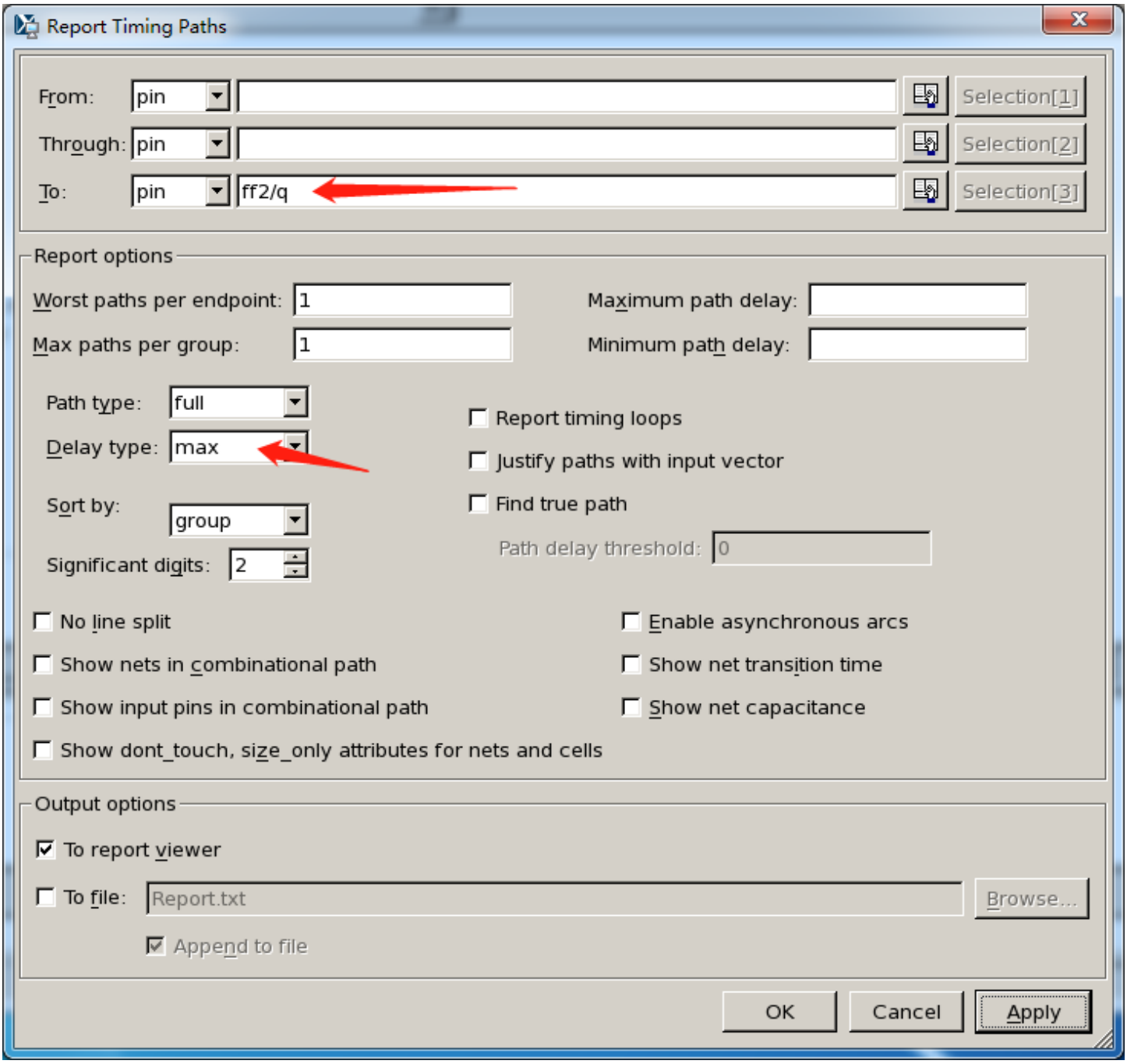
```
Startpoint: ff1/data (internal path startpoint clocked by theclk)
 Endpoint: ff1/q_reg (rising edge-triggered flip-flop clocked by theclk)
 Path Group: theclk
 Path Type: max

 Des/Clust/Port     Wire Load Model       Library
 ------------------------------------------------
 time_test          5KGATES               ssc_core
 dff                5KGATES               ssc_core

 Point                                    Incr       Path
 -----------------------------------------------------------
 clock theclk (rise edge)                 0.00       0.00
 clock network delay (ideal)              0.00       0.00
 input external delay                     4.00       4.00 r
 ff1/data (dff)                           0.00       4.00 r
 ff1/C11/Z_0 (*SELECT_OP_2.1_2.1_1)       0.00       4.00 r
 ff1/q_reg/next_state (**SEQGEN**)        0.00       4.00 r
 data arrival time                                   4.00

 clock theclk (rise edge)                 3.00       3.00
 clock network delay (ideal)              1.00       4.00
 clock uncertainty                       -0.40       3.60
 ff1/q_reg/clocked_on (**SEQGEN**)        0.00       3.60 r
 library setup time                       0.00       3.60
 data required time                                  3.60
 -----------------------------------------------------------
 data required time                                  3.60
 data arrival time                                  -4.00
 -----------------------------------------------------------
 slack (VIOLATED)                                   -0.40
```

1.11. output delay(met)

1.11.1. output delay script file

```
# Create user defined variables
set CLK_PORT [get_ports CLK]
set CLK_PERIOD 3.00
set CLK_SKEW 0.14

set_clock_uncertainty -setup 0.4 $CLK_PORT

set_clock_latency 1.0 $CLK_PORT
set_clock_uncertainty -hold 0.54 $CLK_PORT


create_clock -name theclk -period 20 [get_ports CLK]
set_output_delay -clock theclk -max 8 [get_ports  ff2/q]
set_output_delay -clock theclk -min -3 [get_ports ff2/q]
```

1.11.2. output delay settings



1.11.3. Input delay result

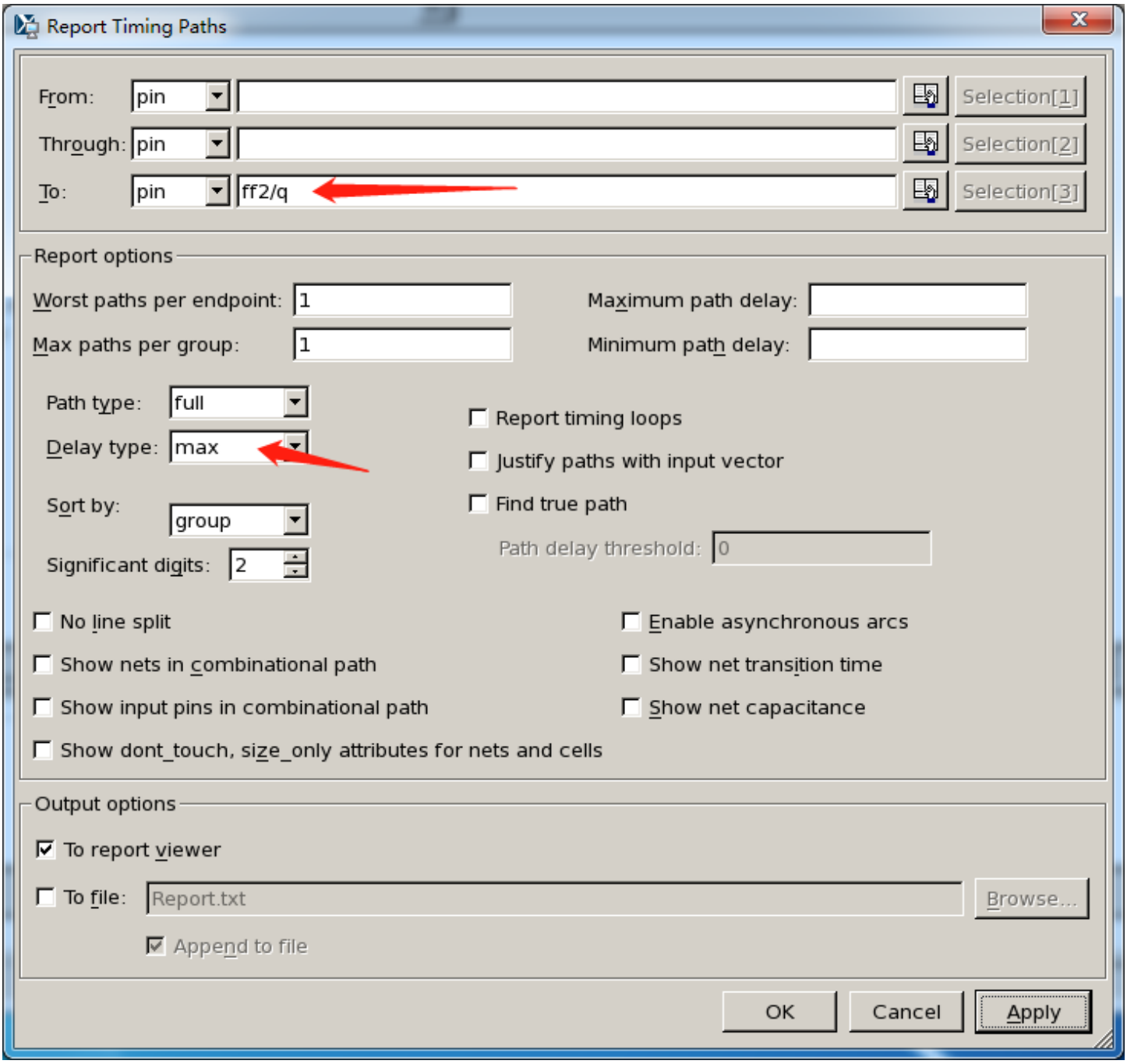
```
Startpoint: ff2/q_reg (rising edge-triggered flip-flop clocked by theclk)
  Endpoint: ff2/q (internal path endpoint clocked by theclk)
  Path Group: theclk
  Path Type: max

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  time_test          5KGATES               ssc_core

  Point                                    Incr       Path
  -----------------------------------------------------------
  clock theclk (rise edge)                 0.00       0.00
  clock network delay (ideal)              1.00       1.00
  ff2/q_reg/clocked_on (**SEQGEN**)        0.00       1.00 r
  ff2/q_reg/Q (**SEQGEN**)                 0.00       1.00 r
  ff2/q (dff)                              0.00       1.00 r
  data arrival time                                   1.00

  clock theclk (rise edge)                20.00      20.00
  clock network delay (ideal)              0.00      20.00
  output external delay                   -8.00      12.00
  data required time                                  12.00
  -----------------------------------------------------------
  data required time                                  12.00
  data arrival time                                   -1.00
  -----------------------------------------------------------
  slack (MET)                                         11.00
```

1.12. output delay(violated)

1.12.1. output delay script file

```
# Create user defined variables
set CLK_PORT [get_ports CLK]
set CLK_PERIOD 3.00
set CLK_SKEW 0.14

set_clock_uncertainty -setup 0.4 $CLK_PORT

set_clock_latency 1.0 $CLK_PORT
set_clock_uncertainty -hold 0.54 $CLK_PORT


create_clock -name theclk -period 5 [get_ports CLK]
set_output_delay -clock theclk -max 8 [get_ports  ff2/q]
set_output_delay -clock theclk -min -3 [get_ports ff2/q]
```

1.12.2. output delay settings

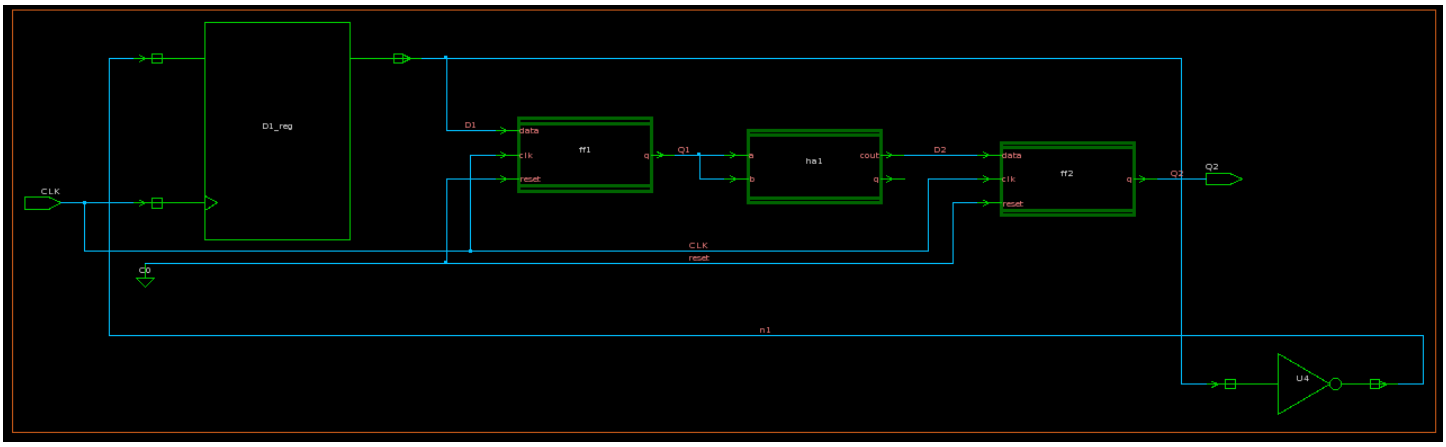


1.12.3. Input delay result

```
Startpoint: ff2/q_reg (rising edge-triggered flip-flop clocked by theclk)
 Endpoint: ff2/q (internal path endpoint clocked by theclk)
 Path Group: theclk
 Path Type: max

 Des/Clust/Port     Wire Load Model       Library
 ------------------------------------------------
 time_test          5KGATES               ssc_core

 Point                                    Incr       Path
 -----------------------------------------------------------
 clock theclk (rise edge)                 0.00       0.00
 clock network delay (ideal)              1.00       1.00
 ff2/q_reg/clocked_on (**SEQGEN**)        0.00       1.00 r
 ff2/q_reg/Q (**SEQGEN**)                 0.00       1.00 r
 ff2/q (dff)                              0.00       1.00 r
 data arrival time                                   1.00

 clock theclk (rise edge)                 5.00       5.00
 clock network delay (ideal)              0.00       5.00
 output external delay                   -8.00      -3.00
 data required time                                 -3.00
 -----------------------------------------------------------
 data required time                                 -3.00
 data arrival time                                  -1.00
 -----------------------------------------------------------
 slack (VIOLATED)                                   -4.00
```

2. Positive flip-flop to Negative flip-flop

2.1. module figure



2.2. module Verilog file

```
`timescale 1ns/1ns

module time_test (

output Q2 ,
input CLK
);

reg  D1;
wire Q1, D2;
reg reset;

dff ff1 (.data(D1), .clk(CLK), .q(Q1), .reset(reset));
dff_sync_reset_ne ff2 (.data(D2), .clk(CLK), .q(Q2), .reset(reset));
halfadder      ha1 (.a(Q1), .b(Q1), .cout(D2));

initial D1 =1;
always @(posedge CLK)
 begin D1 <=  ~D1;
end


endmodule

module dff (
data    , // Data Input
clk     , // Clock Input
reset   , // Reset input
q         // Q output
);
//-----------Input Ports---------------
input data, clk, reset ;
```

```
//-----------Output Ports---------------
output q;

//------------Internal Variables--------
reg q;

//-------------Code Starts Here---------
always @ ( posedge clk)
if (~reset) begin
  q <= 1'b0;
end  else begin
  q <= data;
end

endmodule //End Of Module dff_sync_reset


module halfadder(
a ,
b ,
cout,
q
);
input a,b;
output cout,q;

assign cout = a ^ b;
assign q    = a & b;

endmodule


module dff_sync_reset_ne (
data   , // Data Input
clk    , // Clock Input
reset  , // Reset input
q        // Q output
);
//-----------Input Ports---------------
input data, clk, reset ;

//-----------Output Ports---------------
output q;

//------------Internal Variables--------
reg q;

//-------------Code Starts Here---------
always @ ( negedge clk)
if (~reset) begin
  q <= 1'b0;
end  else begin
  q <= data;
end

endmodule //End Of Module dff_sync_reset
```

2.3. module netlist file

```
module dff ( data, clk, reset, q );
  input data, clk, reset;
  output q;
  wire   N3;

  fdf1a2 q_reg ( .D(N3), .CLK(clk), .Q(q) );
  and2a3 U3 ( .A(reset), .B(data), .Y(N3) );
endmodule


module dff_sync_reset_ne ( data, clk, reset, q );
  input data, clk, reset;
  output q;
  wire   N4, n1;

  fdf1a2 q_reg ( .D(N4), .CLK(n1), .Q(q) );
  inv1a1 U3 ( .A(clk), .Y(n1) );
  and2a3 U4 ( .A(reset), .B(data), .Y(N4) );
endmodule


module halfadder ( a, b, cout, q );
  input a, b;
  output cout, q;


  and2a3 U1 ( .A(b), .B(a), .Y(q) );
  xor2a1 U2 ( .A(b), .B(a), .Y(cout) );
endmodule


module time_test ( Q2, CLK );
  input CLK;
  output Q2;
  wire   D1, Q1, D2, n1;

  dff ff1 ( .data(D1), .clk(CLK), .reset(1'b0), .q(Q1) );
  dff_sync_reset_ne ff2 ( .data(D2), .clk(CLK), .reset(1'b0), .q(Q2) );
  halfadder ha1 ( .a(Q1), .b(Q1), .cout(D2) );
  fdf1a2 D1_reg ( .D(n1), .CLK(CLK), .Q(D1) );
  inv1a1 U4 ( .A(D1), .Y(n1) );
endmodule
```

2.4. library file

Link library /home/zhang/Asic/time/libs/core_typ.db

Target library /home/zhang/Asic/time/libs/core_typ.db

Symbol library /home/zhang/Asic/time/libs/core.sdb

2.5. Setup time check(met)

2.5.1. Setup time check script file

```
# Create user defined variables
set CLK_PORT [get_ports CLK]
set CLK_PERIOD 5.00
set CLK_SKEW 0.14

set INPUT_DELAY 0.1

set OUTPUT_DELAY 0.5

set MAX_AREA 380000

# Time Budget
create_clock -period $CLK_PERIOD -name my_clock $CLK_PORT
set_dont_touch_network my_clock

create_clock -period $CLK_PERIOD -name CLKP [get_ports CLK]

set_multicycle_path 2 -from [get_pins ff1/clk] -to [get_pins ff2/data]


set library_setup_time 0.04
set_clock_uncertainty -setup 0.4 $CLK_PORT

set_clock_latency 1.0 $CLK_PORT
set_clock_uncertainty -hold 0.54 $CLK_PORT

#set_input_delay $INPUT_DELAY -max -clock my_clock [remove_from_collection [all_inputs]
$CLK_PORT]
#set_output_delay $OUTPUT_DELAY -max -clock my_clock [all_outputs]

set library_hold_time 0.01
```

2.5.2. Setup time check result

```
Startpoint: D1_reg (rising edge-triggered flip-flop clocked by CLKP)
 Endpoint: D1_reg (rising edge-triggered flip-flop clocked by CLKP)
 Path Group: CLKP
 Path Type: max

 Des/Clust/Port     Wire Load Model       Library
 ------------------------------------------------
 time_test          5KGATES               ssc_core

 Point                                    Incr       Path
 -----------------------------------------------------------
 clock CLKP (rise edge)                   0.00       0.00
 clock network delay (ideal)              1.00       1.00
 D1_reg/CLK (fdf1a2)                      0.00       1.00 r
 D1_reg/Q (fdf1a2)                        0.62       1.62 f
 U4/Y (inv1a1)                            0.51       2.13 r
 D1_reg/D (fdf1a2)                        0.00       2.13 r
 data arrival time                                   2.13

 clock CLKP (rise edge)                   3.00       3.00
 clock network delay (ideal)              1.00       4.00
 clock uncertainty                       -0.40       3.60
 D1_reg/CLK (fdf1a2)                      0.00       3.60 r
 library setup time                      -0.17       3.43
 data required time                                  3.43
 -----------------------------------------------------------
 data required time                                  3.43
 data arrival time                                  -2.13
 -----------------------------------------------------------
 slack (MET)                                         1.31
```

2.6. Setup time check (violated)

2.6.1. Setup time check script file

```
# Create user defined variables
set CLK_PORT [get_ports CLK]
set CLK_PERIOD 1.00
set CLK_SKEW 0.14


set INPUT_DELAY 0.1

set OUTPUT_DELAY 0.5

set MAX_AREA 380000


# Time Budget
create_clock -period $CLK_PERIOD -name my_clock $CLK_PORT
set_dont_touch_network my_clock

create_clock -period $CLK_PERIOD -name CLKP [get_ports CLK]

set_multicycle_path 2 -from [get_pins ff1/clk] -to [get_pins ff2/data]


set library_setup_time 0.04
set_clock_uncertainty -setup 0.4 $CLK_PORT

set_clock_latency 1.0 $CLK_PORT
set_clock_uncertainty -hold 0.54 $CLK_PORT


set library_hold_time 0.01
```

2.6.2. Setup time check result

```
Startpoint: D1_reg (rising edge-triggered flip-flop clocked by CLKP)
 Endpoint: D1_reg (rising edge-triggered flip-flop clocked by CLKP)
 Path Group: CLKP
 Path Type: max

 Des/Clust/Port     Wire Load Model       Library
 ------------------------------------------------
 time_test          5KGATES               ssc_core

 Point                                    Incr       Path
 ----------------------------------------------------------
 clock CLKP (rise edge)                   0.00       0.00
 clock network delay (ideal)              1.00       1.00
 D1_reg/CLK (fdf1a2)                      0.00       1.00 r
 D1_reg/Q (fdf1a2)                        0.62       1.62 f
 U4/Y (inv1a1)                            0.51       2.13 r
 D1_reg/D (fdf1a2)                        0.00       2.13 r
 data arrival time                                   2.13

 clock CLKP (rise edge)                   1.00       1.00
 clock network delay (ideal)              1.00       2.00
 clock uncertainty                       -0.40       1.60
 D1_reg/CLK (fdf1a2)                      0.00       1.60 r
 library setup time                      -0.17       1.43
 data required time                                  1.43
 ----------------------------------------------------------
 data required time                                  1.43
 data arrival time                                  -2.13
 ----------------------------------------------------------
 slack (VIOLATED)                                   -0.69
```

2.7. Hold time check(met)

2.7.1. Hold time check script file

```
# Create user defined variables
set CLK_PORT [get_ports CLK]
set CLK_PERIOD 4.00
set CLK_SKEW 0.14


set INPUT_DELAY 2.0

set OUTPUT_DELAY 0.5

set MAX_AREA 380000


# Time Budget
create_clock -period $CLK_PERIOD -name my_clock $CLK_PORT
set_dont_touch_network my_clock
set_clock_uncertainty $CLK_SKEW [get_clocks my_clock]

set library_setup_time 0.04
set_clock_uncertainty -setup 0.4 $CLK_PORT

set_clock_latency 2.0 $CLK_PORT
set_clock_uncertainty -hold 0.14 $CLK_PORT

#set_input_delay $INPUT_DELAY -max -clock my_clock [remove_from_collection [all_inputs]
$CLK_PORT]
#set_output_delay $OUTPUT_DELAY -max -clock my_clock [all_outputs]

set library_hold_time 0.51
```

2.7.2. Hold time check result

```
Startpoint: D1_reg (rising edge-triggered flip-flop clocked by my_clock)
Endpoint: D1_reg (rising edge-triggered flip-flop clocked by my_clock)
Path Group: my_clock
Path Type: min

Des/Clust/Port     Wire Load Model       Library
------------------------------------------------
time_test          5KGATES               ssc_core

Point                          Fanout      Incr       Path
-------------------------------------------------------------
clock my_clock (rise edge)                 0.00       0.00
clock network delay (ideal)                3.00       3.00
D1_reg/CLK (fdf1a2)                        0.00       3.00 r
D1_reg/Q (fdf1a2)                          0.55       3.55 r
D1 (net)                         2         0.00       3.55 r
U4/Y (inv1a1)                              0.37       3.92 f
n1 (net)                         1         0.00       3.92 f
D1_reg/D (fdf1a2)                          0.00       3.92 f
data arrival time                                     3.92

clock my_clock (rise edge)                 0.00       0.00
clock network delay (ideal)                3.00       3.00
clock uncertainty                          0.14       3.14
D1_reg/CLK (fdf1a2)                        0.00       3.14 r
library hold time                          0.32       3.46
data required time                                    3.46
-------------------------------------------------------------
data required time                                    3.46
data arrival time                                    -3.92
-------------------------------------------------------------
slack (MET)                                           0.46
```

2.8. Hold time check(violated)

2.8.1. Hold time check script file

```
# Create user defined variables
set CLK_PORT [get_ports CLK]
set CLK_PERIOD 4.00
set CLK_SKEW 0.14


set INPUT_DELAY 2.0

set OUTPUT_DELAY 0.5

set MAX_AREA 380000


# Time Budget
create_clock -period $CLK_PERIOD -name my_clock $CLK_PORT
set_dont_touch_network my_clock
set_clock_uncertainty $CLK_SKEW [get_clocks my_clock]

set library_setup_time 0.04
set_clock_uncertainty -setup 0.4 $CLK_PORT

set_clock_latency 3.0 $CLK_PORT
set_clock_uncertainty -hold 0.84 $CLK_PORT

#set_input_delay $INPUT_DELAY -max -clock my_clock [remove_from_collection [all_inputs]
$CLK_PORT]
#set_output_delay $OUTPUT_DELAY -max -clock my_clock [all_outputs]

set library_hold_time 1.51
```

2.8.2. Hold time check result

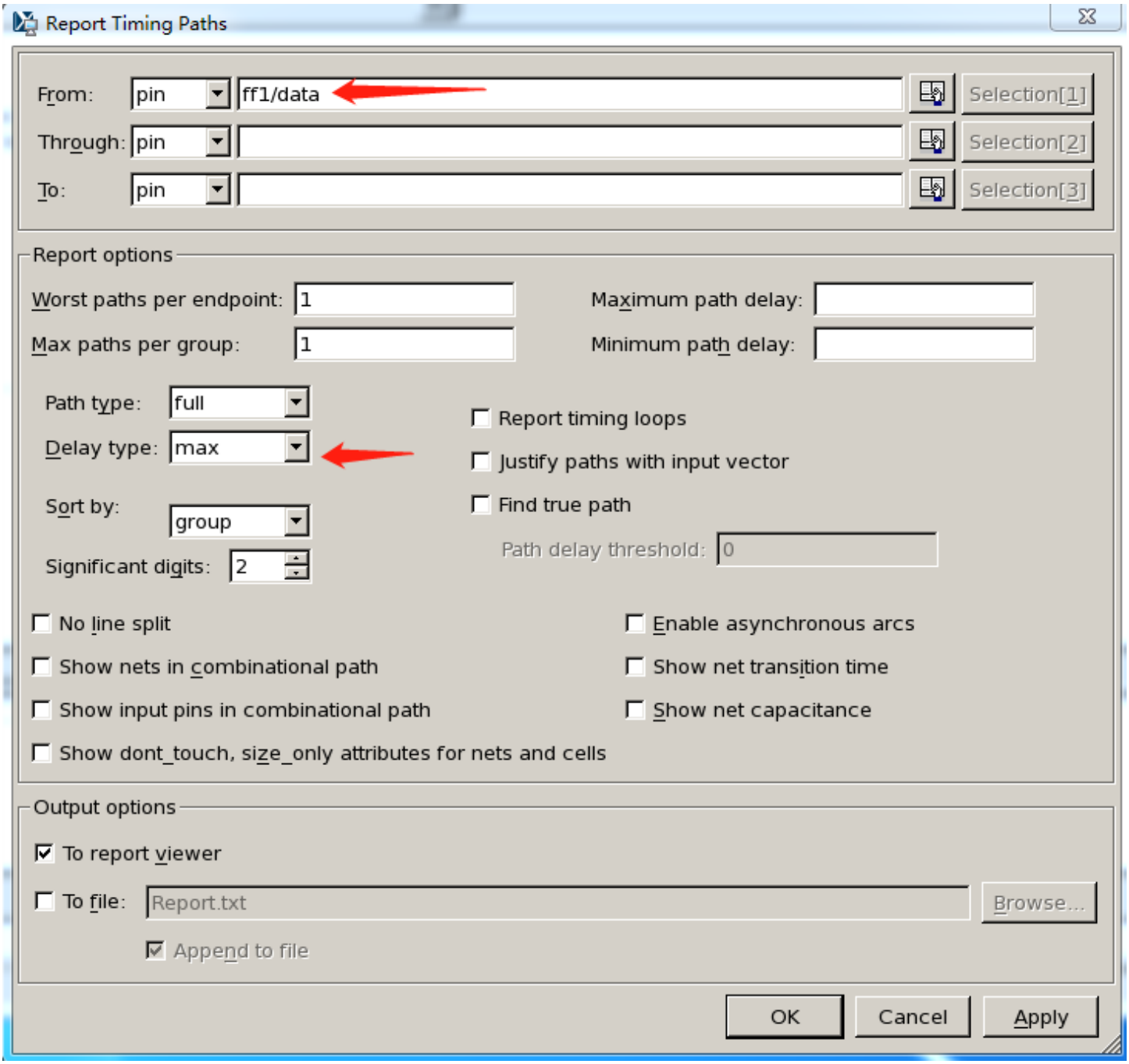
```
Startpoint: D1_reg (rising edge-triggered flip-flop clocked by my_clock)
Endpoint: D1_reg (rising edge-triggered flip-flop clocked by my_clock)
Path Group: my_clock
Path Type: min

Des/Clust/Port     Wire Load Model       Library
------------------------------------------------
time_test          5KGATES               ssc_core

Point                                    Incr       Path
-----------------------------------------------------------
clock my_clock (rise edge)               0.00       0.00
clock network delay (ideal)              3.00       3.00
D1_reg/CLK (fdf1a2)                      0.00       3.00 r
D1_reg/Q (fdf1a2)                        0.55       3.55 r
U4/Y (inv1a1)                            0.37       3.92 f
D1_reg/D (fdf1a2)                        0.00       3.92 f
data arrival time                                   3.92

clock my_clock (rise edge)               0.00       0.00
clock network delay (ideal)              3.00       3.00
clock uncertainty                        0.84       3.84
D1_reg/CLK (fdf1a2)                      0.00       3.84 r
library hold time                        0.32       4.16
data required time                                  4.16
-----------------------------------------------------------
data required time                                  4.16
data arrival time                                  -3.92
-----------------------------------------------------------
slack (VIOLATED)                                   -0.24
```

2.9. Input delay(met)

2.9.1. Input delay script file

```
# Create user defined variables
set CLK_PORT [get_ports CLK]
set CLK_PERIOD 3.00
set CLK_SKEW 0.14

set_clock_uncertainty -setup 0.4 $CLK_PORT

set_clock_latency 1.0 $CLK_PORT
set_clock_uncertainty -hold 0.54 $CLK_PORT


create_clock -name theclk -period 20 [get_ports CLK]

set_input_delay -clock theclk -max 4 [get_ports  ff1/data]
set_input_delay -clock theclk -min 2 [get_ports  ff1/data]
```

2.9.2. Input delay settings



2.9.3. Input delay result

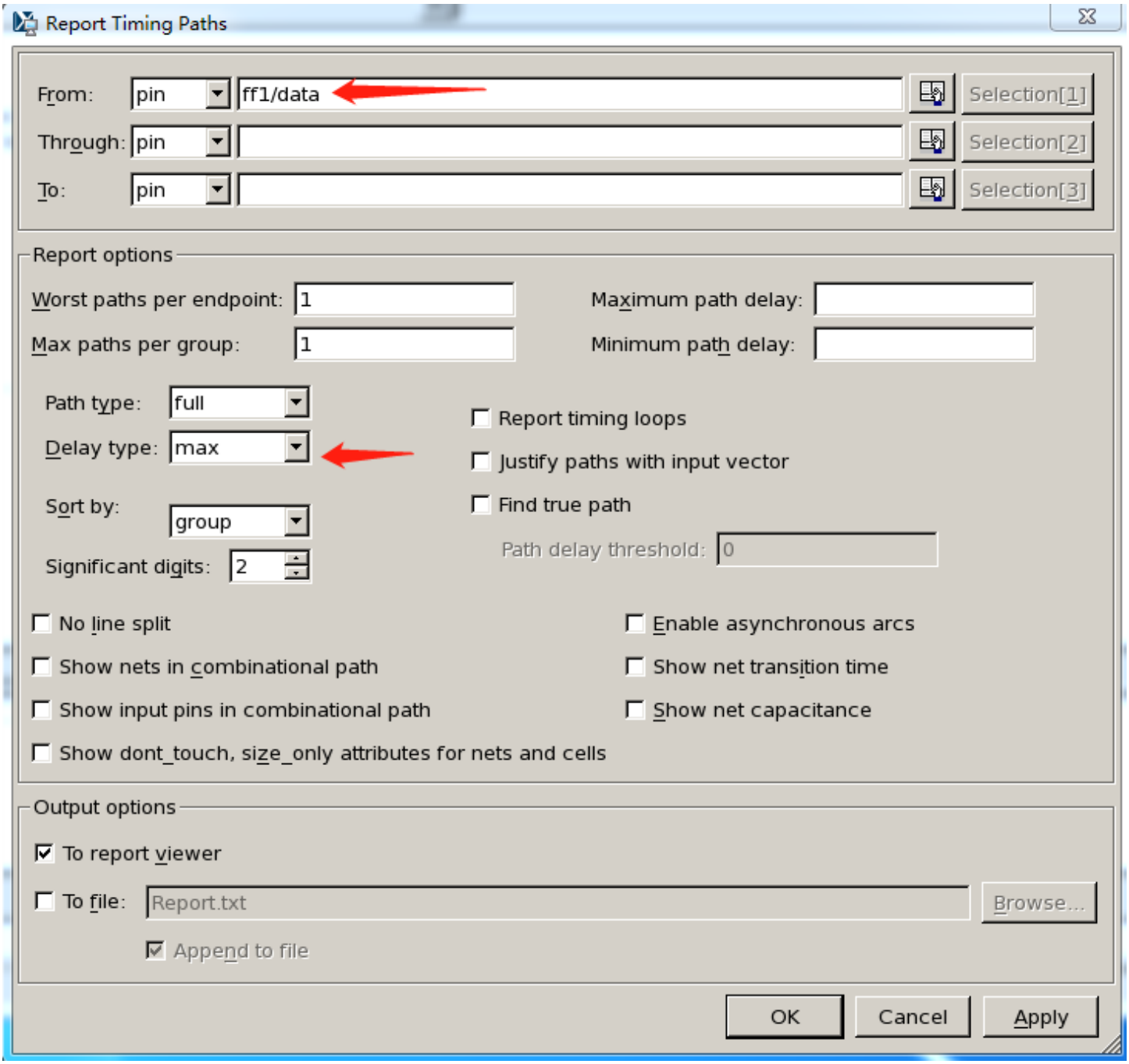
```
Startpoint: ff1/data (internal path startpoint clocked by theclk)
  Endpoint: ff1/q_reg (rising edge-triggered flip-flop clocked by theclk)
  Path Group: theclk
  Path Type: max

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  time_test          5KGATES               ssc_core
  dff                5KGATES               ssc_core

  Point                                    Incr       Path
  -----------------------------------------------------------
  clock theclk (rise edge)                 0.00       0.00
  clock network delay (ideal)              0.00       0.00
  input external delay                     4.00       4.00 r
  ff1/data (dff)                           0.00       4.00 r
  ff1/C11/Z_0 (*SELECT_OP_2.1_2.1_1)       0.00       4.00 r
  ff1/q_reg/next_state (**SEQGEN**)        0.00       4.00 r
  data arrival time                                   4.00

  clock theclk (rise edge)                40.00      40.00
  clock network delay (ideal)              1.00      41.00
  clock uncertainty                       -0.40      40.60
  ff1/q_reg/clocked_on (**SEQGEN**)        0.00      40.60 r
  library setup time                       0.00      40.60
  data required time                                 40.60
  -----------------------------------------------------------
  data required time                                 40.60
  data arrival time                                  -4.00
  -----------------------------------------------------------
  slack (MET)                                        36.60
```

2.10. Input delay(violated)

2.10.1. Input delay script file

```
# Create user defined variables
set CLK_PORT [get_ports CLK]
set CLK_PERIOD 3.00
set CLK_SKEW 0.14

set_clock_uncertainty -setup 0.4 $CLK_PORT

set_clock_latency 1.0 $CLK_PORT
set_clock_uncertainty -hold 0.54 $CLK_PORT


create_clock -name theclk -period 3 [get_ports CLK]

set_input_delay -clock theclk -max 4 [get_ports  ff1/data]
set_input_delay -clock theclk -min 2 [get_ports  ff1/data]
```

2.10.2. Input delay settings



2.10.3. Input delay result

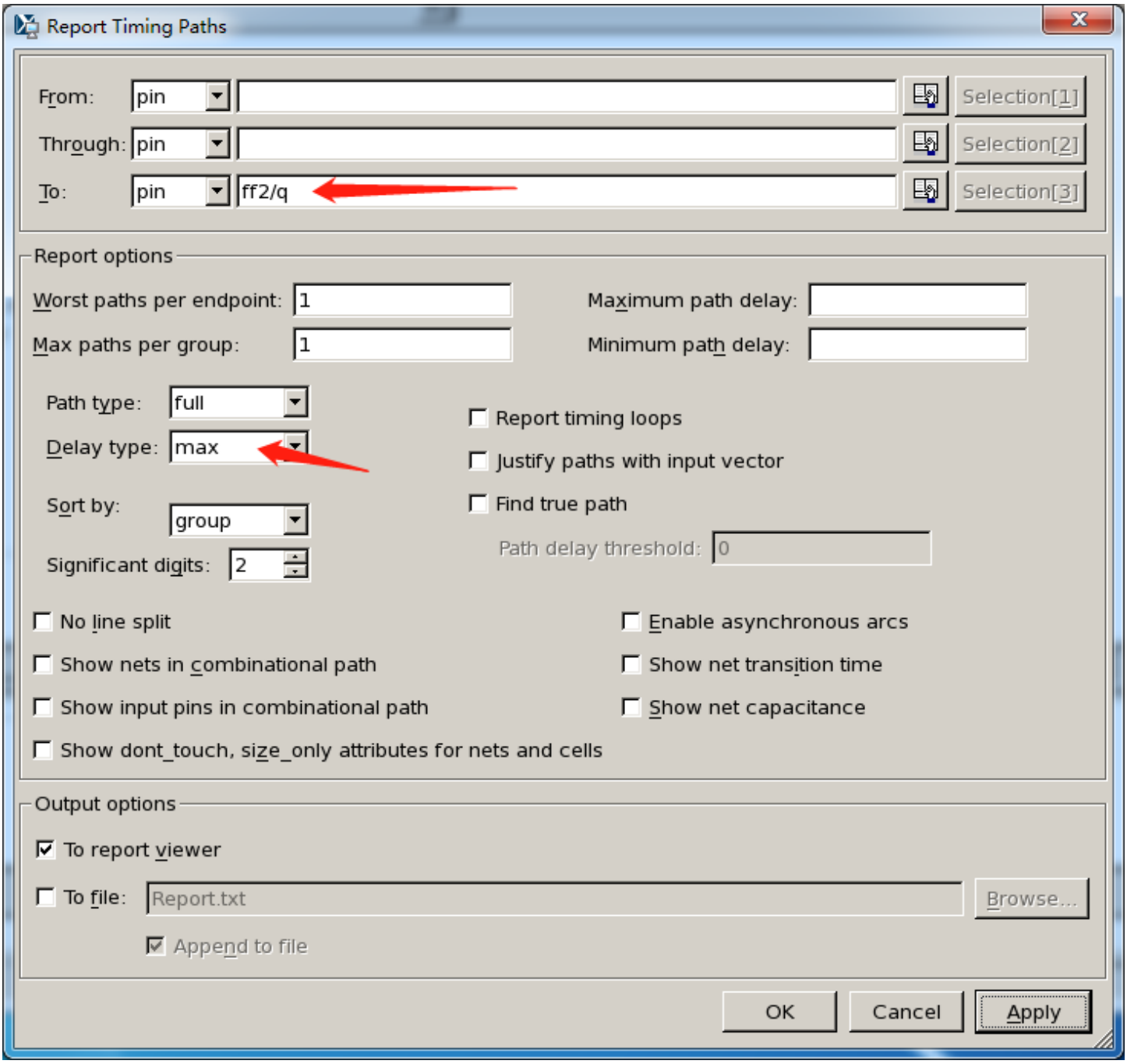
```
Startpoint: ff1/data (internal path startpoint clocked by theclk)
Endpoint: ff1/q_reg (rising edge-triggered flip-flop clocked by theclk)
Path Group: theclk
Path Type: max

Des/Clust/Port     Wire Load Model       Library
------------------------------------------------
time_test          5KGATES               ssc_core
dff                5KGATES               ssc_core

Point                                    Incr       Path
-----------------------------------------------------------
clock theclk (rise edge)                 0.00       0.00
clock network delay (ideal)              0.00       0.00
input external delay                     4.00       4.00 r
ff1/data (dff)                           0.00       4.00 r
ff1/C11/Z_0 (*SELECT_OP_2.1_2.1_1)       0.00       4.00 r
ff1/q_reg/next_state (**SEQGEN**)        0.00       4.00 r
data arrival time                                   4.00

clock theclk (rise edge)                 3.00       3.00
clock network delay (ideal)              1.00       4.00
clock uncertainty                       -0.40       3.60
ff1/q_reg/clocked_on (**SEQGEN**)        0.00       3.60 r
library setup time                       0.00       3.60
data required time                                  3.60
-----------------------------------------------------------
data required time                                  3.60
data arrival time                                  -4.00
-----------------------------------------------------------
slack (VIOLATED)                                   -0.40
```

2.11. Output delay(met)

2.11.1. Output delay script file

```
# Create user defined variables
set CLK_PORT [get_ports CLK]
set CLK_PERIOD 3.00
set CLK_SKEW 0.14

set_clock_uncertainty -setup 0.4 $CLK_PORT

set_clock_latency 1.0 $CLK_PORT
set_clock_uncertainty -hold 0.54 $CLK_PORT


create_clock -name theclk -period 20 [get_ports CLK]
set_output_delay -clock theclk -max 8 [get_ports  ff2/q]
set_output_delay -clock theclk -min -3 [get_ports ff2/q]
```

2.11.2. Output delay settings



2.11.3. Output delay result

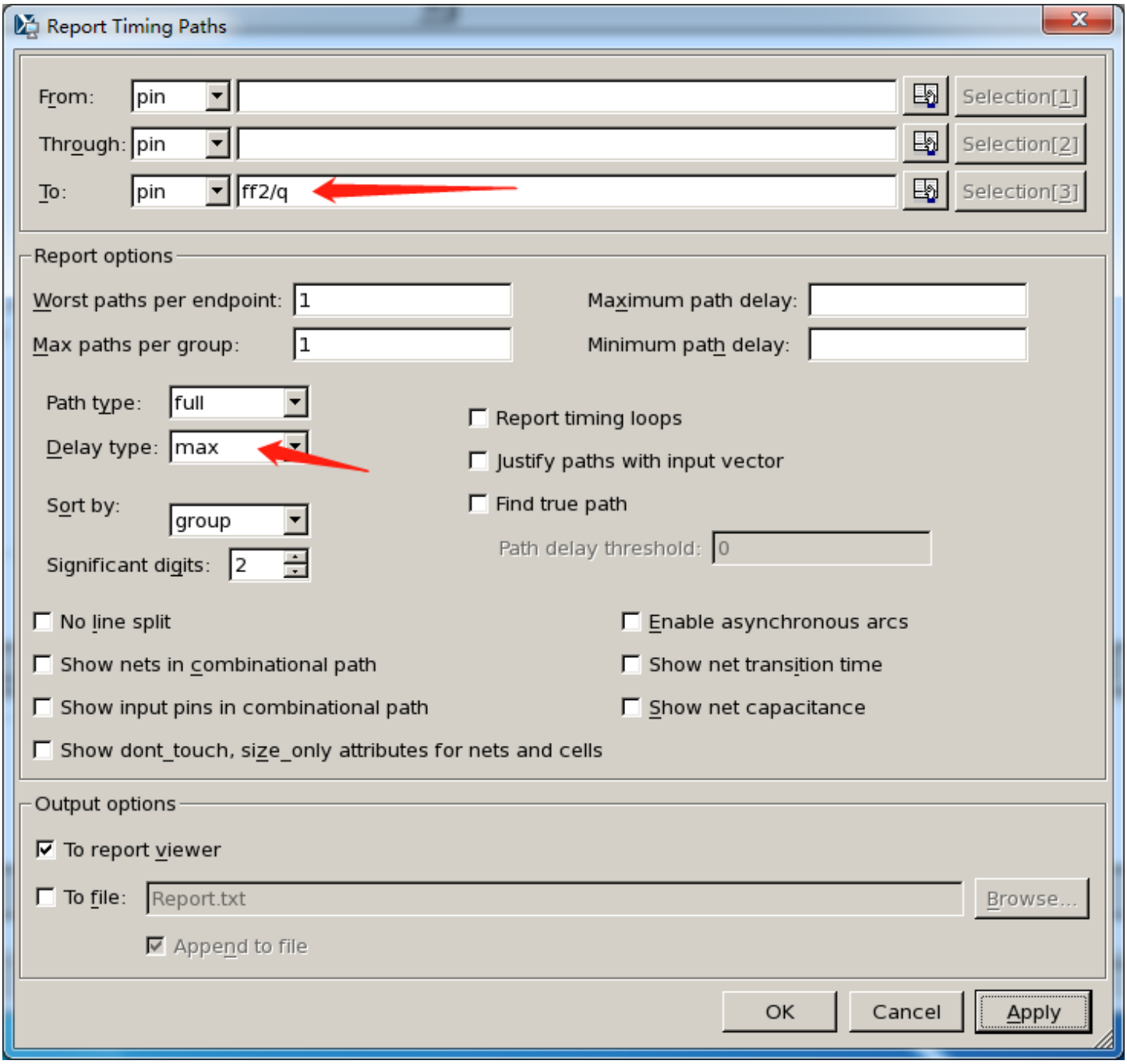
```
Startpoint: ff2/q_reg (rising edge-triggered flip-flop clocked by theclk')
  Endpoint: ff2/q (internal path endpoint clocked by theclk)
  Path Group: theclk
  Path Type: max

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  dff_sync_reset_ne  5KGATES               ssc_core
  time_test          5KGATES               ssc_core

  Point                                    Incr       Path
  -----------------------------------------------------------
  clock theclk' (rise edge)               10.00      10.00
  clock network delay (ideal)              1.00      11.00
  ff2/q_reg/clocked_on (**SEQGEN**)        0.00      11.00 r
  ff2/q_reg/Q (**SEQGEN**)                 0.00      11.00 r
  ff2/q (dff_sync_reset_ne)                0.00      11.00 r
  data arrival time                                  11.00

  clock theclk (rise edge)                20.00      20.00
  clock network delay (ideal)              0.00      20.00
  output external delay                   -8.00      12.00
  data required time                                 12.00
  -----------------------------------------------------------
  data required time                                 12.00
  data arrival time                                 -11.00
  -----------------------------------------------------------
  slack (MET)                                         1.00
```

2.12. Output delay(violated)

2.12.1. Output delay script file

```
# Create user defined variables
set CLK_PORT [get_ports CLK]
set CLK_PERIOD 3.00
set CLK_SKEW 0.14

set_clock_uncertainty -setup 0.4 $CLK_PORT

set_clock_latency 1.0 $CLK_PORT
set_clock_uncertainty -hold 0.54 $CLK_PORT


create_clock -name theclk -period 5 [get_ports CLK]
set_output_delay -clock theclk -max 8 [get_ports  ff2/q]
set_output_delay -clock theclk -min -3 [get_ports ff2/q]
```

2.12.2. Output delay settings

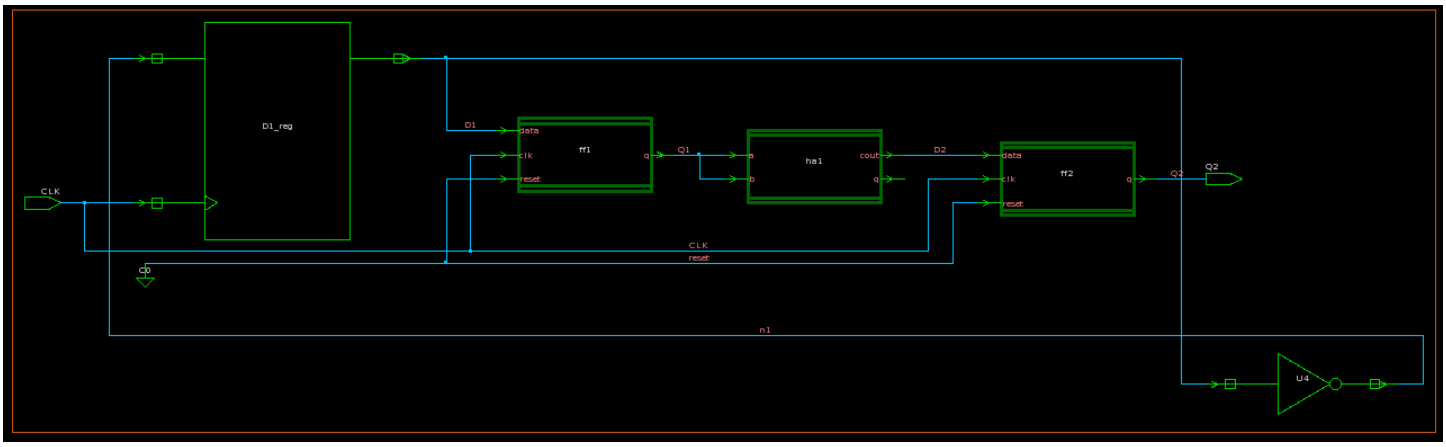


2.12.3. Output delay result

```
Startpoint: ff2/q_reg (rising edge-triggered flip-flop clocked by theclk')
  Endpoint: ff2/q (internal path endpoint clocked by theclk)
  Path Group: theclk
  Path Type: max

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  dff_sync_reset_ne  5KGATES               ssc_core
  time_test          5KGATES               ssc_core

  Point                                    Incr       Path
  ------------------------------------------------------------
  clock theclk' (rise edge)                2.50       2.50
  clock network delay (ideal)              1.00       3.50
  ff2/q_reg/clocked_on (**SEQGEN**)        0.00       3.50 r
  ff2/q_reg/Q (**SEQGEN**)                 0.00       3.50 r
  ff2/q (dff_sync_reset_ne)                0.00       3.50 r
  data arrival time                                   3.50

  clock theclk (rise edge)                 5.00       5.00
  clock network delay (ideal)              0.00       5.00
  output external delay                   -8.00      -3.00
  data required time                                  -3.00
  ------------------------------------------------------------
  data required time                                  -3.00
  data arrival time                                   -3.50
  ------------------------------------------------------------
  slack (VIOLATED)                                    -6.50
```

3. Negative flip-flop to Negative flip-flop

3.1. module figure



3.2. module Verilog file

```
`timescale 1ns/1ns

module time_test (

output Q2 ,
input CLK
);

reg  D1;
wire Q1, D2;
reg reset;

dff_sync_reset_ne ff1 (.data(D1), .clk(CLK), .q(Q1), .reset(reset));
dff_sync_reset_ne ff2 (.data(D2), .clk(CLK), .q(Q2), .reset(reset));
halfadder      ha1 (.a(Q1), .b(Q1), .cout(D2));

initial D1 =1;
always @(posedge CLK)
 begin D1 <=  ~D1;
end


endmodule

module dff (
data    , // Data Input
clk     , // Clock Input
reset   , // Reset input
q         // Q output
);
```

```
//-----------Input Ports--------------
input data, clk, reset ;

//-----------Output Ports--------------
output q;

//------------Internal Variables--------
reg q;

//-------------Code Starts Here---------
always @ ( posedge clk)
if (~reset) begin
  q <= 1'b0;
end  else begin
  q <= data;
end

endmodule //End Of Module dff_sync_reset


module halfadder(
a ,
b ,
cout,
q
);
input a,b;
output cout,q;

assign cout = a ^ b;
assign q    = a & b;

endmodule


module dff_sync_reset_ne (
data   , // Data Input
clk    , // Clock Input
reset  , // Reset input
q        // Q output
);
//-----------Input Ports--------------
input data, clk, reset ;

//-----------Output Ports--------------
output q;

//------------Internal Variables--------
reg q;

//-------------Code Starts Here---------
always @ ( negedge clk)
if (~reset) begin
  q <= 1'b0;
end  else begin
  q <= data;
end

endmodule //End Of Module dff_sync_reset
```

3.3. module netlist file

```
module dff_sync_reset_ne_0 ( data, clk, reset, q );
  input data, clk, reset;
  output q;
  wire   N4, n1;

  fdf1a3 q_reg ( .D(N4), .CLK(n1), .Q(q) );
  inv1a1 U3 ( .A(clk), .Y(n1) );
  and2a3 U4 ( .A(reset), .B(data), .Y(N4) );
endmodule


module halfadder ( a, b, cout, q );
  input a, b;
  output cout, q;


  and2a3 U1 ( .A(b), .B(a), .Y(q) );
  xor2a1 U2 ( .A(b), .B(a), .Y(cout) );
endmodule


module dff_sync_reset_ne_1 ( data, clk, reset, q );
  input data, clk, reset;
  output q;
  wire   N4, n2;

  fdf1a3 q_reg ( .D(N4), .CLK(n2), .Q(q) );
  inv1a1 U3 ( .A(clk), .Y(n2) );
  and2a3 U4 ( .A(reset), .B(data), .Y(N4) );
endmodule


module time_test ( Q2, CLK );
  input CLK;
  output Q2;
  wire   D1, Q1, D2, n1;

  dff_sync_reset_ne_0 ff1 ( .data(D1), .clk(CLK), .reset(1'b0), .q(Q1) );
  dff_sync_reset_ne_1 ff2 ( .data(D2), .clk(CLK), .reset(1'b0), .q(Q2) );
  halfadder ha1 ( .a(Q1), .b(Q1), .cout(D2) );
  fdf1a2 D1_reg ( .D(n1), .CLK(CLK), .Q(D1) );
  inv1a1 U4 ( .A(D1), .Y(n1) );
endmodule
```

3.4. library file

Link library /home/zhang/Asic/time/libs/core_typ.db

Target library /home/zhang/Asic/time/libs/core_typ.db

Symbol library /home/zhang/Asic/time/libs/core.sdb

3.5. Setup time check(met)

3.5.1. Setup time check script file

```
# Create user defined variables
set CLK_PORT [get_ports CLK]
set CLK_PERIOD 5.00
set CLK_SKEW 0.14

set INPUT_DELAY 0.1

set OUTPUT_DELAY 0.5

set MAX_AREA 380000

# Time Budget
create_clock -period $CLK_PERIOD -name my_clock $CLK_PORT
set_dont_touch_network my_clock

create_clock -period $CLK_PERIOD -name CLKP [get_ports CLK]

set_multicycle_path 2 -from [get_pins ff1/clk] -to [get_pins ff2/data]


set library_setup_time 0.04
set_clock_uncertainty -setup 0.4 $CLK_PORT

set_clock_latency 1.0 $CLK_PORT
set_clock_uncertainty -hold 0.54 $CLK_PORT

#set_input_delay $INPUT_DELAY -max -clock my_clock [remove_from_collection [all_inputs]
$CLK_PORT]
#set_output_delay $OUTPUT_DELAY -max -clock my_clock [all_outputs]

set library_hold_time 0.01
```

3.5.2. Setup time check result

```
Startpoint: D1_reg (rising edge-triggered flip-flop clocked by CLKP)
 Endpoint: D1_reg (rising edge-triggered flip-flop clocked by CLKP)
 Path Group: CLKP
 Path Type: max

 Des/Clust/Port     Wire Load Model       Library
 ------------------------------------------------
 time_test          5KGATES               ssc_core

 Point                                    Incr       Path
 -----------------------------------------------------------
 clock CLKP (rise edge)                   0.00       0.00
 clock network delay (ideal)              1.00       1.00
 D1_reg/CLK (fdf1a2)                      0.00       1.00 r
 D1_reg/Q (fdf1a2)                        0.62       1.62 f
 U4/Y (inv1a1)                            0.51       2.13 r
 D1_reg/D (fdf1a2)                        0.00       2.13 r
 data arrival time                                   2.13

 clock CLKP (rise edge)                   3.00       3.00
 clock network delay (ideal)              1.00       4.00
 clock uncertainty                       -0.40       3.60
 D1_reg/CLK (fdf1a2)                      0.00       3.60 r
 library setup time                      -0.17       3.43
 data required time                                  3.43
 -----------------------------------------------------------
 data required time                                  3.43
 data arrival time                                  -2.13
 -----------------------------------------------------------
 slack (MET)                                         1.31
```

3.6. Setup time check (violated)

3.6.1. Setup time check script file

```
# Create user defined variables
set CLK_PORT [get_ports CLK]
set CLK_PERIOD 1.00
set CLK_SKEW 0.14


set INPUT_DELAY 0.1

set OUTPUT_DELAY 0.5

set MAX_AREA 380000


# Time Budget
create_clock -period $CLK_PERIOD -name my_clock $CLK_PORT
set_dont_touch_network my_clock

create_clock -period $CLK_PERIOD -name CLKP [get_ports CLK]

set_multicycle_path 2 -from [get_pins ff1/clk] -to [get_pins ff2/data]


set library_setup_time 0.04
set_clock_uncertainty -setup 0.4 $CLK_PORT

set_clock_latency 1.0 $CLK_PORT
set_clock_uncertainty -hold 0.54 $CLK_PORT


set library_hold_time 0.01
```

3.6.2. Setup time check result

```
Startpoint: D1_reg (rising edge-triggered flip-flop clocked by CLKP)
 Endpoint: D1_reg (rising edge-triggered flip-flop clocked by CLKP)
 Path Group: CLKP
 Path Type: max

 Des/Clust/Port     Wire Load Model       Library
 ------------------------------------------------
 time_test          5KGATES               ssc_core

 Point                                    Incr       Path
 -----------------------------------------------------------
 clock CLKP (rise edge)                   0.00       0.00
 clock network delay (ideal)              1.00       1.00
 D1_reg/CLK (fdf1a2)                      0.00       1.00 r
 D1_reg/Q (fdf1a2)                        0.62       1.62 f
 U4/Y (inv1a1)                            0.51       2.13 r
 D1_reg/D (fdf1a2)                        0.00       2.13 r
 data arrival time                                   2.13

 clock CLKP (rise edge)                   1.00       1.00
 clock network delay (ideal)              1.00       2.00
 clock uncertainty                       -0.40       1.60
 D1_reg/CLK (fdf1a2)                      0.00       1.60 r
 library setup time                      -0.17       1.43
 data required time                                  1.43
 -----------------------------------------------------------
 data required time                                  1.43
 data arrival time                                  -2.13
 -----------------------------------------------------------
 slack (VIOLATED)                                   -0.69
```

3.7. Hold time check(met)

3.7.1. Hold time check script file

```
# Create user defined variables
set CLK_PORT [get_ports CLK]
set CLK_PERIOD 4.00
set CLK_SKEW 0.14


set INPUT_DELAY 2.0

set OUTPUT_DELAY 0.5

set MAX_AREA 380000


# Time Budget
create_clock -period $CLK_PERIOD -name my_clock $CLK_PORT
set_dont_touch_network my_clock
set_clock_uncertainty $CLK_SKEW [get_clocks my_clock]

set library_setup_time 0.04
set_clock_uncertainty -setup 0.4 $CLK_PORT

set_clock_latency 2.0 $CLK_PORT
set_clock_uncertainty -hold 0.14 $CLK_PORT

#set_input_delay $INPUT_DELAY -max -clock my_clock [remove_from_collection [all_inputs]
$CLK_PORT]
#set_output_delay $OUTPUT_DELAY -max -clock my_clock [all_outputs]

set library_hold_time 0.51
```

3.7.2. Hold time check result

```
Startpoint: D1_reg (rising edge-triggered flip-flop clocked by my_clock)
Endpoint: D1_reg (rising edge-triggered flip-flop clocked by my_clock)
Path Group: my_clock
Path Type: min

Des/Clust/Port     Wire Load Model       Library
------------------------------------------------
time_test          5KGATES               ssc_core

Point                          Fanout      Incr       Path
-------------------------------------------------------------
clock my_clock (rise edge)                 0.00       0.00
clock network delay (ideal)                3.00       3.00
D1_reg/CLK (fdf1a2)                        0.00       3.00 r
D1_reg/Q (fdf1a2)                          0.55       3.55 r
D1 (net)                         2         0.00       3.55 r
U4/Y (inv1a1)                              0.37       3.92 f
n1 (net)                         1         0.00       3.92 f
D1_reg/D (fdf1a2)                          0.00       3.92 f
data arrival time                                     3.92

clock my_clock (rise edge)                 0.00       0.00
clock network delay (ideal)                3.00       3.00
clock uncertainty                          0.14       3.14
D1_reg/CLK (fdf1a2)                        0.00       3.14 r
library hold time                          0.32       3.46
data required time                                    3.46
-------------------------------------------------------------
data required time                                    3.46
data arrival time                                    -3.92
-------------------------------------------------------------
slack (MET)                                           0.46
```

3.8. Hold time check(violated)

3.8.1. Hold time check script file

```
# Create user defined variables
set CLK_PORT [get_ports CLK]
set CLK_PERIOD 4.00
set CLK_SKEW 0.14


set INPUT_DELAY 2.0

set OUTPUT_DELAY 0.5

set MAX_AREA 380000


# Time Budget
create_clock -period $CLK_PERIOD -name my_clock $CLK_PORT
set_dont_touch_network my_clock
set_clock_uncertainty $CLK_SKEW [get_clocks my_clock]

set library_setup_time 0.04
set_clock_uncertainty -setup 0.4 $CLK_PORT

set_clock_latency 3.0 $CLK_PORT
set_clock_uncertainty -hold 0.84 $CLK_PORT

#set_input_delay $INPUT_DELAY -max -clock my_clock [remove_from_collection [all_inputs]
$CLK_PORT]
#set_output_delay $OUTPUT_DELAY -max -clock my_clock [all_outputs]

set library_hold_time 1.51
```

3.8.2. Hold time check result

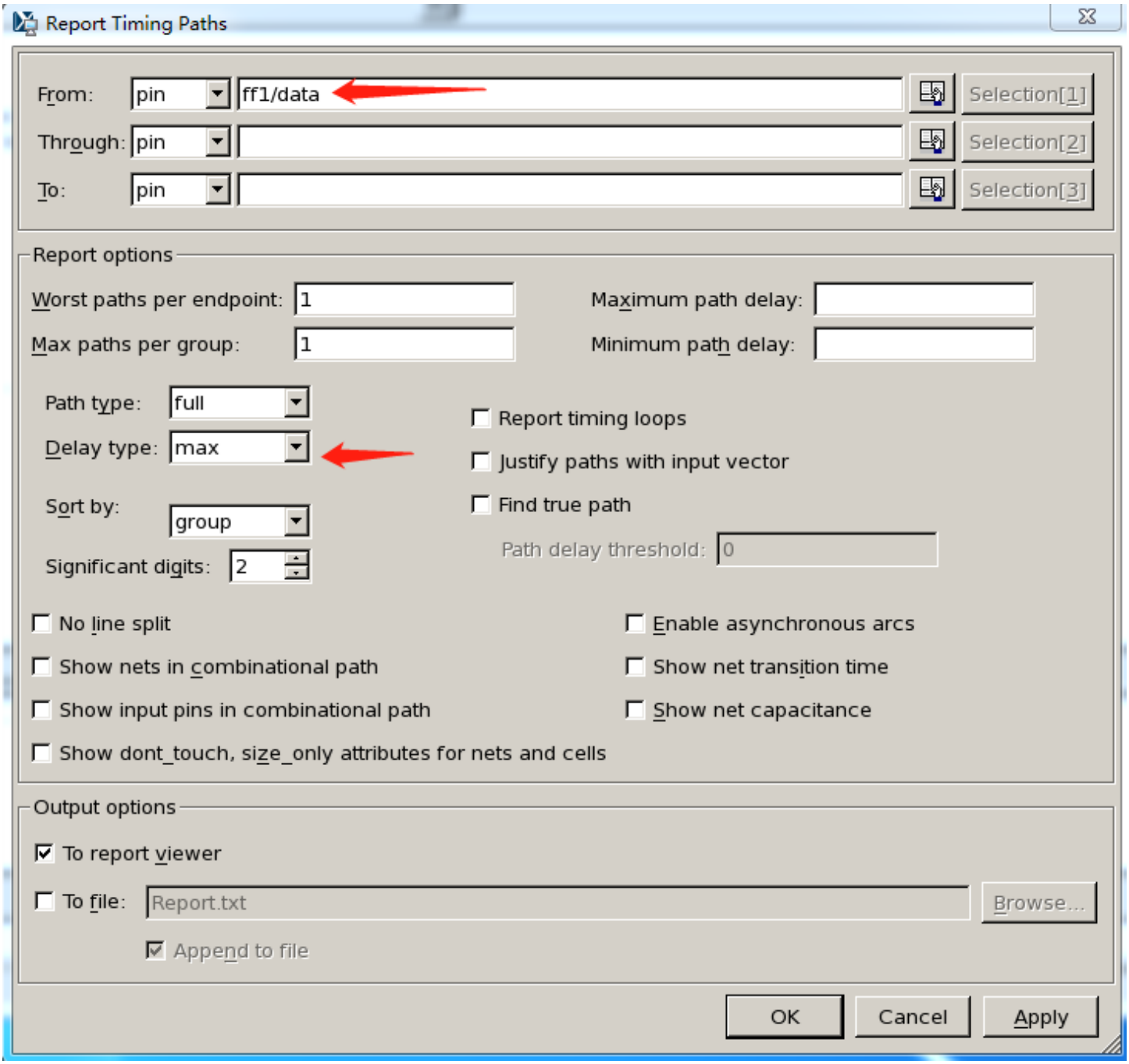
```
Startpoint: D1_reg (rising edge-triggered flip-flop clocked by my_clock)
Endpoint: D1_reg (rising edge-triggered flip-flop clocked by my_clock)
Path Group: my_clock
Path Type: min

Des/Clust/Port     Wire Load Model       Library
------------------------------------------------
time_test          5KGATES               ssc_core

Point                                    Incr       Path
-----------------------------------------------------------
clock my_clock (rise edge)               0.00       0.00
clock network delay (ideal)              3.00       3.00
D1_reg/CLK (fdf1a2)                      0.00       3.00 r
D1_reg/Q (fdf1a2)                        0.55       3.55 r
U4/Y (inv1a1)                            0.37       3.92 f
D1_reg/D (fdf1a2)                        0.00       3.92 f
data arrival time                                   3.92

clock my_clock (rise edge)               0.00       0.00
clock network delay (ideal)              3.00       3.00
clock uncertainty                        0.84       3.84
D1_reg/CLK (fdf1a2)                      0.00       3.84 r
library hold time                        0.32       4.16
data required time                                  4.16
-----------------------------------------------------------
data required time                                  4.16
data arrival time                                  -3.92
-----------------------------------------------------------
slack (VIOLATED)                                   -0.24
```

3.9. Input delay(met)

3.9.1. Input delay script file

```
# Create user defined variables
set CLK_PORT [get_ports CLK]
set CLK_PERIOD 3.00
set CLK_SKEW 0.14

set_clock_uncertainty -setup 0.4 $CLK_PORT

set_clock_latency 1.0 $CLK_PORT
set_clock_uncertainty -hold 0.54 $CLK_PORT


create_clock -name theclk -period 20 [get_ports CLK]

set_input_delay -clock theclk -max 4 [get_ports  ff1/data]
set_input_delay -clock theclk -min 2 [get_ports  ff1/data]
```

3.9.2. Input delay settings



3.9.3. Input delay result

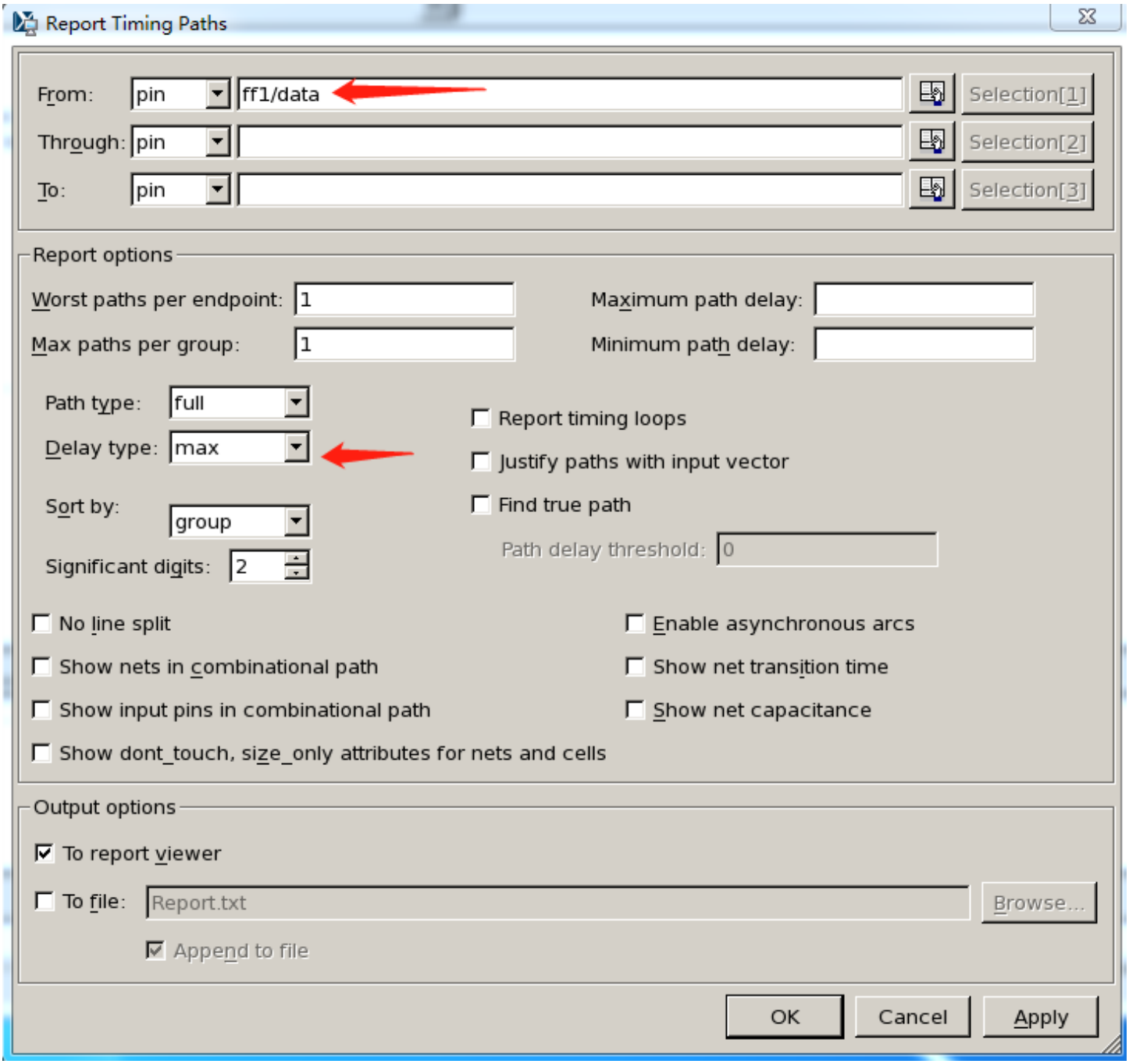
```
Startpoint: ff1/data (internal path startpoint clocked by theclk)
  Endpoint: ff1/q_reg (rising edge-triggered flip-flop clocked by theclk')
  Path Group: theclk
  Path Type: max

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  time_test          5KGATES               ssc_core
  dff_sync_reset_ne  5KGATES               ssc_core

  Point                                    Incr       Path
  ------------------------------------------------------------
  clock theclk (rise edge)                 0.00       0.00
  clock network delay (ideal)              0.00       0.00
  input external delay                     4.00       4.00 r
  ff1/data (dff_sync_reset_ne)             0.00       4.00 r
  ff1/C12/Z_0 (*SELECT_OP_2.1_2.1_1)       0.00       4.00 r
  ff1/q_reg/next_state (**SEQGEN**)        0.00       4.00 r
  data arrival time                                   4.00

  clock theclk' (rise edge)               10.00      10.00
  clock network delay (ideal)              1.00      11.00
  clock uncertainty                       -0.40      10.60
  ff1/q_reg/clocked_on (**SEQGEN**)        0.00      10.60 r
  library setup time                       0.00      10.60
  data required time                                 10.60
  ------------------------------------------------------------
  data required time                                 10.60
  data arrival time                                  -4.00
  ------------------------------------------------------------
  slack (MET)                                         6.60
```

3.10. Input delay(violated)

3.10.1. Input delay script file

```
# Create user defined variables
set CLK_PORT [get_ports CLK]
set CLK_PERIOD 3.00
set CLK_SKEW 0.14

set_clock_uncertainty -setup 0.4 $CLK_PORT

set_clock_latency 1.0 $CLK_PORT
set_clock_uncertainty -hold 0.54 $CLK_PORT


create_clock -name theclk -period 3 [get_ports CLK]

set_input_delay -clock theclk -max 4 [get_ports  ff1/data]
set_input_delay -clock theclk -min 2 [get_ports  ff1/data]
```

3.10.2. Input delay settings



3.10.3. Input delay result

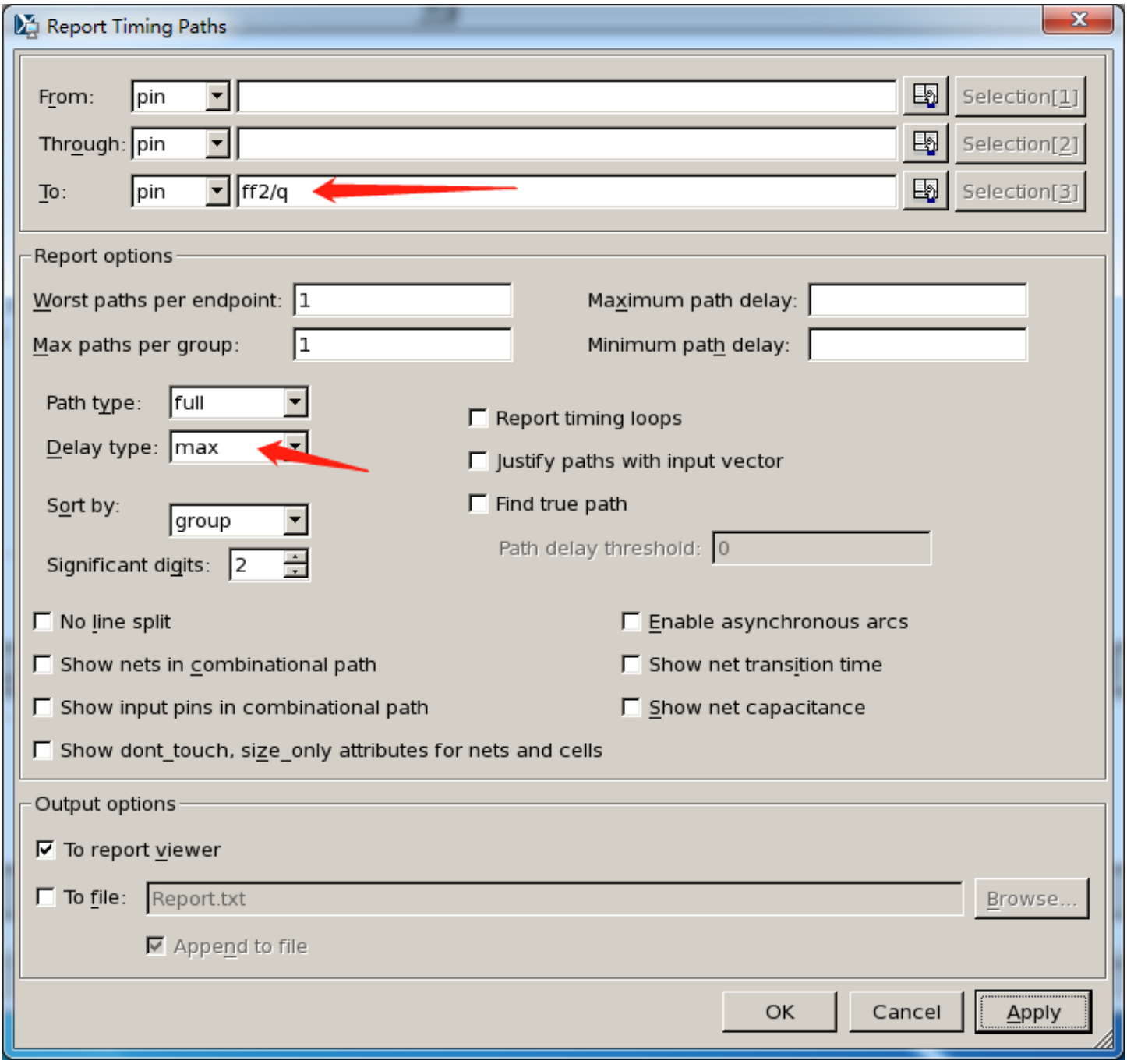
```
Startpoint: ff1/data (internal path startpoint clocked by theclk)
  Endpoint: ff1/q_reg (rising edge-triggered flip-flop clocked by theclk')
  Path Group: theclk
  Path Type: max

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  time_test          5KGATES               ssc_core
  dff_sync_reset_ne  5KGATES               ssc_core

  Point                                    Incr       Path
  ------------------------------------------------------------
  clock theclk (rise edge)                 0.00       0.00
  clock network delay (ideal)              0.00       0.00
  input external delay                     4.00       4.00 r
  ff1/data (dff_sync_reset_ne)             0.00       4.00 r
  ff1/C12/Z_0 (*SELECT_OP_2.1_2.1_1)       0.00       4.00 r
  ff1/q_reg/next_state (**SEQGEN**)        0.00       4.00 r
  data arrival time                                   4.00

  clock theclk' (rise edge)                1.50       1.50
  clock network delay (ideal)              1.00       2.50
  clock uncertainty                       -0.40       2.10
  ff1/q_reg/clocked_on (**SEQGEN**)        0.00       2.10 r
  library setup time                       0.00       2.10
  data required time                                  2.10
  ------------------------------------------------------------
  data required time                                  2.10
  data arrival time                                  -4.00
  ------------------------------------------------------------
  slack (VIOLATED)                                   -1.90
```

3.11. Output delay(met)

3.11.1. Output delay script file

```
# Create user defined variables
set CLK_PORT [get_ports CLK]
set CLK_PERIOD 3.00
set CLK_SKEW 0.14

set_clock_uncertainty -setup 0.4 $CLK_PORT

set_clock_latency 1.0 $CLK_PORT
set_clock_uncertainty -hold 0.54 $CLK_PORT


create_clock -name theclk -period 20 [get_ports CLK]
set_output_delay -clock theclk -max 8 [get_ports  ff2/q]
set_output_delay -clock theclk -min -3 [get_ports ff2/q]
```

3.11.2. Output delay settings



3.11.3. Output delay result

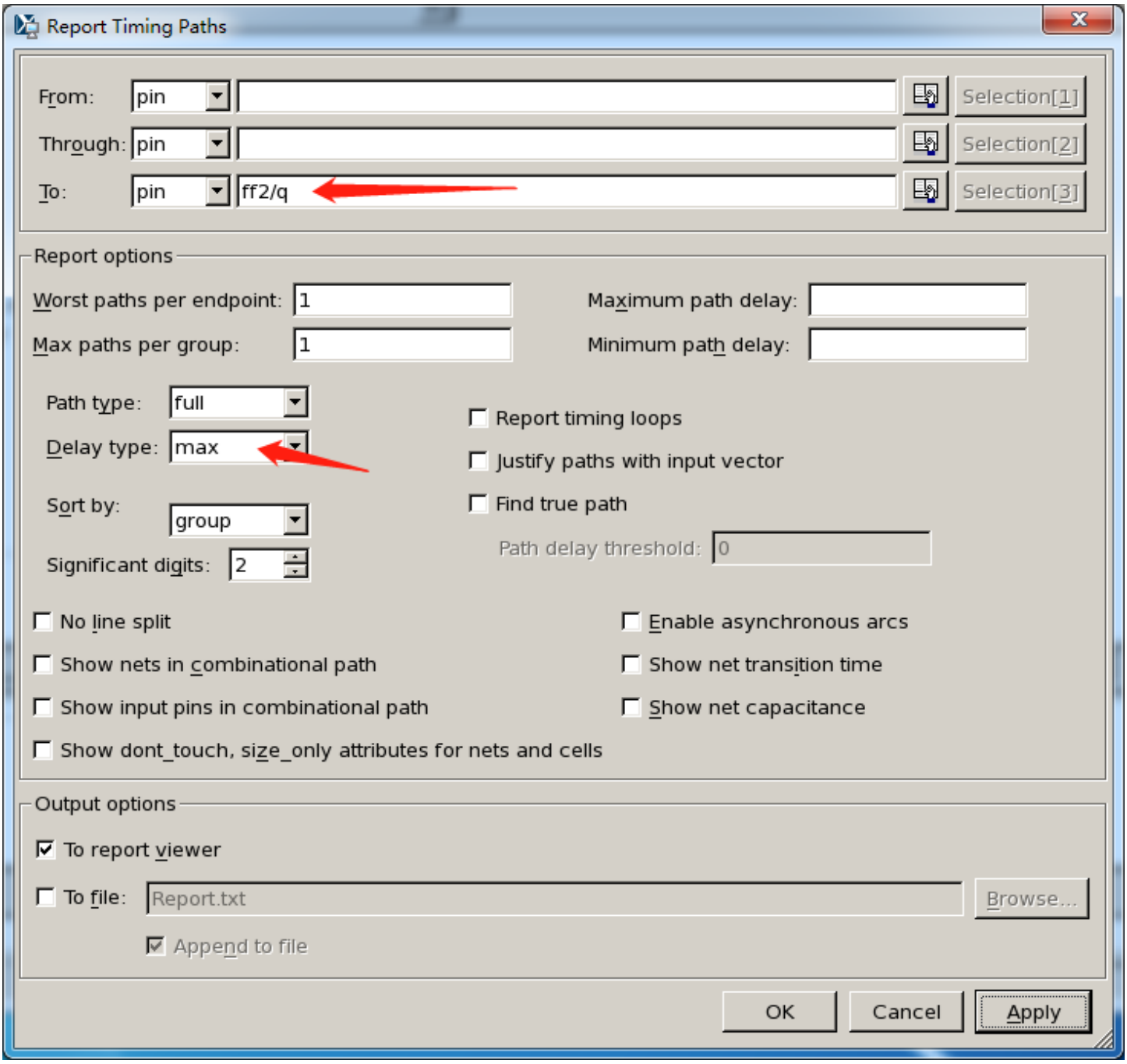
```
Startpoint: ff2/q_reg (rising edge-triggered flip-flop clocked by theclk')
  Endpoint: ff2/q (internal path endpoint clocked by theclk)
  Path Group: theclk
  Path Type: max

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  dff_sync_reset_ne  5KGATES               ssc_core
  time_test          5KGATES               ssc_core

  Point                                    Incr       Path
  ------------------------------------------------------------
  clock theclk' (rise edge)               10.00      10.00
  clock network delay (ideal)              1.00      11.00
  ff2/q_reg/clocked_on (**SEQGEN**)        0.00      11.00 r
  ff2/q_reg/Q (**SEQGEN**)                 0.00      11.00 r
  ff2/q (dff_sync_reset_ne)                0.00      11.00 r
  data arrival time                                  11.00

  clock theclk (rise edge)                20.00      20.00
  clock network delay (ideal)              0.00      20.00
  output external delay                   -8.00      12.00
  data required time                                 12.00
  ------------------------------------------------------------
  data required time                                 12.00
  data arrival time                                 -11.00
  ------------------------------------------------------------
  slack (MET)                                         1.00
```

3.12. Output delay(violated)

3.12.1. Output delay script file

```
# Create user defined variables
set CLK_PORT [get_ports CLK]
set CLK_PERIOD 3.00
set CLK_SKEW 0.14

set_clock_uncertainty -setup 0.4 $CLK_PORT

set_clock_latency 1.0 $CLK_PORT
set_clock_uncertainty -hold 0.54 $CLK_PORT


create_clock -name theclk -period 5 [get_ports CLK]
set_output_delay -clock theclk -max 8 [get_ports  ff2/q]
set_output_delay -clock theclk -min -3 [get_ports ff2/q]
```

3.12.2. Output delay settings

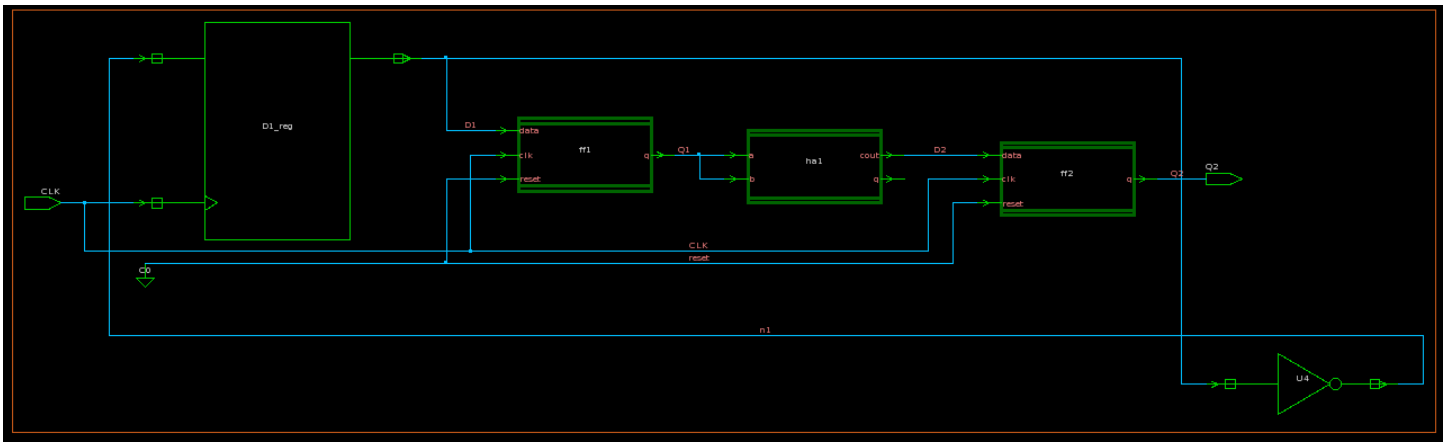


3.12.3. Input delay result

```
Startpoint: ff2/q_reg (rising edge-triggered flip-flop clocked by theclk')
  Endpoint: ff2/q (internal path endpoint clocked by theclk)
  Path Group: theclk
  Path Type: max

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  dff_sync_reset_ne  5KGATES               ssc_core
  time_test          5KGATES               ssc_core

  Point                                    Incr       Path
  -----------------------------------------------------------
  clock theclk' (rise edge)                2.50       2.50
  clock network delay (ideal)              1.00       3.50
  ff2/q_reg/clocked_on (**SEQGEN**)        0.00       3.50 r
  ff2/q_reg/Q (**SEQGEN**)                 0.00       3.50 r
  ff2/q (dff_sync_reset_ne)                0.00       3.50 r
  data arrival time                                   3.50

  clock theclk (rise edge)                 5.00       5.00
  clock network delay (ideal)              0.00       5.00
  output external delay                   -8.00      -3.00
  data required time                                 -3.00
  -----------------------------------------------------------
  data required time                                 -3.00
  data arrival time                                  -3.50
  -----------------------------------------------------------
  slack (VIOLATED)                                   -6.50
```

4. Negative flip-flop to Positive flip-flop

4.1. module figure



4.2. module Verilog file

```
`timescale 1ns/1ns

module time_test (

output Q2 ,
input CLK
);

reg  D1;
wire Q1, D2;
reg reset;

dff_sync_reset_ne ff1 (.data(D1), .clk(CLK), .q(Q1), .reset(reset));
dff ff2 (.data(D2), .clk(CLK), .q(Q2), .reset(reset));
halfadder      ha1 (.a(Q1), .b(Q1), .cout(D2));

initial D1 =1;
always @(posedge CLK)
 begin D1 <=  ~D1;
end


endmodule

module dff (
data    , // Data Input
clk     , // Clock Input
reset   , // Reset input
q         // Q output
);
```

```
//-----------Input Ports--------------
input data, clk, reset ;

//-----------Output Ports--------------
output q;

//------------Internal Variables--------
reg q;

//-------------Code Starts Here---------
always @ ( posedge clk)
if (~reset) begin
  q <= 1'b0;
end  else begin
  q <= data;
end

endmodule //End Of Module dff_sync_reset


module halfadder(
a ,
b ,
cout,
q
);
input a,b;
output cout,q;

assign cout = a ^ b;
assign q    = a & b;

endmodule


module dff_sync_reset_ne (
data   , // Data Input
clk    , // Clock Input
reset  , // Reset input
q        // Q output
);
//-----------Input Ports--------------
input data, clk, reset ;

//-----------Output Ports--------------
output q;

//------------Internal Variables--------
reg q;

//-------------Code Starts Here---------
always @ ( negedge clk)
if (~reset) begin
  q <= 1'b0;
end  else begin
  q <= data;
end

endmodule //End Of Module dff_sync_reset
```

4.3. module netlist file

```
module dff_sync_reset_ne_0 ( data, clk, reset, q );
  input data, clk, reset;
  output q;
  wire   N4, n1;

  fdf1a3 q_reg ( .D(N4), .CLK(n1), .Q(q) );
  inv1a1 U3 ( .A(clk), .Y(n1) );
  and2a3 U4 ( .A(reset), .B(data), .Y(N4) );
endmodule


module halfadder ( a, b, cout, q );
  input a, b;
  output cout, q;


  and2a3 U1 ( .A(b), .B(a), .Y(q) );
  xor2a1 U2 ( .A(b), .B(a), .Y(cout) );
endmodule


module dff_sync_reset_ne_1 ( data, clk, reset, q );
  input data, clk, reset;
  output q;
  wire   N4, n2;

  fdf1a3 q_reg ( .D(N4), .CLK(n2), .Q(q) );
  inv1a1 U3 ( .A(clk), .Y(n2) );
  and2a3 U4 ( .A(reset), .B(data), .Y(N4) );
endmodule


module time_test ( Q2, CLK );
  input CLK;
  output Q2;
  wire   D1, Q1, D2, n1;

  dff_sync_reset_ne_0 ff1 ( .data(D1), .clk(CLK), .reset(1'b0), .q(Q1) );
  dff_sync_reset_ne_1 ff2 ( .data(D2), .clk(CLK), .reset(1'b0), .q(Q2) );
  halfadder ha1 ( .a(Q1), .b(Q1), .cout(D2) );
  fdf1a2 D1_reg ( .D(n1), .CLK(CLK), .Q(D1) );
  inv1a1 U4 ( .A(D1), .Y(n1) );
endmodule
```

4.4. library file

Link library /home/zhang/Asic/time/libs/core_typ.db

Target library /home/zhang/Asic/time/libs/core_typ.db

Symbol library /home/zhang/Asic/time/libs/core.sdb

4.5. Setup time check(met)

4.5.1. Setup time check script file

```
# Create user defined variables
set CLK_PORT [get_ports CLK]
set CLK_PERIOD 5.00
set CLK_SKEW 0.14

set INPUT_DELAY 0.1

set OUTPUT_DELAY 0.5

set MAX_AREA 380000

# Time Budget
create_clock -period $CLK_PERIOD -name my_clock $CLK_PORT
set_dont_touch_network my_clock

create_clock -period $CLK_PERIOD -name CLKP [get_ports CLK]

set_multicycle_path 2 -from [get_pins ff1/clk] -to [get_pins ff2/data]


set library_setup_time 0.04
set_clock_uncertainty -setup 0.4 $CLK_PORT

set_clock_latency 1.0 $CLK_PORT
set_clock_uncertainty -hold 0.54 $CLK_PORT

#set_input_delay $INPUT_DELAY -max -clock my_clock [remove_from_collection [all_inputs]
$CLK_PORT]
#set_output_delay $OUTPUT_DELAY -max -clock my_clock [all_outputs]

set library_hold_time 0.01
```

4.5.2. Setup time check result

```
Startpoint: D1_reg (rising edge-triggered flip-flop clocked by CLKP)
 Endpoint: D1_reg (rising edge-triggered flip-flop clocked by CLKP)
 Path Group: CLKP
 Path Type: max

 Des/Clust/Port     Wire Load Model       Library
 ------------------------------------------------
 time_test          5KGATES               ssc_core

 Point                                    Incr       Path
 -----------------------------------------------------------
 clock CLKP (rise edge)                   0.00       0.00
 clock network delay (ideal)              1.00       1.00
 D1_reg/CLK (fdf1a2)                      0.00       1.00 r
 D1_reg/Q (fdf1a2)                        0.62       1.62 f
 U4/Y (inv1a1)                            0.51       2.13 r
 D1_reg/D (fdf1a2)                        0.00       2.13 r
 data arrival time                                   2.13

 clock CLKP (rise edge)                   3.00       3.00
 clock network delay (ideal)              1.00       4.00
 clock uncertainty                       -0.40       3.60
 D1_reg/CLK (fdf1a2)                      0.00       3.60 r
 library setup time                      -0.17       3.43
 data required time                                  3.43
 -----------------------------------------------------------
 data required time                                  3.43
 data arrival time                                  -2.13
 -----------------------------------------------------------
 slack (MET)                                         1.31
```

4.6. Setup time check (violated)

4.6.1. Setup time check script file

```
# Create user defined variables
set CLK_PORT [get_ports CLK]
set CLK_PERIOD 1.00
set CLK_SKEW 0.14


set INPUT_DELAY 0.1

set OUTPUT_DELAY 0.5

set MAX_AREA 380000


# Time Budget
create_clock -period $CLK_PERIOD -name my_clock $CLK_PORT
set_dont_touch_network my_clock

create_clock -period $CLK_PERIOD -name CLKP [get_ports CLK]

set_multicycle_path 2 -from [get_pins ff1/clk] -to [get_pins ff2/data]


set library_setup_time 0.04
set_clock_uncertainty -setup 0.4 $CLK_PORT

set_clock_latency 1.0 $CLK_PORT
set_clock_uncertainty -hold 0.54 $CLK_PORT


set library_hold_time 0.01
```

4.6.2. Setup time check result

```
Startpoint: D1_reg (rising edge-triggered flip-flop clocked by CLKP)
 Endpoint: D1_reg (rising edge-triggered flip-flop clocked by CLKP)
 Path Group: CLKP
 Path Type: max

 Des/Clust/Port     Wire Load Model       Library
 ------------------------------------------------
 time_test          5KGATES               ssc_core

 Point                                    Incr       Path
 -----------------------------------------------------------
 clock CLKP (rise edge)                   0.00       0.00
 clock network delay (ideal)              1.00       1.00
 D1_reg/CLK (fdf1a2)                      0.00       1.00 r
 D1_reg/Q (fdf1a2)                        0.62       1.62 f
 U4/Y (inv1a1)                            0.51       2.13 r
 D1_reg/D (fdf1a2)                        0.00       2.13 r
 data arrival time                                   2.13

 clock CLKP (rise edge)                   1.00       1.00
 clock network delay (ideal)              1.00       2.00
 clock uncertainty                       -0.40       1.60
 D1_reg/CLK (fdf1a2)                      0.00       1.60 r
 library setup time                      -0.17       1.43
 data required time                                  1.43
 -----------------------------------------------------------
 data required time                                  1.43
 data arrival time                                  -2.13
 -----------------------------------------------------------
 slack (VIOLATED)                                   -0.69
```

4.7. Hold time check(met)

4.7.1. Hold time check script file

```
# Create user defined variables
set CLK_PORT [get_ports CLK]
set CLK_PERIOD 4.00
set CLK_SKEW 0.14


set INPUT_DELAY 2.0

set OUTPUT_DELAY 0.5

set MAX_AREA 380000


# Time Budget
create_clock -period $CLK_PERIOD -name my_clock $CLK_PORT
set_dont_touch_network my_clock
set_clock_uncertainty $CLK_SKEW [get_clocks my_clock]

set library_setup_time 0.04
set_clock_uncertainty -setup 0.4 $CLK_PORT

set_clock_latency 2.0 $CLK_PORT
set_clock_uncertainty -hold 0.14 $CLK_PORT

#set_input_delay $INPUT_DELAY -max -clock my_clock [remove_from_collection [all_inputs]
$CLK_PORT]
#set_output_delay $OUTPUT_DELAY -max -clock my_clock [all_outputs]

set library_hold_time 0.51
```

4.7.2. Hold time check result

```
Startpoint: D1_reg (rising edge-triggered flip-flop clocked by my_clock)
Endpoint: D1_reg (rising edge-triggered flip-flop clocked by my_clock)
Path Group: my_clock
Path Type: min

Des/Clust/Port     Wire Load Model       Library
------------------------------------------------
time_test          5KGATES               ssc_core

Point                          Fanout      Incr       Path
-------------------------------------------------------------
clock my_clock (rise edge)                 0.00       0.00
clock network delay (ideal)                3.00       3.00
D1_reg/CLK (fdf1a2)                        0.00       3.00 r
D1_reg/Q (fdf1a2)                          0.55       3.55 r
D1 (net)                         2         0.00       3.55 r
U4/Y (inv1a1)                              0.37       3.92 f
n1 (net)                         1         0.00       3.92 f
D1_reg/D (fdf1a2)                          0.00       3.92 f
data arrival time                                     3.92

clock my_clock (rise edge)                 0.00       0.00
clock network delay (ideal)                3.00       3.00
clock uncertainty                          0.14       3.14
D1_reg/CLK (fdf1a2)                        0.00       3.14 r
library hold time                          0.32       3.46
data required time                                    3.46
-------------------------------------------------------------
data required time                                    3.46
data arrival time                                    -3.92
-------------------------------------------------------------
slack (MET)                                           0.46
```

4.8. Hold time check(violated)

4.8.1. Hold time check script file

```
# Create user defined variables
set CLK_PORT [get_ports CLK]
set CLK_PERIOD 4.00
set CLK_SKEW 0.14


set INPUT_DELAY 2.0

set OUTPUT_DELAY 0.5

set MAX_AREA 380000


# Time Budget
create_clock -period $CLK_PERIOD -name my_clock $CLK_PORT
set_dont_touch_network my_clock
set_clock_uncertainty $CLK_SKEW [get_clocks my_clock]

set library_setup_time 0.04
set_clock_uncertainty -setup 0.4 $CLK_PORT

set_clock_latency 3.0 $CLK_PORT
set_clock_uncertainty -hold 0.84 $CLK_PORT

#set_input_delay $INPUT_DELAY -max -clock my_clock [remove_from_collection [all_inputs]
$CLK_PORT]
#set_output_delay $OUTPUT_DELAY -max -clock my_clock [all_outputs]

set library_hold_time 1.51
```

4.8.2. Hold time check result

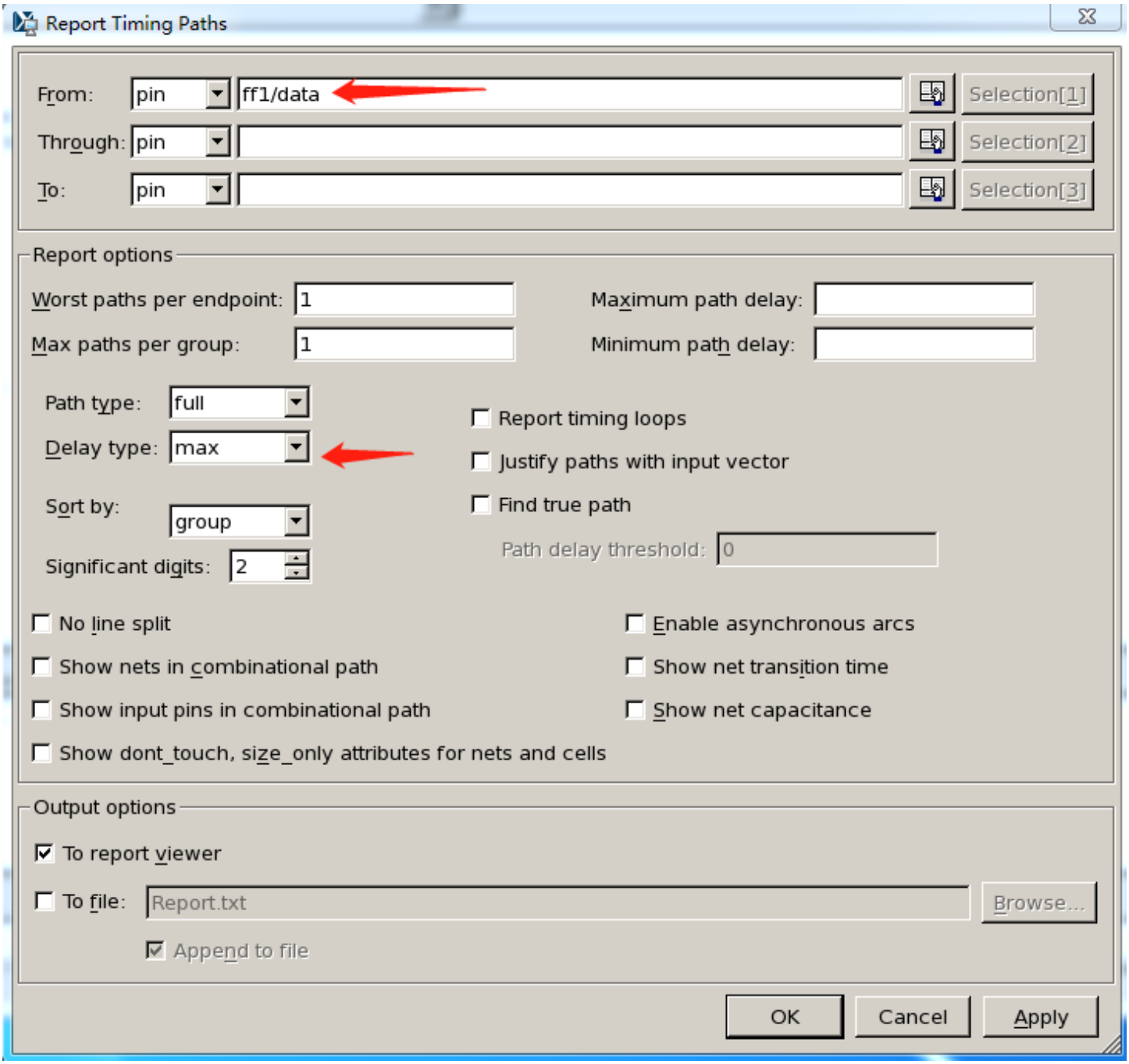
```
Startpoint: D1_reg (rising edge-triggered flip-flop clocked by my_clock)
Endpoint: D1_reg (rising edge-triggered flip-flop clocked by my_clock)
Path Group: my_clock
Path Type: min

Des/Clust/Port     Wire Load Model       Library
------------------------------------------------
time_test          5KGATES               ssc_core

Point                                    Incr       Path
-----------------------------------------------------------
clock my_clock (rise edge)               0.00       0.00
clock network delay (ideal)              3.00       3.00
D1_reg/CLK (fdf1a2)                      0.00       3.00 r
D1_reg/Q (fdf1a2)                        0.55       3.55 r
U4/Y (inv1a1)                            0.37       3.92 f
D1_reg/D (fdf1a2)                        0.00       3.92 f
data arrival time                                   3.92

clock my_clock (rise edge)               0.00       0.00
clock network delay (ideal)              3.00       3.00
clock uncertainty                        0.84       3.84
D1_reg/CLK (fdf1a2)                      0.00       3.84 r
library hold time                        0.32       4.16
data required time                                  4.16
-----------------------------------------------------------
data required time                                  4.16
data arrival time                                  -3.92
-----------------------------------------------------------
slack (VIOLATED)                                   -0.24
```

4.9. Input delay(met)

4.9.1. Input delay script file

```
# Create user defined variables
set CLK_PORT [get_ports CLK]
set CLK_PERIOD 3.00
set CLK_SKEW 0.14

set_clock_uncertainty -setup 0.4 $CLK_PORT

set_clock_latency 1.0 $CLK_PORT
set_clock_uncertainty -hold 0.54 $CLK_PORT


create_clock -name theclk -period 20 [get_ports CLK]

set_input_delay -clock theclk -max 4 [get_ports  ff1/data]
set_input_delay -clock theclk -min 2 [get_ports  ff1/data]
```

4.9.2. Input delay settings



4.9.3. Input delay result

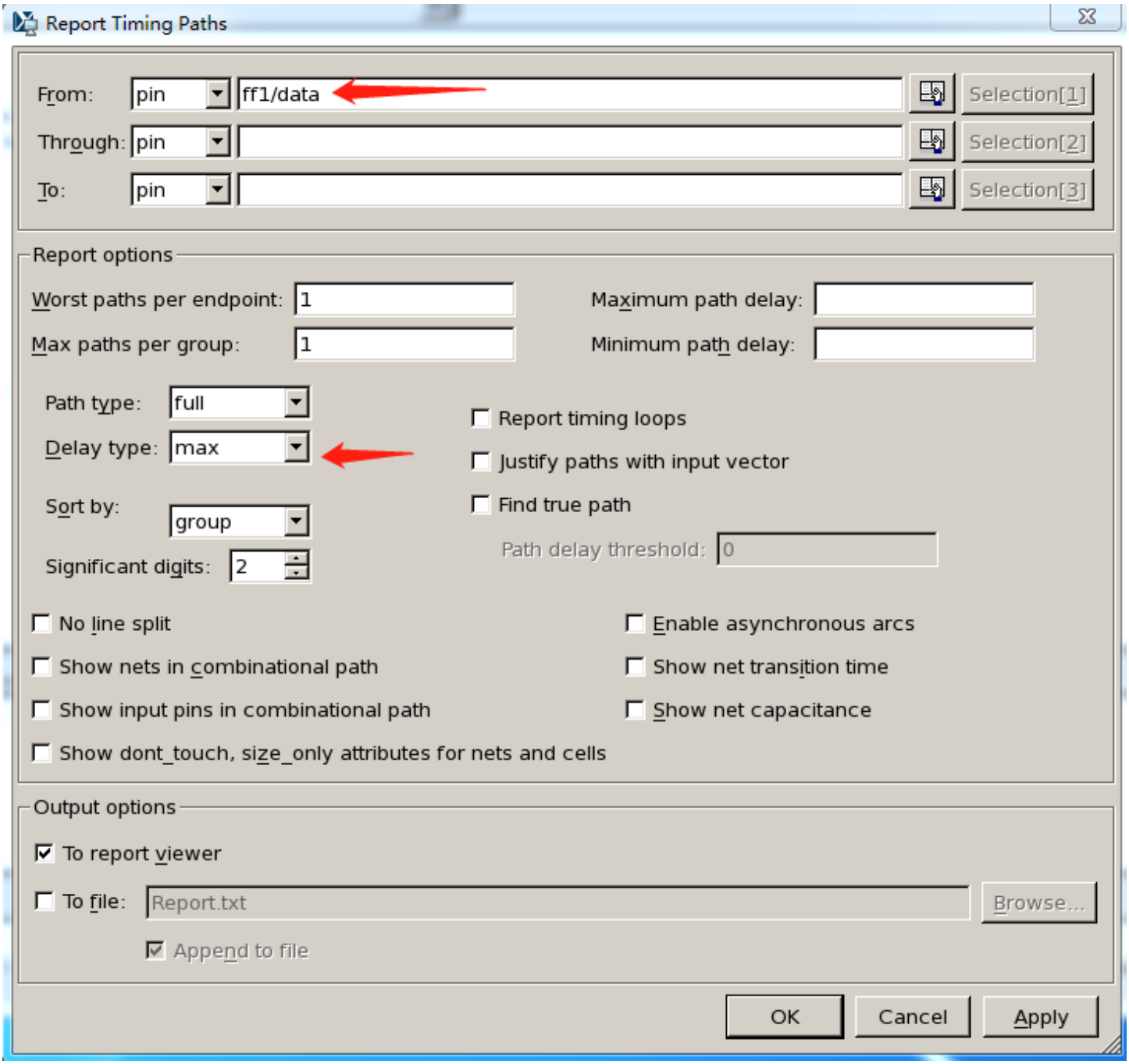
```
Startpoint: ff1/data (internal path startpoint clocked by theclk)
 Endpoint: ff1/q_reg (rising edge-triggered flip-flop clocked by theclk')
 Path Group: theclk
 Path Type: max

 Des/Clust/Port     Wire Load Model       Library
 ------------------------------------------------
 time_test          5KGATES               ssc_core
 dff_sync_reset_ne  5KGATES               ssc_core

 Point                                    Incr       Path
 -----------------------------------------------------------
 clock theclk (rise edge)                 0.00       0.00
 clock network delay (ideal)              0.00       0.00
 input external delay                     4.00       4.00 r
 ff1/data (dff_sync_reset_ne)             0.00       4.00 r
 ff1/C12/Z_0 (*SELECT_OP_2.1_2.1_1)       0.00       4.00 r
 ff1/q_reg/next_state (**SEQGEN**)        0.00       4.00 r
 data arrival time                                   4.00

 clock theclk' (rise edge)               10.00      10.00
 clock network delay (ideal)              1.00      11.00
 clock uncertainty                       -0.40      10.60
 ff1/q_reg/clocked_on (**SEQGEN**)        0.00      10.60 r
 library setup time                       0.00      10.60
 data required time                                 10.60
 -----------------------------------------------------------
 data required time                                 10.60
 data arrival time                                  -4.00
 -----------------------------------------------------------
 slack (MET)                                         6.60
```

4.10. Input delay(violated)

4.10.1. Input delay script file

```
# Create user defined variables
set CLK_PORT [get_ports CLK]
set CLK_PERIOD 3.00
set CLK_SKEW 0.14

set_clock_uncertainty -setup 0.4 $CLK_PORT

set_clock_latency 1.0 $CLK_PORT
set_clock_uncertainty -hold 0.54 $CLK_PORT


create_clock -name theclk -period 3 [get_ports CLK]

set_input_delay -clock theclk -max 4 [get_ports  ff1/data]
set_input_delay -clock theclk -min 2 [get_ports  ff1/data]
```

4.10.2. Input delay settings



4.10.3. Input delay result

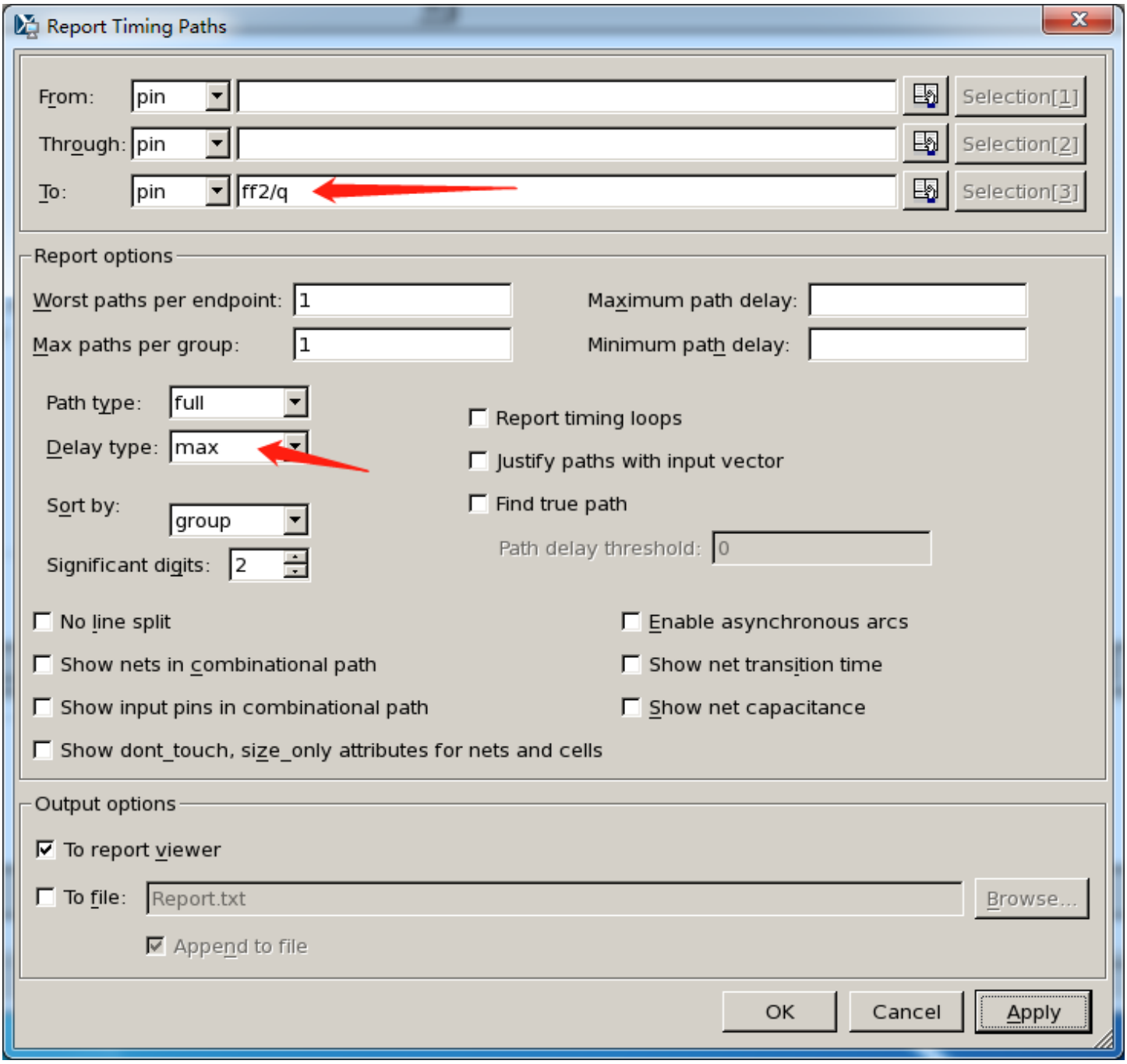
```
Startpoint: ff1/data (internal path startpoint clocked by theclk)
  Endpoint: ff1/q_reg (rising edge-triggered flip-flop clocked by theclk')
  Path Group: theclk
  Path Type: max

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  time_test          5KGATES               ssc_core
  dff_sync_reset_ne  5KGATES               ssc_core

  Point                                    Incr       Path
  -----------------------------------------------------------
  clock theclk (rise edge)                 0.00       0.00
  clock network delay (ideal)              0.00       0.00
  input external delay                     4.00       4.00 r
  ff1/data (dff_sync_reset_ne)             0.00       4.00 r
  ff1/C12/Z_0 (*SELECT_OP_2.1_2.1_1)       0.00       4.00 r
  ff1/q_reg/next_state (**SEQGEN**)        0.00       4.00 r
  data arrival time                                   4.00

  clock theclk' (rise edge)                1.50       1.50
  clock network delay (ideal)              1.00       2.50
  clock uncertainty                       -0.40       2.10
  ff1/q_reg/clocked_on (**SEQGEN**)        0.00       2.10 r
  library setup time                       0.00       2.10
  data required time                                  2.10
  -----------------------------------------------------------
  data required time                                  2.10
  data arrival time                                  -4.00
  -----------------------------------------------------------
  slack (VIOLATED)                                   -1.90
```

4.11. Output delay(met)

4.11.1. Output delay script file

```
# Create user defined variables
set CLK_PORT [get_ports CLK]
set CLK_PERIOD 3.00
set CLK_SKEW 0.14

set_clock_uncertainty -setup 0.4 $CLK_PORT

set_clock_latency 1.0 $CLK_PORT
set_clock_uncertainty -hold 0.54 $CLK_PORT


create_clock -name theclk -period 20 [get_ports CLK]
set_output_delay -clock theclk -max 8 [get_ports  ff2/q]
set_output_delay -clock theclk -min -3 [get_ports ff2/q]
```

4.11.2. Output delay settings



4.11.3. Output delay result

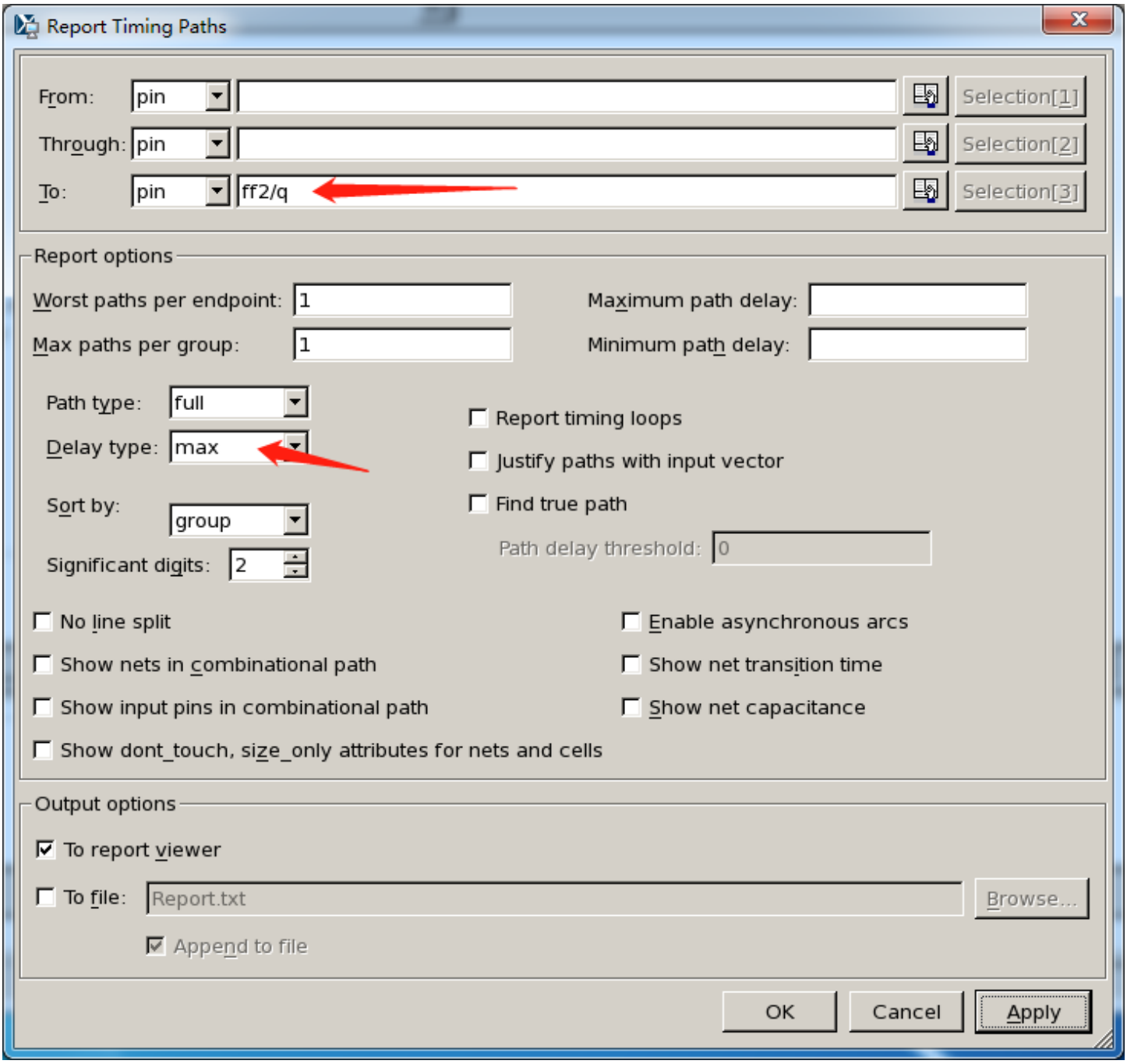
```
Startpoint: ff2/q_reg (rising edge-triggered flip-flop clocked by theclk)
  Endpoint: ff2/q (internal path endpoint clocked by theclk)
  Path Group: theclk
  Path Type: max

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  time_test          5KGATES               ssc_core

  Point                                    Incr       Path
  -----------------------------------------------------------
  clock theclk (rise edge)                 0.00       0.00
  clock network delay (ideal)              1.00       1.00
  ff2/q_reg/clocked_on (**SEQGEN**)        0.00       1.00 r
  ff2/q_reg/Q (**SEQGEN**)                 0.00       1.00 r
  ff2/q (dff)                              0.00       1.00 r
  data arrival time                                   1.00

  clock theclk (rise edge)                20.00      20.00
  clock network delay (ideal)              0.00      20.00
  output external delay                   -8.00      12.00
  data required time                                  12.00
  -----------------------------------------------------------
  data required time                                  12.00
  data arrival time                                   -1.00
  -----------------------------------------------------------
  slack (MET)                                         11.00
```

4.12. Output delay(violated)

4.12.1. Output delay script file

```
# Create user defined variables
set CLK_PORT [get_ports CLK]
set CLK_PERIOD 3.00
set CLK_SKEW 0.14

set_clock_uncertainty -setup 0.4 $CLK_PORT

set_clock_latency 1.0 $CLK_PORT
set_clock_uncertainty -hold 0.54 $CLK_PORT


create_clock -name theclk -period 5 [get_ports CLK]
set_output_delay -clock theclk -max 8 [get_ports  ff2/q]
set_output_delay -clock theclk -min -3 [get_ports ff2/q]
```

4.12.2. Output delay settings

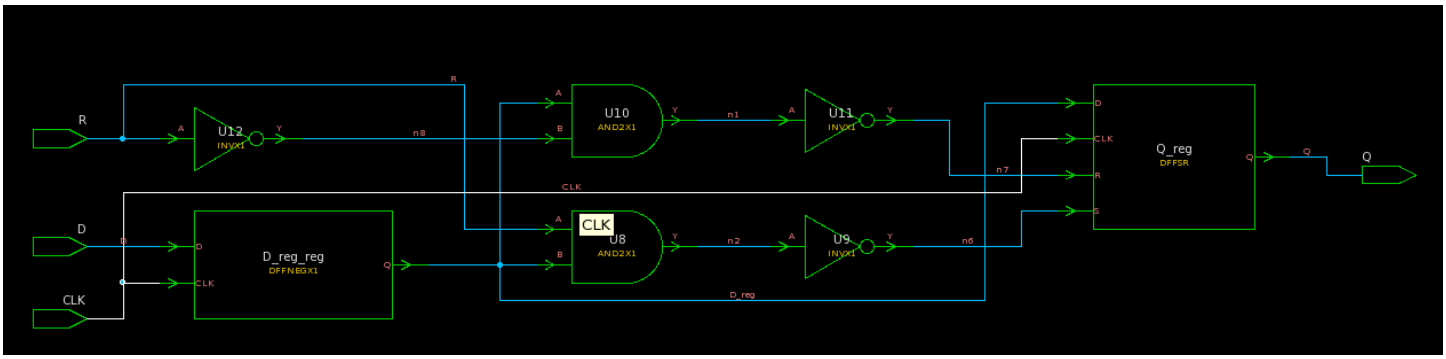


4.12.3. Output delay result

```
Startpoint: ff2/q_reg (rising edge-triggered flip-flop clocked by theclk)
  Endpoint: ff2/q (internal path endpoint clocked by theclk)
  Path Group: theclk
  Path Type: max

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  time_test          5KGATES               ssc_core

  Point                                    Incr       Path
  -----------------------------------------------------------
  clock theclk (rise edge)                 0.00       0.00
  clock network delay (ideal)              1.00       1.00
  ff2/q_reg/clocked_on (**SEQGEN**)        0.00       1.00 r
  ff2/q_reg/Q (**SEQGEN**)                 0.00       1.00 r
  ff2/q (dff)                              0.00       1.00 r
  data arrival time                                   1.00

  clock theclk (rise edge)                 5.00       5.00
  clock network delay (ideal)              0.00       5.00
  output external delay                   -8.00      -3.00
  data required time                                 -3.00
  -----------------------------------------------------------
  data required time                                 -3.00
  data arrival time                                  -1.00
  -----------------------------------------------------------
  slack (VIOLATED)                                   -4.00
```

5. Recovery time and removal time

5.1. module figure



5.2. module Verilog file

```
module dff_async (input CLK,
                  input D, R,
                  output reg Q);

    reg D_reg;
    always @(negedge CLK) D_reg <= D;

    always @(posedge CLK or posedge D_reg) begin
        if(D_reg) Q <= R;
        else Q <= D_reg;
    end
endmodule
```

5.3. module gate-level file

```
module dff_async ( CLK, D, R, Q );
  input CLK, D, R;
  output Q;
  wire   D_reg, n10, n11, n12, n13, n14;

  DFFPOSX1 D_reg_reg ( .D(D), .CLK(CLK), .Q(D_reg) );
  DFFSR Q_reg ( .D(D_reg), .CLK(CLK), .R(n13), .S(n12), .Q(Q) );
  AND2X1 U11 ( .A(R), .B(D_reg), .Y(n10) );
  INVX1 U12 ( .A(n10), .Y(n12) );
  AND2X1 U13 ( .A(D_reg), .B(n14), .Y(n11) );
  INVX1 U14 ( .A(n11), .Y(n13) );
  INVX1 U15 ( .A(R), .Y(n14) );
endmodule
```

5.4. time script file

```
#/* All verilog files, separated by spaces         */
set my_verilog_files [list /home/zhang/Asic/time/dff_async_fr/dff_async_fr.v]

#/* Top-level Module                               */
set my_toplevel dff_async

#/************************************************/
#/* No modifications needed below                 */
#/************************************************/
set OSU_FREEPDK [format "%s%s"  [getenv "PDK_DIR"] "/osu_soc/lib/files"]
set search_path [concat  $search_path $OSU_FREEPDK]
set alib_library_analysis_path $OSU_FREEPDK
set link_library [set target_library [concat  [list
/export/opt/FreePDK45/osu_soc/lib/files/gscl45nm.db] [list dw_foundation.sldb]]]
set target_library "/export/opt/FreePDK45/osu_soc/lib/files/gscl45nm.db"
define_design_lib WORK -path ./
set verilogout_show_unconnected_pins "true"
analyze -f verilog $my_verilog_files

elaborate $my_toplevel

current_design $my_toplevel

link
uniquify
compile -ungroup_all -map_effort medium

compile -incremental_mapping -map_effort medium
set filename [format "%s%s"  $my_toplevel "_gatelevel.v"]
write -f verilog -output $filename
#quit
```

5.5. recovery time check (met)

```
Startpoint: D_reg_reg (falling edge-triggered flip-flop clocked by CLK)
Endpoint: Q_reg (recovery check against rising-edge clock CLK)
Path Group: **async_default**
Path Type: max

Point                                    Incr       Path
-----------------------------------------------------------
clock CLK (fall edge)                    6.00       6.00
clock network delay (ideal)              0.00       6.00
D_reg_reg/CLK (DFFNEGX1)                 0.00       6.00 f
D_reg_reg/Q (DFFNEGX1)                   0.08       6.08 f
U8/Y (AND2X1)                            0.04       6.12 f
U9/Y (INVX1)                             0.00       6.13 r
Q_reg/S (DFFSR)                          0.00       6.13 r
data arrival time                                   6.13

clock CLK (rise edge)                   12.00      12.00
clock network delay (ideal)              0.00      12.00
clock reconvergence pessimism            0.00      12.00
Q_reg/CLK (DFFSR)                                  12.00 r
library recovery time                    0.02      12.02
data required time                                 12.02
-----------------------------------------------------------
data required time                                 12.02
data arrival time                                  -6.13
-----------------------------------------------------------
slack (MET)                                         5.89
```

5.6. recovery time check(violet)

```
Startpoint: D_reg_reg (falling edge-triggered flip-flop clocked by CLK)
Endpoint: Q_reg (recovery check against rising-edge clock CLK)
Path Group: **async_default**
Path Type: max

Point                                    Incr       Path
-----------------------------------------------------------
clock CLK (fall edge)                    6.00       6.00
clock network delay (ideal)              8.00      14.00
D_reg_reg/CLK (DFFNEGX1)                 0.00      14.00 f
D_reg_reg/Q (DFFNEGX1)                   0.08      14.08 f
U8/Y (AND2X1)                            0.04      14.12 f
U9/Y (INVX1)                             0.00      14.13 r
Q_reg/S (DFFSR)                          0.00      14.13 r
data arrival time                                  14.13

clock CLK (rise edge)                   12.00      12.00
clock network delay (ideal)              8.00      20.00
clock reconvergence pessimism            0.00      20.00
clock uncertainty                      -12.00       8.00
Q_reg/CLK (DFFSR)                                   8.00 r
library recovery time                    0.02       8.02
data required time                                  8.02
-----------------------------------------------------------
data required time                                  8.02
data arrival time                                 -14.13
-----------------------------------------------------------
slack (VIOLATED)                                   -6.11
```

5.7. removal time check(met)

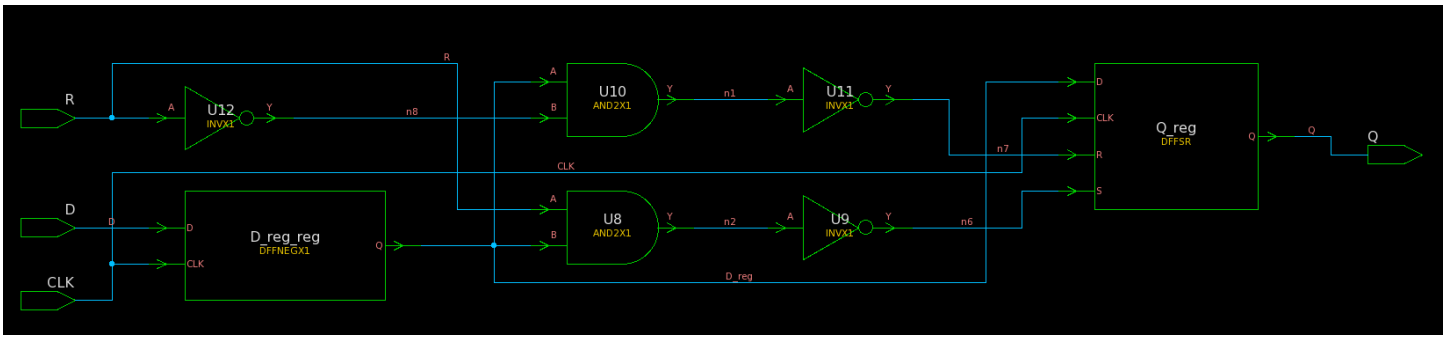
```
Startpoint: D_reg_reg (falling edge-triggered flip-flop clocked by CLK)
Endpoint: Q_reg (removal check against rising-edge clock CLK)
Path Group: **async_default**
Path Type: min

Point                                    Incr       Path
-----------------------------------------------------------
clock CLK (fall edge)                    6.00       6.00
clock network delay (ideal)              0.00       6.00
D_reg_reg/CLK (DFFNEGX1)                 0.00       6.00 f
D_reg_reg/Q (DFFNEGX1)                   0.08       6.08 f
U10/Y (AND2X1)                           0.03       6.11 f
U11/Y (INVX1)                            0.01       6.12 r
Q_reg/R (DFFSR)                          0.00       6.12 r
data arrival time                                   6.12

clock CLK (rise edge)                    0.00       0.00
clock network delay (ideal)              0.00       0.00
clock reconvergence pessimism            0.00       0.00
clock uncertainty                       -0.80      -0.80
Q_reg/CLK (DFFSR)                                  -0.80 r
library removal time                     0.21      -0.59
data required time                                 -0.59
-----------------------------------------------------------
data required time                                 -0.59
data arrival time                                  -6.12
-----------------------------------------------------------
slack (MET)                                         6.71
```

5.8. removal time check(violet)

```
Startpoint: D_reg_reg (falling edge-triggered flip-flop clocked by CLK)
Endpoint: Q_reg (removal check against rising-edge clock CLK)
Path Group: **async_default**
Path Type: min

Point                                          Incr       Path
-----------------------------------------------------------------
clock CLK (fall edge)                          6.00       6.00
clock network delay (ideal)                    8.00      14.00
D_reg_reg/CLK (DFFNEGX1)                       0.00      14.00 f
D_reg_reg/Q (DFFNEGX1)                         0.08      14.08 f
U10/Y (AND2X1)                                 0.03      14.11 f
U11/Y (INVX1)                                  0.01      14.12 r
Q_reg/R (DFFSR)                                0.00      14.12 r
data arrival time                                        14.12

clock CLK (rise edge)                          0.00       0.00
clock network delay (ideal)                    8.00       8.00
clock reconvergence pessimism                  0.00       8.00
clock uncertainty                             12.00      20.00
Q_reg/CLK (DFFSR)                                        20.00 r
library removal time                           0.21      20.21
data required time                                       20.21
-----------------------------------------------------------------
data required time                                       20.21
data arrival time                                       -14.12
-----------------------------------------------------------------
slack (VIOLATED)                                         -6.09
```

6. Half-cycle paths

6.1. Module figure



6.2. Module Verilog file

```
module dff_async (input CLK,
                  input D, R,
                  output reg Q);
     reg D_reg;
     always @(negedge CLK) D_reg <= D;

     always @(posedge CLK or posedge D_reg) begin
          if(D_reg) Q <= R;
          else Q <= D_reg;
     end
endmodule
```

6.3. Module gate-level file

```
module dff_async ( CLK, D, R, Q );
  input CLK, D, R;
  output Q;
  wire   D_reg, n10, n11, n12, n13, n14;

  DFFPOSX1 D_reg_reg ( .D(D), .CLK(CLK), .Q(D_reg) );
  DFFSR Q_reg ( .D(D_reg), .CLK(CLK), .R(n13), .S(n12), .Q(Q) );
  AND2X1 U11 ( .A(R), .B(D_reg), .Y(n10) );
  INVX1 U12 ( .A(n10), .Y(n12) );
  AND2X1 U13 ( .A(D_reg), .B(n14), .Y(n11) );
  INVX1 U14 ( .A(n11), .Y(n13) );
  INVX1 U15 ( .A(R), .Y(n14) );
endmodule
```

6.4. Module script file (met)

```
set link_path {* /export/opt/FreePDK45/osu_soc/lib/files/gscl45nm.db}


read_verilog /home/zhang/Asic/time/dff_async_gatelevel.v


link_design dff_async


#Create clock with period 10 (default waveform)

create_clock -name CLK -period 12 [get_ports CLK]


#Report the setup time check (should pass)

report_timing -path full -delay max -nworst 1 -max_paths 1 -significant_digits 2 -sort_by
group -group **CLK**

set_clock_uncertainty -0.8 -hold [get_clocks CLK]

report_timing -path full -delay min -nworst 1 -max_paths 1 -significant_digits 2 -sort_by
group -group **CLK**


#Add clock uncertainty for setup and clock latency

set_clock_latency -source 8 [get_clocks CLK]

set_clock_uncertainty 5 -setup -hold [get_clocks CLK]


#Report the setup time check (should fail)

report_timing -path full -delay max -nworst 1 -max_paths 1 -significant_digits 2 -sort_by
group -group **CLK**


report_timing -path full -delay min -nworst 1 -max_paths 1 -significant_digits 2 -sort_by
group -group **CLK**
```

6.5. Half cycle （met）

```
Startpoint: D_reg_reg (falling edge-triggered flip-flop clocked by CLK)
Endpoint: Q_reg (rising edge-triggered flip-flop clocked by CLK)
Path Group: CLK
Path Type: max

Point                                    Incr       Path
-----------------------------------------------------------
clock CLK (fall edge)                    6.00       6.00
clock network delay (ideal)              8.00      14.00
D_reg_reg/CLK (DFFNEGX1)                 0.00      14.00 f
D_reg_reg/Q (DFFNEGX1)                   0.06      14.06 r
Q_reg/D (DFFSR)                          0.00      14.06 r
data arrival time                                  14.06

clock CLK (rise edge)                   12.00      12.00
clock network delay (ideal)              8.00      20.00
clock reconvergence pessimism            0.00      20.00
clock uncertainty                       -5.00      15.00
Q_reg/CLK (DFFSR)                                  15.00 r
library setup time                      -0.08      14.92
data required time                                 14.92
-----------------------------------------------------------
data required time                                 14.92
data arrival time                                 -14.06
-----------------------------------------------------------
slack (MET)                                         0.86
```

6.6. Module script file (violeted)

```
set link_path {* /export/opt/FreePDK45/osu_soc/lib/files/gscl45nm.db}


read_verilog /home/zhang/Asic/time/dff_async_gatelevel.v


link_design dff_async


#Create clock with period 10 (default waveform)

create_clock -name CLK -period 12 [get_ports CLK]


#Report the setup time check (should pass)

report_timing -path full -delay max -nworst 1 -max_paths 1 -significant_digits 2 -sort_by
group -group **CLK**

set_clock_uncertainty -0.8 -hold [get_clocks CLK]

report_timing -path full -delay min -nworst 1 -max_paths 1 -significant_digits 2 -sort_by
group -group **CLK**


#Add clock uncertainty for setup and clock latency

set_clock_latency -source 8 [get_clocks CLK]

set_clock_uncertainty 8 -setup -hold [get_clocks CLK]


#Report the setup time check (should fail)

report_timing -path full -delay max -nworst 1 -max_paths 1 -significant_digits 2 -sort_by
group -group **CLK**


report_timing -path full -delay min -nworst 1 -max_paths 1 -significant_digits 2 -sort_by
group -group **CLK**
```

6.7. Half-cycle (violeted)

```
Startpoint: D_reg_reg (falling edge-triggered flip-flop clocked by CLK)
Endpoint: Q_reg (rising edge-triggered flip-flop clocked by CLK)
Path Group: CLK
Path Type: max

Point                                    Incr       Path
-----------------------------------------------------------
clock CLK (fall edge)                    6.00       6.00
clock network delay (ideal)              8.00      14.00
D_reg_reg/CLK (DFFNEGX1)                 0.00      14.00 f
D_reg_reg/Q (DFFNEGX1)                   0.06      14.06 r
Q_reg/D (DFFSR)                          0.00      14.06 r
data arrival time                                  14.06

clock CLK (rise edge)                   12.00      12.00
clock network delay (ideal)              8.00      20.00
clock reconvergence pessimism            0.00      20.00
clock uncertainty                       -8.00      12.00
Q_reg/CLK (DFFSR)                                  12.00 r
library setup time                      -0.08      11.92
data required time                                 11.92
-----------------------------------------------------------
data required time                                 11.92
data arrival time                                 -14.06
-----------------------------------------------------------
slack (VIOLATED)                                   -2.14
```

7. Multicycle setup specification

7.1. Script file

```
set link_path {* /export/opt/FreePDK45/osu_soc/lib/files/gscl45nm.db}


read_verilog /home/zhang/Asic/time/dff_async_fr/dff_async_multi_gatelevel.v


link_design dff_async


#Create clock with period 10 (default waveform)

create_clock -name CLKM -period 12 [get_ports CLKM]
create_clock -name CLKP -period 3 [get_ports CLKP]


#Report the setup time check (should pass)

report_timing -path full -delay max -nworst 1 -max_paths 1 -significant_digits 2 -sort_by
group -group **CLKP**

set_clock_uncertainty -0.8 -hold [get_clocks CLKM]

report_timing -path full -delay min -nworst 1 -max_paths 1 -significant_digits 2 -sort_by
group -group **CLKP**


#Add clock uncertainty for setup and clock latency

set_clock_latency -source 8 [get_clocks CLKM]

set_clock_uncertainty 8 -setup -hold [get_clocks CLKM]


#Report the setup time check (should fail)

report_timing -path full -delay max -nworst 1 -max_paths 1 -significant_digits 2 -sort_by
group -group **CLKM**


report_timing -path full -delay min -nworst 1 -max_paths 1 -significant_digits 2 -sort_by
group -group **CLKM**
```

7.2. Setup (violated)

```
Startpoint: D_reg_reg (falling edge-triggered flip-flop clocked by CLKP)
Endpoint: Q_reg (rising edge-triggered flip-flop clocked by CLKM)
Path Group: CLKM
Path Type: max

Point                                    Incr       Path
-----------------------------------------------------------
clock CLKP (fall edge)                  10.50      10.50
clock network delay (ideal)              8.00      18.50
D_reg_reg/CLK (DFFNEGX1)                 0.00      18.50 f
D_reg_reg/Q (DFFNEGX1)                   0.06      18.56 r
Q_reg/D (DFFSR)                          0.00      18.56 r
data arrival time                                  18.56

clock CLKM (rise edge)                  12.00      12.00
clock network delay (ideal)              8.00      20.00
clock reconvergence pessimism            0.00      20.00
clock uncertainty                       -8.00      12.00
Q_reg/CLK (DFFSR)                                  12.00 r
library setup time                      -0.08      11.92
data required time                                 11.92
-----------------------------------------------------------
data required time                                 11.92
data arrival time                                 -18.56
-----------------------------------------------------------
slack (VIOLATED)                                   -6.64
```

7.3. Hold(violated)

```
Startpoint: D_reg_reg (falling edge-triggered flip-flop clocked by CLKP)
Endpoint: Q_reg (rising edge-triggered flip-flop clocked by CLKM)
Path Group: CLKM
Path Type: min

Point                                    Incr       Path
-----------------------------------------------------------
clock CLKP (fall edge)                   1.50       1.50
clock network delay (ideal)              8.00       9.50
D_reg_reg/CLK (DFFNEGX1)                 0.00       9.50 f
D_reg_reg/Q (DFFNEGX1)                   0.06       9.56 r
Q_reg/D (DFFSR)                          0.00       9.56 r
data arrival time                                   9.56

clock CLKM (rise edge)                   0.00       0.00
clock network delay (ideal)              8.00       8.00
clock reconvergence pessimism            0.00       8.00
clock uncertainty                        8.00      16.00
Q_reg/CLK (DFFSR)                                  16.00 r
library hold time                       -0.01      15.99
data required time                                 15.99
-----------------------------------------------------------
data required time                                 15.99
data arrival time                                  -9.56
-----------------------------------------------------------
slack (VIOLATED)                                   -6.43
```

7.4. Script file(met)

```
set link_path {* /export/opt/FreePDK45/osu_soc/lib/files/gscl45nm.db}


read_verilog /home/zhang/Asic/time/dff_async_fr/dff_async_multi_gatelevel.v


link_design dff_async


#Create clock with period 10 (default waveform)

create_clock -name CLKM -period 12 [get_ports CLKM]
create_clock -name CLKP -period 3 [get_ports CLKP]


#Report the setup time check (should pass)

report_timing -path full -delay max -nworst 1 -max_paths 1 -significant_digits 2 -sort_by
group -group **CLKP**

set_clock_uncertainty -0.8 -hold [get_clocks CLKM]

report_timing -path full -delay min -nworst 1 -max_paths 1 -significant_digits 2 -sort_by
group -group **CLKP**


#Add clock uncertainty for setup and clock latency

set_clock_latency -source 8 [get_clocks CLKM]

set_clock_uncertainty 1 -setup -hold [get_clocks CLKM]


#Report the setup time check (should fail)

report_timing -path full -delay max -nworst 1 -max_paths 1 -significant_digits 2 -sort_by
group -group **CLKM**


report_timing -path full -delay min -nworst 1 -max_paths 1 -significant_digits 2 -sort_by
group -group **CLKM**
```

7.5. Setup (met)

```
Startpoint: D_reg_reg (falling edge-triggered flip-flop clocked by CLKP)
Endpoint: Q_reg (rising edge-triggered flip-flop clocked by CLKM)
Path Group: CLKM
Path Type: max

Point                                    Incr       Path
-----------------------------------------------------------
clock CLKP (fall edge)                  10.50      10.50
clock network delay (ideal)              8.00      18.50
D_reg_reg/CLK (DFFNEGX1)                 0.00      18.50 f
D_reg_reg/Q (DFFNEGX1)                   0.06      18.56 r
Q_reg/D (DFFSR)                          0.00      18.56 r
data arrival time                                  18.56

clock CLKM (rise edge)                  12.00      12.00
clock network delay (ideal)              8.00      20.00
clock reconvergence pessimism            0.00      20.00
clock uncertainty                       -1.00      19.00
Q_reg/CLK (DFFSR)                                  19.00 r
library setup time                      -0.08      18.92
data required time                                 18.92
-----------------------------------------------------------
data required time                                 18.92
data arrival time                                 -18.56
-----------------------------------------------------------
slack (MET)                                         0.36
```

7.6. Hold（met）

```
Startpoint: D_reg_reg (falling edge-triggered flip-flop clocked by CLKP)
Endpoint: Q_reg (rising edge-triggered flip-flop clocked by CLKM)
Path Group: CLKM
Path Type: min

Point                                    Incr       Path
-----------------------------------------------------------
clock CLKP (fall edge)                   1.50       1.50
clock network delay (ideal)              8.00       9.50
D_reg_reg/CLK (DFFNEGX1)                 0.00       9.50 f
D_reg_reg/Q (DFFNEGX1)                   0.06       9.56 r
Q_reg/D (DFFSR)                          0.00       9.56 r
data arrival time                                   9.56

clock CLKM (rise edge)                   0.00       0.00
clock network delay (ideal)              8.00       8.00
clock reconvergence pessimism            0.00       8.00
clock uncertainty                        1.00       9.00
Q_reg/CLK (DFFSR)                                   9.00 r
library hold time                       -0.01       8.99
data required time                                  8.99
-----------------------------------------------------------
data required time                                  8.99
data arrival time                                  -9.56
-----------------------------------------------------------
slack (MET)                                         0.57
```

8. Non-integer multiple clocks

8.1. Script files (met)

```
set link_path {* /export/opt/FreePDK45/osu_soc/lib/files/gscl45nm.db}


read_verilog /home/zhang/Asic/time/dff_async_fr/dff_async_multi_gatelevel.v


link_design dff_async


#Create clock with period 10 (default waveform)

create_clock -name CLKM -period 15 [get_ports CLKM]
create_clock -name CLKP -period 17 [get_ports CLKP]


#Report the setup time check (should pass)

report_timing -path full -delay max -nworst 1 -max_paths 1 -significant_digits 2 -sort_by
group -group **CLKP**

set_clock_uncertainty 0.1 -hold [get_clocks CLKM]

report_timing -path full -delay min -nworst 1 -max_paths 1 -significant_digits 2 -sort_by
group -group **CLKP**


#Add clock uncertainty for setup and clock latency

set_clock_latency -source 8 [get_clocks CLKM]

set_clock_uncertainty 0.2 -setup -hold [get_clocks CLKM]


#Report the setup time check (should fail)

report_timing -path full -delay max -nworst 1 -max_paths 1 -significant_digits 2 -sort_by
group -group **CLKM**


report_timing -path full -delay min -nworst 1 -max_paths 1 -significant_digits 2 -sort_by
group -group **CLKM**
```

8.2. Script files (violeted)

```
set link_path {* /export/opt/FreePDK45/osu_soc/lib/files/gscl45nm.db}


read_verilog /home/zhang/Asic/time/dff_async_fr/dff_async_multi_gatelevel.v


link_design dff_async


#Create clock with period 10 (default waveform)

create_clock -name CLKM -period 13 [get_ports CLKM]
create_clock -name CLKP -period 14 [get_ports CLKP]


#Report the setup time check (should pass)

report_timing -path full -delay max -nworst 1 -max_paths 1 -significant_digits 2 -sort_by
group -group **CLKP**

set_clock_uncertainty -0.8 -hold [get_clocks CLKM]

report_timing -path full -delay min -nworst 1 -max_paths 1 -significant_digits 2 -sort_by
group -group **CLKP**


#Add clock uncertainty for setup and clock latency

set_clock_latency -source 8 [get_clocks CLKM]

set_clock_uncertainty 1 -setup -hold [get_clocks CLKM]


#Report the setup time check (should fail)

report_timing -path full -delay max -nworst 1 -max_paths 1 -significant_digits 2 -sort_by
group -group **CLKM**


report_timing -path full -delay min -nworst 1 -max_paths 1 -significant_digits 2 -sort_by
group -group **CLKM**
```

8.3. Setup (met)

```
Startpoint: D_reg_reg (falling edge-triggered flip-flop clocked by CLKP)
 Endpoint: Q_reg (rising edge-triggered flip-flop clocked by CLKM)
 Path Group: CLKM
 Path Type: max

 Point                                    Incr       Path
 -----------------------------------------------------------
 clock CLKP (fall edge)                  59.50      59.50
 clock network delay (ideal)              8.00      67.50
 D_reg_reg/CLK (DFFNEGX1)                 0.00      67.50 f
 D_reg_reg/Q (DFFNEGX1)                   0.06      67.56 r
 Q_reg/D (DFFSR)                          0.00      67.56 r
 data arrival time                                  67.56

 clock CLKM (rise edge)                  60.00      60.00
 clock network delay (ideal)              8.00      68.00
 clock reconvergence pessimism            0.00      68.00
 clock uncertainty                       -0.20      67.80
 Q_reg/CLK (DFFSR)                                  67.80 r
 library setup time                      -0.08      67.72
 data required time                                 67.72
 -----------------------------------------------------------
 data required time                                 67.72
 data arrival time                                 -67.56
 -----------------------------------------------------------
 slack (MET)                                         0.16
```

8.4. Setup (violeted)

```
Startpoint: D_reg_reg (falling edge-triggered flip-flop clocked by CLKP)
Endpoint: Q_reg (rising edge-triggered flip-flop clocked by CLKM)
Path Group: CLKM
Path Type: max

Point                                    Incr       Path
-----------------------------------------------------------
clock CLKP (fall edge)                  77.00      77.00
clock network delay (ideal)              8.00      85.00
D_reg_reg/CLK (DFFNEGX1)                 0.00      85.00 f
D_reg_reg/Q (DFFNEGX1)                   0.06      85.06 r
Q_reg/D (DFFSR)                          0.00      85.06 r
data arrival time                                  85.06

clock CLKM (rise edge)                  78.00      78.00
clock network delay (ideal)              8.00      86.00
clock reconvergence pessimism            0.00      86.00
clock uncertainty                       -1.00      85.00
Q_reg/CLK (DFFSR)                                  85.00 r
library setup time                      -0.08      84.92
data required time                                 84.92
-----------------------------------------------------------
data required time                                 84.92
data arrival time                                 -85.06
-----------------------------------------------------------
slack (VIOLATED)                                   -0.14
```

8.5. Hold(met)

```
Startpoint: D_reg_reg (falling edge-triggered flip-flop clocked by CLKP)
Endpoint: Q_reg (rising edge-triggered flip-flop clocked by CLKM)
Path Group: CLKM
Path Type: min

Point                                    Incr       Path
-----------------------------------------------------------
clock CLKP (fall edge)                 195.50     195.50
clock network delay (ideal)              8.00     203.50
D_reg_reg/CLK (DFFNEGX1)                 0.00     203.50 f
D_reg_reg/Q (DFFNEGX1)                   0.06     203.56 r
Q_reg/D (DFFSR)                          0.00     203.56 r
data arrival time                                 203.56

clock CLKM (rise edge)                 195.00     195.00
clock network delay (ideal)              8.00     203.00
clock reconvergence pessimism            0.00     203.00
clock uncertainty                        0.10     203.10
Q_reg/CLK (DFFSR)                                 203.10 r
library hold time                       -0.01     203.09
data required time                                203.09
-----------------------------------------------------------
data required time                                203.09
data arrival time                                -203.56
-----------------------------------------------------------
slack (MET)                                         0.47
```

8.6. Hold(violated)

```
Startpoint: D_reg_reg (falling edge-triggered flip-flop clocked by CLKP)
Endpoint: Q_reg (rising edge-triggered flip-flop clocked by CLKM)
Path Group: CLKM
Path Type: min

Point                                    Incr       Path
-----------------------------------------------------------
clock CLKP (fall edge)                  91.00      91.00
clock network delay (ideal)              8.00      99.00
D_reg_reg/CLK (DFFNEGX1)                 0.00      99.00 f
D_reg_reg/Q (DFFNEGX1)                   0.06      99.06 r
Q_reg/D (DFFSR)                          0.00      99.06 r
data arrival time                                  99.06

clock CLKM (rise edge)                  91.00      91.00
clock network delay (ideal)              8.00      99.00
clock reconvergence pessimism            0.00      99.00
clock uncertainty                        1.00     100.00
Q_reg/CLK (DFFSR)                                 100.00 r
library hold time                       -0.01      99.99
data required time                                 99.99
-----------------------------------------------------------
data required time                                 99.99
data arrival time                                 -99.06
-----------------------------------------------------------
slack (VIOLATED)                                   -0.93
```

9. Phase shift clocks

9.1. Script file(met)

```
set link_path {* /export/opt/FreePDK45/osu_soc/lib/files/gscl45nm.db}


read_verilog /home/zhang/Asic/time/dff_async_fr/dff_async_shift_gatelevel.v


link_design dff_async


#Create clock with period 10 (default waveform)

create_clock -name CKM   -period 2.0    -waveform {0 1.0}    [get_ports CKM]
create_clock -name CKM90 -period 2.0    -waveform {0.5 1.5}      [get_ports CKM90]


#Report the setup time check (should pass)

set_clock_uncertainty 1 -hold [get_clocks CKM90]

report_timing -path full -delay max -nworst 1 -max_paths 1 -significant_digits 2 -sort_by
group -group **CKM**

set_clock_uncertainty 0.1 -hold [get_clocks CKM90]

report_timing -path full -delay min -nworst 1 -max_paths 1 -significant_digits 2 -sort_by
group -group **CKM**


#Add clock uncertainty for setup and clock latency

set_clock_latency -source 8 [get_clocks CKM90]

set_clock_uncertainty 0.2 -setup [get_clocks CKM]


#Report the setup time check (should fail)

report_timing -path full -delay max -nworst 1 -max_paths 1 -significant_digits 2 -sort_by
group -group **CKM90**

set_clock_uncertainty 0.2 -setup [get_clocks CKM]
report_timing -path full -delay min -nworst 1 -max_paths 1 -significant_digits 2 -sort_by
group -group **CKM90**
```

9.2. Setup(met)

```
Startpoint: D_reg_reg (falling edge-triggered flip-flop clocked by CKM)
Endpoint: Q_reg (rising edge-triggered flip-flop clocked by CKM90)
Path Group: CKM90
Path Type: max

Point                                    Incr       Path
-----------------------------------------------------------
clock CKM (fall edge)                    1.00       1.00
clock network delay (ideal)              8.00       9.00
D_reg_reg/CLK (DFFNEGX1)                 0.00       9.00 f
D_reg_reg/Q (DFFNEGX1)                   0.06       9.06 r
Q_reg/D (DFFSR)                          0.00       9.06 r
data arrival time                                   9.06

clock CKM90 (rise edge)                  2.50       2.50
clock network delay (ideal)              8.00      10.50
clock reconvergence pessimism            0.00      10.50
Q_reg/CLK (DFFSR)                                  10.50 r
library setup time                      -0.08      10.42
data required time                                 10.42
-----------------------------------------------------------
data required time                                 10.42
data arrival time                                  -9.06
-----------------------------------------------------------
slack (MET)                                         1.36
```

9.3. Hold(met)

```
Startpoint: D_reg_reg (falling edge-triggered flip-flop clocked by CKM)
Endpoint: Q_reg (rising edge-triggered flip-flop clocked by CKM90)
Path Group: CKM90
Path Type: min

Point                                    Incr       Path
-----------------------------------------------------------
clock CKM (fall edge)                    1.00       1.00
clock network delay (ideal)              8.00       9.00
D_reg_reg/CLK (DFFNEGX1)                 0.00       9.00 f
D_reg_reg/Q (DFFNEGX1)                   0.06       9.06 r
Q_reg/D (DFFSR)                          0.00       9.06 r
data arrival time                                   9.06

clock CKM90 (rise edge)                  0.50       0.50
clock network delay (ideal)              8.00       8.50
clock reconvergence pessimism            0.00       8.50
clock uncertainty                        0.10       8.60
Q_reg/CLK (DFFSR)                                   8.60 r
library hold time                       -0.01       8.59
data required time                                  8.59
-----------------------------------------------------------
data required time                                  8.59
data arrival time                                  -9.06
-----------------------------------------------------------
slack (MET)                                         0.47
```

9.4. Script file (violated)

```
set link_path {* /export/opt/FreePDK45/osu_soc/lib/files/gscl45nm.db}


read_verilog /home/zhang/Asic/time/dff_async_fr/dff_async_shift_gatelevel.v


link_design dff_async


#Create clock with period 10 (default waveform)

create_clock -name CKM   -period 2.0    -waveform {0 1.0}    [get_ports CKM]
create_clock -name CKM90 -period 2.0    -waveform {0.5 1.5}      [get_ports CKM90]


#Report the setup time check (should pass)

set_clock_uncertainty 2 -hold [get_clocks CKM90]

report_timing -path full -delay max -nworst 1 -max_paths 1 -significant_digits 2 -sort_by
group -group **CKM**


report_timing -path full -delay min -nworst 1 -max_paths 1 -significant_digits 2 -sort_by
group -group **CKM**


#Add clock uncertainty for setup and clock latency

set_clock_latency -source 8 [get_clocks CKM90]

set_clock_uncertainty 4.5 -setup [get_clocks CKM90]


#Report the setup time check (should fail)

report_timing -path full -delay max -nworst 1 -max_paths 1 -significant_digits 2 -sort_by
group -group **CKM90**

report_timing -path full -delay min -nworst 1 -max_paths 1 -significant_digits 2 -sort_by
group -group **CKM90**
```

9.5. Setup (violated)

```
Startpoint: D_reg_reg (falling edge-triggered flip-flop clocked by CKM)
Endpoint: Q_reg (rising edge-triggered flip-flop clocked by CKM90)
Path Group: CKM90
Path Type: max

Point                                    Incr       Path
-----------------------------------------------------------
clock CKM (fall edge)                    1.00       1.00
clock network delay (ideal)              8.00       9.00
D_reg_reg/CLK (DFFNEGX1)                 0.00       9.00 f
D_reg_reg/Q (DFFNEGX1)                   0.06       9.06 r
Q_reg/D (DFFSR)                          0.00       9.06 r
data arrival time                                   9.06

clock CKM90 (rise edge)                  2.50       2.50
clock network delay (ideal)              8.00      10.50
clock reconvergence pessimism            0.00      10.50
clock uncertainty                       -4.50       6.00
Q_reg/CLK (DFFSR)                                   6.00 r
library setup time                      -0.08       5.92
data required time                                  5.92
-----------------------------------------------------------
data required time                                  5.92
data arrival time                                  -9.06
-----------------------------------------------------------
slack (VIOLATED)                                   -3.14
```

9.6. Hold(violated)

```
Startpoint: D_reg_reg (falling edge-triggered flip-flop clocked by CKM)
Endpoint: Q_reg (rising edge-triggered flip-flop clocked by CKM90)
Path Group: CKM90
Path Type: min

Point                                    Incr       Path
-----------------------------------------------------------
clock CKM (fall edge)                    1.00       1.00
clock network delay (ideal)              8.00       9.00
D_reg_reg/CLK (DFFNEGX1)                 0.00       9.00 f
D_reg_reg/Q (DFFNEGX1)                   0.06       9.06 r
Q_reg/D (DFFSR)                          0.00       9.06 r
data arrival time                                   9.06

clock CKM90 (rise edge)                  0.50       0.50
clock network delay (ideal)              8.00       8.50
clock reconvergence pessimism            0.00       8.50
clock uncertainty                        2.00      10.50
Q_reg/CLK (DFFSR)                                  10.50 r
library hold time                       -0.01      10.49
data required time                                 10.49
-----------------------------------------------------------
data required time                                 10.49
data arrival time                                  -9.06
-----------------------------------------------------------
slack (VIOLATED)                                   -1.43
```