SPIROC 2

User Guide (Draft)

Monday, 4th february 2009

Introduction

The **CALICE** collaboration has designed an analogue HCAL prototype using Scintillating fibers read out by SiPM detectors. That 8000-channel physics prototype is currently in test beam at Fermilab. The read-out of that detector is ensured by an analogue front-end chip called FLC_SIPM . A new front-end chip called **SPIROC** (standing for Silicon PM Integrated Read Out Chip) has been designed to read out the upcoming technological demonstrator foreseen in 2009.

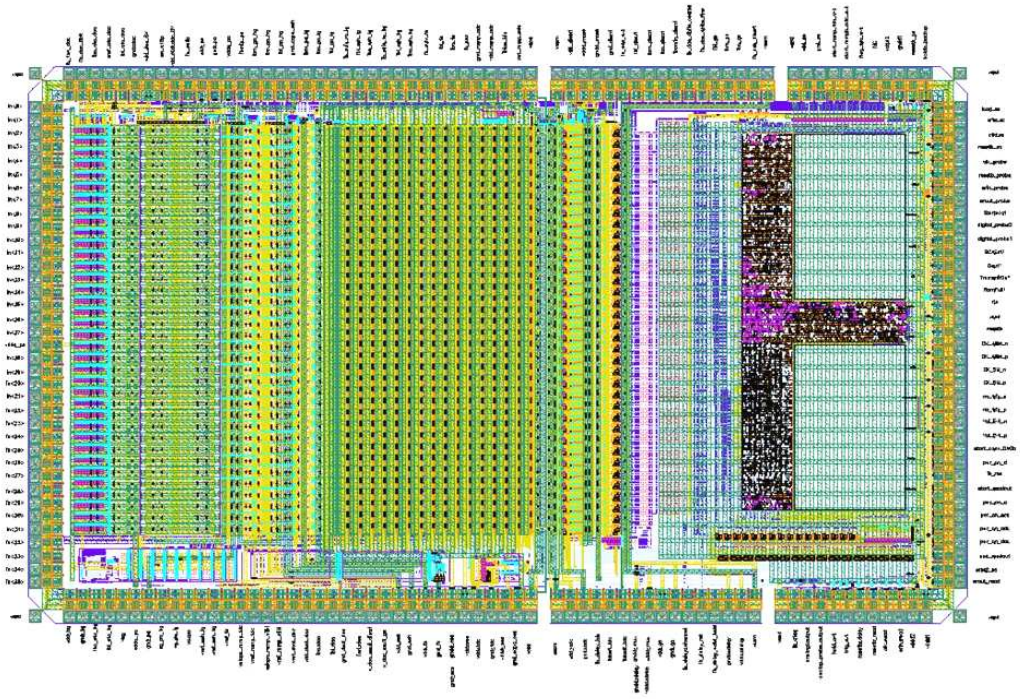
1 Presentation

SPIROC (SiPM Integrated Read Out Chip): Dedicated very front-end electronics for an ILC prototype hadronic calorimeter with SiPM readout.

SPIROC is a dedicated very front-end electronics for an ILC prototype hadronic calorimeter with SiPM readout. It has been realized in 0.35m SiGe technology. It has been developed to match the requirements of large dynamic range, low noise, low consumption, high precision and large number of readout channels needed.

SPIROC is an auto-triggered, bi-gain, 36-channel ASIC which allows to measure on each channel the charge from one photoelectron to 2000 and the time with a 100ps accurate TDC.
An analog memory array with a depth of 16 for each is used to store the time information and the charge measurement. A 12-bit Wilkinson ADC has been embedded to digitize the analog memory contents (time and charge on 2 gains). The data are then stored in a 4kbytes RAM. A very complex digital part has been integrated to manage all theses features and to transfer the data to the DAQ.

SPIROC 2 is the second iteration which corrects the bugs observed of the first version **(SPIROC 1).**



SPIROC layout

2 SPIROC description and global overview

SPIROC description

SPIROC main characteristics are the following:

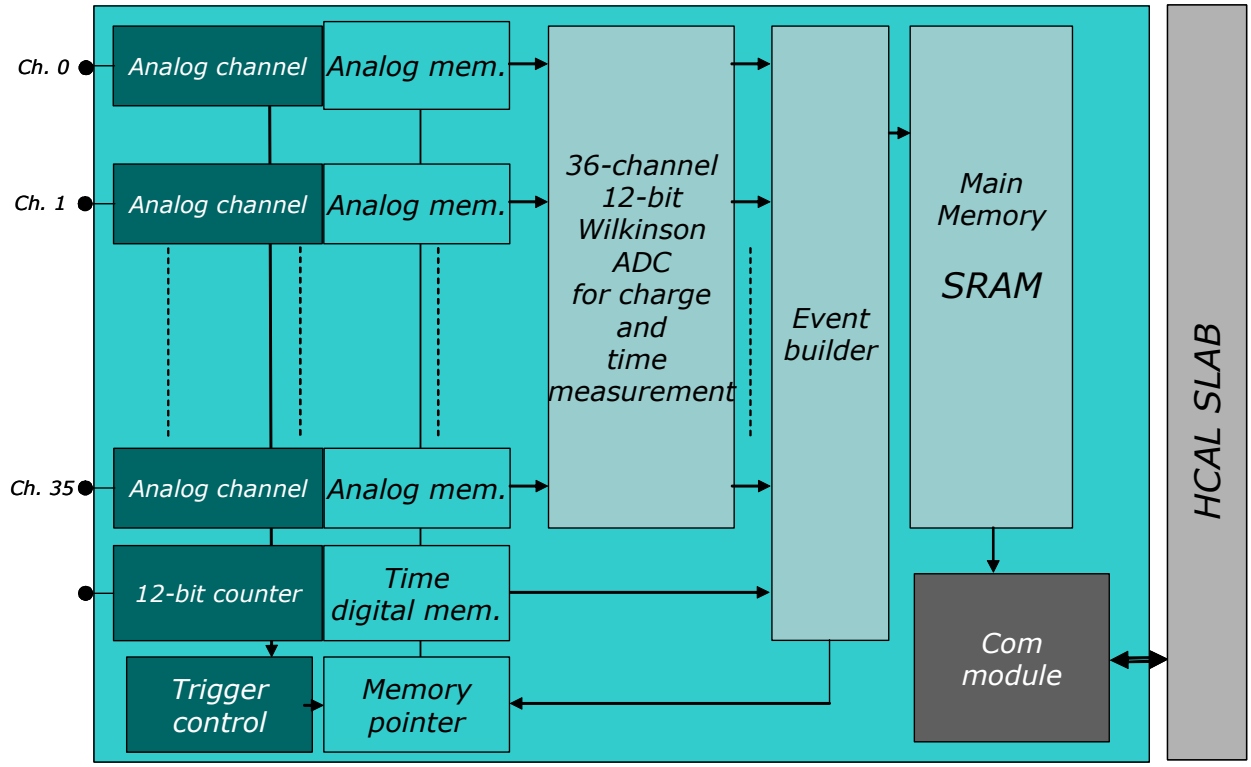
- AMS SiGe 0.35µm technology
- 32mm² (4.2mm × 7.2mm) area
- 5V/3.5V power supply
- 25µW per channel (in idle mode)
- Package: CQFP240

- Internal input 8-bit DAC (0-5V) for SiPM gain adjustment

- Energy measurement :
  - 2 gains / 12 bit ADC 1 pe → 2000 pe
  - Variable shaping time from 50ns to 100ns
  - pe/noise ratio : 11

- Time measurement :
  - 1 TDC (12 bits) step~100 ps
  - pe/noise ratio on trigger channel : 24
  - Fast shaper : ~15ns
  - Auto-Trigger on ½ pe

Global overview



3 Pinout

Pin	*Pin Name*	*Pin Type*	*Description*	*Comments*	Bank (on die)
1	**gnd_dac**	Power	Analogue (8-bit Digital to Analogue Convertor) Ground	**to GND**	Top
2	ibi_ota_dac	Analogue Bias	8-bit DAC OTA input stage bias current		Top
3	vref_ota_dac	Analogue Bias	8-bit DAC OTA reference bias voltage	to 4.5V	Top
4	ibo_ota_dac	Analogue Bias	8-bit DAC OTA output stage bias current		Top
5	ib_dac_8bits	Analogue Bias	8-bit input DAC bias current 1		Top
6	ib_1nA_dac	Analogue Bias	8-bit input DAC bias current 2		Top
7	**vssa**	Power	Analogue part Bulk	**to GND**	Top Left
8	***NC***				
9	in<0>	Analogue Input	Channel 0 to 17 inputs		Left
10	in<1>	Analogue Input	Channel 0 to 17 inputs		Left
11	in<2>	Analogue Input	Channel 0 to 17 inputs		Left
12	in<3>	Analogue Input	Channel 0 to 17 inputs		Left
13	in<4>	Analogue Input	Channel 0 to 17 inputs		Left
14	in<5>	Analogue Input	Channel 0 to 17 inputs		Left
15	in<6>	Analogue Input	Channel 0 to 17 inputs		Left
16	in<7>	Analogue Input	Channel 0 to 17 inputs		Left
17	in<8>	Analogue Input	Channel 0 to 17 inputs		Left
18	in<9>	Analogue Input	Channel 0 to 17 inputs		Left
19	in<10>	Analogue Input	Channel 0 to 17 inputs		Left
20	in<11>	Analogue Input	Channel 0 to 17 inputs		Left
21	in<12>	Analogue Input	Channel 0 to 17 inputs		Left
22	in<13>	Analogue Input	Channel 0 to 17 inputs		Left
23	in<14>	Analogue Input	Channel 0 to 17 inputs		Left
24	in<15>	Analogue Input	Channel 0 to 17 inputs		Left
25	in<16>	Analogue Input	Channel 0 to 17 inputs		Left
26	in<17>	Analogue Input	Channel 0 to 17 inputs		Left
27	**vdda_pa**	Power	Analogue (PreAmplifier) Power Supply	**to 3.3V**	Left
28	in<18>	Analogue Input	Channel 18 to 35 inputs		Left
29	in<19>	Analogue Input	Channel 18 to 35 inputs		Left
30	in<20>	Analogue Input	Channel 18 to 35 inputs		Left
31	in<21>	Analogue Input	Channel 18 to 35 inputs		Left
32	in<22>	Analogue Input	Channel 18 to 35 inputs		Left
33	in<23>	Analogue Input	Channel 18 to 35 inputs		Left
34	in<24>	Analogue Input	Channel 18 to 35 inputs		Left
35	in<25>	Analogue Input	Channel 18 to 35 inputs		Left
36	in<26>	Analogue Input	Channel 18 to 35 inputs		Left
37	in<27>	Analogue Input	Channel 18 to 35 inputs		Left
38	in<28>	Analogue Input	Channel 18 to 35 inputs		Left
39	in<29>	Analogue Input	Channel 18 to 35 inputs		Left
40	in<30>	Analogue Input	Channel 18 to 35 inputs		Left
41	in<31>	Analogue Input	Channel 18 to 35 inputs		Left
42	in<32>	Analogue Input	Channel 18 to 35 inputs		Left
43	in<33>	Analogue Input	Channel 18 to 35 inputs		Left
44	in<34>	Analogue Input	Channel 18 to 35 inputs		Left
45	in<35>	Analogue Input	Channel 18 to 35 inputs		Left
46	***NC***				
47	**vssa**	Power	Analogue part Bulk	**to GND**	Bottom Left

48	**vdd_bg**	Power	Analogue (BandGap) Power Supply	**to 3.3V**	Bottom
49	**gnd_bg**	Power	Analogue (BandGap) Ground	**to GND**	Bottom
50	ibo_ota_bg	Analogue Bias	BandGap OTA output stage bias current		Bottom
51	vbg	Analogue Output	BandGap output		Bottom
52	**vdda_pa**	Power	Analogue (PreAmplifiers) Power Supply	**to 3.3V**	Bottom
53	**gnd_pa**	Power	Analogue (PreAmplifiers) Ground	**to GND**	Bottom
54	vg_pa_hg	Analogue Bias	High Gain PreAmps bias voltage		Bottom
55	vg_pa_lg	Analogue Bias	Low Gain PreAmps bias voltage		Bottom
56	va_pa	Analogue Bias	Pre Amps bias voltage		Bottom
57	vref_ssh_lg	Analogue Bias	Low Gain Slow Shapers bias voltage		Bottom
58	vref_ssh_hg	Analogue Bias	High Gain Slow Shapers bias voltage		Bottom
59	vref_fs	Analogue Bias	Fast Shapers bias voltage		Bottom
60	vslope_ramp_tdc	Analogue Bias	TDC bias voltage 1		Bottom
61	vref_ramp_tdc	Analogue Bias	TDC bias voltage 2		Bottom
62	vslope_ramp_wilki	Analogue Bias	ADC bias voltage 1		Bottom
63	vref_ramp_wilki	Analogue Bias	ADC bias voltage 2		Bottom
64	vref_dual_dac	Analogue Bias	10-bit dual DAC OTAs bias voltage		Bottom
65	**vdd_dual_dac**	Power	Analogue (10-bit dual DAC) Power Supply	**to 3.3V**	Bottom
66	ibo_dac	Analogue Bias	10-bit dual DAC OTAs Output stage bias		Bottom
67	ibi_dac	Analogue Bias	10-bit dual DAC OTAs Input stage bias		Bottom
68	**gnd_dual_dac**	Power	Analogue (10-bit dual DAC) Ground	**to GND**	Bottom
69	iref_dac	Analogue Bias	10-bit dual DAC bias current		Bottom
70	v_dac_seuil_discri	Analogue Output	10-bit dual DAC output 1 (Trigger Discriminator Threshold)		Bottom
71	v_dac_seuil_gs	Analogue Output	10-bit dual DAC output 2 (Gain Selection Discriminator Threshold)		Bottom
72	**vdd_ssh**	Power	Analogue (Slow Shaper) Power Supply	**to 3.3V**	Bottom
73	**gnd_ssh**	Power	Analogue (Slow Shaper) Ground	**to GND**	Bottom
74	**vdd_fs**	Power	Analogue (Fast Shaper) Power Supply	**to 3.3V**	Bottom
75	**gnd_fs**	Power	Analogue (Fast Shaper) Ground	**to GND**	Bottom
76	**gnd_sca**	Power	Analogue (Switched Capacitor Array) Ground	**to GND**	Bottom
77	**vdd_sca**	Power	Analogue (Switched Capacitor Array) Power Supply	**to 3.3V**	Bottom
78	**vdd_tdc**	Power	Analogue (Time to Digital Convertor) Power Supply	**to 3.3V**	Bottom
79	**gnd_tdc**	Power	Analogue (Time to Digital Convertor) Ground	**to GND**	Bottom
80	**vddd_sca**	Power	SCA Digital part Power Supply	**to 3.3V**	Bottom
81	**gnd_capa_sca**	Power	Analogue SCA capacitors Ground	**to GND**	Bottom
82	**vssa**	Power	Analogue part Bulk	**to GND**	Bottom
83	**vssm**	Power	Mixed part Bulk	**to GND**	Bottom
84	**vdd_adc**	Power	Mixed (ADC Discriminator) Power Supply	**to 3.3V**	Bottom
85	**gnd_adc**	Power	Mixed (ADC Discriminator) Ground	**to GND**	Bottom
86	ib_delay_tdc	Analogue Bias	TDC delay cell bias current		Bottom
87	ibias1_tdc	Analogue Bias	TDC ramp1 amplifier bias current		Bottom
88	ibias2_tdc	Analogue Bias	TDC ramp2 amplifier bias current		Bottom
89	**gndd_delay**	Power	Digital (Discriminator Delay) Ground	**to GND**	Bottom
90	**vddd_delay**	Power	Digital (Discriminator Delay) Power Supply	**to 3.3V**	Bottom
91	**vdd_gs**	Power	Mixed (Gain Selection) Power Supply	**to 3.3V**	Bottom
92	**gnd_gs**	Power	Mixed (Gain Selection) Ground	**to GND**	Bottom
93	ib_delay_channel	Analogue Bias	Channel trigger delay cell bias current		Bottom
94	ib_delay_rst	Analogue Bias	SCA "Reset" Signal delay cell bias current		Bottom
95	ib_delay_valid_hold	Analogue Bias	SCA "Valid Hold" delay cell bias current		Bottom
96	**gnda_delay**	Power	Analogue (Discriminator Delay) Ground	**to GND**	Bottom

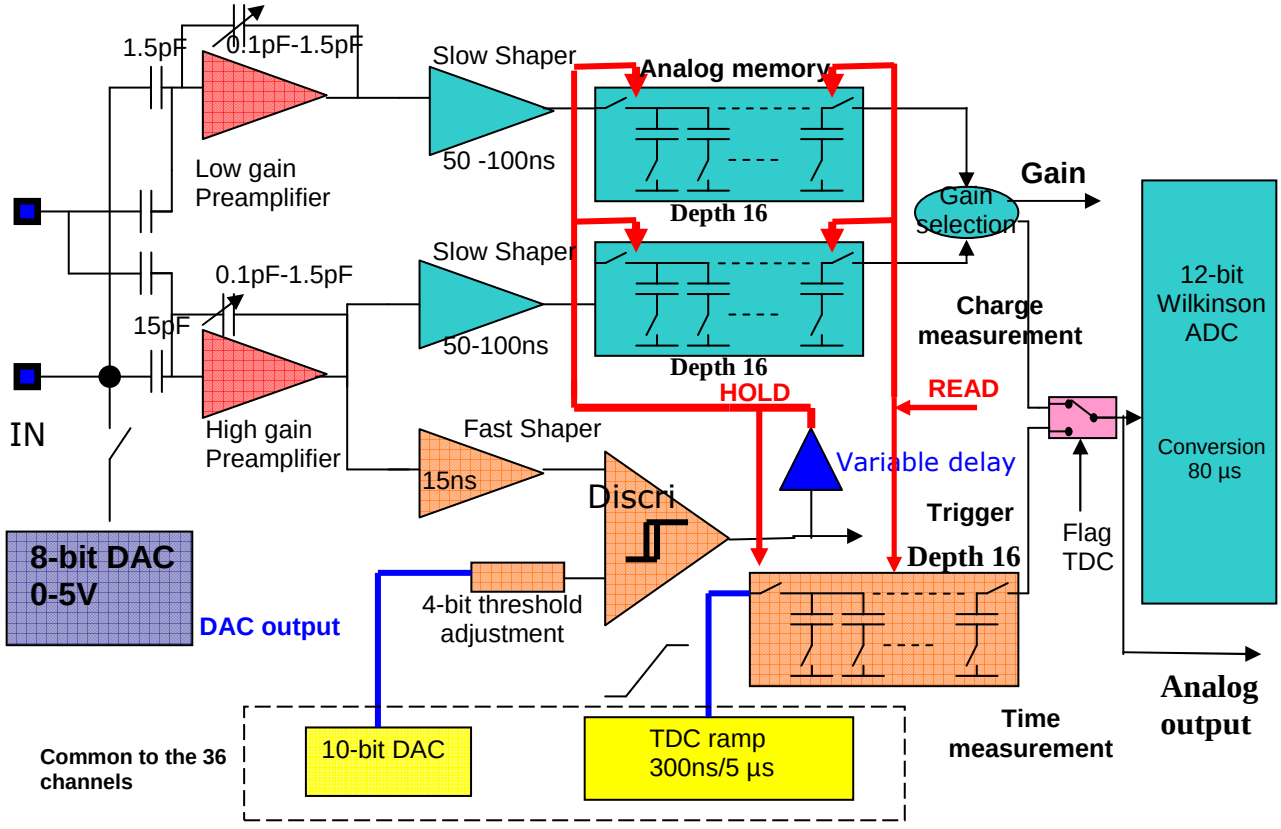
97	**vdda_delay**	Power	Analogue (Discriminator Delay) Power Supply	**to 3.3V**	Bottom
98	**vssm**	Power	Mixed part Bulk	**to GND**	Bottom
99	**vssd**	Power	Digital part Bulk	**to GND**	Bottom
100	ib_otaq	Analogue Bias	Analogue outputs OTA bias		Bottom
101	analog_output	Analogue Output	SCA Analogue Output		Bottom
102	analog_probe_output	Analogue Output	Analogue Probe Output		Bottom
103	hold_ext	Digital Input	External channel trigger signal	Active ↑	Bottom
104	srout_read	Digital Output	Read Register Output		Bottom
105	resetb_delay	Digital Input	Delay cells reset signal	Active L	Bottom
106	resetb_read	Digital Input	Read Register Reset	Active L	Bottom
107	clk_read	Digital Input	Read Register Clock		Bottom
108	srin_read	Digital Input	Read Register Input		Bottom
109	**vddd2**	Power	Digital (Digital ASIC) Power Supply	**to 3.3V**	Bottom
110	**vddd1**	Power	Digital (LVDS receivers & digital glue) Power Supply	**to 3.3V**	Bottom
111	**vssd**	Power	Digital part Bulk	**to GND**	Bottom Right
112	***NC***				
113	digital_probe2	Digital Output	Digital Probe 2 Output		Right
114	digital_probe1	Digital Output	Digital Probe 1 Output		Right
115	pwr_on_sca	Digital Input	SCA Power Pulsing Control	Active H	Right
116	trig_ext	Digital Input	External forced OR36 signal	Active ↑	Right
117	pwr_on_dac	Digital Input	DAC Power Pulsing Control	Active H	Right
118	pwr_on_adc	Digital Input	ADC Power Pulsing Control	Active H	Right
119	pwr_on_a	Digital Input	Analogue Part Power Pulsing Control	Active H	Right
120	pwr_on_d	Digital Input	Digital Power Pulsing Control	Active H	Right
121	ib_rec	Analogue Bias	LVDS receiver bias current		Right
122	StartAcq	Digital Input	Start & maintain acquisition on analogue memory	Active H	Right
123	Val_Evt_p	Digital (LVDS) Input	v_dac_discri	Active L	Right
124	Val_Evt_n				Right
125	Raz_Chn_p	Digital (LVDS) Input	Erase active Analogue Column.	Active H	Right
126	Raz_Chn_n				Right
127	CK_5M_p	Digital (LVDS) Input	Slow Clock (Acquisition = 5MHz , ReadOut = 1MHz)		Right
128	CK_5M_n				Right
129	CK_40M_p	Digital (LVDS) Input	40MHz Clock		Right
130	CK_40M_n				Right
131	**vssd**	Power	Digital part Bulk	**to GND**	Right
132	resetb	Digital Input	Reset ASIC digital part	Active L	Right
133	rtn	Power	Open Collector Ground	**to GND**	Right
134	Dout1b	Digital OC Output	Data Serial Output	Open Collector	Right
135	Dout2b	Digital OC Output	Data Serial Output	Open Collector	Right
136	TransmitOn1b	Digital OC Output	Active data readout	Open Collector / Active H	Right
137	TransmitOn2b	Digital OC Output	Active data readout	Open Collector / Active H	Right
138	ChipSatb	Digital OC Output	Analogue memory full / Acq stopped by DAQ	Open Collector / Active H	Right
139	start_convb	Digital Input	Start conversion signal	Active L	Right
140	start_readout1	Digital Input	Digital RAM start reading signal	Active H	Right

141	start_readout2	Digital Input	Digital RAM start reading signal	Active H	Right
142	end_readout1	Digital Output	Digital RAM end reading signal	Active H	Right
143	end_readout2	Digital Output	Digital RAM end reading signal	Active H	Right
144	select	Digital Input	Select Slow Control Register (1) or Probe Register (0)		Right
145	sr_rstb	Digital Input	Selected Register Reset	Active L	Right
146	sr_ck	Digital Input	Selected Register Clock	Active ↑	Right
147	sr_in	Digital Input	Selected Register Input		Right
148	sr_out	Digital Output	Selected Register Output		Right
149	sr_load	Digital Input	Slow Control Register Load Signal	Active ↑	Right
150	***NC***				
151	**vssd**	Power	Digital part Bulk	**to GND**	Top Right
152	holdb_backup	Digital Input	Backup Analogue Memory Hold Signal	Active L	Top
153	resetb_pa	Digital Input	Charge PreAmp Reset Signal	Active L	Top
154	**gndd1**	Power	Digital (LVDS receivers & Digital glue) Ground	**to GND**	Top
155	**vddd2**	Power	Digital (Digital ASIC) Power Supply	**to 3.3V**	Top
156	flag_tdc_ext	Digital Input	External charge or time SCA select command		Top
157	start_rampb_adc_ext	Digital Input	External ADC Ramp Start Signal	Active L	Top
158	start_ramp_tdc_ext	Digital Input	External TDC Ramp1 to Ramp2 Switch Signal	Active H	Top
159	**gnd_sc**	Power	Digital (Slow Control Register) Ground	**to GND**	Top
160	**vdd_sc**	Power	Digital (Slow Control Register) Power Supply	**to 3.3V**	Top
161	**vssd**	Power	Digital part Bulk	**to GND**	Top
162	**vssm**	Power	Mixed part Bulk	**to GND**	Top
163	ib_adc_discri	Analogue Bias	ADC discriminator bias current		Top
164	ibo_gs	Analogue Bias	Gain Selector output stage bias current		Top
165	ibm_gs	Analogue Bias	Gain Selector middle stage bias current		Top
166	ibi_gs	Analogue Bias	Gain Selector input stage bias current		Top
167	ib_dac_4bits_fine	Analogue Bias	4-bit DAC fine adjustement bias current		Top
168	ib_dac_4bits_coarse	Analogue Bias	4-bit DAC coarse adjustement bias current		Top
169	ibomin_discri	Analogue Bias	Discriminator output stage minimum bias current		Top
170	ibo_discri	Analogue Bias	Discriminator output stage bias current		Top
171	ibm_discri	Analogue Bias	Discriminator middle stage bias current		Top
172	ibi_discri	Analogue Bias	Discriminator input stage bias current		Top
173	in_adc_ext	Analogue Input	ADC External input		Top
174	**gnd_discri**	Power	Analogue (Discriminator) Ground	**to GND**	Top
175	**gndd_mask**	Power	Digital (Mask & Discriminator) Ground	**to GND**	Top
176	**vddd_mask**	Power	Digital (Mask & Discriminator) Power Supply	**to 3.3V**	Top
177	**vdd_discri**	Power	Analogue (Discriminator) Power Supply	**to 3.3V**	Top
178	**vssm**	Power	Mixed part Bulk	**to GND**	Top
179	**vssa**	Power	Analogue part Bulk	**to GND**	Top
180	out_ramp_adc	Analogue Output	ADC ramp output		Top
181	ibias_adc	Analogue Bias	ADC ramp amplifier bias current		Top
182	**vdd_ramp_adc**	Power	Analogue (ADC Ramp) Power Supply	**to 3.3V**	Top
183	**gnd_ramp_adc**	Power	Analogue (ADC Ramp) Ground	**to GND**	Top
184	ib_sca	Analogue Bias	SCA bias current		Top
185	ibo_fs	Analogue Bias	Fast Shaper output stage bias		Top
186	ibi_fs	Analogue Bias	Fast Shaper input stage bias		Top
187	ib_suiv_fs	Analogue Bias	Fast Shaper follower bias current		Top
188	ibo_ssh_hg	Analogue Bias	High Gain Slow Shaper output bias current		Top
189	ibi_ssh_hg	Analogue Bias	High Gain Slow Shaper input bias current		Top
190	ib_suiv_rc_hg	Analogue Bias	High Gain Slow Shaper follower bias current		Top
191	ibo_ssh_lg	Analogue Bias	Low Gain Slow Shaper output bias current		Top

192	ibi_ssh_lg	Analogue Bias	Low Gain Slow Shaper input bias current		Top
193	ib_suiv_rc_lg	Analogue Bias	Low Gain Slow Shaper follower bias current		Top
194	ibi_pa_lg	Analogue Bias	Low Gain PreAmps input stage bias current		Top
195	ibo_pa_lg	Analogue Bias	Low Gain PreAmps output stage bias current		Top
196	ibm_pa_lg	Analogue Bias	Low Gain PreAmps middle stage bias current		Top
197	**gnd_capa_ssh**	Power	Analogue (Slow Shaper Capacitor) Ground	**to GND**	Top
198	ibi_pa_hg	Analogue Bias	High Gain PreAmps input stage bias current		Top
199	ibo_pa_hg	Analogue Bias	High Gain PreAmps output stage bias current		Top
200	ibm_pa_hg	Analogue Bias	High Gain PreAmps middle stage bias current		Top
201	ibmin_pa	Analogue Bias	Pre Amps input & output stage minimum bias current		Top
202	**vdda_pa**	Power	Analogue (PreAmplifier) Power Supply	**to 3.3V**	Top
203	**gnd_pa**	Power	Analogue (PreAmplifier) Ground	**to GND**	Top
204	**vdd_pa**	Power	Analogue (PreAmplifier) Power Supply	**to 3.3V**	Top
205	in_calib	Analogue Input	Calibration input		Top
206	**vdd_ota_dac_5V**	Power	Analogue (8-bit DAC OTA) Power Supply	**to 5V**	Top
207	sw_c15p	Digital Input	Short high gain PA input coupling capacitor Signal	Active H (Caution: 5 Volts)	Top
208	**vdd_dac_5V**	Power	Analogue (8-bit Digital to Analogue Convertor) Power Supply	**to 5V**	Top

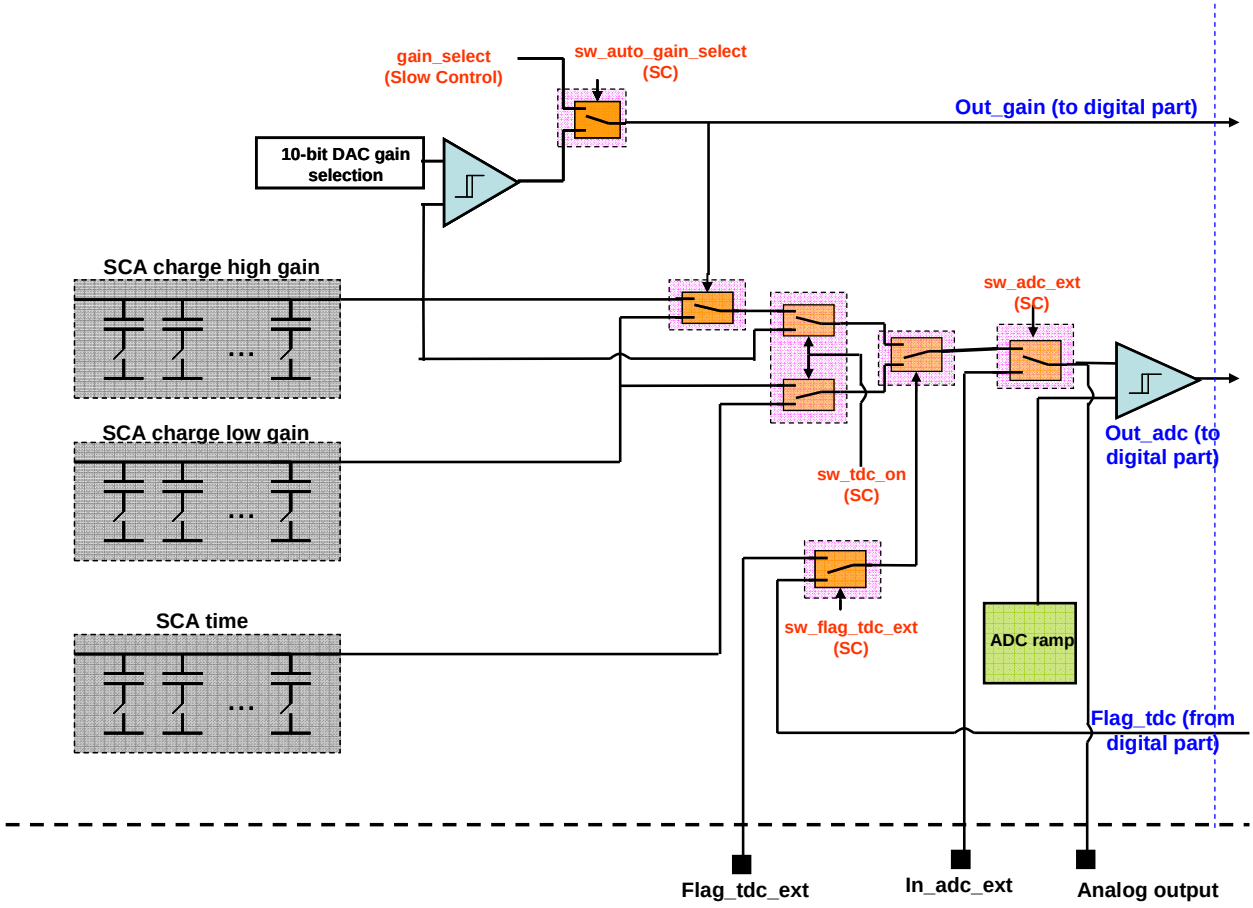
4 Spiroc Analog Part

The analogue core is composed of 36 channels embedding an input DAC for SiPM high voltage adjustment on 5V to tune gain channel by channel. Two preamplifiers allow the requested dynamic range and are followed by a trigger line made of a fast shaper and a discriminator. The charge measurement line is made of two variable slow shapers and two 16-depth SCAs. The block scheme of a channel is shown on the next figure.

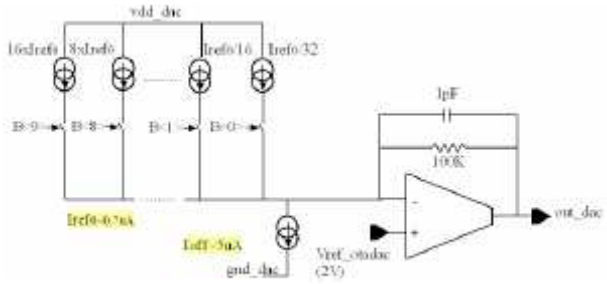


5 Embedded ADC

The ADC used in SPIROC is based on a Wilkinson structure. Its resolution is 12 bits. As the default accuracy of 12 bits is not always needed, the number of bits of the counter can be adjusted from 8 to 12 bits.
This type of ADC is particularly adapted to this application which needs a common analogue voltage ramp for the 36 channels and one discriminator for each channel. The ADC is able to convert 36 analogue values (charge or time) in one run (about 100 µs at 40 MHz). If the SCA is full, 32 runs are needed (16 for charges and 16 for times).



6 Embedded DAC



Reference voltages all referred to an integrated bandgap.

I_{ref0} and I_{off0} can be changed thanks to an external resistor and are used to adjust the dynamic range of the dac.

- All Bits OFF => out_dac= V_{ref_dac}+100K*I_{off}=2V+500mV= 2.5V
- All Bits ON => out_dac= 2.5-(32*I_{ref0})*100k=260mV

Two integrated 10-bit DAC to deliver threshold voltages of the 2 discriminators (trigger discriminator and gain selection discriminator).

7 Spiroc Digital Part

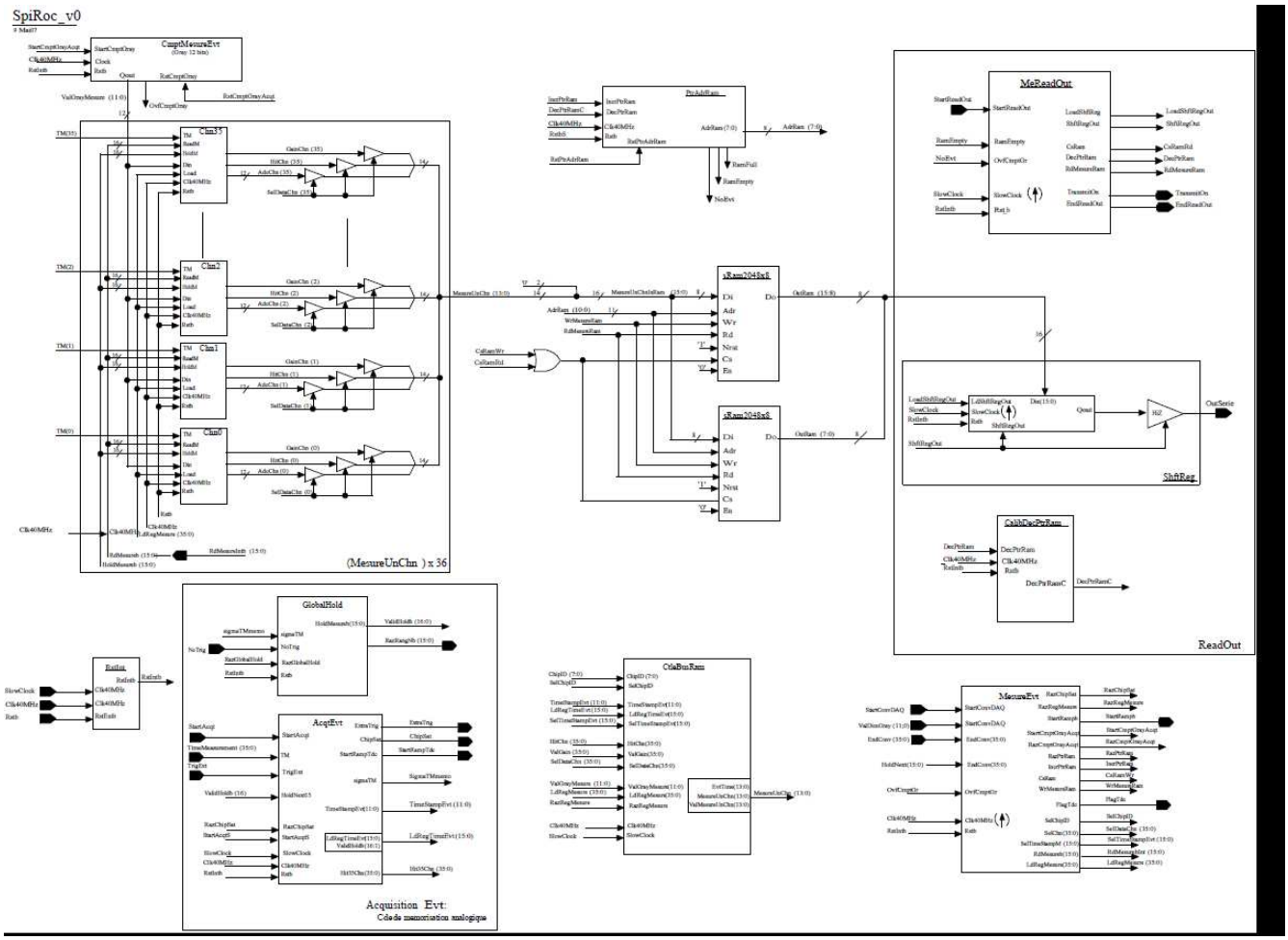
The system on chip has been designed to match the ILC beam structure. The complete readout process needs at least 3 different steps:

*a. **acquisition phase***

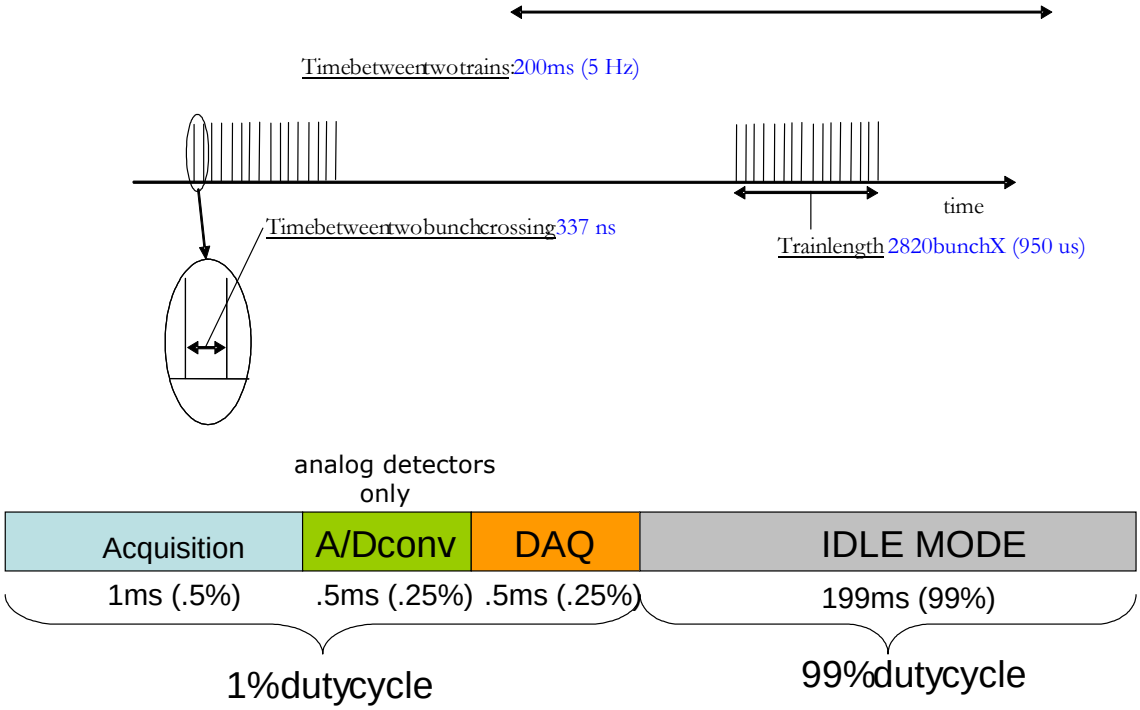
*b. **conversion phase***

*c. **readout phase***

*d. **and possibly idle phase***



The digital part of ***SPIROC*** is built around 3 modules which represent the different phases of the ILC working shown in the next figure.
The acquisition module permits to capture data during the bunch crossing train. Measure and Read-Out ones are activated during inter bunch crossing to convert and save data in the memory in a first step and to read out data to the external concentrator with a reduced numbers of lines.

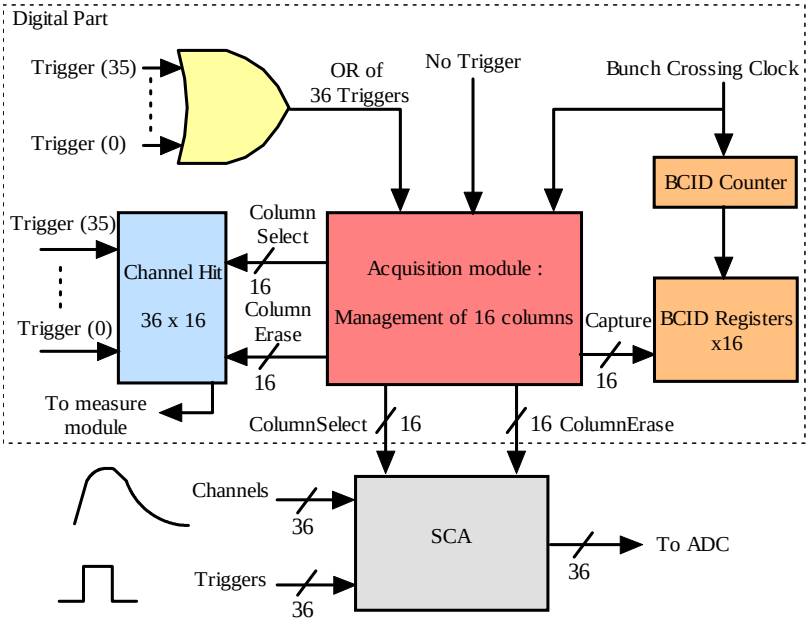


Digital part phases versus time.

Acquisition	A/D conversion	DAQ
When an event occurs : • Charge is stored in analogue memory • Time is stored in digital (coarse) and analogue (fine) memory • Trigger is automatically rearmed at next coarse time flag (bunch crossing ID) Depth of memory is 16	The data (charge and time) stored in the analogue memory are sequentially converted into digital data and stored in a SRAM.	The events stored in the RAM are readout through a serial link when the chip gets the token allowing the data transmission. When the transmission is done, the token is transferred to the next chip. 256 chips can be read out through one serial link

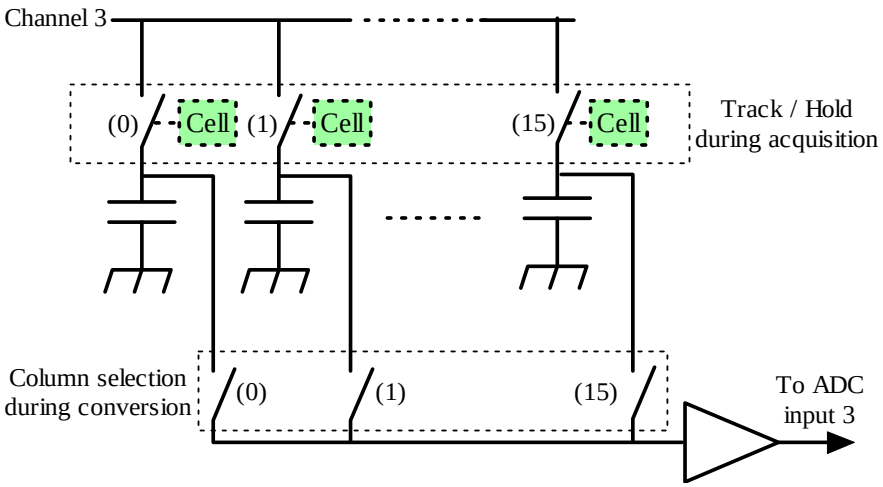
a. Acquisition module

This module given in the next figure allows to select the right column where analogue value should be stored

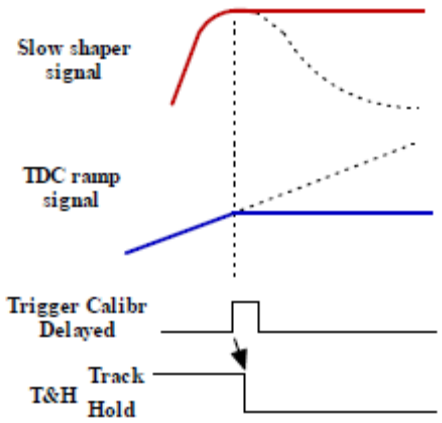


Detailed block diagram of acquisition module.

During idle mode, a capture window is open at the first empty column. When a trigger occurs, data can be captured in this column by means of a “Track and Hold Cell” inside the SCA..
When next bunch crossing occurs, it closes the capture window and selects the next column.



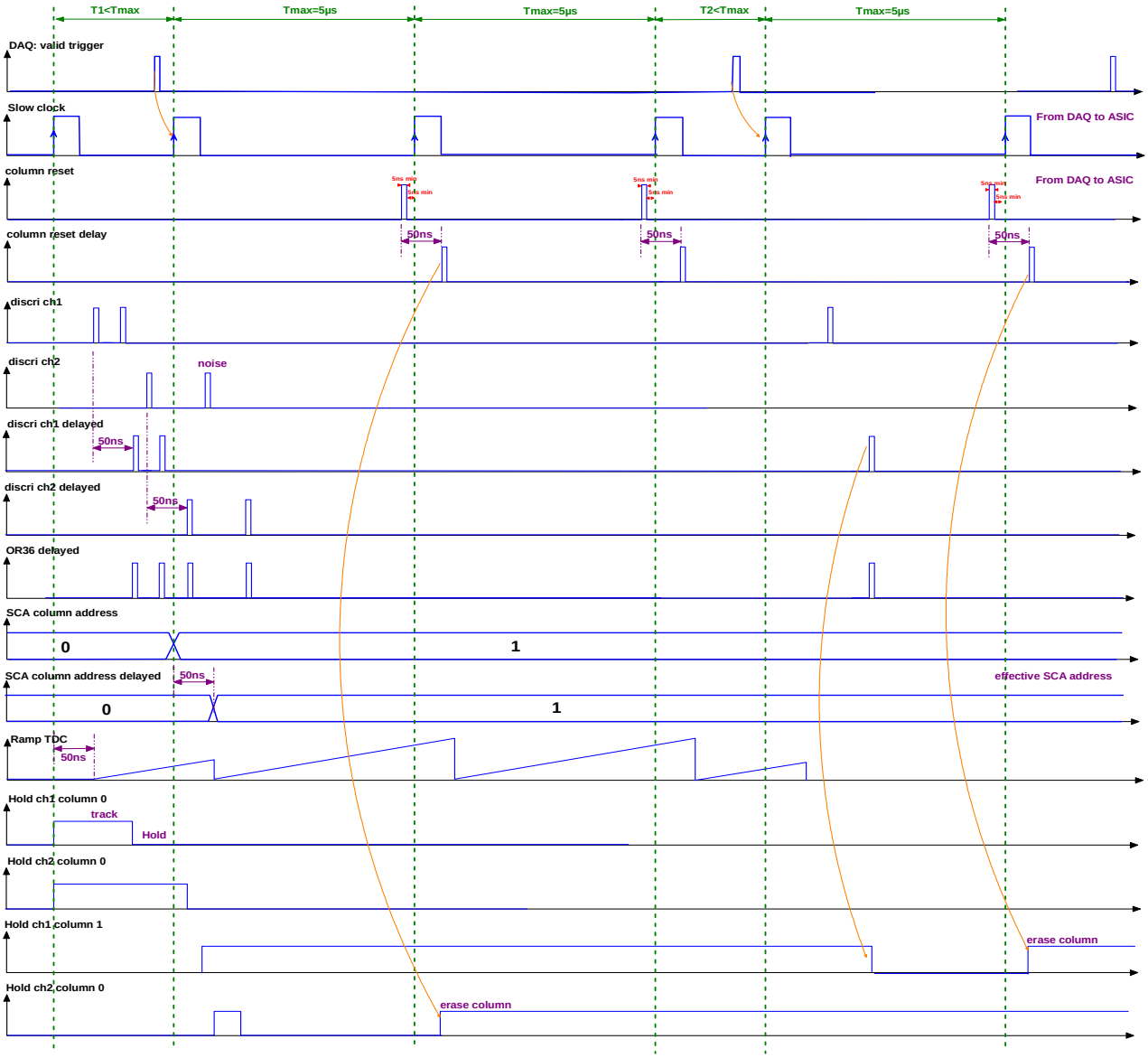
SCA for one channel with track and hold Cell.



Operation of T&H cell

An external signal is available to erase the present column named “No Trigger”. It can be used to erase the column if a trigger was due to noise.

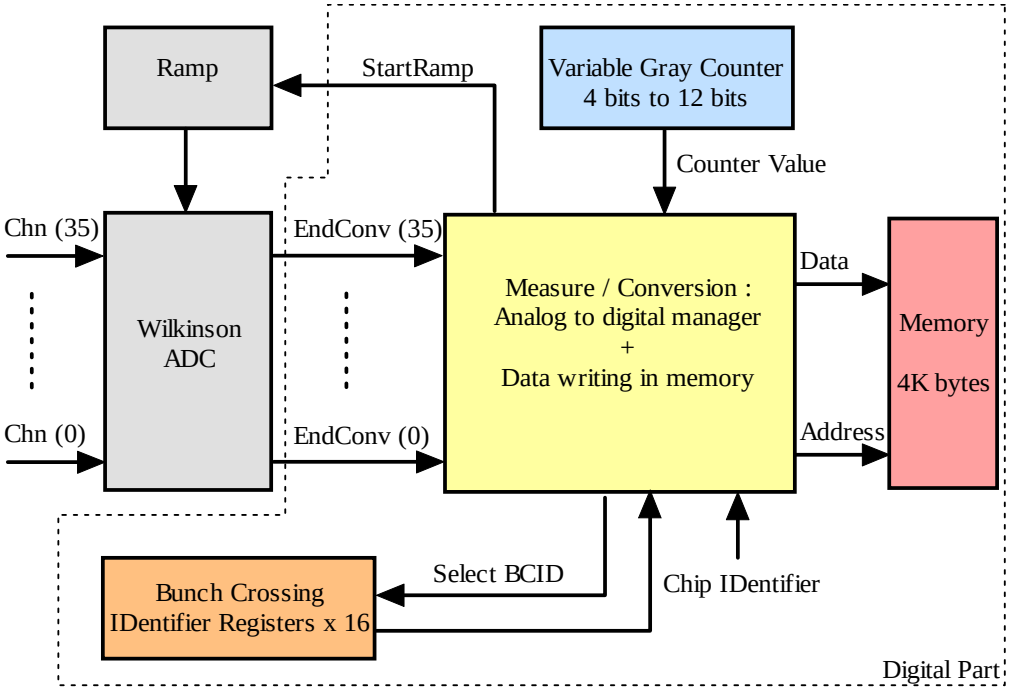
The Acquisition part has been developed with asynchronous cells to meet time and low consumption requirements. Besides, this allows no coupling between digital clock and analogue part during acquisition.



b. Measure module

The main purpose of this module is to convert analogue value stored in the SCA in digital ones.

The next figure represents the detailed block diagram of the measure and conversion module.

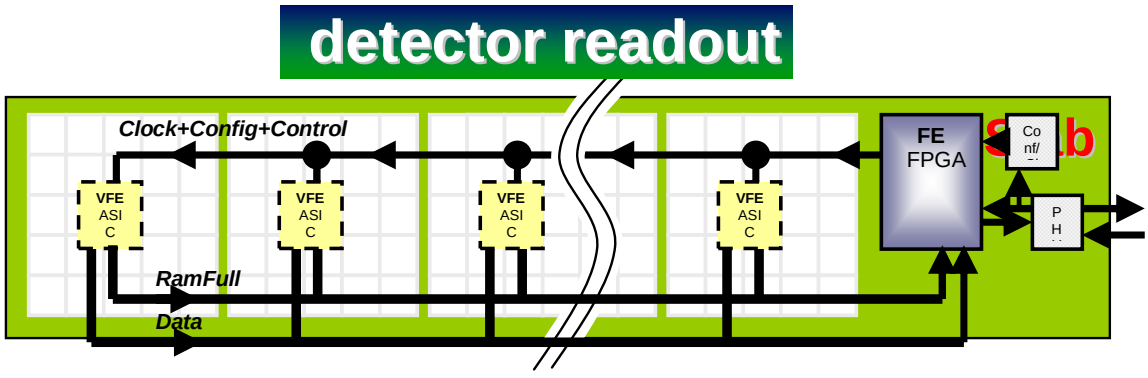


36 charges and 36 times stored in SCA must be converted for each column. That means 32 ADC conversions (16 charges and 16 times). When conversion is over, data are stored in the memory in order to start a new conversion.
As the default accuracy of 12 bits is not always needed for conversion, the number of bits of this counter can be adjusted from 4 to 12 bits.

c. Readout module

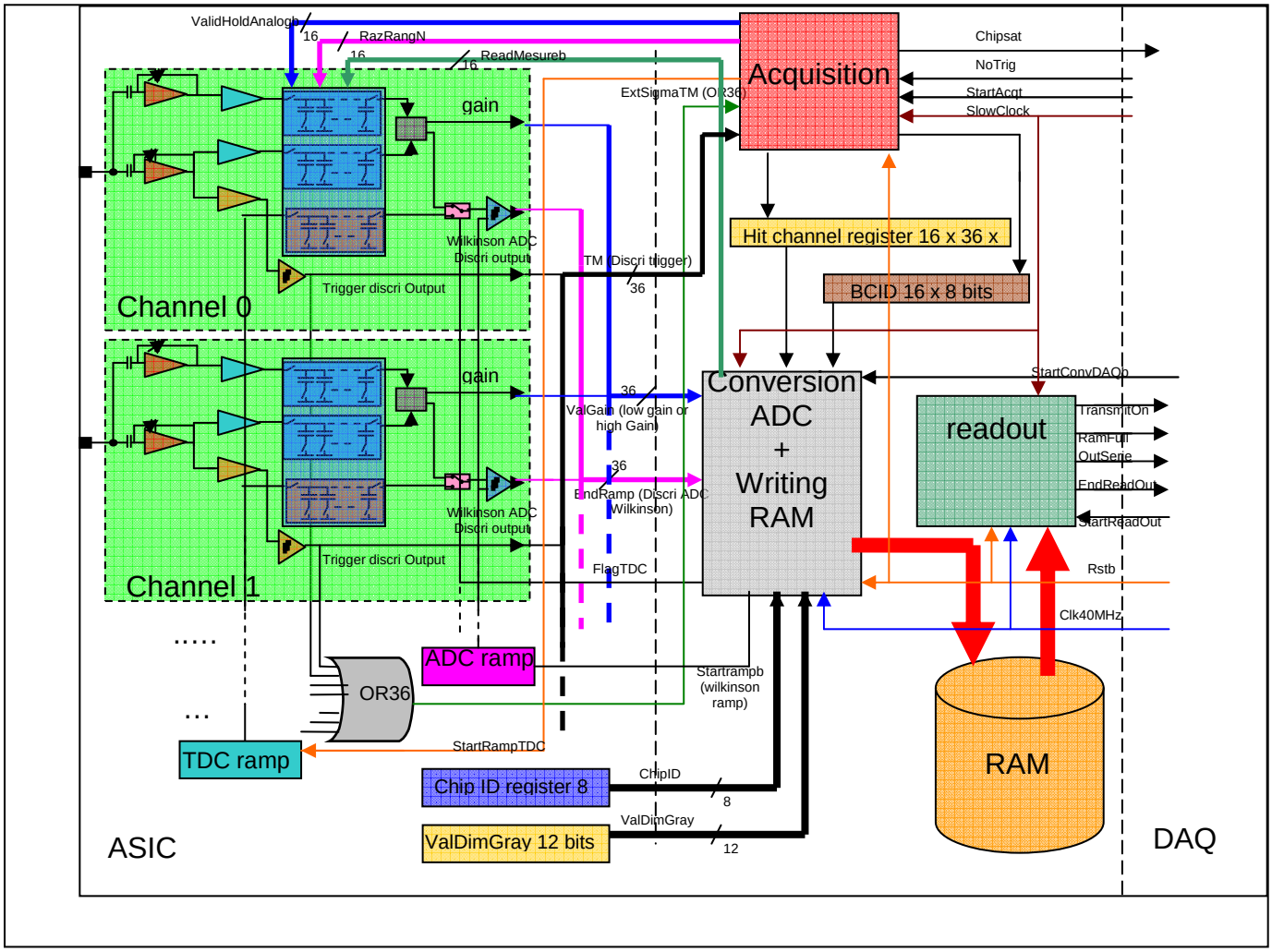
The Readout module permits to empty the memory where all data are stored. To minimize lines between board and external concentrator, data are transferred on a single line..

In the worst case, about 20K bits of data are transferred to the concentrator with a clock of 5 MHz. As the data line to the concentrator is common to all the daisy-chained ASICs, one ASIC can take the data line for a maximum of 4 ms.



d. Idle mode

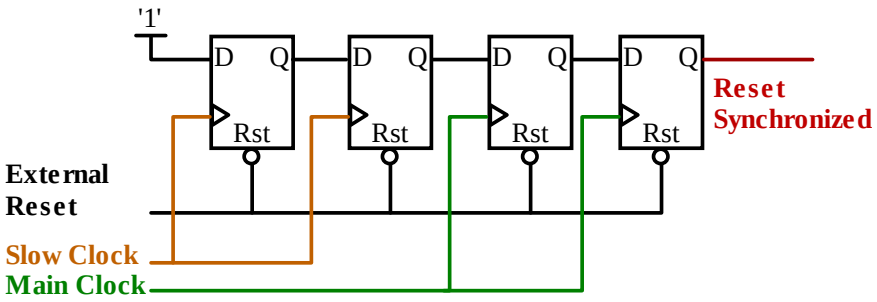
When all these operations are done, the chip goes *to idle mode* to save power. In the ILC beam structure 99 % of power can be saved.


ValidHoldAnalogb
16
RazRangN
16
ReadMesureb
16
Acquisition
Chipsat
NoTrig
StartAcqt
SlowClock
ExtSigmaTM (OR36)
gain
Wilkinson ADC
Discri output
Trigger discri Output
Channel 0
TM (Discri trigger)
36
Hit channel register 16 x 36 x
BCID 16 x 8 bits
gain
Wilkinson ADC
Discri output
Trigger discri Output
Channel 1
36
ValGain (low gain or high Gain)
36
EndRamp (Discri ADC Wilkinson)
Conversion ADC + Writing RAM
StartConvDAQb
readout
TransmitOn
RamFull
OutSerie
EndReadOut
StartReadOut
FlagTDC
Rstb
Clk40MHz
.....
...
ADC ramp
OR36
Startrampb (wilkinson ramp)
TDC ramp
StartRampTDC
Chip ID register 8
ChipID
8
ValDimGray
ValDimGray 12 bits
12
RAM
ASIC
DAQ

8 Master reset of digital part

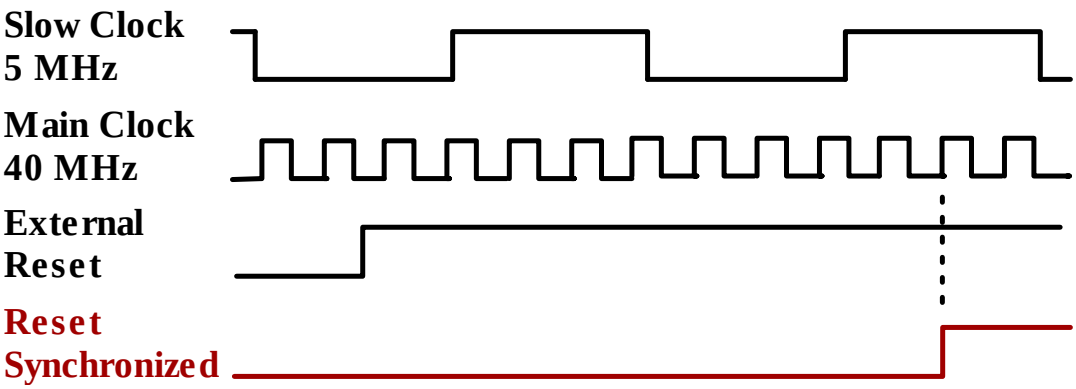
General Reset of the digital part is active low and synchronous with rising edge of Main Clock. It is active for the 2 clock domains (Slow Clock and Main Clock).

To prevent timing violation when Reset is released, it must be synchronised with the 2 clock domains. Reset logic is given below.



Master Reset logic

This circuit inserts latency when Reset is released (start of digital part). Latency is equal to 2 periods of Slow Clock + 2 periods of Main Clock (450 ns with 5 MHz and 40 MHz). This is shown in the next Figure.



Release of master reset

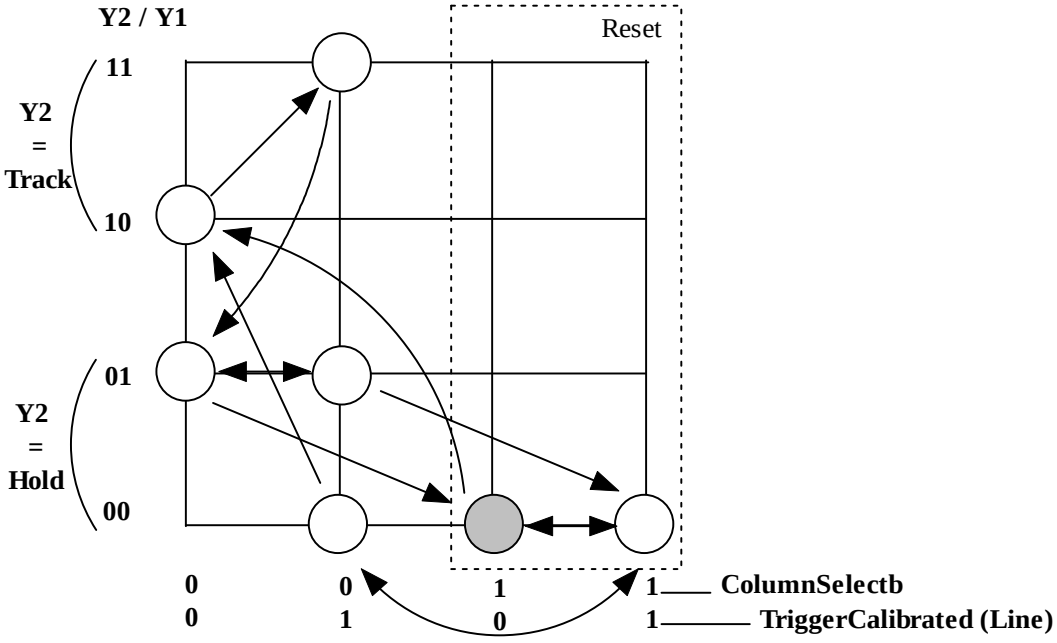
9 The Track & Hold digital cell

T&H cell allows to lock the capacitor value only when a calibrated trigger occurs within the selected column.

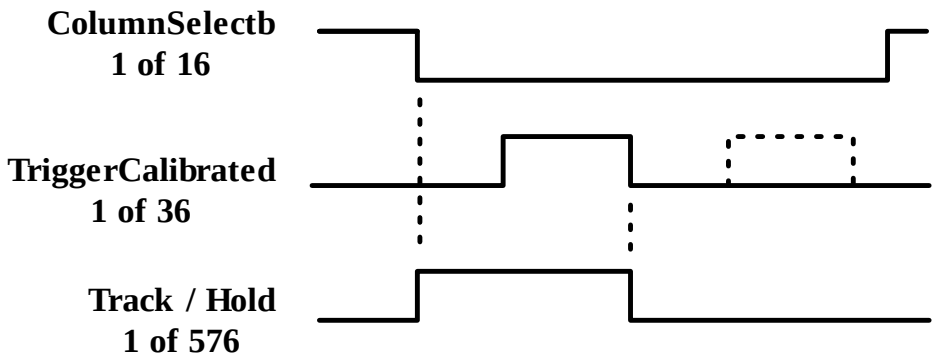
The hold of the capacitor is made when the trigger disappears.

The selected column is given by the acquisition module and the channel trigger gives the line.

The operation of the asynchronous cell is described below.



This operation above is the same as the chronogram in the next figure.



Chronogram of T&H cell

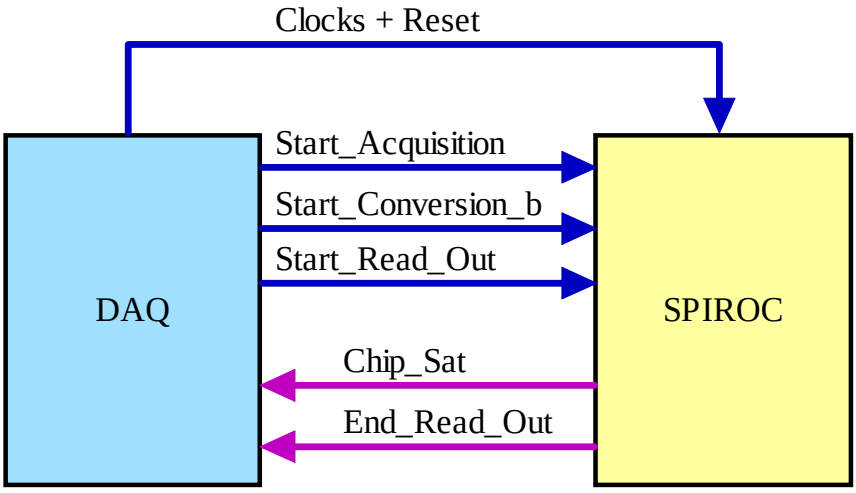
10 “Backup” track and hold

A “ backup” track and hold is included in the chip. It consists is a basic 1-deep analog memory. This track and hold may be activated by slow control (sw_sca_backup).

The signal “Hold_backupb” is used to store the signal. (“track” Hold_backupb=1 and “hold” Hold_backupb=0)

11 Link between DAQ and SPIROC

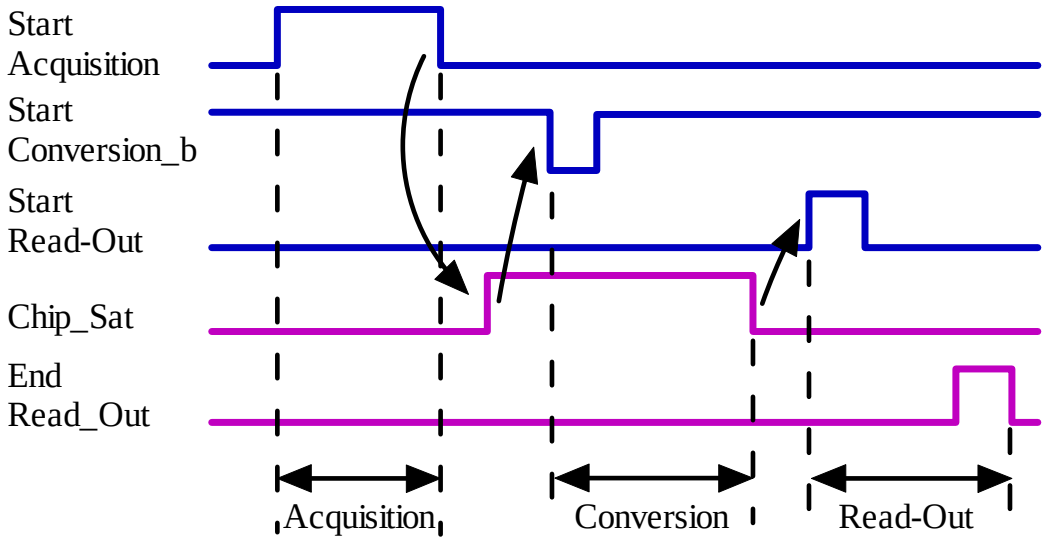
The 3 modules of the digitals parts are activated by signals from the DAQ. These signals are given below.



Main Signals between DAQ and SPIROC

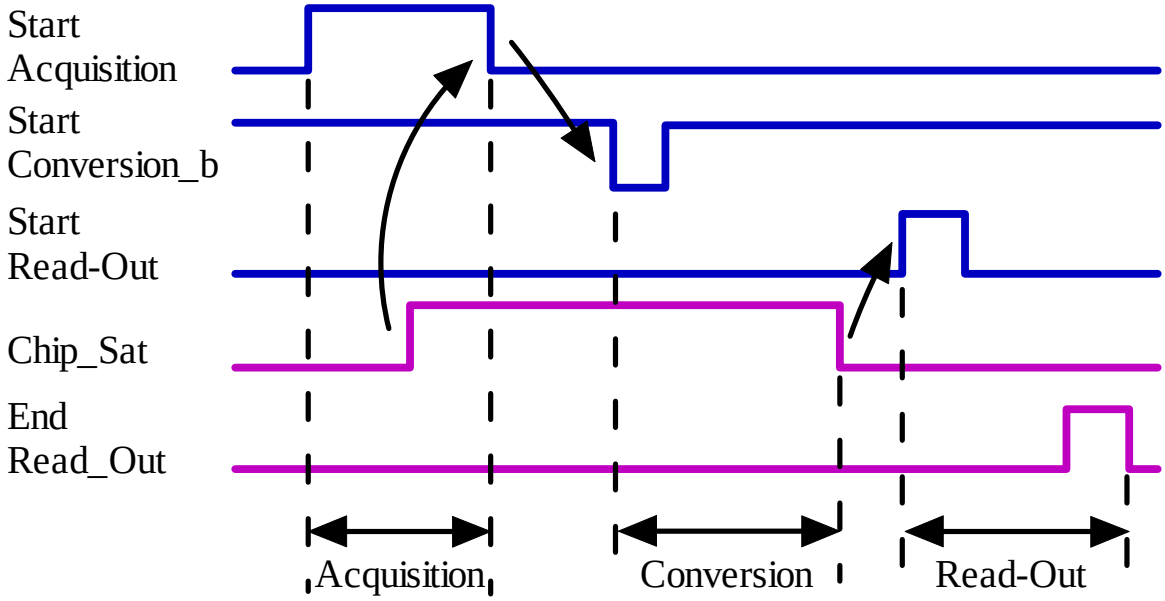
The rising edge of the Start_Acquisition signal is the beginning of the acquisition phase for the digital part. The end of the acquisition is given by the falling edge of this signal.

The chronogram of the sequence is given below In this case, the DAQ stops the acquisition even if the chip is not full (end of bunch crossing for example). The falling edge of Chip_Sat represents the end of the conversion.



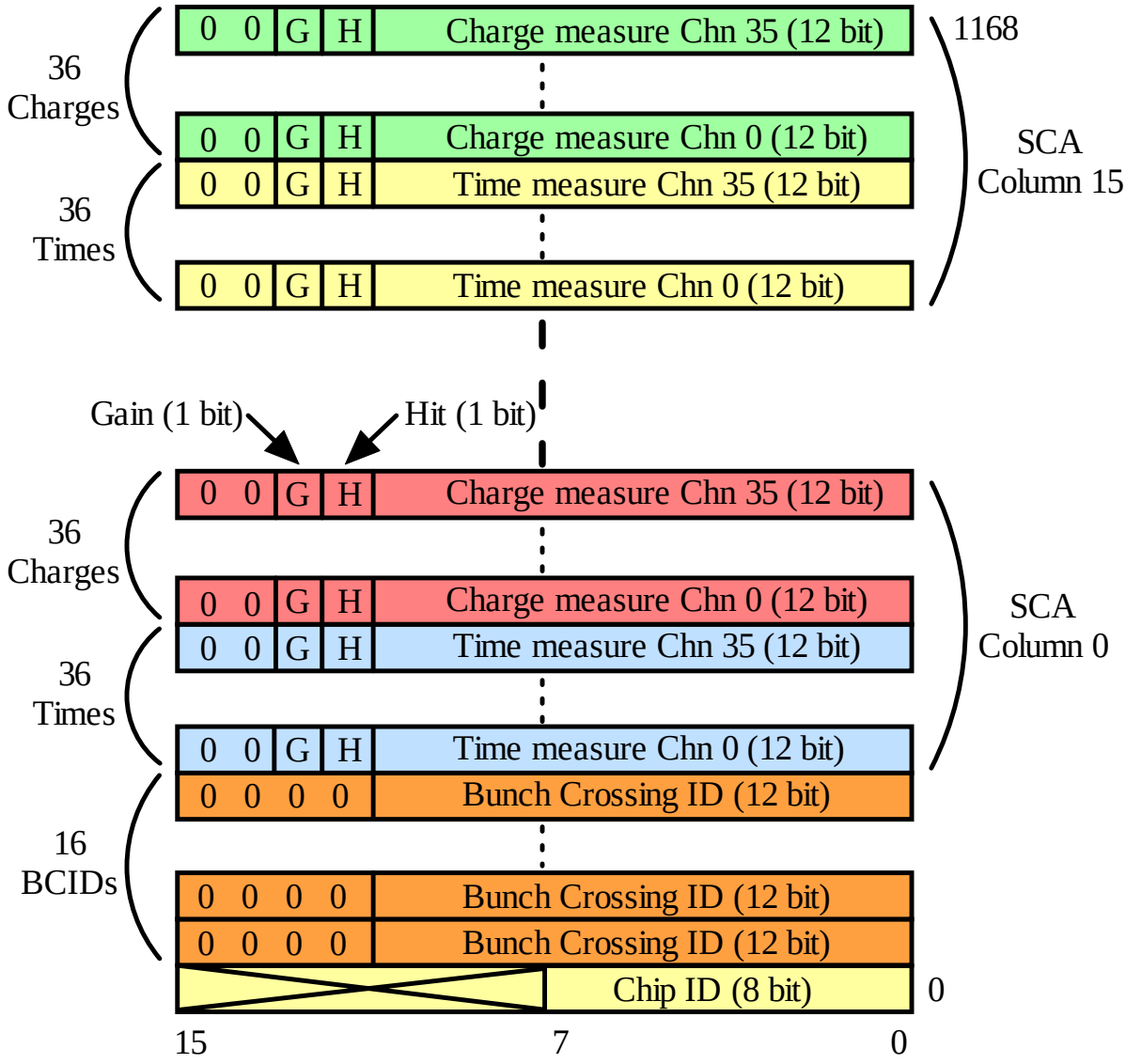
Chronogram with chip not full

Another case is possible when the chip is full during the acquisition phase. This is shown on next figure



Chronogram with chip full

12 Spiroc RAM mapping



13 Slow control and probe registers

2 shift registers are integrated and coupled: a probe register to select and watch different points in the chip and a Slow Control register to load serially the Slow control parameters.

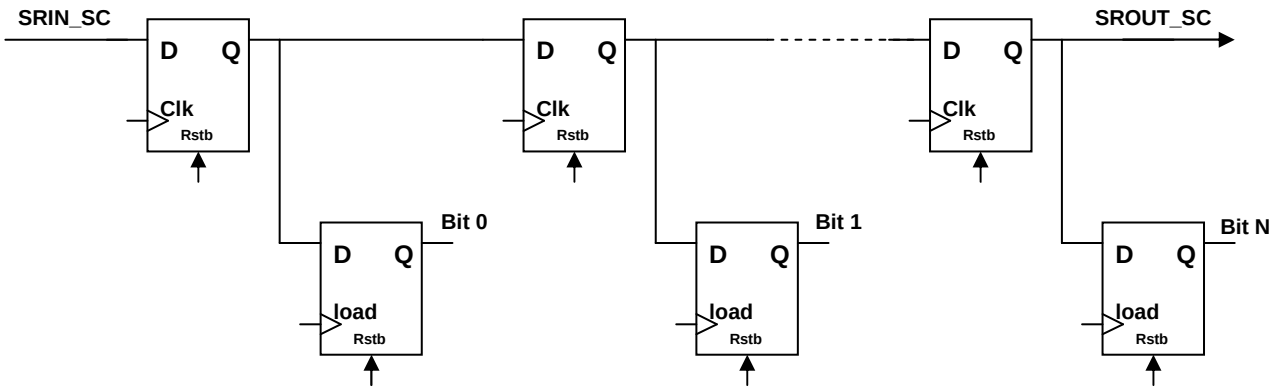
The probe register allows seeing different signals in the chip:

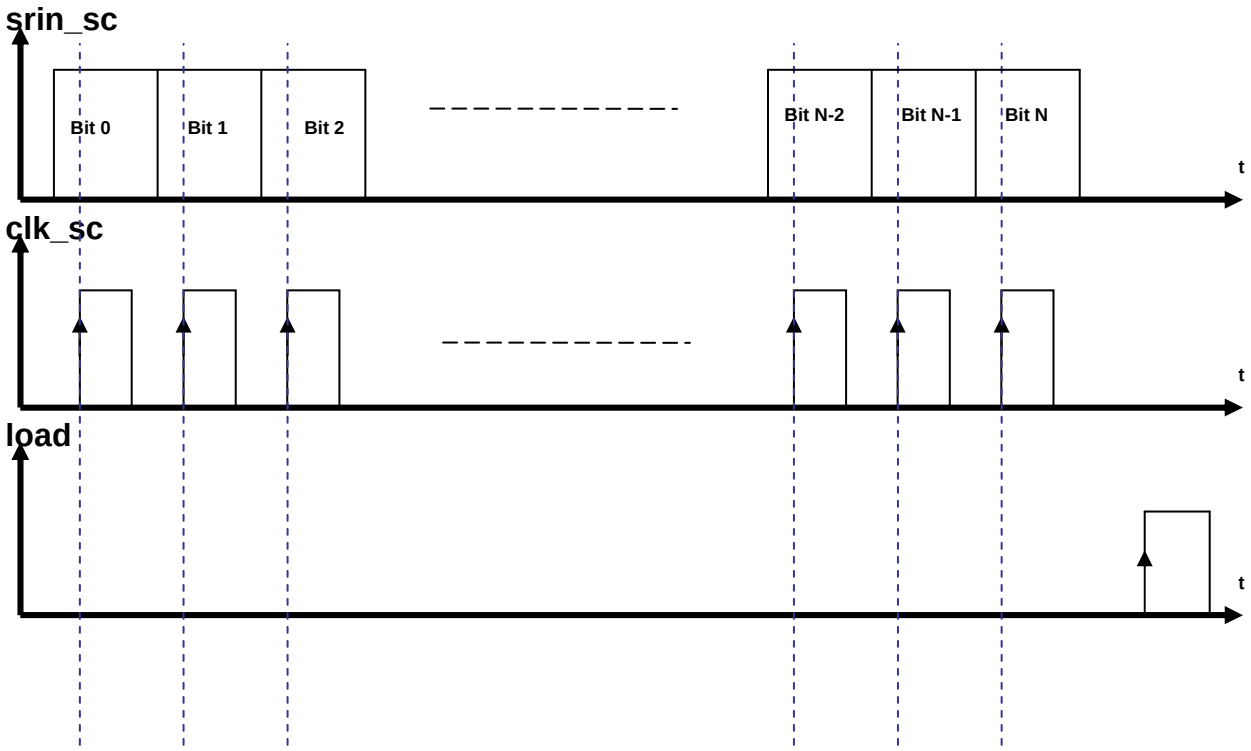
- 2 digital probe (“probe 1” and “probe 2”) for digital signals
- 1 analog probe (“analog probe”) for intermediate analog signals

The data input (sr_in), clock (sr_clk) and reset (sr_rstb) of these 2 registers are sent to the Slow Control or probe register inputs depending of the level of the external select signal. Unfortunatly, the reset of both registers is active low (rstb) and thus the Slow Ccontrol register is reseted when the select command is swithed from vdd to 0. It means that this **select command has to be set to vdd** and that the **Read register can’t be used in SPIROC2**.

Slow control register

- One slow control register to load serially the 712 slow controls parameters:



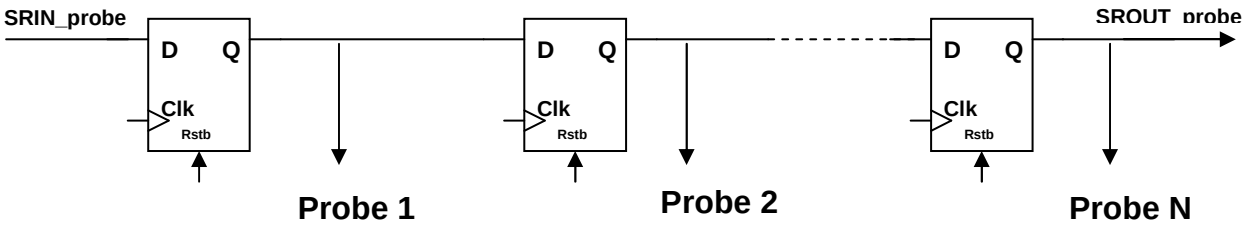


Labview Register Name	bits	Register description	Subadd	ASIC Register Name
EC : Trig Ext (OR36)	1	Enable external trig_ext (OR36)	0	sw_trig_ext
EC : Flag TDC Ext	1	Enable external flag_tdc_ext signal	1	sw_flag_tdc_ext
EC : Start Ramp ADC Ext	1	Enable external startb_ramp_adc signal	2	sw_ramp_adc_ext
EC : Start Ramp TDC Ext	1	Enable external start_ramp_tdc signal	3	sw_ramp_tdc_ext
GC : ADC Gray (12 bits)	12	ADC Gray counter resolution register (from LSB to MSB)	4	adc_res_register (gray counter) (12 bits)
GC : Chip ID (8 bits)	8	Chip ID (from LSB to MSB)	16	chip_ID_register (8 bits)
NC	5		24	
GC : ADC Ramp Slope	2	ADC ramp slope (ramp slope 12, 10 or 8 bits)	29	resolution adc
PP: ADC Ramp Current Source	1	Enable adc ramp current source power pulsing	31	pwr_on_adc_ramp_current_source
PP: ADC Ramp Integrator	1	Enable adc ramp integrator power pulsing	32	pwr_on_adc_ramp_integrator
ID : Input 8-bit DAC	324	Input 8-bit DAC Data from channel 0 to 35 – (DAC0…DAC7 + DAC ON)	33	input_dac_8bits
GC : Capacitor HG PA Comp	4	High gain preamp compensation capacitances commands (0…3)	357	sw_pa_comp_hg
GC : Capacitor HG PA Fdbck	4	High gain preamp feedback capacitances commands (0…3)	361	sw_pa_cf_hgb (active high)
GC : Capacitor LG PA Fdbck	4	Low gain preamp feedback capacitances commands (3…0)	365	sw_pa_cf_lgb (active high)
GC : Capacitor LG PA Comp	4	Low gain preamp compensation capacitances commands (3…0)	369	sw_pa_comp_lg
PP: Preamplifier	1	Enable preamp power pulsing	373	pwr_on_pa
PA : PreAmp & Ctest config	72	Disable charge preamp + Enable test capacitor (from channel 0 to 35)	374	sw_pa_enable+ sw_pa_ctest_enable

PP: **Low Gain SSh Follower**	1	Enable low gain slow shaper follower power pulsing	446	pwr_on_suiv_ssh_lg
GC : **Time Constant LG Shaper**	3	Low gain shaper time constant commands (2…0)	447	sw_rc_lg (active low)
PP: **Low Gain Slow Shaper**	1	Enable low gain slow shaper power pulsing	450	pwr_on_ssh_lg
PP: **High Gain SSh Follower**	1	Enable high gain slow shaper follower power pulsing	451	pwr_on_suiv_ssh_hg
GC : **Time Constant HG Shaper**	3	High gain shaper time constant commands (2…0)	452	sw_rc_hg (active low)
PP: **High Gain Slow Shaper**	1	Enable high gain slow shaper power pulsing	455	pwr_on_ssh_hg
PP: **Fast Shapers Follower**	1	Enable fast shaper follower power pulsing	456	pwr_on_suiv_fs
PP: **Fast Shaper**	1	Enable fast shaper power pulsing	457	pwr_on_fs
GC : **backup SCA**	1	Enable backup SCA	458	sw_sca_backup
PP: **SCA**	1	Enable SCA power pulsing	459	pwr_on_sca
GC : **DAC 1 : Trigger**	10	10-bit DAC (LSB-MSB) discri_trigger_threshold	460	dac1
GC : **DAC 2 : Gain Sel.**	10	10-bit DAC (LSB-MSB) discri_gs_threshold	470	dac2
PP: **10-bit Dual DAC**	1	Enable 10-bit dual DAC power pulsing	480	pwr_on_dual_dac
PP: **10-bit Dual DAC OTA**	1	Enable 10-bit dual DAC OTA power pulsing	481	pwr_on_ota_dual_dac
PP: **Bandgap OTA**	1	Enable bandgap OTA power pulsing	482	pwr_on_bandgap
PP: **Delay (Start Ramp TDC)**	1	Enable Delay cell power pulsing for the signal “start_ramp_tdc”	483	pwr_on_delay_start_ramp_tdc
GC : **Delay (Start Ramp TDC)**	6	Delay for the ”start_ramp_tdc” signal (From MSB to LSB)	484	delay_start_ramp_tdc
GC : **TDC Ramp Slope**	1	TDC ramp slope (fast = 0 or slow = 1)	490	sw_ramp_slope (fast or slow)
PP: **TDC Ramp**	1	Enable TDC ramp power pulsing	491	pwr_on_tdc_ramp
PP: **ADC Discri**	1	Enable ADC discri power pulsing	492	pwr_on_discri_adc
PP: **Gain Select Discri**	1	Enable gain selection discri power pulsing	493	pwr_on_discri_gs
GC : **Auto Gain**	1	Auto gain selection	494	sw_auto_gain_select
GC : **Gain Select**	1	Forces the gain value when auto gain selection is OFF	495	gain_select (High Gain or Low Gain)
EC : **ADC Ext Input**	1	External ADC signal input	496	sw_in_adc_ext
GC : **Switch TDC On**	1	Switch for time signal charge signal readout / high gain and low gain charge	497	sw_tdc_on
DM : **Discriminator Mask**	36	Allows to Mask Discriminator (channel 35 to 0)	498	mask_discri
EC : **Hold Ext**	1	Enable external hold_ext signal	534	cmd_hold_ext
PP: **Discri Delay**	1	Enable discri delay power pulsing	535	pwr_on_delay_discri
GC : **Delay (Trigger)**	6	Delay for the ”trigger” signals (From MSB to LSB)	536	delay_discri
DD : **Discri 4-bit DAC Threshold Adjust**	144	Discri 4-bit DAC – from channel 35 to 0 (from LSB to MSB)	542	dac_4_bit_theshold_adjust
GC : **Adjust 4-bit DAC**	1	Fine (1) or coarse (0) adjustment on discri 4-bit DAC	686	sw_fine_adjust
PP: **4-bit DAC**	1	Enable 4 bit dac power pulsing	687	pwr_on_dac4b
PP: **Trigger Discriminator**	1	Enable trigger discri power pulsing	688	pwr_on_discri
PP: **Delay (ValidHold)**	1	Enable Delay cell power pulsing for the ”ValidHold” signal	689	pwr_on_delay_ValidHold

GC : Delay (ValidHold)	6	Delay for the ”ValidHold” signal (From MSB to LSB)	690	delay_ValidHold (6 bits)
PP: Delay (RstColumn)	1	Enable Delay cell power pulsing for the ”RstColumn” signal	696	pwr_on_delay_RstColumn
GC : Delay (RstColumn)	6	Delay for the ”RstColumn” signal (From MSB to LSB)	697	delay_RstColumn (6 bits)
NC	2		703	
EC : End_ReadOut	1	Enable End_ReadOutX signals	705	
EC : Start_ReadOut	1	Enable Start_ReadOutX signals	706	
EC : ChipSat	1	Enable Opened collector ChipSat signal	707	
EC : TransmitOn2	1	Enable Opened collector TransmitOn2 signal	708	
EC : TransmitOn1	1	Enable Opened collector TransmitOn1 signal	709	
EC : Dout2	1	Enable Opened collector Dout2 signal	710	
EC : Dout1	1	Enable Opened collector Dout1 signal	711	
Total	**712**		712	

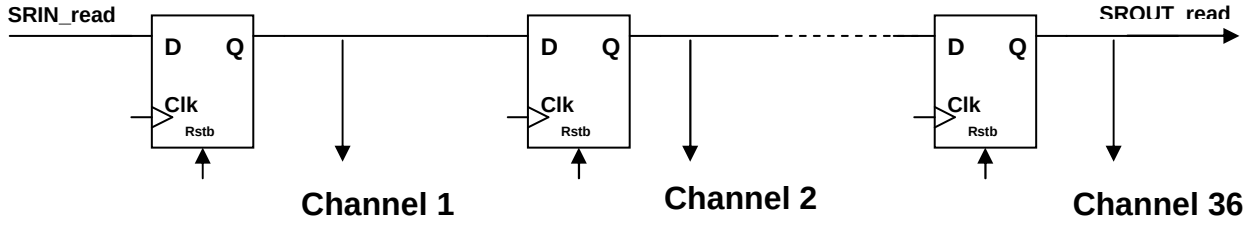
Probe register



Labview Signal name	Probe	Comments	Probe output	Subadd
ExtraTrig (OR36)	1		Digital probe 1	0
Flag_TDC	1		Digital probe 2	1
Startb_ramp_ADC	1		Digital probe 2	2
Start_ramp_TDC	1		Digital probe 2	3
Out_PA_HG/Out_PA_LG	72	From channel 35 to 0	Analogue probe	4
Holdb_SCA	576	From channel 0 to 35 and from column 0 to 15	Digital probe 2	76
Out_ADC_Discri	36	From channel 0 to 35	Digital probe 2	652
Out_Gain_Select_Discri	36	From channel 0 to 35	Digital probe 2	688
Threshold	36	From channel 35 to 0	Analogue probe	724
Out_fs	36	From channel 0 to 35	Analogue probe	760
Out_t_delayed	36	From channel 35 to 0	Digital probe 1	796
Out_t	36	From channel 0 to 35	Digital probe 1	832
Start_ramp_TDC	1		Digital probe 2	868
Start_ramp_TDC_delayed	1		Digital probe 2	869
Out_ramp_TDC	1		Analogue probe	870
Rst_SCA/Rst_SCA_delayed	32	From column 0 to15	Digital probe 2	871
ValidHold/ValidHold_delayed	32	From column 0 to15	Digital probe 2	903
Read	16	From column 0 to15	Digital probe 2	935
NC	1		none	951
Total	**952**			952

14 Multiplexed output “Read registers”

Read register (multiplexed analog output)

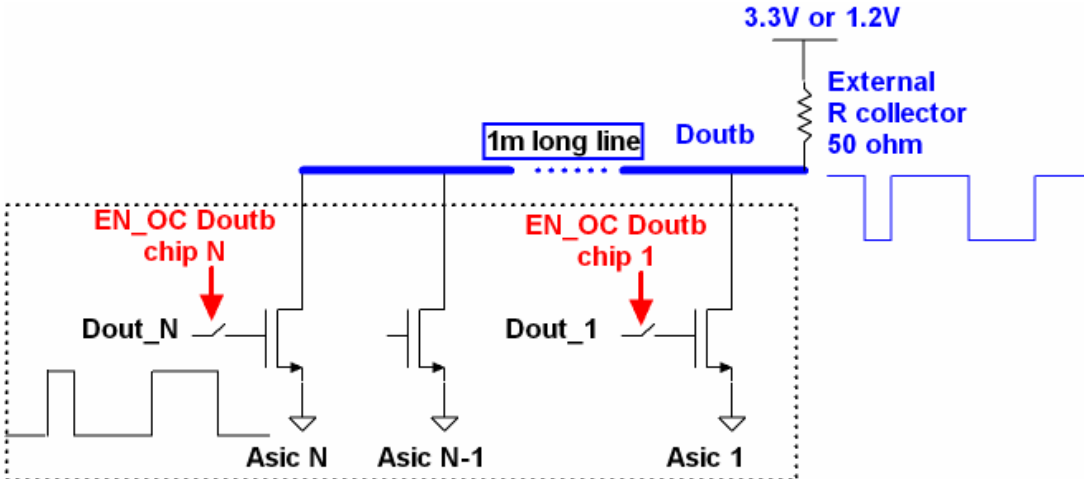


SPIROC1/2 Analogue output Truth Table

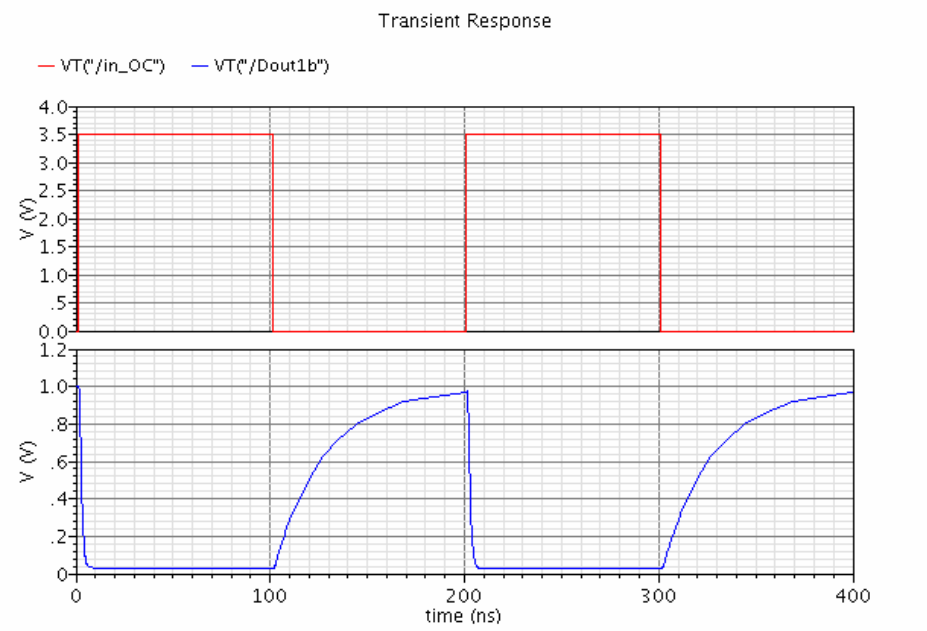
SC: ADC Ext Input	SC: Flag TDC Ext	Pin: Flag TDC Ext	SC: Switch TDC	SC: AutoGain	SC: GainSelect	OUTPUT
0	**0**	**X**	**X**	**X**	**X**	managed by Digital ASIC (Flag TDC Int)
0	**1**	**0**	**0**	**X**	**X**	**TDC Ramp**
0	**1**	**0**	**1**	**X**	**X**	**High Gain**
0	**1**	**1**	**0**	**0**	**X**	depends on GainSelect Discriminator
0	**1**	**1**	**0**	**1**	**0**	**High Gain**
0	**1**	**1**	**0**	**1**	**1**	**Low Gain**
0	**1**	**1**	**1**	**X**	**X**	**Low Gain**
1	**X**	**X**	**X**	**X**	**X**	**ADC Ext Input**

15 Digital open-collectors outputs/inputs

Dout1b, Dout2b, TransmitOn1b, TransmitOn2b, Chipsatb are open collector signals.



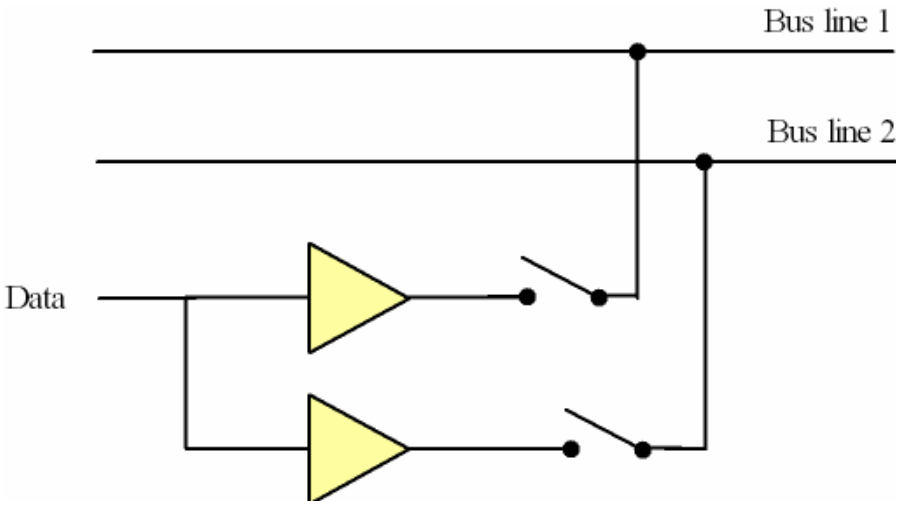
Big internal drivers (Ron=a few ohms) are integrated for each signal to output them on a 5m long line and with an external resistor of 50 Ω. The Figure 17 exhibits a simulation with a 5 m long line (equivalent to 500 pF), Rcollector=50Ω, vdd=1.2V.



OC drivers simulation

Redundancy of the OC lines:

To ensure the realibility of the lines used in the daisy chain, the Doutb, transmitonb, start and end readout signals have been doubled. The selection of the line to be daisy chained is made using SC parameters.

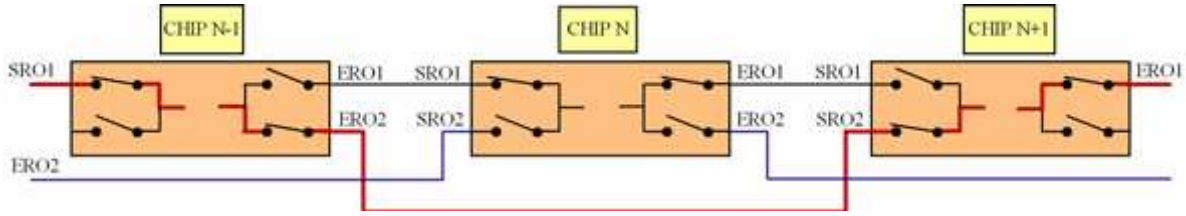


Extra buffers for redundancy

StartReadout and EndReadout bypass:

The bypass of one bad ASIC of the daisy chain can be performed as the StartRO and EndReadout signals have been doubled.

The bypass has to be made on the PCB using switches or resistors. The selection of the line is made using the SC parameters.



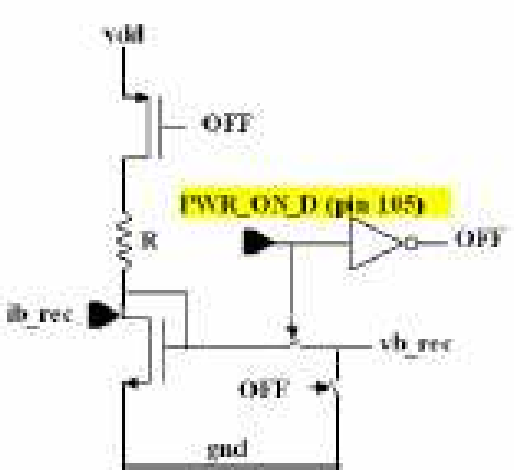
StartReaout and EndReaout bypass

16 Power pulsing signals

The new electronics readout is intended to be embedded in the detector. One important feature is the reduction of the power consumption. The huge number of electronic channels makes crucial such a reduction to 25 µWatt per channel using the power pulsing scheme, possible thanks to the ILC bunch pattern: 2 ms of acquisition, conversion and readout data for 198 ms of dead time. However, to save more power, during each mode, the unused stages are off.

- **pwr_on_a :** analog part (preamplifiers, slow shapers, fast shapers, trigger discriminators, tdc ramp)
- **pwr_on_sca :** sca part
- **pwr_on_adc :** conversion part (gain selection discriminators, adc discriminators, adc ramp), output analog buffers.
- **pwr_on_dac :** Bandgap, 10-bit dual DAC
- **pwr_on_d:** digital part

Bias currents interrupted (see slow control parameters) during interbunch (see figure below).

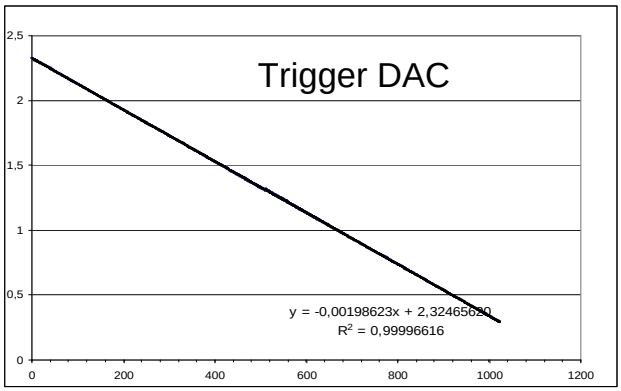


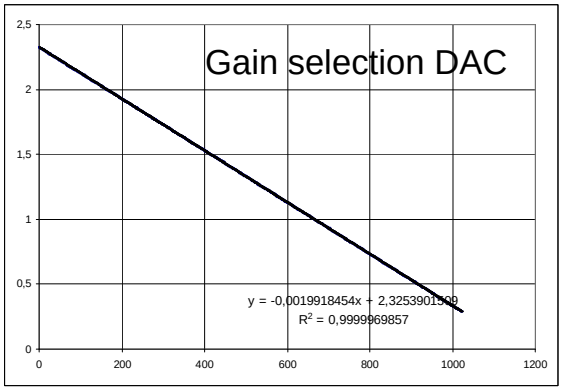
17 Trigger and gain selection DAC linarity measurement

Threshold DAC

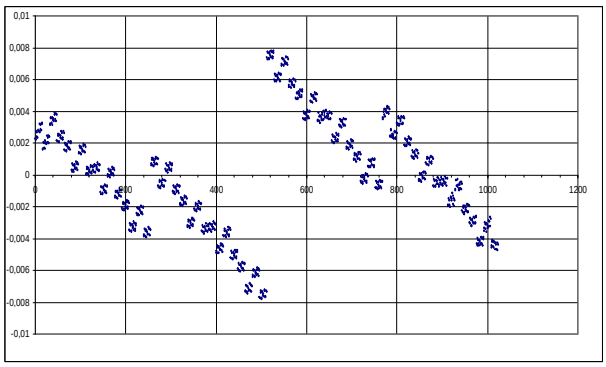
Their linearity have been measured: the residuals of the both DACs are within ±5 mV for a 2.6V dynamic range which corresponds to an Integral Non Linearity of 0.2% (2LSB). The slope is 2.5mV per DAC unit.

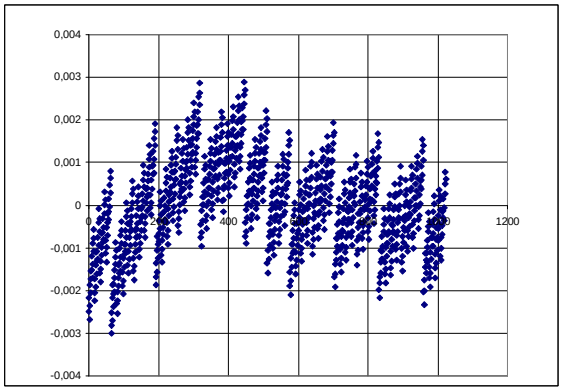
Linearity





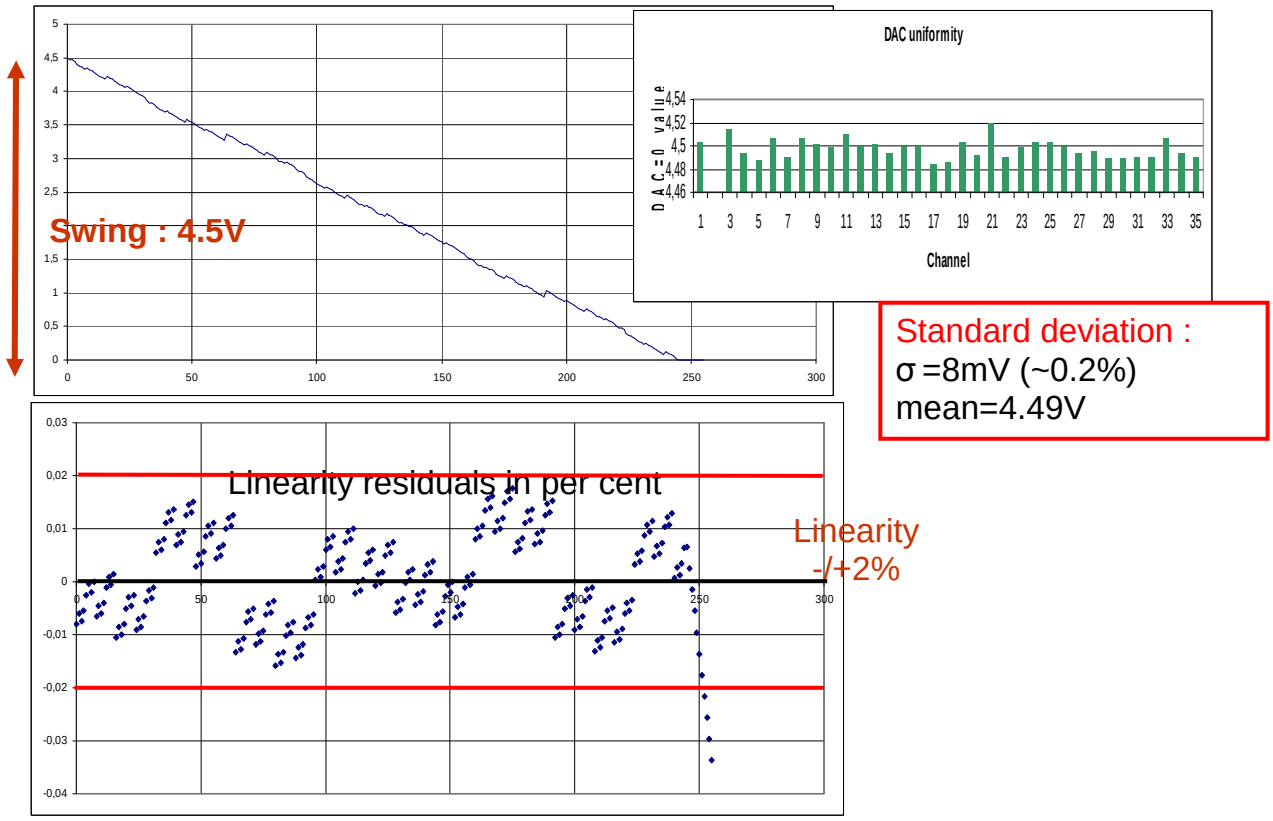
Residuals (mV)

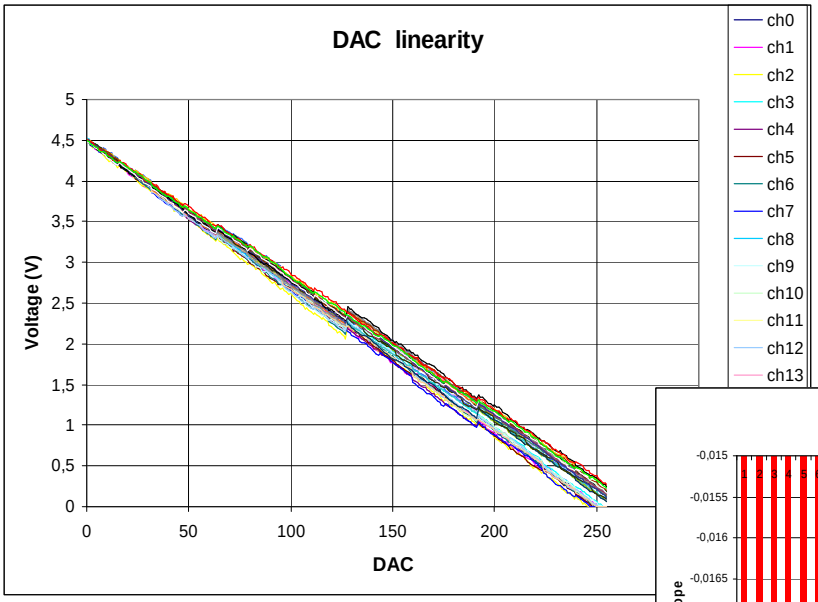




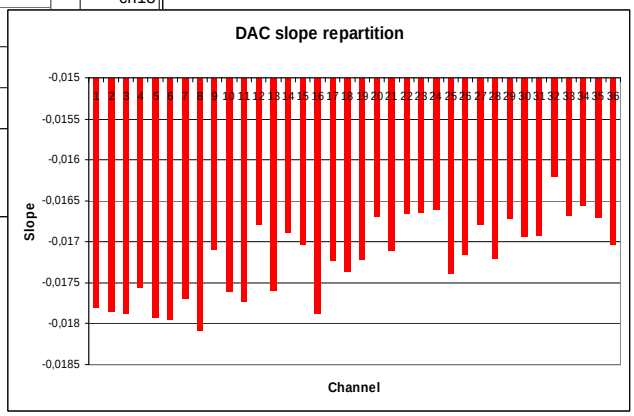
18 Input 8-bit DAC linarity measurements

The input DAC span goes from 4.5V down to 0.5V with a LSB of 20 mV. The default value is 4.5V in order to operate the SiPM at minimum over-voltage when the DAC is not loaded. The linearity is ±2% (5LSB), just enough for the SiPM operation but consistent with the allocated area. Also, the dispersion between channels, although not fundamental could also be improved. The power dissipation is well within the specs and the 100nA bias current to V_{dd} makes the chip difficult to measure without special precautions.





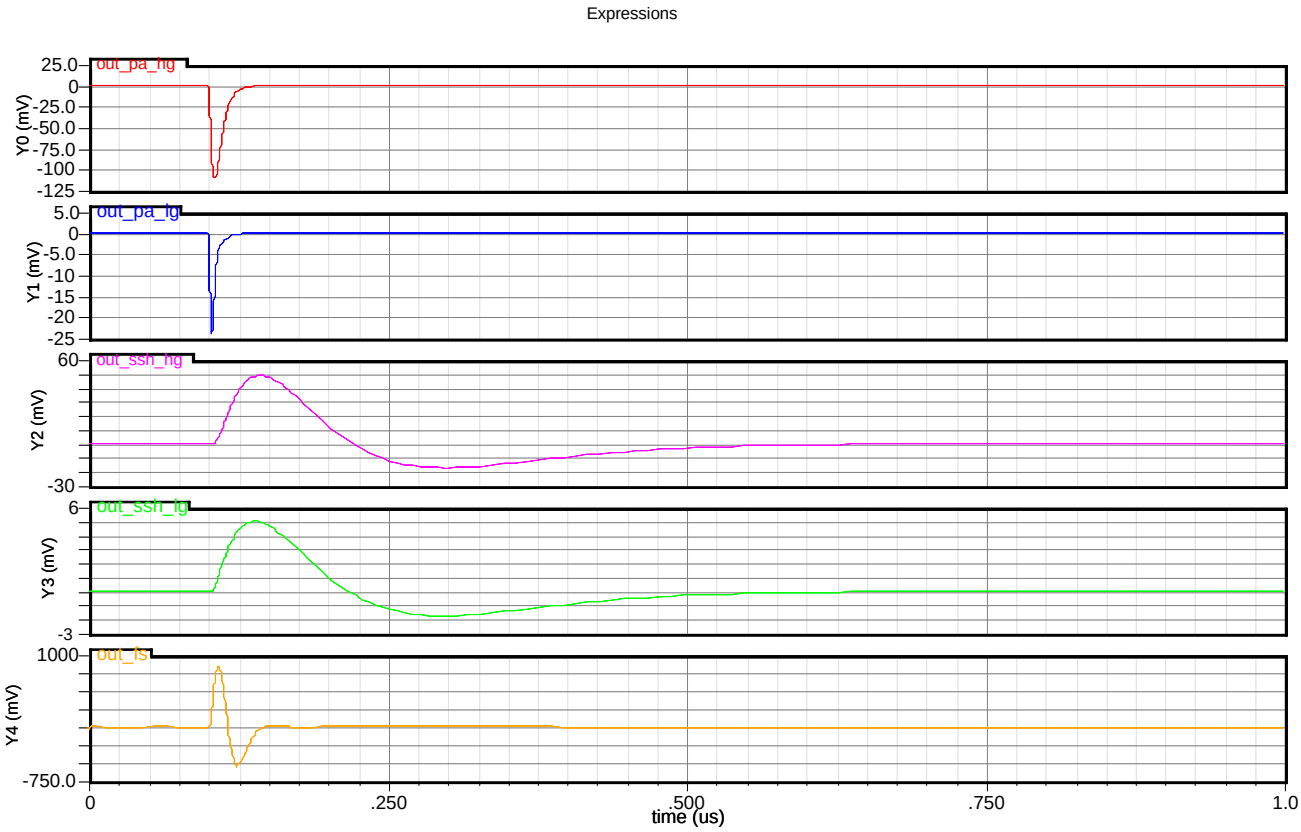
Standard deviation :
σ =0.49mV (~2.8%)
mean=0.0172 V



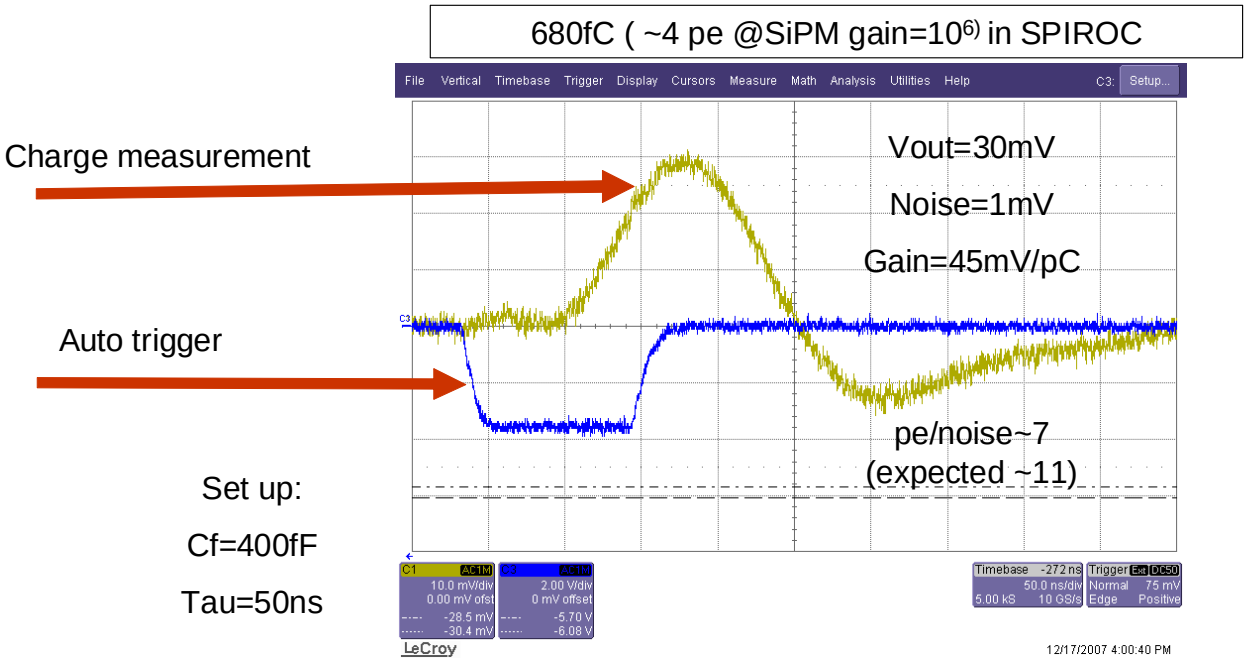
19 Charge output

Temporal signals

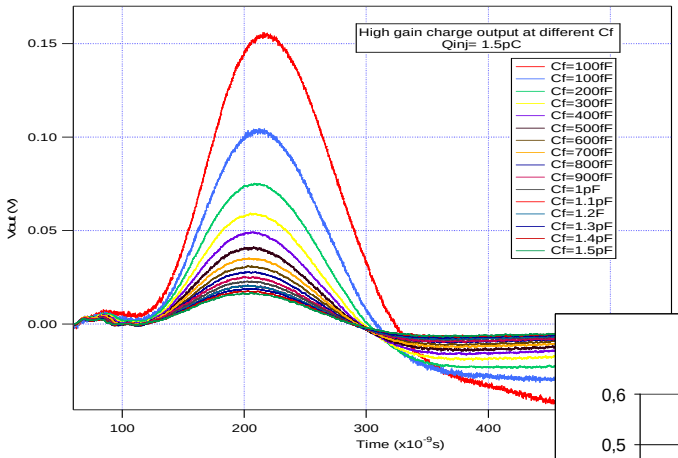
User: raux Date: Jan 8, 2008 Time: 3:16:24 PM CET

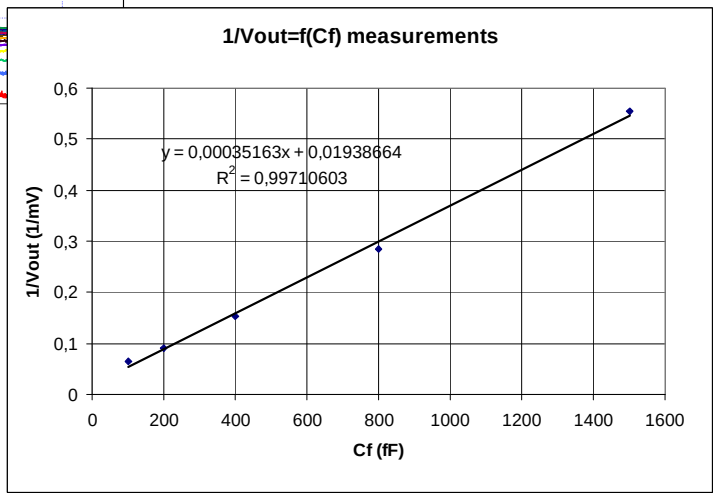


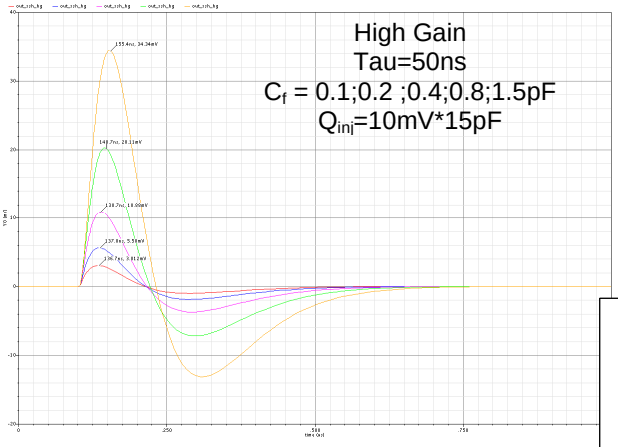
High gain channel output

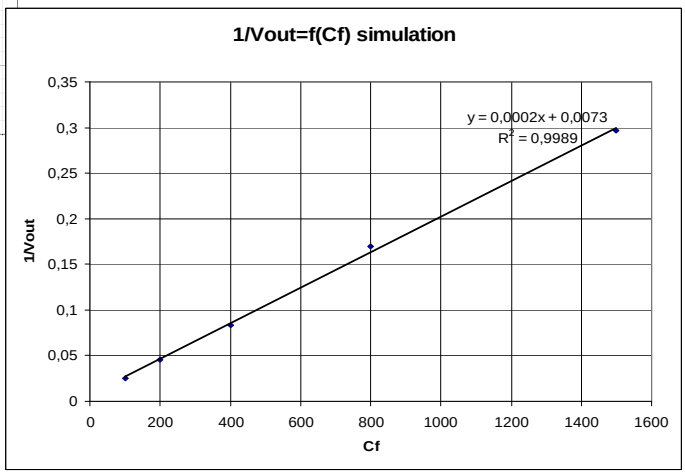


- **High gain output**

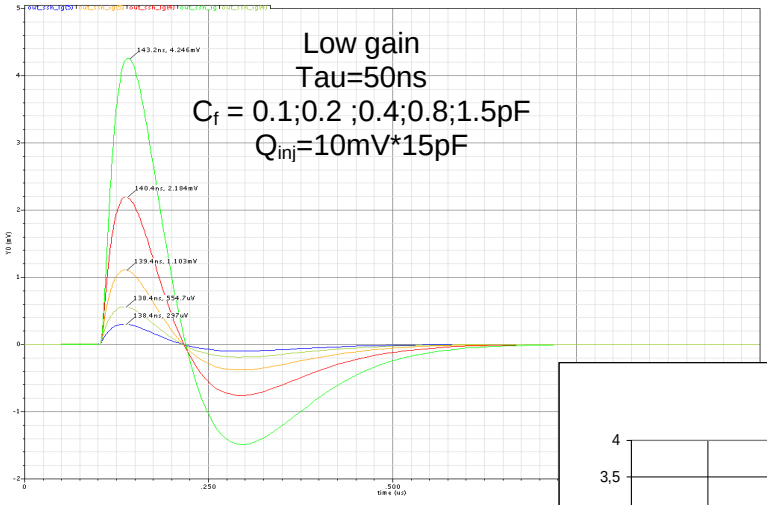


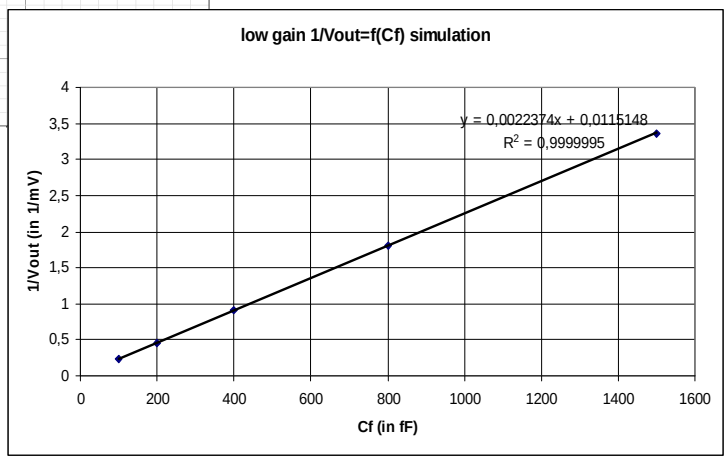


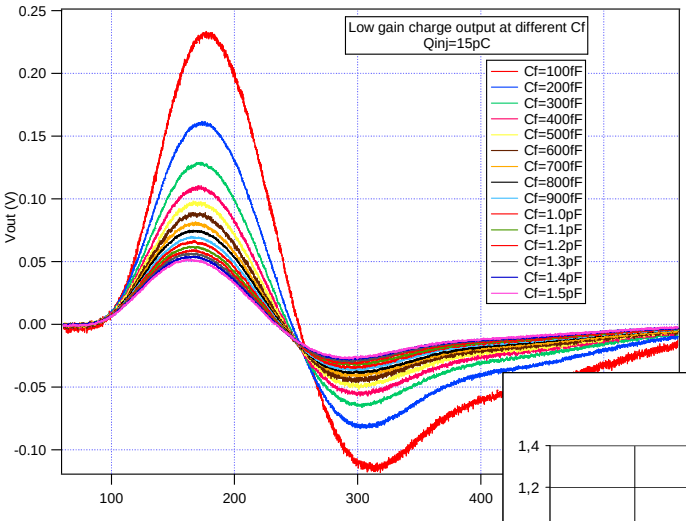


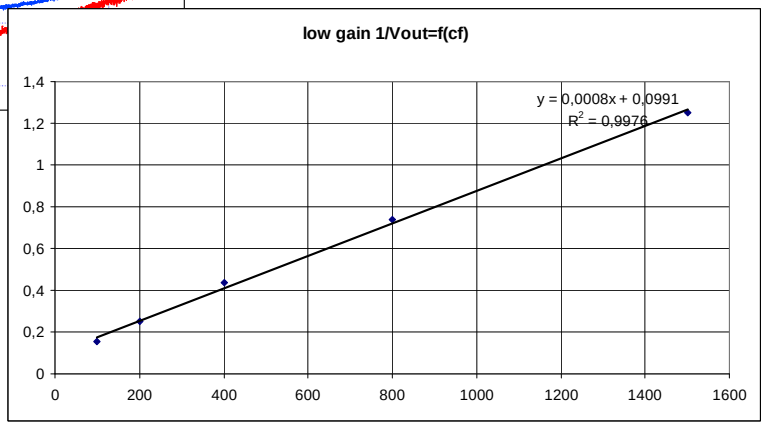


- **Low gain output**

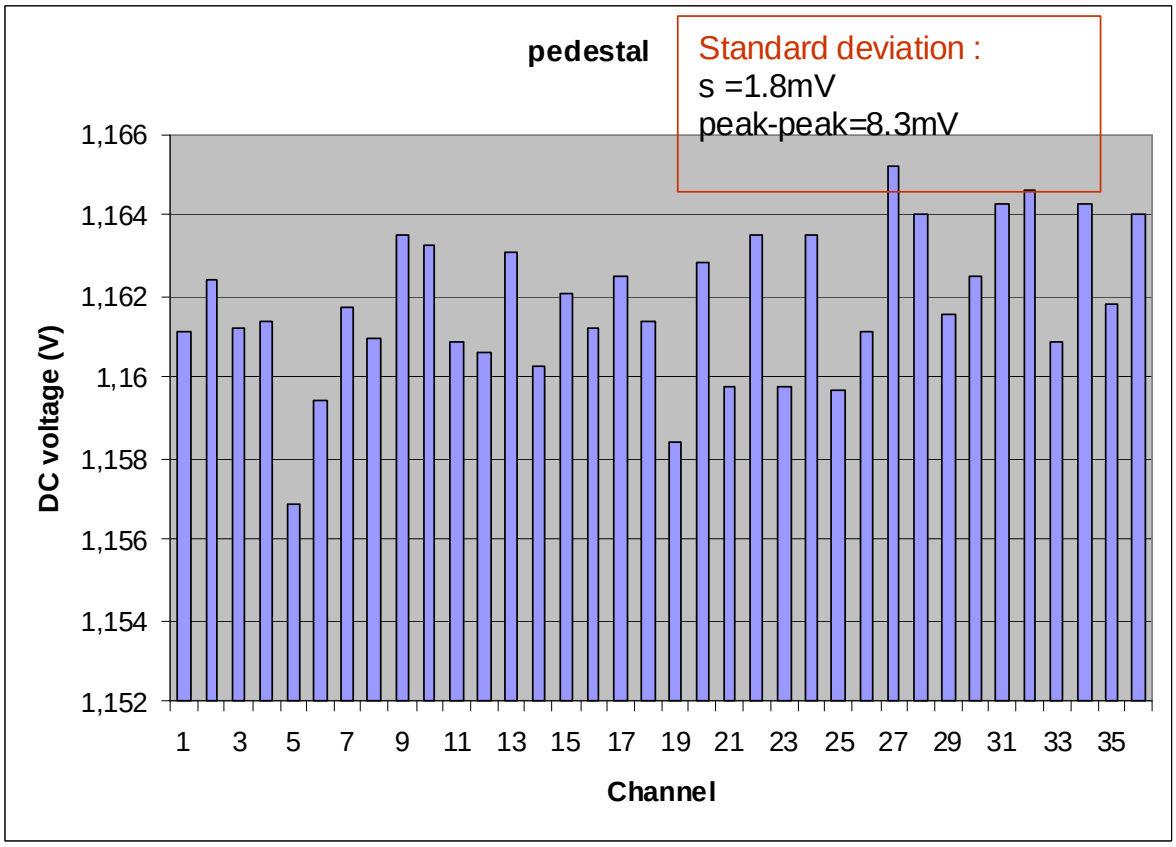

Low gain
Tau=50ns
C_f = 0.1;0.2 ;0.4;0.8;1.5pF
Q_{inj}=10mV*15pF


low gain 1/Vout=f(Cf) simulation
y = 0,0022374x + 0,0115148
R² = 0,9999995
1/Vout (in 1/mV)
Cf (in fF)


Low gain charge output at different Cf
Qinj=15pC
Cf=100fF
Cf=200fF
Cf=300fF
Cf=400fF
Cf=500fF
Cf=600fF
Cf=700fF
Cf=800fF
Cf=900fF
Cf=1.0pF
Cf=1.1pF
Cf=1.2pF
Cf=1.3pF
Cf=1.4pF
Cf=1.5pF
Vout (V)

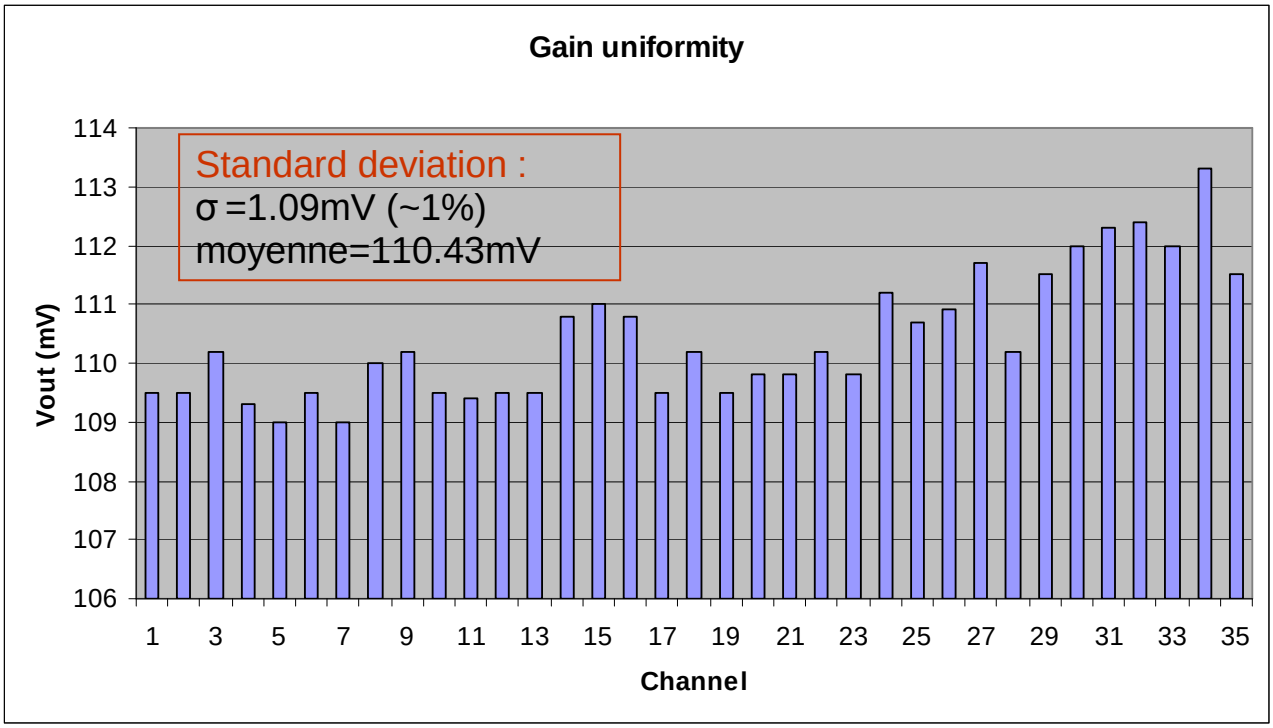

low gain 1/Vout=f(cf)
y = 0,0008x + 0,0991
R² = 0,9976

Pedestals mesurements

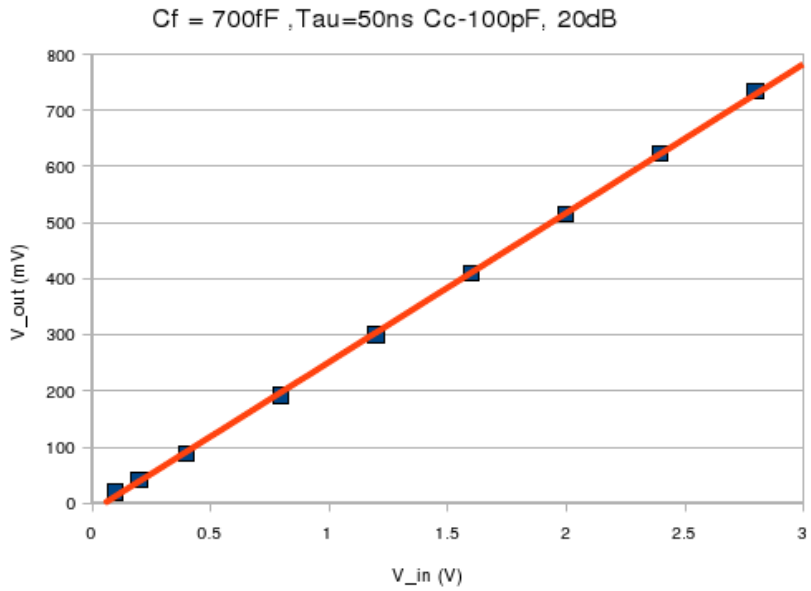


Gain uniformity measurement

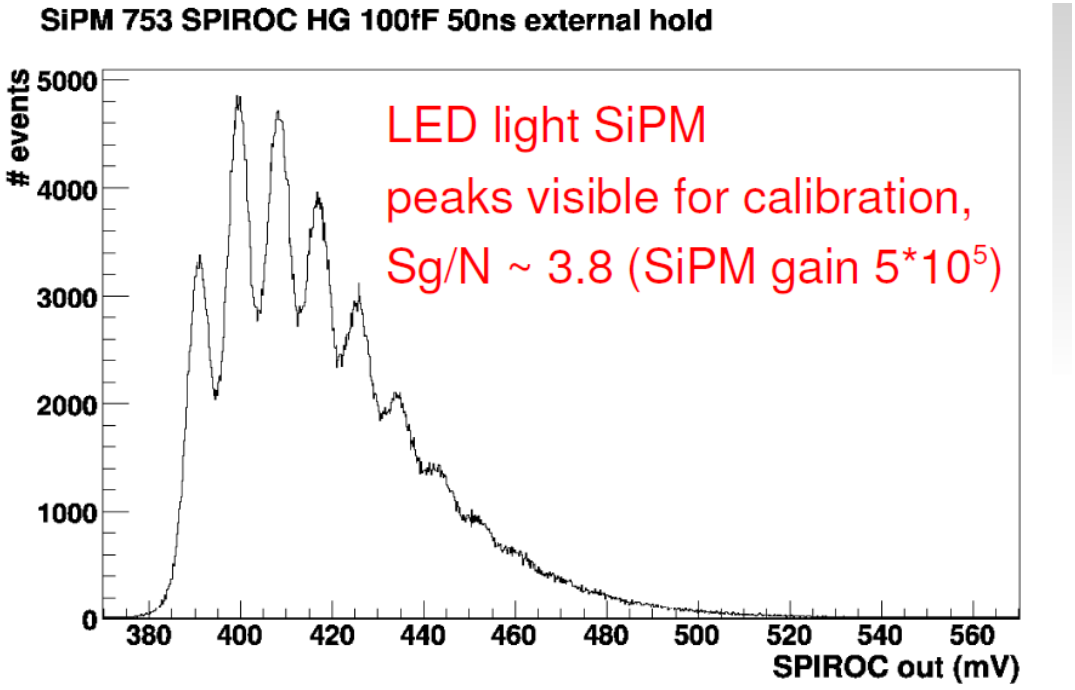
o 1.6pC injected, Cf=400fF, tau=50ns



Linearity

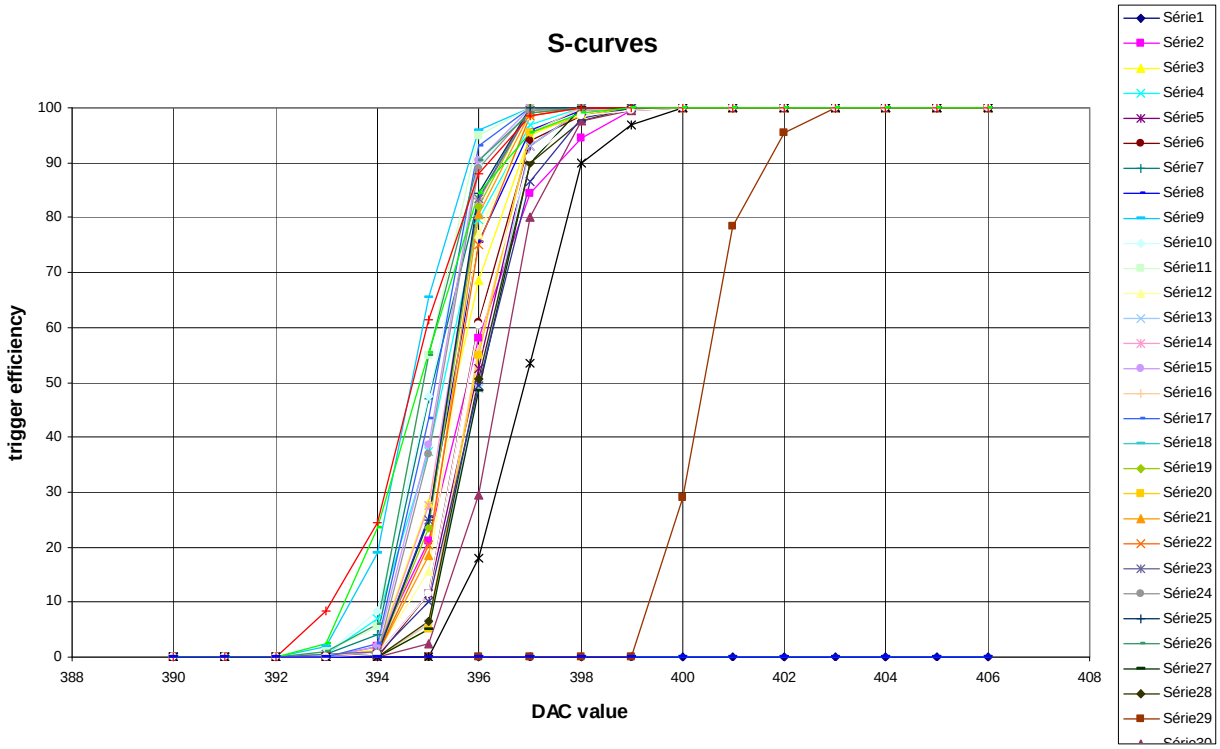


Single photo electron spectrum :
The photoelectron to noise ratio of 4 allows to nicely resolve the single photoelectrons peaks. The next figure shows the single photo electron spectrum.



20 Trigger measurements S-curves

- Cf=400fF, Qinj=150fC, tau=50ns


S-curves
trigger efficiency
DAC value
0
10
20
30
40
50
60
70
80
90
100
388
390
392
394
396
398
400
402
404
406
408
Série1
Série2
Série3
Série4
Série5
Série6
Série7
Série8
Série9
Série10
Série11
Série12
Série13
Série14
Série15
Série16
Série17
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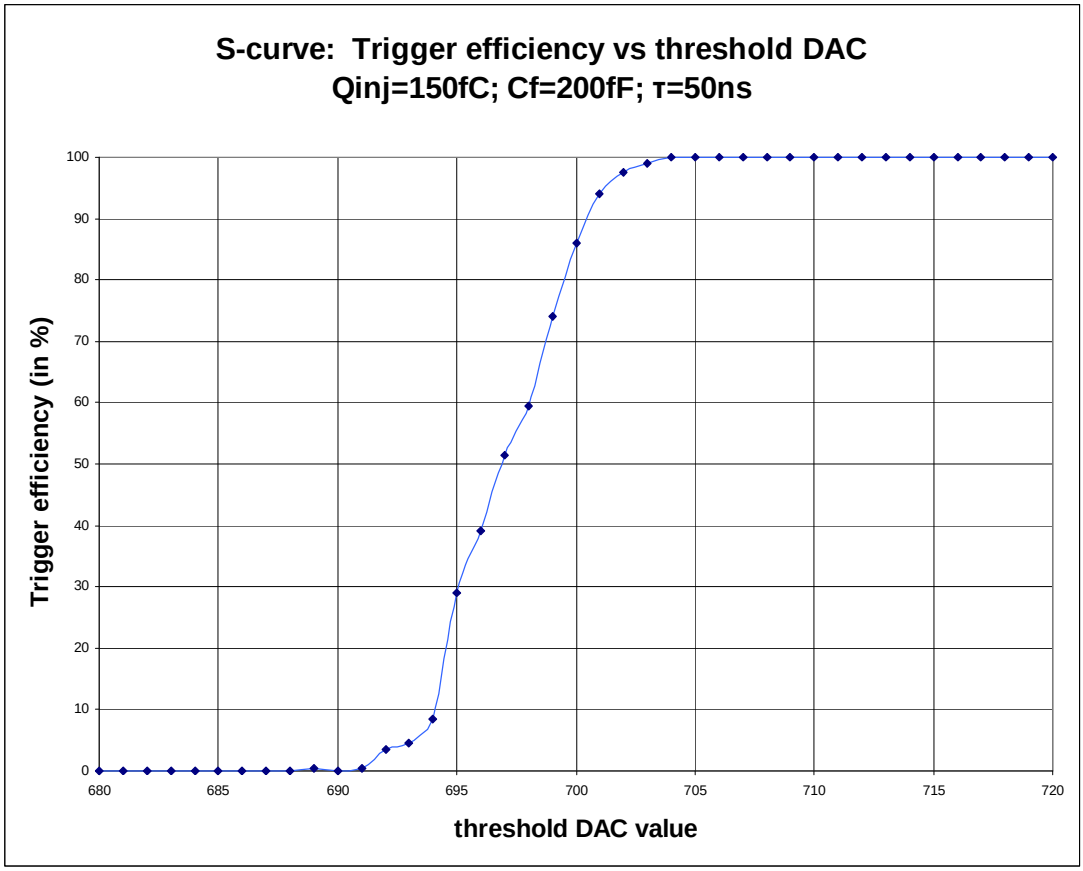
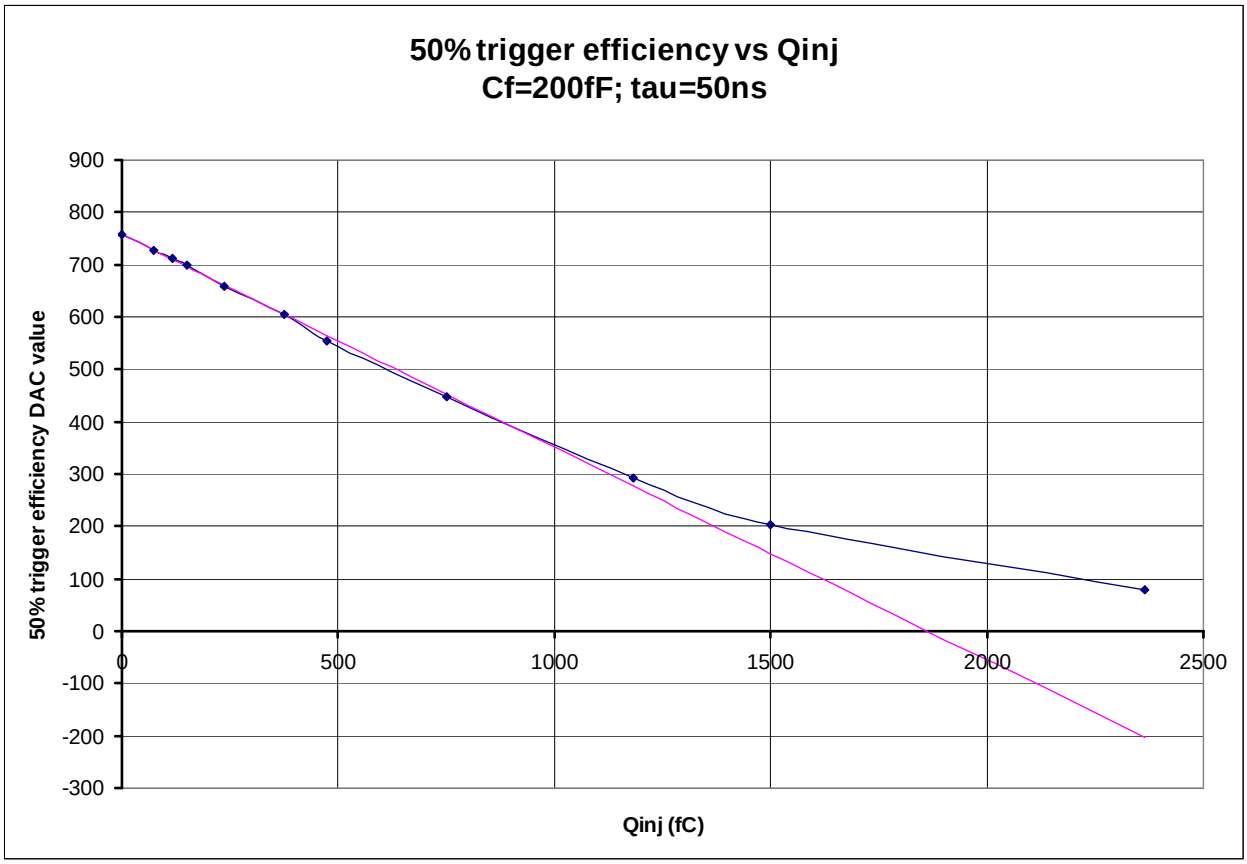
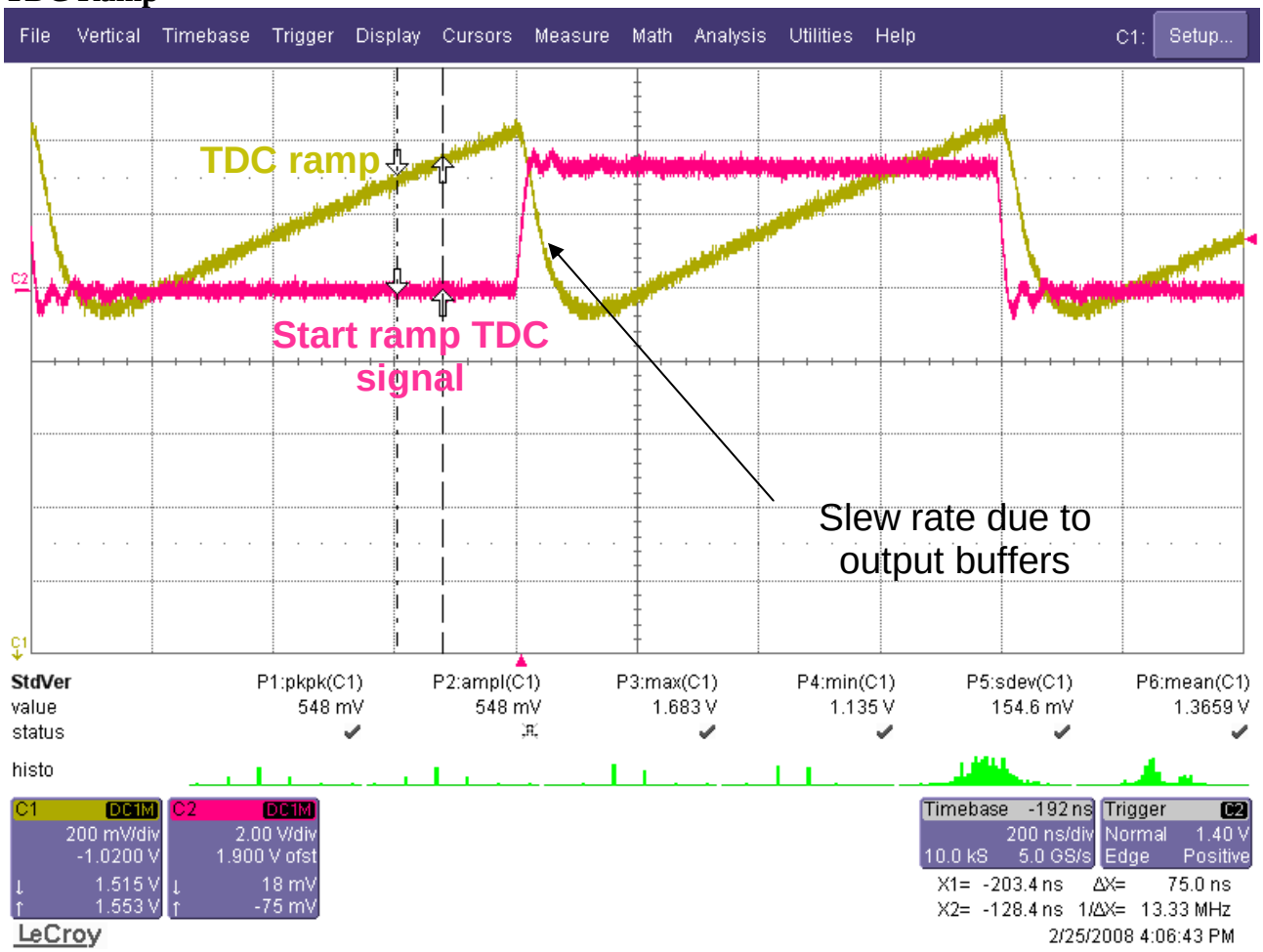
Série24
Série25
Série26
Série27
Série28
Série29

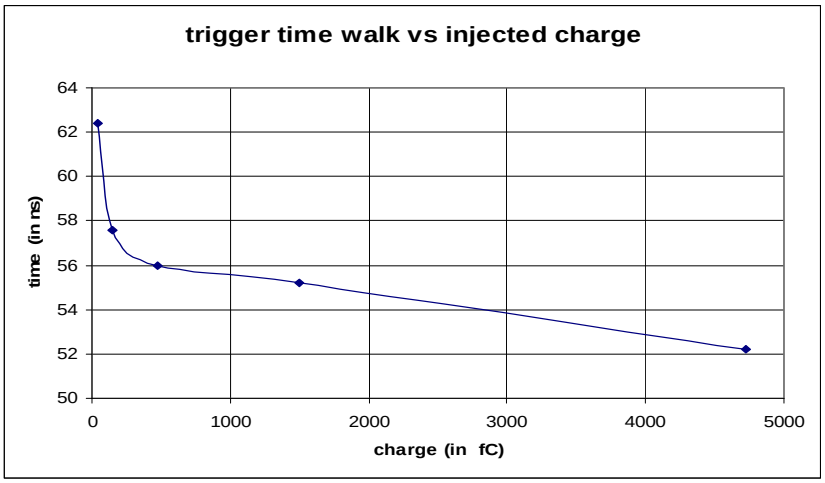

S-curve: Trigger efficiency vs threshold DAC
Qinj=150fC; Cf=200fF; τ=50ns
Trigger efficiency (in %)
threshold DAC value
0
10
20
30
40
50
60
70
80
90
100
680
685
690
695
700
705
710
715
720


50% trigger efficiency vs Qinj
Cf=200fF; tau=50ns
50% trigger efficiency DAC value
900
800
700
600
500
400
300
200
100
0
-100
-200
-300
0
500
1000
1500
2000
2500
Qinj (fC)

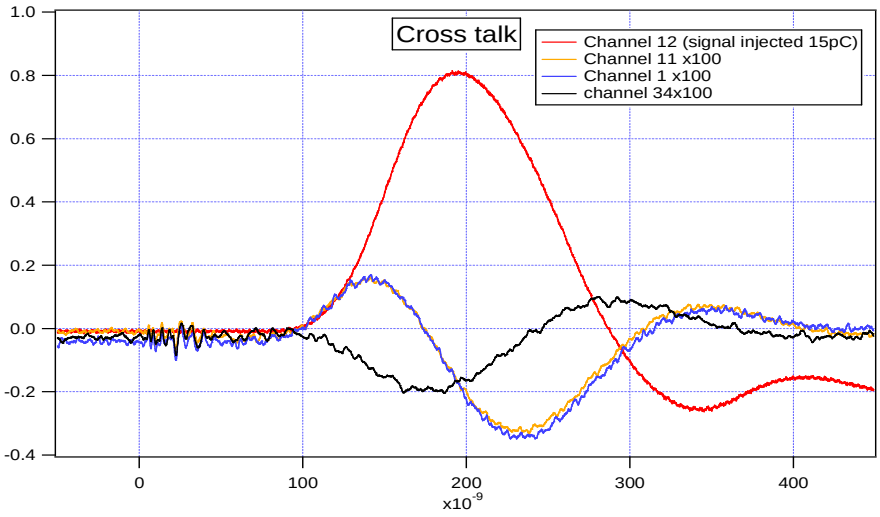
- **TDC Ramp**


File Vertical Timebase Trigger Display Cursors Measure Math Analysis Utilities Help
C1: Setup...
TDC ramp
Start ramp TDC signal
Slew rate due to output buffers
StdVer
value
status
histo
P1:pkpk(C1) 548 mV
P2:ampl(C1) 548 mV
P3:max(C1) 1.683 V
P4:min(C1) 1.135 V
P5:sdev(C1) 154.6 mV
P6:mean(C1) 1.3659 V
C1 DC1M 200 mV/div -1.0200 V 1.515 V 1.553 V
C2 DC1M 2.00 V/div 1.900 V ofst 18 mV -75 mV
Timebase -192 ns 200 ns/div 10.0 kS 5.0 GS/s
Trigger C2 Normal 1.40 V Edge Positive
X1= -203.4 ns ΔX= 75.0 ns
X2= -128.4 ns 1/ΔX= 13.33 MHz
LeCroy
2/25/2008 4:06:43 PM

- **Trigger Time walk :**
  - The trigger time walk between large signal and small signal is about 6ns



- **Charge output Cross-talk**
  - Very low Cross-Talk: 0.3% (long distance cross talk due to slow shaper voltage reference: If this voltage decoupled with 100µF, it becomes negligible ~0.04%)



21 Digital parts