Xin Xin

Address: 4328 Scorpius St, Orlando, FL 32816
Email: xin.xin@ucf.edu
Homepage: https://xinx2013.github.io/
Phone: (+1) 407 823 1753

Research Interests

My research focuses on sustainable, reliable, and high-performance memory systems, e.g., main memory (DRAM) sustainability/reliability/efficiency, processing-in-memory (PIM)/near-data-processing (NDP), hybrid DRAM-NVM system, and memory-based accelerators.

Education

University of Pittsburgh — Pittsburgh, PA
Ph.D. in Electrical and Computer Engineering — Jan. 2018 - Jun. 2023
Advisor: Jun Yang

Tsinghua University — Beijing, China
M.E. in Electrical Engineering — Sep. 2013 - Jul. 2016
Advisors: Tianling Ren and Yi Yang

Lanzhou University — Lanzhou, China
B.S. in Electrical Engineering — Sep. 2009 - Jul. 2013

Professional Experiences

University of Central Florida — Orlando, FL
Tenure-Track Assistant Professor — Aug. 2023 - *present*

Alibaba Group — Sunnyvale, CA
Research Intern — Aug. 2021 - Dec. 2021

Huada Electronic Design Co., Ltd. — Beijing, China
Digital Design Engineer — Aug. 2016 - Aug. 2017

University of Pittsburgh — Pittsburgh, PA
Graduate Research Assistant — Jan. 2018 - Jul. 2023

Tsinghua University — Beijing, China
Graduate Research Assistant — Spe. 2013 - Jul. 2016

Teaching Experiences

Assistant Professor, University of Central Florida — Orlando, FL
EEL 5706 - Resilient Computer System Design — Aug. 2024 - Dec. 2024
EEL 4781 - Computer Communication Networks — Jan. 2024 - Apr. 2024

Teaching Assistant, University of Pittsburgh — Pittsburgh, PA
ECE 1869 - Introduction to Electrical Engineering — Jan. 2021 - May 2021
ECE 1212 - Electronic Circuit Design Laboratory — Aug. 2020 - Dec. 2020
ECE 1110 - Computer Organization and Architecture — Jan. 2020 - May 2020
ECE 0202 - Embedded Processors and Interfacing — Aug. 2019 - Dec. 2019

Publications

C1 Weidong Cao, Jian Gao, **Xin Xin**, Xuan Zhang, "Addition is Most You Need: Efficient Floating-Point SRAM Compute-in-Memory by Harnessing Mantissa Addition," in Proceedings of the 61st ACM/IEEE Design Automation Conference. **(DAC 2024)**

C2 Yanan Guo, Dingyuan Cao, **Xin Xin**, Youtao Zhang, Jun Yang, "Uncore Encore: Covert Channels Exploiting Uncore Frequency Scaling," in Proceedings of the 56th IEEE/ACM International Symposium on Microarchitecture. **(MICRO 2023)**

C3 Yanan Guo, **Xin Xin**, Youtao Zhang, Jun Yang, "Leaky Way: A Conflict-Based Cache Covert Channel Bypassing Set Associativity," in Proceedings of the 55th IEEE/ACM International Symposium on Microarchitecture. **(MICRO 2022)**

C4 **Xin Xin**, Wanyi Zhu, and Li Zhao, "Architecting DDR5 DRAM Caches for Non-Volatile Memory Systems," in Proceedings of the 59th ACM/IEEE Design Automation Conference. **(DAC 2022)**

C5 **Xin Xin**, Yanan Guo, Youtao Zhang, and Jun Yang, "SAM: Accelerating Strided Memory Accesses," in Proceedings of the 54th IEEE/ACM International Symposium on Microarchitecture. **(MICRO 2021)**

C6 Congming Gao, **Xin Xin**, Youyou Lu, Youtao Zhang, Jun Yang, and Jiwu Shu, "ParaBit: Processing Parallel Bitwise Operations in NAND Flash Memory based SSDs," in Proceedings of the 54th IEEE/ACM International Symposium on Microarchitecture. **(MICRO 2021)**

C7 **Xin Xin**, Youtao Zhang, and Jun Yang, "Reducing DRAM Access Latency via Helper Rows," in Proceedings of the 57th ACM/IEEE Design Automation Conference. **(DAC 2020)**

C8 **Xin Xin**, Youtao Zhang, and Jun Yang, "ELP2IM: Efficient and Low Power Bitwise Operation Processing in DRAM," in Proceedings of the 26th International Symposium on High-Performance Computer Architecture. **(HPCA 2020)**

C9 **Xin Xin**, Youtao Zhang, and Jun Yang, "ROC: DRAM-based Processing with Reduced Operation Cycles," in Proceedings of the 56th ACM/IEEE Design Automation Conference. **(DAC 2019)**

J1 **Xin Xin**, Haiming Zhao, Huiwen Cao, He Tian, Yi Yang, and Tianling Ren, "In situ observation of electrical property of thin-layer black phosphorus based on dry transfer method," Applied Physics Express, 2016, 9(4): 45202.

J2 Ziming Zhang*, **Xin Xin***, Qingfeng Yan, Qiang Li, Yi Yang, and Tianling Ren, "Two-step heating synthesis of sub-3 millimeter-sized orthorhombic black phosphorus single crystal by chemical vapor transport reaction method," Science China Materials, 2016, 59(2): 122-134. *(* eequal contribution)*

Professional Services

Reviewer
2025 International Symposium on Computer Architecture (ISCA'25)
2025 IEEE International Symposium on High-Performance Computer Architecture (HPCA'25)
2025, 2024 ACM Special Interest Group on Measurement and Evaluation (SIGMETRICS'25 & 24)
2024 IEEE Computer Society Annual Symposium on VLSI (ISVLSI'24)
IEEE Computer Architecture Letters
Transactions on Embedded Computing Systems
Transactions on Parallel and Distributed Systems
Journal of Systems Architecture

Services
2024 International Symposium on Secure and Private Execution Environment Design (SEED'24): local chair
2020 57th IEEE/ACM International Symposium on Microarchitecture (MICRO'20): Student Assistant

Research Experiences

1. Bandwidth Efficiency Optimization Aug. 2020 - Present

- Exploring under-utilized resources in commodity DRAM memories to improve bandwidth efficiency for specific applications with irregular access patterns, e.g., strided accesses and metadata accesses (C2).

- We employed the unused internal bandwidth in server memories to tackle the over-fetching problem of strided memory accesses with near-zero hardware overhead.
- We leveraged the under-utilized channel bandwidth in large memory subsystems to mitigate the metadata overhead with negligible hardware overhead.

2. In-Place Processing in Memory Jan. 2018 - Present

- Exploiting the intrinsic architecture of commodity DRAM memories to enable logic operations, e.g., AND and OR, inside DRAM chips and avoid redundant data movement (C3, C4, C9).
- We employed the parasitic capacitance on bitlines to develop a Boolean logic function for input variables located in DRAM cells.
- We augmented the cells with specific components to implement bulk logic operations with reduced latency and high energy efficiency.

3. Hybrid DRAM-NVM Memory Performance Optimization Aug. 2021 - Present

- Reducing the performance penalty for an Optane system under the memory mode where DRAM is used as an off-chip cache for NVM (C1).
- We allocated a dedicated channel for tag transfer to reduce the miss overhead.
- We proposed a novel swap operation to mitigate the writeback overhead.

4. Memory Latency Optimization Aug. 2020 - May 2021

- Reducing the overhead of restoring charges back to DRAM cells, which accounts for a significant proportion of a row access cycle (C5).
- We repurposed the novel Row-Clone operations in recent PIM designs for restore truncation, i.e., cloning a row and selectively discarding the copy to avoid the restore.
- We augmented the proposed design by increasing the reuse possibility of the copied row.

5. Fundamental Device Design Jan. 2014 - May. 2016

- Designing and characterizing novel integrated circuits and semiconductor devices, with a focus on their electrical properties, e.g., on-off ratio and mobility (J1, J2).
- We set up a manufacturing process, including photolithography, deposition, plasma etching, etc., for device fabrication using emerging 2-dimensional materials such as black phosphorus (BP).
- We discovered that the electrical conduction of BP devices is time-dependent and exhibits an irregular reinstating phase.

Honors And Awards

University of Pittsburgh EGSO Travel Grant	2021
NSF/HPCA Travel Grant	2020
DAC 2020 Young Student Fellow	2020
Graduated with the Highest Honor set by the Government of Beijing	2016
Graduated with the Highest Honor set by Lanzhou University	2013

Talks

Architecting DDR5 DRAM Caches for Non-Volatile Memory Systems. *DAC 2022*
Improving the Next-Generation (DDR5) Optane Memory. *Alibaba Group 2021*
Accelerating Strided Memory Accesses. *MICRO 2021*
Reducing DRAM Access Latency via Helper Rows. *DAC 2020*
Efficient and Low Power Bitwise Operation Processing in DRAM. *HPCA 2020*
DRAM-based Processing with Reduced Operation Cycles. *DAC 2019*