Lab Code [10 points]
Filename: Parity.sv
AndrewID: xinyew

```
 1 `default_nettype none
 2 module Parity
 3     (input logic d2, d1, p2, d0, p1, p0,
 4     output logic valid);
 5
 6     logic nor_1, nor_2, nor_3, nor_4, nor_5, nor_6, nor_7, nor_8, nor_9,
 7             nor_10, nor_11, nor_12;
 8     logic not_d2, not_d1, not_p2, not_d0, not_p1, not_p0;
 9
10     not (not_d2, d2),
11         (not_d1, d1),
12         (not_p2, p2),
13         (not_d0, d0),
14         (not_p1, p1),
15         (not_p0, p0);
16     //term 1
17     nor (nor_1, d1, not_d0, p0);
18     //term 2
19     nor (nor_2, not_d2, d0, p1);
20     //term 3
21     nor (nor_3, d1, d0, not_p0);
22     //term 4
23     nor (nor_4, not_d2, not_d0, not_p1);
24     //term 5
25     nor (nor_5, p2, p1, not_p0);
26     //term 6
27     nor (nor_6, d2, not_d0, p1);
28     //term 7
29     nor (nor_7, p2, not_p1, p0);
30     //term 8
31     nor (nor_8, not_p2, not_p1, not_p0);
32     //term 9
33     nor (nor_9, not_p2, p1, p0);
34     //term 10
35     nor (nor_10, not_d1, d0, p0);
36     //term 11
37     nor (nor_11, d2, d0, not_p1);
38     //term 12
39     nor (nor_12, not_d1, not_d0, not_p0);
40
41     nor (valid, nor_1, nor_2, nor_3, nor_4, nor_5, nor_6, nor_7, nor_8,
42         nor_9, nor_10, nor_11, nor_12);
43
44 endmodule: Parity
45
46 module Parity_test;
47     logic [5:0] vector;
48     logic valid;
49
50     Parity DUT(.d2(vector[5]),
51                .d1(vector[4]),
52                .p2(vector[3]),
53                .d0(vector[2]),
54                .p1(vector[1]),
55                .p0(vector[0]),
56                .valid(valid));
57
58     initial begin
59         $monitor($time,,
60             "vector = %b, valid = %b", vector, valid);
61         for (vector=6'b0; vector < 6'b111111; vector++)
62             #1;
63         #1 $finish;
64     end
65
66 endmodule: Parity_test
```

Lab Code [10 points]
Filename: chipInterface.sv
AndrewID: xinyew

```
 1 `default_nettype none
 2 module chipInterface
 3     (input logic SW[17:0],
 4     output logic LEDR[17:0]);
 5
 6     Parity PAR(.d2(SW[5]),
 7                .d1(SW[4]),
 8                .p2(SW[3]),
 9                .d0(SW[2]),
10                .p1(SW[1]),
11                .p0(SW[0]),
12                .valid(LEDR[17]));
13
14 endmodule: chipInterface
```