Problem 2: [4 points] Drill problem
Filename: hw1prob2_test.sv
AndrewID: xinyew

```
`default_nettype none

module hw1prob2_test
  (output logic a, b, c,
   input logic out);

  initial begin
    $monitor($time,
      "a = %b, b = %b, c = %b, out = %b",
      a, b, c, out);
        a = 0;
        b = 0;
        c = 0;

     #10 c = 1;
     #10 b = 1;
     #10 a = 1;
     #10 c = 0;
     #10 b = 0;
     #10 c = 1;

     #10 a = 0;
         b = 1;
         c = 0;
     #10 $finish;
  end
endmodule: hw1prob2_test


module system();
  logic wire_a, wire_b, wire_c, test_out;

  hw1prob2 DUT (.a(wire_a),
                .b(wire_b),
                .c(wire_c),
                .f(test_out));

  hw1prob2_test mt (.a(wire_a),
                    .b(wire_b),
                    .c(wire_c),
                    .out(test_out));

endmodule: system
```

Problem 5: [4 points] Drill problem
Filename: hw1prob5.sv
AndrewID: xinyew

```
 1 `default_nettype none
 2
 3 module hw1prob5
 4   (input  logic A, B, C,
 5    output logic Fsop, Gsop, Fpos, Gpos);
 6
 7    logic notA, notB, notC;
 8    logic notA_and_notC, A_and_notB_and_C, A_and_notB_and_notC;
 9    logic notA_and_notB_and_C, A_and_B_and_C, notA_and_B_and_notC;
10    logic A_or_notC, notA_or_C, notB_or_notC, A_or_B_or_C;
11    logic notA_or_B_or_notC, A_or_notB_or_notC, notA_or_notB_or_C;
12
13    not    g1(notA, A);
14    not    g2(notB, B);
15    not    g3(notC, C);
16
17    and #2 g4(notA_and_notC, notA, notC);
18    and #2 g5(A_and_notB_and_C, A, notB, C);
19    and #2 g6(A_and_notB_and_notC, A, notB, notC);
20    and #2 g7(notA_and_notB_and_C, notA, notB, C);
21    and #2 g8(A_and_B_and_C, A, B, C);
22    and #2 g9(notA_and_B_and_notC, notA, B, notC);
23
24    or  #2 g12(A_or_notC, A, notC);
25    or  #2 g13(notA_or_C, notA, C);
26    or  #2 g14(notB_or_notC, notB, notC);
27    or  #2 g15(A_or_B_or_C, A, B, C);
28    or  #2 g16(notA_or_B_or_notC, notA, B, notC);
29    or  #2 g17(A_or_notB_or_notC, A, notB, notC);
30    or  #2 g18(notA_or_notB_or_C, notA, notB, C);
31
32    or  #2 g10(Fsop, notA_and_notC, A_and_notB_and_C);
33    or  #2 g11(Gsop, A_and_notB_and_notC, notA_and_notB_and_C,
34                A_and_B_and_C, notA_and_B_and_notC);
35
36    and #2 g19(Fpos, A_or_notC, notA_or_C, notB_or_notC);
37    and #2 g20(Gpos, A_or_B_or_C, notA_or_B_or_notC,
38                A_or_notB_or_notC,notA_or_notB_or_C);
39
40 endmodule: hw1prob5
```

Problem 6: [4 points] Drill problem
Filename: hw1prob6.sv
AndrewID: xinyew

```
  1 `default_nettype none
  2 module circuit(
  3   input  logic a, b, c, d,
  4   output logic f);
  5
  6   logic notB, notC, notD;
  7   logic f1, f2;
  8
  9   not     g1(notB, b);
 10   not     g2(notC, c);
 11   not     g3(notD, d);
 12
 13   and #2 g4(f1, b, notC, d),
 14          g5(f2, notB, notD);
 15
 16   or  #2 g6(f, f1, f2, a);
 17
 18 endmodule: circuit
 19
 20
 21 module testbench();
 22   logic f;
 23   logic [3:0] vector;
 24
 25   circuit dut(.f(f),
 26               .a(vector[3]),
 27               .b(vector[2]),
 28               .c(vector[1]),
 29               .d(vector[0])
 30               );
 31
 32   initial begin
 33     $monitor("A: %b B: %b C: %b D: %b F: %b at time %d", vector[3], vector[2]...
Line length of 111 (max is 80)
 34           vector[3] = 0;
 35           vector[2] = 0;
 36           vector[1] = 0;
 37           vector[0] = 0;
 38
 39       #20 vector[3] = 0;
 40           vector[2] = 0;
 41           vector[1] = 0;
 42           vector[0] = 1;
 43
 44       #20 vector[3] = 0;
 45           vector[2] = 0;
 46           vector[1] = 1;
 47           vector[0] = 0;
 48
 49       #20 vector[3] = 0;
 50           vector[2] = 0;
 51           vector[1] = 1;
 52           vector[0] = 1;
 53
 54       #20 vector[3] = 0;
 55           vector[2] = 1;
 56           vector[1] = 0;
 57           vector[0] = 0;
 58
 59       #20 vector[3] = 0;
 60           vector[2] = 1;
 61           vector[1] = 0;
 62           vector[0] = 1;
 63
 64       #20 vector[3] = 0;
 65           vector[2] = 1;
 66           vector[1] = 1;
 67           vector[0] = 0;
 68
```

```
 69        #20 vector[3] = 0;
 70            vector[2] = 1;
 71            vector[1] = 1;
 72            vector[0] = 1;
 73
 74        #20 vector[3] = 1;
 75            vector[2] = 0;
 76            vector[1] = 0;
 77            vector[0] = 0;
 78
 79        #20 vector[3] = 1;
 80            vector[2] = 0;
 81            vector[1] = 0;
 82            vector[0] = 1;
 83
 84        #20 vector[3] = 1;
 85            vector[2] = 0;
 86            vector[1] = 1;
 87            vector[0] = 0;
 88
 89        #20 vector[3] = 1;
 90            vector[2] = 0;
 91            vector[1] = 1;
 92            vector[0] = 1;
 93
 94        #20 vector[3] = 1;
 95            vector[2] = 1;
 96            vector[1] = 0;
 97            vector[0] = 0;
 98
 99        #20 vector[3] = 1;
100            vector[2] = 1;
101            vector[1] = 0;
102            vector[0] = 1;
103
104        #20 vector[3] = 1;
105            vector[2] = 1;
106            vector[1] = 1;
107            vector[0] = 0;
108
109        #20 vector[3] = 1;
110            vector[2] = 1;
111            vector[1] = 1;
112            vector[0] = 1;
113
114        #20 $finish;
115    end
116
117 endmodule: testbench
```

Problem 8: [16 points]
AndrewID: xinyew

Compilation Errors:

```
hw1prob8.sv: file does not exist
hw1prob8_test.sv: file does not exist
```

```
Problem 8: [16 points]
Filename: hw1prob8.sv
AndrewID: xinyew

File hw1prob8.sv was not found
```

```
Problem 8: [16 points]
Filename: hw1prob8_test.sv
AndrewID: xinyew

File hw1prob8_test.sv was not found
```