

Problem 2: [4 points] Drill problem
Filename: hw1prob2_test.sv
AndrewID: xinyew

```
1 `default_nettype none
2
3 module hw1prob2_test
4   (output logic a, b, c,
5     input logic out);
6
7   initial begin
8     $monitor($time,
9       "a = %b, b = %b, c = %b, out = %b",
10      a, b, c, out);
11     a = 0;
12     b = 0;
13     c = 0;
14
15     #10 c = 1;
16     #10 b = 1;
17     #10 a = 1;
18     #10 c = 0;
19     #10 b = 0;
20     #10 c = 1;
21
22     #10 a = 0;
23     b = 1;
24     c = 0;
25     #10 $finish;
26   end
27 endmodule: hw1prob2_test
28
29
30 module system();
31   logic wire_a, wire_b, wire_c, test_out;
32
33   hw1prob2 DUT (.a(wire_a),
34     .b(wire_b),
35     .c(wire_c),
36     .f(test_out));
37
38   hw1prob2_test mt (.a(wire_a),
39     .b(wire_b),
40     .c(wire_c),
41     .out(test_out));
42
43 endmodule: system
```

Problem 5: [4 points] Drill problem
Filename: hw1prob5.sv
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```
1 `default_nettype none
2
3 module hw1prob5
4   (input  logic A, B, C,
5    output logic Fsop, Gsop, Fpos, Gpos);
6
7   logic notA, notB, notC;
8   logic notA_and_notC, A_and_notB_and_C, A_and_notB_and_notC;
9   logic notA_and_notB_and_C, A_and_B_and_C, notA_and_B_and_notC;
10  logic A_or_notC, notA_or_C, notB_or_notC, A_or_B_or_C;
11  logic notA_or_B_or_notC, A_or_notB_or_notC, notA_or_notB_or_C;
12
13  not    g1(notA, A);
14  not    g2(notB, B);
15  not    g3(notC, C);
16
17  and #2 g4(notA_and_notC, notA, notC);
18  and #2 g5(A_and_notB_and_C, A, notB, C);
19  and #2 g6(A_and_notB_and_notC, A, notB, notC);
20  and #2 g7(notA_and_notB_and_C, notA, notB, C);
21  and #2 g8(A_and_B_and_C, A, B, C);
22  and #2 g9(notA_and_B_and_notC, notA, B, notC);
23
24  or  #2 g12(A_or_notC, A, notC);
25  or  #2 g13(notA_or_C, notA, C);
26  or  #2 g14(notB_or_notC, notB, notC);
27  or  #2 g15(A_or_B_or_C, A, B, C);
28  or  #2 g16(notA_or_B_or_notC, notA, B, notC);
29  or  #2 g17(A_or_notB_or_notC, A, notB, notC);
30  or  #2 g18(notA_or_notB_or_C, notA, notB, C);
31
32  or  #2 g10(Fsop, notA_and_notC, A_and_notB_and_C);
33  or  #2 g11(Gsop, A_and_notB_and_notC, notA_and_notB_and_C,
34           A_and_B_and_C, notA_and_B_and_notC);
35
36  and #2 g19(Fpos, A_or_notC, notA_or_C, notB_or_notC);
37  and #2 g20(Gpos, A_or_B_or_C, notA_or_B_or_notC,
38           A_or_notB_or_notC, notA_or_notB_or_C);
39
40 endmodule: hw1prob5
```

Problem 6: [4 points] Drill problem
Filename: hw1prob6.sv
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```
1 `default_nettype none
2 module circuit(
3     input  logic a, b, c, d,
4     output logic f);
5
6     logic notB, notC, notD;
7     logic f1, f2;
8
9     not      g1(notB, b);
10    not      g2(notC, c);
11    not      g3(notD, d);
12
13    and #2 g4(f1, b, notC, d),
14          g5(f2, notB, notD);
15
16    or  #2 g6(f, f1, f2, a);
17
18 endmodule: circuit
19
20
21 module testbench();
22     logic f;
23     logic [3:0] vector;
24
25     circuit dut(.f(f),
26                .a(vector[3]),
27                .b(vector[2]),
28                .c(vector[1]),
29                .d(vector[0])
30                );
31
32     initial begin
33         $monitor("A: %b B: %b C: %b D: %b F: %b at time %d",
34                 vector[3], vector[2], vector[1], vector[0], f, $time);
35         vector[3] = 0;
36         vector[2] = 0;
37         vector[1] = 0;
38         vector[0] = 0;
39
40         #20 vector[3] = 0;
41             vector[2] = 0;
42             vector[1] = 0;
43             vector[0] = 1;
44
45         #20 vector[3] = 0;
46             vector[2] = 0;
47             vector[1] = 1;
48             vector[0] = 0;
49
50         #20 vector[3] = 0;
51             vector[2] = 0;
52             vector[1] = 1;
53             vector[0] = 1;
54
55         #20 vector[3] = 0;
56             vector[2] = 1;
57             vector[1] = 0;
58             vector[0] = 0;
59
60         #20 vector[3] = 0;
61             vector[2] = 1;
62             vector[1] = 0;
63             vector[0] = 1;
64
65         #20 vector[3] = 0;
66             vector[2] = 1;
67             vector[1] = 1;
68             vector[0] = 0;
69
70     end
```

```
70      #20 vector[3] = 0;
71      vector[2] = 1;
72      vector[1] = 1;
73      vector[0] = 1;
74
75      #20 vector[3] = 1;
76      vector[2] = 0;
77      vector[1] = 0;
78      vector[0] = 0;
79
80      #20 vector[3] = 1;
81      vector[2] = 0;
82      vector[1] = 0;
83      vector[0] = 1;
84
85      #20 vector[3] = 1;
86      vector[2] = 0;
87      vector[1] = 1;
88      vector[0] = 0;
89
90      #20 vector[3] = 1;
91      vector[2] = 0;
92      vector[1] = 1;
93      vector[0] = 1;
94
95      #20 vector[3] = 1;
96      vector[2] = 1;
97      vector[1] = 0;
98      vector[0] = 0;
99
100     #20 vector[3] = 1;
101     vector[2] = 1;
102     vector[1] = 0;
103     vector[0] = 1;
104
105     #20 vector[3] = 1;
106     vector[2] = 1;
107     vector[1] = 1;
108     vector[0] = 0;
109
110     #20 vector[3] = 1;
111     vector[2] = 1;
112     vector[1] = 1;
113     vector[0] = 1;
114
115     #20 $finish;
116 end
117
118 endmodule: testbench
```

Problem 8: [16 points]

AndrewID: xinyew

Compilation Errors:

hw1prob8.sv: file does not exist

hw1prob8_test.sv: file does not exist

Problem 8: [16 points]

Filename: hw1prob8.sv

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File hw1prob8.sv was not found

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