Problem 2: [4 points] Drill problem
Filename: hw1prob2_test.sv
AndrewID: xinyew

```
`default_nettype none

module hw1prob2_test
  (output logic a, b, c,
   input logic out);

  initial begin
    $monitor($time,
      "a = %b, b = %b, c = %b, out = %b",
      a, b, c, out);
        a = 0;
        b = 0;
        c = 0;

     #10 c = 1;
     #10 b = 1;
     #10 a = 1;
     #10 c = 0;
     #10 b = 0;
     #10 c = 1;

     #10 a = 0;
         b = 1;
         c = 0;
     #10 $finish;
  end
endmodule: hw1prob2_test


module system();
  logic wire_a, wire_b, wire_c, test_out;

  hw1prob2 DUT (.a(wire_a),
                .b(wire_b),
                .c(wire_c),
                .f(test_out));

  hw1prob2_test mt (.a(wire_a),
                    .b(wire_b),
                    .c(wire_c),
                    .out(test_out));

endmodule: system
```

Problem 5: [4 points] Drill problem
Filename: hw1prob5.sv
AndrewID: xinyew

```
  1 `default_nettype none
  2
  3 module hw1prob5
  4   (input  logic A, B, C,
  5    output logic Fsop, Gsop, Fpos, Gpos);
  6
  7    logic notA, notB, notC;
  8    logic notA_and_notC, A_and_notB_and_C, A_and_notB_and_notC;
  9    logic notA_and_notB_and_C, A_and_B_and_C, notA_and_B_and_notC;
 10    logic A_or_notC, notA_or_C, notB_or_notC, A_or_B_or_C;
 11    logic notA_or_B_or_notC, A_or_notB_or_notC, notA_or_notB_or_C;
 12
 13    not    g1(notA, A);
 14    not    g2(notB, B);
 15    not    g3(notC, C);
 16
 17    and #2 g4(notA_and_notC, notA, notC);
 18    and #2 g5(A_and_notB_and_C, A, notB, C);
 19    and #2 g6(A_and_notB_and_notC, A, notB, notC);
 20    and #2 g7(notA_and_notB_and_C, notA, notB, C);
 21    and #2 g8(A_and_B_and_C, A, B, C);
 22    and #2 g9(notA_and_B_and_notC, notA, B, notC);
 23
 24    or  #2 g12(A_or_notC, A, notC);
 25    or  #2 g13(notA_or_C, notA, C);
 26    or  #2 g14(notB_or_notC, notB, notC);
 27    or  #2 g15(A_or_B_or_C, A, B, C);
 28    or  #2 g16(notA_or_B_or_notC, notA, B, notC);
 29    or  #2 g17(A_or_notB_or_notC, A, notB, notC);
 30    or  #2 g18(notA_or_notB_or_C, notA, notB, C);
 31
 32    or  #2 g10(Fsop, notA_and_notC, A_and_notB_and_C);
 33    or  #2 g11(Gsop, A_and_notB_and_notC, notA_and_notB_and_C, A_and_B_and_C, ...
Line length of 98 (max is 80)
 34
 35    and #2 g19(Fpos, A_or_notC, notA_or_C, notB_or_notC);
 36    and #2 g20(Gpos, A_or_B_or_C, notA_or_B_or_notC, A_or_notB_or_notC,notA_or...
Line length of 89 (max is 80)
 37
 38 endmodule: hw1prob5
```

Problem 6: [4 points] Drill problem
AndrewID: xinyew

Compilation Errors:

```
hw1prob6.sv: file does not exist
```

```
Problem 6: [4 points] Drill problem
Filename: hw1prob6.sv
AndrewID: xinyew

File hw1prob6.sv was not found
```

Problem 8: [16 points]
AndrewID: xinyew

Compilation Errors:

```
hw1prob8.sv: file does not exist
hw1prob8_test.sv: file does not exist
```

```
Problem 8: [16 points]
Filename: hw1prob8.sv
AndrewID: xinyew

File hw1prob8.sv was not found
```

```
Problem 8: [16 points]
Filename: hw1prob8_test.sv
AndrewID: xinyew

File hw1prob8_test.sv was not found
```