dsPIC33EPXXXGM3XX/6XX/7XX Family Silicon Errata and Data Sheet Clarification

The dsPIC33EPXXXGM3XX/6XX/7XX family devices that you have received conform functionally to the current Device Data Sheet (DS70000689**D**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1. The silicon issues are summarized in Table 2.

The errata described in this document will be addressed in future revisions of dsPIC33EPXXXGM3XX/6XX/7XX family silicon.

Note:	This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of Table 2 apply to the current silicon revision (**A2**).

Data Sheet clarifications and corrections start on Page 17, following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® IDE and Microchip's programmers, debuggers and emulation tools, which are available at the Microchip corporate web site (www.microchip.com).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with a hardware debugger:

1. Using the appropriate interface, connect the device to the hardware debugger.
2. Open an MPLAB IDE project.
3. Configure the MPLAB IDE project for the appropriate device and hardware debugger.
4. Based on the version of MPLAB IDE you are using, do one of the following:
   a) For MPLAB IDE 8, select *Programmer > Reconnect*.
   b) For MPLAB X IDE, select *Window > Dashboard* and click the **Refresh Debug Tool Status** icon ().
5. Depending on the development tool used, the part number *and* Device Revision ID value appear in the **Output** window.

Note:	If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The DEVREV values for the various dsPIC33EPXXXGM3XX/6XX/7XX family silicon revisions are shown in Table 1.

TABLE 1: SILICON DEVREV VALUES

Part Number	Device ID[1]	Revision ID for Silicon Revision[2]		
		A0	A1	A2
dsPIC33EP128GM304	0x1B40	0x4000	0x4001	0x4002
dsPIC33EP128GM604	0x1B48			
dsPIC33EP128GM306	0x1B43			
dsPIC33EP128GM706	0x1B4B			
dsPIC33EP128GM310	0x1B47			
dsPIC33EP128GM710	0x1B4F			
dsPIC33EP256GM304	0x1B80			
dsPIC33EP256GM604	0x1B88			
dsPIC33EP256GM306	0x1B83			
dsPIC33EP256GM706	0x1B8B			
dsPIC33EP256GM310	0x1B87			
dsPIC33EP256GM710	0x1B8F			
dsPIC33EP512GM304	0x1BC0			
dsPIC33EP512GM604	0x1BC8			
dsPIC33EP512GM306	0x1BC3			
dsPIC33EP512GM706	0x1BCB			
dsPIC33EP512GM310	0x1BC7			
dsPIC33EP512GM710	0x1BCF			

Note 1: The Device IDs (DEVID and DEVREV) are located at the last two implemented addresses of configuration memory space. They are shown in hexadecimal in the format “DEVID DEVREV”.

2: Refer to the *“dsPIC33EPXXXGM3XX/6XX/7XX Flash Programming Specification”* (DS70000685) for detailed information on Device and Revision IDs for your specific device.

TABLE 2: SILICON ISSUE SUMMARY

Module	Feature	Item Number	Issue Summary	Affected Revisions(1)		
				A0	A1	A2
Core	CPU	1.	Limited execution speed (44/64-pin and 100/121-pin devices).	X	—	—
Core	Program Memory	2.	The address error trap may occur while accessing certain program memory locations.	X	X	X
SPI	Frame Sync Pulse	3.	When in SPI Slave mode with the Frame Sync pulse set as an input, FRMDLY must be set to '0'.	X	X	X
SPI	Frame Master Mode	4.	Received data is right-shifted under certain conditions.	X	X	X
Input Capture	External Sync	5.	Input Capture and Output Compare modules cannot be synchronized.	X	X	X
PWM	Immediate Update	6.	Dead time is not asserted when PDCx is updated to cause an immediate transition on the PWMxH and PWMxL outputs.	X	X	X
PWM	PWM Override	7.	Under certain circumstances, updates to the OVRENH and OVRENL bits may be ignored by the PWMx module.	X	X	—
PWM	Complementary Mode	8.	With dead time greater than zero, 0% and 100% duty cycles cannot be obtained on PWMxL and PWMxH outputs.	X	X	X
PWM	Center-Aligned Mode	9.	Under certain conditions, the PWMxH and PWMxL outputs are deasserted.	X	X	X
PWM	Current Reset Mode	10.	PWM Resets only occur on alternate cycles in Current Reset mode.	X	X	X
PWM	Master Time Base Mode	11.	When the Immediate Update is disabled, certain changes to the PHASEx register may result in missing dead time.	X	X	X
PWM	Redundant/ Push-Pull Output Mode	12.	When the Immediate Update is disabled, changing the duty cycle value from a non-zero value to zero will produce a glitch pulse equal to 1 PWM clock.	X	X	X
PWM	Complementary Mode	13.	If PWM override is turned off during dead time, then the PWM generator may not provide dead time on the corresponding PWMxH-PWMxL edge transition.	X	X	X
ADC	DONE bit	14.	DONE bit does not work when an external interrupt is selected as the ADC trigger source.	X	X	X
ADC	Analog Channel	15.	Selecting the same ANx input for CH0 and CH1 results in erroneous readings for CH1.	X	X	X
CAN	DMA	16.	Write collisions on a DMA-enabled CAN module do not generate DMAC error traps.	X	X	X
JTAG	I/O	17.	$\overline{\text{MCLR}}$ pin operation may be disabled.	X	X	X
JTAG	I/O	18.	Active-high logic pulse on the I/O pin with TMS function at POR.	X	X	X
QEI	Velocity Counter	19.	Under certain circumstances, the Velocity Counter x register (VELxCNT) misses count pulses.	X	X	X
FRC	FRC Accuracy	20.	Change in the FRC accuracy.	X	—	—

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

TABLE 2: SILICON ISSUE SUMMARY (CONTINUED)

Module	Feature	Item Number	Issue Summary	Affected Revisions(1)		
				A0	A1	A2
Op Amp	Op Amp Offset Voltage	21.	Drift in the op amp offset voltage.	X	X	X
CPU	`div.sd`	22.	When using the signed 32-by-16-bit division instruction, `div.sd`, the Overflow bit is not getting set when an overflow occurs.	X	X	X
Output Compare	PWM Mode	23.	In the scaled down timer source for the Output Compare module, the first PWM pulse may not appear on the OCx pin.	X	X	X
Output Compare	Interrupt	24.	Under certain circumstances, an Output Compare match may cause the Output Compare x Interrupt Flag (OCxIF) bit to become set prior to the Change-of-State (COS) of the OCx pin.	X	X	X
CPU	`DO` Loop	25.	PSV access, including Table Reads or Writes in the last instruction of a `DO` loop, is not allowed.	X	X	X
PWM	PWM SWAP	26.	In Center-Aligned mode, there is missing dead time when SWAP is disabled.	X	X	X
PWM	Center-Aligned Mode	27.	Updates to the PHASEx registers occur only at the middle of the center-aligned PWM cycle.	X	X	X
ADC	Integral Nonlinearity (INL) Specification	28.	The AC/DC electrical characteristic, Integral Nonlinearity error in the ADC module, is not within the specifications published in the data sheet.	X	X	X

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

Silicon Errata Issues

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (**A2**).

1. Module: Core

For 44/64-pin and 100/121-pin devices, code execution may be unreliable under the following conditions:

- From -40°C to +85°C for FOSC above 120 MHz (60 MIPS)
- From +85°C to +125°C for FOSC above 100 MHz (50 MIPS)
- From +125°C to +150°C for FOSC above 60 MHz (30 MIPS)

Work around

Do not use clock speeds above 120 MHz for applications operating in the industrial temperature range (-40°C to +85°C) or above 100 MHz for temperatures in the extended range (+85°C to +125°C), or above 60 MHz for the high-temperature range (+125°C to +150°C).

Affected Silicon Revisions

A0	A1	A2					
X							

2. Module: Core

An unexpected address error trap may occur during accesses to program memory addresses, 001h through 200h. This has been observed when one or more interrupt requests are asserted while reading or writing program memory addresses using `TBLRDH/L`, `TBLWTH/L` or PSV-based instructions.

Work around

Before executing instructions that read or write program memory addresses, 001h through 200h, disable interrupts using the `DISI` instruction.

Affected Silicon Revisions

A0	A1	A2					
X	X	X					

3. Module: SPI

When in SPI Slave mode (MSTEN bit (SPIxCON1<5>) = `0`) and using the Frame Sync pulse output feature (FRMEN bit (SPIxCON2<15>) = `1`) in Slave mode (SPIFSD bit (SPIxCON2<14>) = `1`), the Frame Sync Pulse Edge Select bit (FRMDLY bit (SPIxCON2<1>) = `0`) must be set to '`0`'.

Work around

None. The Frame Sync Pulse Edge Select bit, FRMDLY, cannot be set to produce a Frame Sync pulse that coincides with the first bit clock.

Affected Silicon Revisions

A0	A1	A2					
X	X	X					

4. Module: SPI

When SPI is operating in Master mode and Framed SPI mode is enabled (SPIxCON1<5> = `1` and SPIxCON2<15> = `1`), received data may be shifted to the right by one bit when the following conditions are also true:

- The Frame Sync pulse is configured as an output (SPISFD (SPIxCON2<14>) = `0`).
- Input data is sampled at the end of data output time (SMP (SPIxCON1<9>) = `1`).

Work around

Clear the SMP bit while using SPI Frame Master mode; this changes data sampling to the start of data output time.

Affected Silicon Revisions

A0	A1	A2					
X	X	X					

5. Module: Input Capture

When an input capture module is selected as the Sync source for either an output compare module or another input capture module, synchronization may fail.

Work around

None.

Affected Silicon Revisions

A0	A1	A2					
X	X	X					

6. Module: PWM

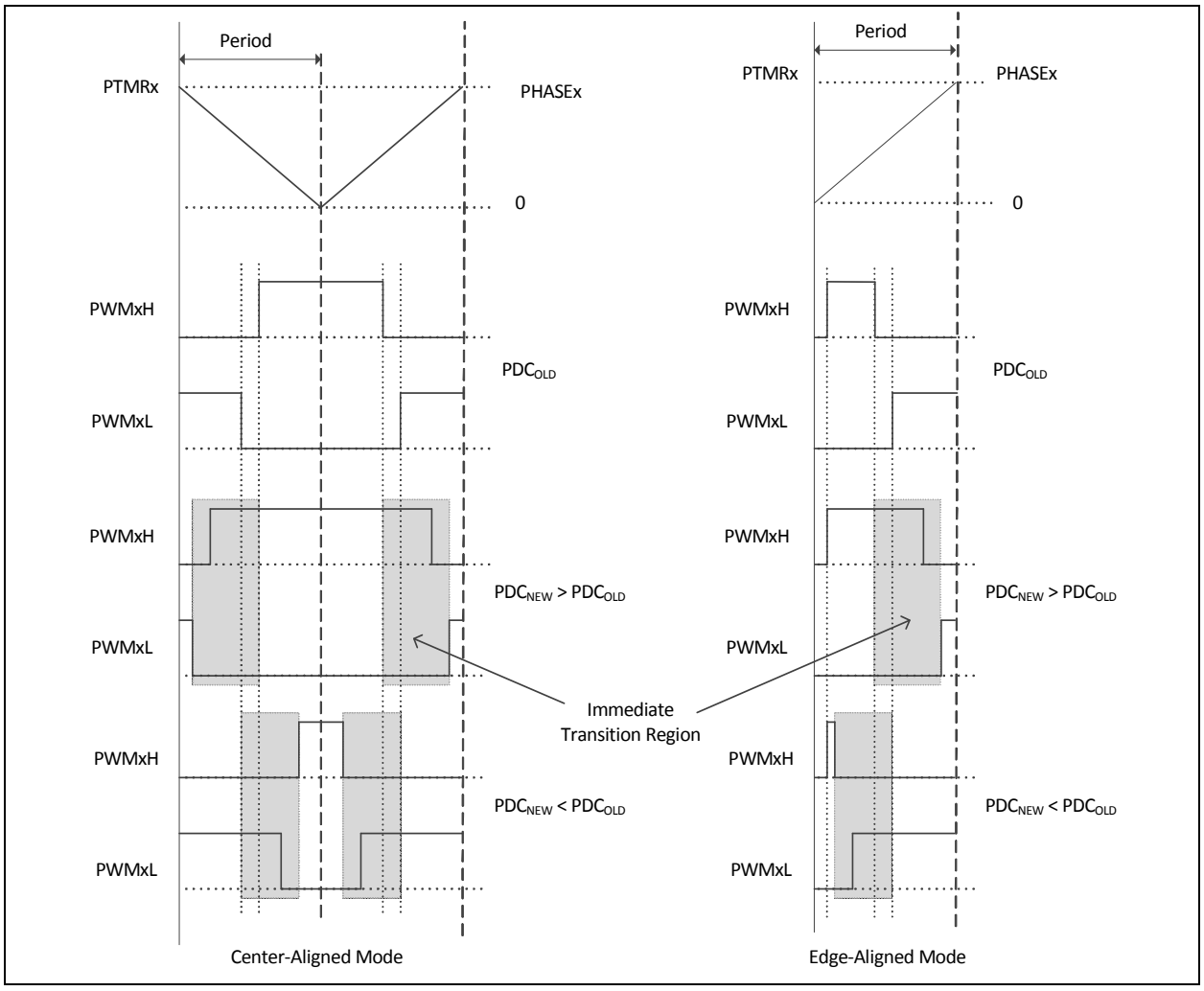
The PWM generator may not assert dead time on the edges of transitions. This has been observed when all of the following conditions are present:

- The PWM generator is configured to operate in Complementary mode with Independent Time Base (ITB) or master time base;
- Immediate update is enabled; and
- The value in the PDC register is updated in such a manner that the PWMxH and PWMxL outputs make an immediate transition.

The current duty cycle, PDCOLD, newly calculated duty cycle, PDCNEW, and the point at which a write to the Duty Cycle register occurs within the PWM time base, will determine if the PWMxH and PWMxL outputs make an immediate transition. PWMxH and PWMxL outputs make an immediate transition if the Duty Cycle register is written with a new value, PDCNEW, at a point of time when the PWM time base is counting a value that is in between PDCNEW and PDCOLD. Additionally, writing to the Duty Cycle register, close to the instant of time where dead time is being applied, may result in a reduced dead time which is effective on the PWMxH and PWMxL transition edges.

In Figure 1, if the duty cycle write occurred in the shaded box, then PWMxH and PWMxL will make an immediate transition without dead time.

FIGURE 1: TIMING DIAGRAMS FOR CENTER-ALIGNED AND EDGE-ALIGNED MODES



Work around

None.

In most applications, the duty cycle update timing can be controlled using the TRIGx trigger, or Special Event Trigger, such that the above mentioned conditions are avoided altogether.

Affected Silicon Revisions

A0	A1	A2					
X	X	X					

7. Module: PWM

Under certain circumstances, an update to the IOCONx register to turn off the override will be ignored by the PWMx module. The issue has been observed to occur when the IOCONx update to turn off the override occurs close to the time when dead time is being applied.

Work around

1. Turn off the PWM dead time.
2. Alternatively, turn off the PWM override with the following procedure:
   a) Disable the PWMx module (PTEN = 0)
   b) Clear the Override Enable bits (OVRENH = 0 and OVRENL = 0)
   c) Enable the PWMx module (PTEN = 1)

Affected Silicon Revisions

A0	A1	A2					
X	X	—					

8. Module: PWM

This issue is applicable when a PWM generator is configured to operate in Independent Time Base mode with either Center-Aligned Complementary mode or Edge-Aligned Complementary mode. When dead time is non-zero, PWMxL is not asserted for 100% of the time when PDCx is zero. Similarly, when dead time is non-zero, PWMxH is not asserted for 100% of the time when PDCx is equal to PHASEx. This issue also applies to Master Time Base mode.

Work around

In Center-Aligned mode:

- To obtain 0% duty cycle, zero out the ALTDTRx register and then write zero to the PDCx register.
- To obtain 100% duty cycle, zero out the ALTDTRx register and then write (PHASEx + 2) to the PDCx register.

In Edge-Aligned mode:

- To obtain 0% duty cycle, zero out the registers, DTRx and ALTDTRx, and then write zero to the PDCx register.
- To obtain 100% duty cycle, zero out the registers, DTRx and ALTDTRx, and then write (PHASEx + 1) to the PDCx register.

Alternatively, in both Center-Aligned and Edge-Aligned PWM modes, 0% and 100% duty cycle can be obtained by enabling the PWM override (IOCONx<9:8> = 0b11) with the Output Override Synchronization bit (IOCONx<0> = 1) set:

- For 0% duty cycle, set the value of the Override Data (IOCONx<7:6>) for the PWMxH and PWMxL pins as '0b01'
- For 100% duty cycle, set the value of the Override Data (IOCONx<7:6>) for the PWMxH and PWMxL pins as '0b10'

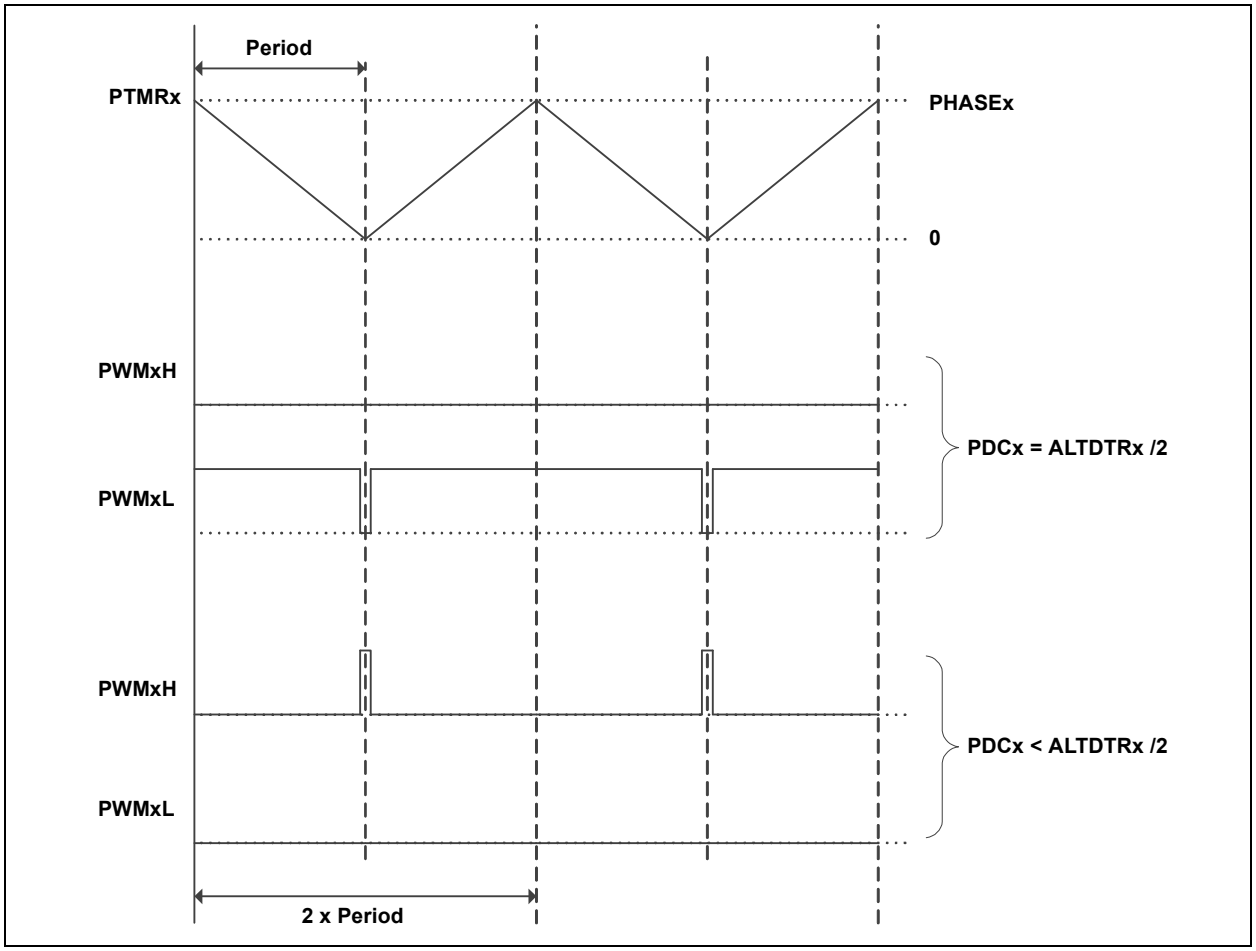
Affected Silicon Revisions

A0	A1	A2					
X	X	X					

9. Module: PWM

In Center-Aligned Complementary mode with Independent Time Base, if the value in the PDCx register is less than one-half the value in the ALTDTRx register, the PWM generator will force the PWMxL to low, and on the PWMxH, generates pulses of a width less than twice the dead time, as shown in Figure 2.

FIGURE 2: PWM GENERATOR TIMING DIAGRAM



Work around

Include a software routine to ensure that the duty cycle value written to the PDCx register is at least one-half of the value in ALTDTRx. Example 1 shows one method, with PDCtemp representing the variable which has the value to be written to the PDCx register. Alternatively, for duty cycle values less than half the desired dead-time value, zero out the ALTDTRx register or dynamically reduce the value in the ALTDTRx register, such that ALTDTRx is always equal to 2 * PDCx, as shown in Example 2.

EXAMPLE 1: WORK AROUND CODE

```
Altdtr_by2 = ALTDTRx / 2;
if (PDCtemp < Altdtr_by2)
{
PDCx = Altdtr_by2;
}
else
{
PDCx = PDCtemp;
}
```

EXAMPLE 2: WORK AROUND CODE

```
#define DESIRED_DEADTIME 100
if (PDCtemp < (DESIRED_DEADTIME/2))
{
ALTDTRx = PDCtemp * 2;
PDCx = PDCtemp;
}
else
{
ALTDTRx = DESIRED_DEADTIME;
PDCx = PDCtemp;
}
```

Affected Silicon Revisions

A0	A1	A2					
X	X	X					

10. Module: PWM

When the PWM generator is configured to operate in Current Reset mode (XPRES (PWMCONx<1>) = 1 with Independent Time Base mode (ITB (PWMCONx<9>) = 1), the PWM Reset will happen only in every alternate PWM cycle.

Work around

1. Generate an interrupt when the comparator state changes. This interrupt should be high priority and could be either a comparator interrupt or PWM Fault interrupt. The current-limit interrupt does not function in this mode. Inside the interrupt, update PHASEx (period value) with a value less than the programmed duty cycle and then immediately update the PHASEx register with the value, as required by the application (PWM_period) shown in Example 3.

EXAMPLE 3: WORK AROUND CODE

```
PWMx ISR:
{
PHASEx = PDCx - 100;
PHASEx = PWM_period;
PWMxIF =0;
}
```

2. When the External Current Reset signal is applied to the PWM generator (configured using Current-Limit Signal Source Select bits (CLSRC<4:0>) in the PWM Fault Current-Limit Control registers (FCLCONx<14:10>)), depending on the PWM resolution selected, PCLKDIV<2:0> (PTCON2<2:0>), the maximum pulse width of the External Current Reset signal is to be restricted to less than the values as shown in Table 3.

TABLE 3: MAXIMUM EXTERNAL CURRENT RESET SIGNAL WIDTH

PCLKDIV<2:0>	Max. External Current Reset Signal Width (in nS)
000	20
001	40
010	80
011	160
100	320
101	640
110	1280

Affected Silicon Revisions

A0	A1	A2					
X	X	X					

11. Module: PWM

In Edge-Aligned Complementary mode, changes to the PHASEx register under certain circumstances will result in missing dead time at the PWMxH-to-PWMxL transition. This has been observed only when all of the following are true:

- Master Time Base mode is enabled (PWMCONx<9> = 0);
- PHASEx is changed after the PWMx module is enabled; and
- The PHASEx register value is changed, so that either PHASEx < DTRx or PHASEx > PDCx.

Work around

None.

Affected Silicon Revisions

A0	A1	A2					
X	X	X					

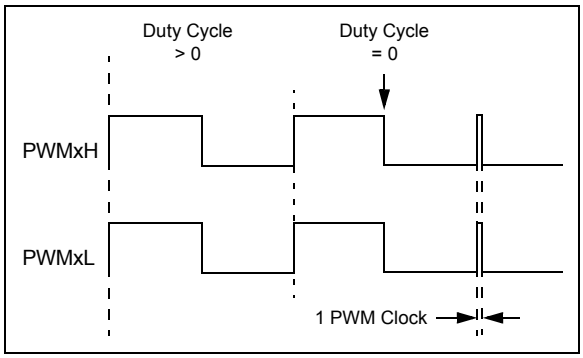
12. Module: PWM

In certain output modes, the PWMx module produces a pulse glitch of one PWM clock in width (Figure 3). This has been observed only when all of the following are true:

- Either Redundant or Push-Pull Output mode is selected (IOCONx<11:10> = 10 or 01);
- Immediate Update is disabled (PWMCONx<0> = 0); and
- The value of the current Duty Cycle register (either the PDCx or MDC register, as determined by PWMCONx<8>) is updated to zero from any non-zero value.

The pulse glitch has been observed to occur at the beginning of the following PWM boundary period.

FIGURE 3:



Work around

If the application requires a duty cycle of zero, two possible work arounds are available.

1. Use the PWM overrides to force the output to a low state, instead of writing a '0' to the Duty Cycle register. When using this method, the PWM override must be disabled when the duty cycle is a non-zero value. If output override synchronization is configured to occur on CPU clock boundaries (IOCONx<0> = 0), enabling and disabling the override must be timed to occur as closely as possible to the PWM period boundary.
2. Configure the module for Immediate Update (PWMCONx<0> = 1) *before* enabling the module. In this mode, writes to the Duty Cycle register have an immediate effect on the output. As with the previous work around, writes to the Duty Cycle register must be timed to occur as close to the PWM period boundary as possible in order to avoid distortion of the output.

Affected Silicon Revisions

A0	A1	A2					
X	X	X					

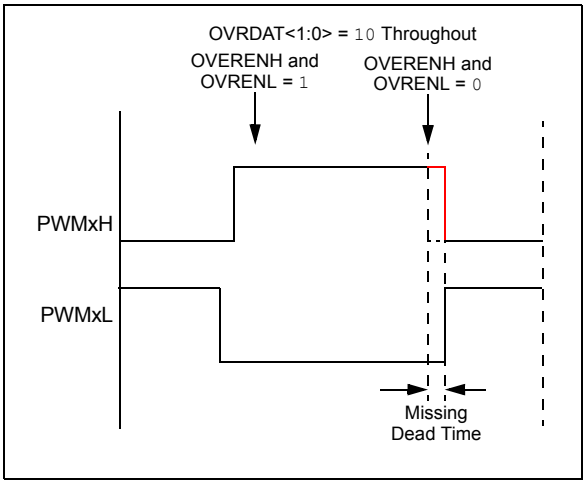
13. Module: PWM

In Complementary Output mode, the expected dead time between transitions of the PWMxH and PWMxL outputs may not be asserted when the following occurs:

- Output override synchronization is configured to occur on the CPU clock boundary (IOCONx<0> = 0);
- Both PWMxH and PWMxL overrides are enabled prior to the event (OVRENH and OVRENL are both '1'), and
- Both overrides are disabled (OVRENH and OVRENL are both '0') at the instant the dead time should be asserted (Figure 4).

This has been observed in both Center-Aligned and Edge-Aligned modes.

FIGURE 4:



Work around

None.

Affected Silicon Revisions

A0	A1	A2					
X	X	X					

14. Module: ADC

The ADC Conversion Status (DONE) bit (ADxCON1<0>) does not indicate completion of a conversion when an external interrupt is selected as the ADC trigger source (SSRC<2:0> bits (ADxCON1<7:5>) = 0x1).

Work around

Use an ADC interrupt or poll the ADxIF bit in the IFSx registers to determine the completion of the conversion.

Affected Silicon Revisions

A0	A1	A2					
X	X	X					

15. Module: ADC

Selecting the same ANx input (AN0 or AN3) for CH0 and CH1 to achieve a 1.1 Msps sampling rate results in erroneous readings for CH1.

Work around

Bring the analog signal into the device using both AN0 and AN3, connect externally, and then assign one input to CH0 and the other to CH1.

If selecting AN0 on CH1 (CH123Sx = 0), select AN3 on CH0 (CH0Sx = 3). Conversely, if selecting AN3 on CH1 (CH123Sx = 1), select AN0 on CH0 (CH0Sx = 0).

Affected Silicon Revisions

A0	A1	A2					
X	X	X					

16. Module: CAN

When DMA is used with the CAN module, and the CPU and DMA write to a CAN Special Function Register (SFR) at the same time, the DMAC error trap does not occur. In addition, neither the PWCOL<3:0> bits of the DMAPWC SFR nor the DMACERR bit of the INTCON1 SFR become set. Since the PWCOLx bits are not set, subsequent DMA requests to that channel are not ignored.

Work around

There is no work around; however, under normal circumstances, this situation must not arise. When DMA is used with the CAN module, the application must not be writing to the CAN SFRs.

Affected Silicon Revisions

A0	A1	A2					
X	X	X					

17. Module: JTAG

The $\overline{\text{MCLR}}$ pin (normally input only) may be set as an output pin through the JTAG interface. If it is set at an output high level, subsequent device Resets are prevented until the device is powered down.

Work around

None.

Affected Silicon Revisions

A0	A1	A2					
X	X	X					

18. Module: JTAG

At Power-on Reset (POR), when JTAG is disabled in the Configuration bits, the I/O pin with TMS function produces an active-high logic pulse with a pulse width in the order of milliseconds.

Work around

None.

Affected Silicon Revisions

A0	A1	A2					
X	X	X					

19. Module: QEI

The Velocity Counter x (VELxCNT) is a 16-bit wide register that increments or decrements based on the signal from the quadrature decoder logic. Reading this register results in a Counter Reset. Typically, the user application must read the velocity counter at a rate of 1 kHz-4 kHz.

As a result of this issue, the velocity counter may miss a count if the user application reads the Velocity Counter x register at the same time as a (+1 or -1) count increment occurs.

Work around

None.

Affected Silicon Revisions

A0	A1	A2					
X	X	X					

20. Module: FRC

Refer to Table 4 for a change in the FRC accuracy at FRC Frequency = 7.3728 MHz.

TABLE 4: INTERNAL FRC ACCURACY

AC CHARACTERISTICS		Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended -40°C ≤ TA ≤ +150°C for High Temperature					
Param No.	**Characteristic**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**	
Internal FRC Accuracy @ FRC Frequency = 7.3728 MHz							
F20a	FRC	-2	0.5	2	%	-40°C ≤ TA ≤ +85°C	VDD = 3.0-3.6V
F20b	FRC	-3	1.5	3	%	-40°C ≤ TA ≤ +125°C	VDD = 3.0-3.6V
HF20	FRC	-4	—	4	%	-40°C ≤ TA ≤ +150°C	VDD = 3.0-3.6V

Work around

None.

Affected Silicon Revisions

A0	A1	A2					
X							

21. Module: Op Amp

When operating at lower temperatures (< 0°C), there is a drift in the op amp offset voltage. Refer to Table 5 for a change in the op amp offset voltage at different operating temperatures.

TABLE 5: OP AMP SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	**Symbol**	**Characteristic**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
CM42	VOFFSET	Op Amp Offset Voltage	—	±20	±70	mV	0°C ≤ TA ≤ +125°C
CM42	VOFFSET	Op Amp Offset Voltage	—	—	±500	mV	-40°C ≤ TA < 0°C

Work around

None.

Affected Silicon Revisions

A0	A1	A2					
X	X	X					

22. Module: CPU

When using the signed 32-by-16-bit division instruction, `div.sd`, the Overflow bit does not always get set when an overflow occurs.

Work around

Test for and handle overflow conditions outside of the `div.sd` instruction.

Affected Silicon Revisions

A0	A1	A2					
X	X	X					

23. Module: Output Compare

The first PWM pulse may not appear on the OCx pin if the timer source of the Output Compare x module is scaled down.

The first pulse on the OCx pin is missed in PWM mode when the timer source for the Output Compare x module is scaled down (1:8, 1:64 or 1:256) using the Timerx Input Clock Prescale Select bits, TCKPS<1:0> (TxCON<5:4>).

Work around

- Configure the prescaler for the source timer to 1:1 for Output Compare 3, 4, 5 and 6.
- The Output Compare 1 or 2 module can be used. The scaled down timer (1:8, 1:64 or 1:256) can be used as a source for the Output Compare 1 and 2 modules.

Affected Silicon Revisions

A0	A1	A2					
X	X	X					

24. Module: Output Compare

Under certain circumstances, an output compare match may cause the Output Compare Interrupt Flag (OCxIF) bit to become set prior to the Change-of-State (COS) of the OCx pin. This has been observed when all of the following are true:

- The module is in One-Shot mode (OCM<2:0> = `001`, `010` or `100`);
- One of the timer modules is being used as the time base; and
- A timer prescaler other than 1:1 is selected

If the module is re-initialized by clearing the OCM<2:0> bits after the One-Shot mode compare, the OCx pin may not be driven as expected.

Work around

After OCxIF is set, allow an interval (in CPU cycles) of at least twice the prescaler factor to elapse before clearing the OCM<2:0> bits. For example, for a prescaler value of 1:8, allow 16 CPU cycles to elapse after the interrupt.

Affected Silicon Revisions

A0	A1	A2					
X	X	X					

25. Module: CPU

Table Write (`TBLWTL`, `TBLWTH`) instructions cannot be the first or last instruction of a `DO` loop.

Work around

None.

Affected Silicon Revisions

A0	A1	A2					
X	X	X					

26. Module: PWM

In Center-Aligned Complementary mode with Independent Time Base, the expected dead time between transitions of the PWMxH and PWMxL outputs may not be asserted at all times if the SWAP (IOCONx<1>) bit setting is changed from '`1`' to '`0`' in order to remap PWMxH and PWMxL to their respective pins, after the PWM module is enabled.

Work around

None.

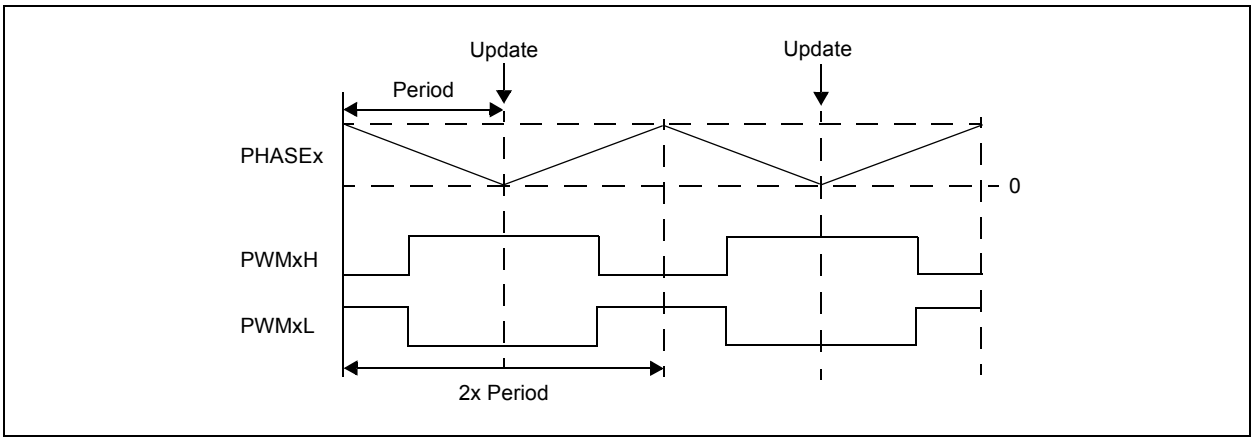
Affected Silicon Revisions

A0	A1	A2					
X	X	X					

27. Module: PWM

In Center-Aligned Complementary mode with Independent Time Base, updates to the PHASEx register take effect in the middle of a Center-Aligned PWM cycle, as shown in Figure 5. This occurs only when the Immediate Update feature is disabled (IUE = 0). If Immediate Update is enabled (IUE = 1), the PHASEx register updates will take effect immediately.

FIGURE 5:



Work around

None.

Affected Silicon Revisions

A0	A1	A2					
X	X	X					

28. Module: ADC

In the AC/DC electrical characteristics, the Integral Nonlinearity (INL) error for the ADC2 module differs in 12-Bit ADC mode with the operating temperature range from the specifications published in the *"dsPIC33EPXXXGM3XX/6XX/7XX Family Data Sheet"*. The updated text is shown in **bold** in Table 33-57 below:

TABLE 33-57: ADCx MODULE SPECIFICATIONS (12-BIT MODE)

AC CHARACTERISTICS			Standard Operating Conditions (see Note 1): 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	Symbol	Characteristic	Min.	Typ.	Max.	Units	Conditions
ADC Accuracy (12-Bit Mode) – VREF-							
AD20a	Nr	Resolution	12 data bits			bits	
AD21a	INL	Integral Nonlinearity	**-3.0**	—	**+3.0**	LSb	**-40°C ≤ TA ≤ +85°C Only** VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.6V (Note 2)
			-6.0	**—**	**6.0**	LSb	**+85°C ≤ TA ≤ +125°C Only** VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.6V (Note 2)

Work around

None.

Affected Silicon Revisions

A0	A1	A2					
X	X	X					

Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS70000689**D**):

Note:	Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

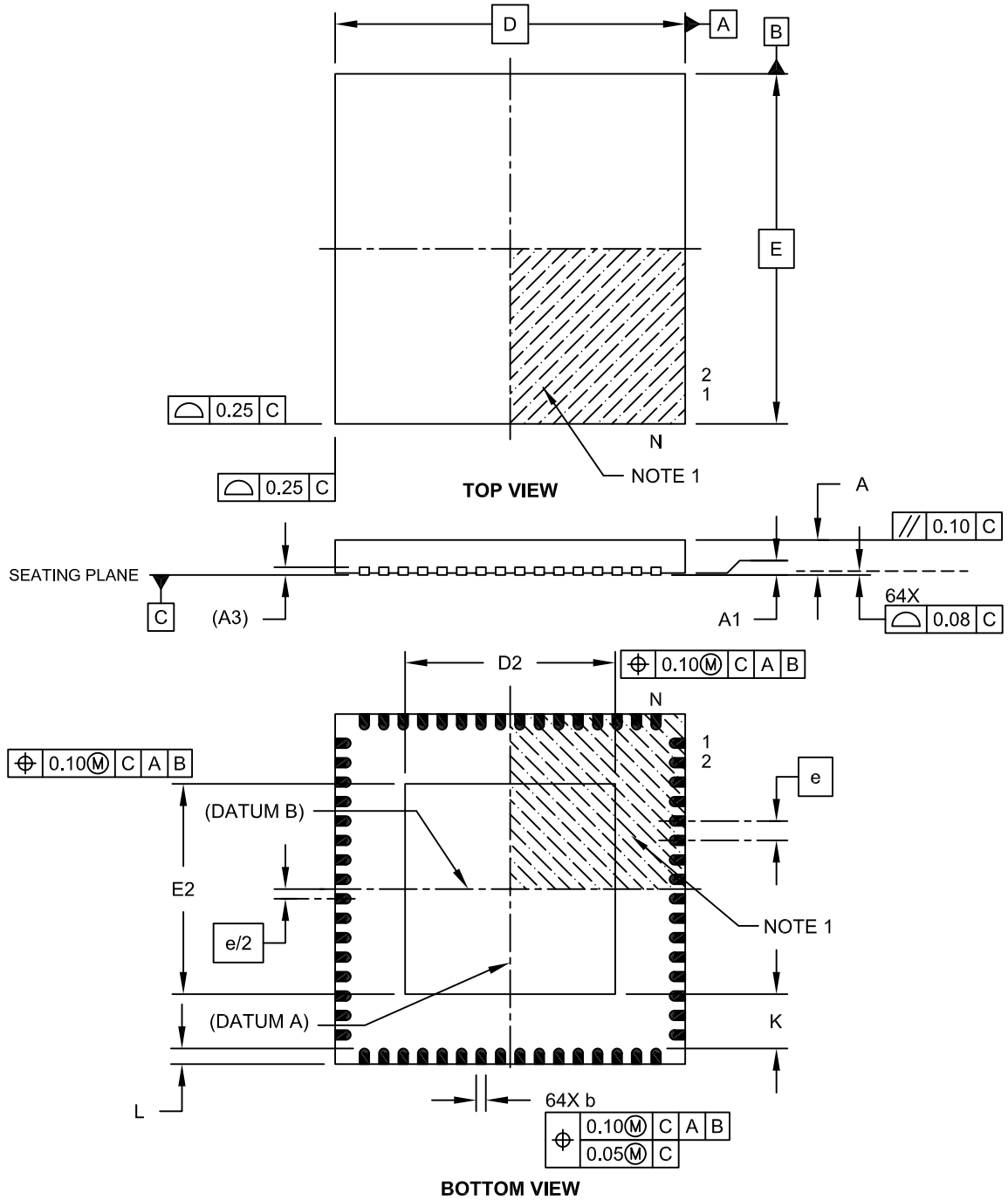
1. Module: Packaging Information

In the *"dsPIC33EPXXXGM3XX/6XX/7XXFamily Data Sheet"*, **Section 35.2 "Package Details"**, dimensions for the 64-Lead Plastic Quad Flat, No Lead Package (MR) - 9x9x0.9 mm Body with 7.15 x 7.15 Exposed Pad [QFN] is mentioned. However, the dsPIC33EPXXXGM3XX/6XX/7XX family devices are not available in this package.

The dsPIC33EPXXXGM3XX/6XX/7XX family devices are available in the 64-Lead Plastic Quad Flat, No Lead Package (MR) – 9x9x0.9 mm Body with 5.40 x 5.40 Exposed Pad [QFN], and the package dimensions are shown on the following pages.

64-Lead Plastic Quad Flat, No Lead Package (MR) – 9x9x0.9 mm Body with 5.40 x 5.40 Exposed Pad [QFN]

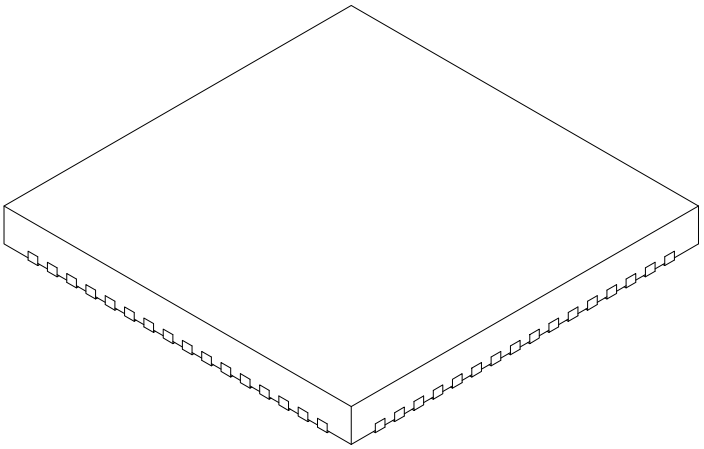
Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-154A Sheet 1 of 2

64-Lead Plastic Quad Flat, No Lead Package (MR) – 9x9x0.9 mm Body with 5.40 x 5.40 Exposed Pad [QFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		64	
Pitch	e		0.50 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3		0.20 REF	
Overall Width	E		9.00 BSC	
Exposed Pad Width	E2	5.30	5.40	5.50
Overall Length	D		9.00 BSC	
Exposed Pad Length	D2	5.30	5.40	5.50
Contact Width	b	0.20	0.25	0.30
Contact Length	L	0.30	0.40	0.50
Contact-to-Exposed Pad	K	0.20	-	-

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated.
3. Dimensioning and tolerancing per ASME Y14.5M.

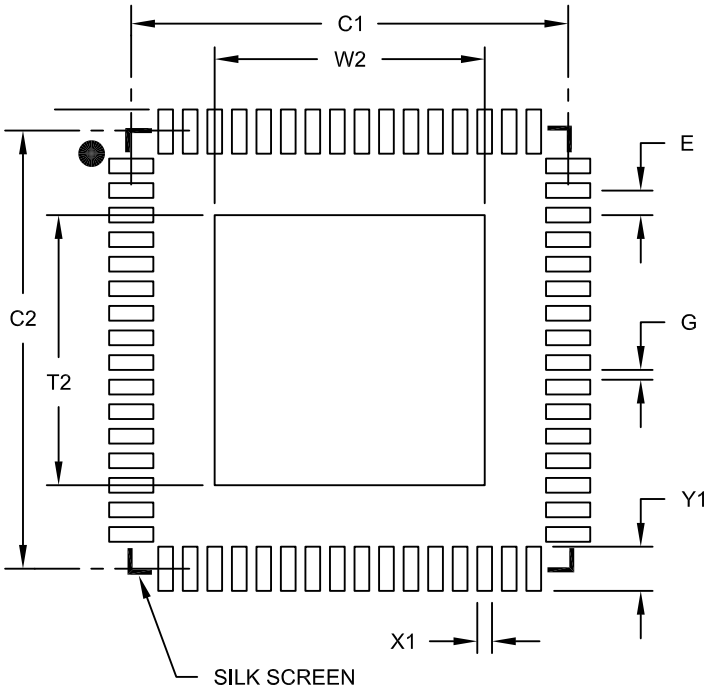
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-154A Sheet 2 of 2

64-Lead Plastic Quad Flat, No Lead Package (MR) – 9x9x0.9 mm Body [QFN]
With 0.40 mm Contact Length and 5.40x5.40mm Exposed Pad

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Optional Center Pad Width	W2			5.50
Optional Center Pad Length	T2			5.50
Contact Pad Spacing	C1		8.90	
Contact Pad Spacing	C2		8.90	
Contact Pad Width (X64)	X1			0.30
Contact Pad Length (X64)	Y1			0.85
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2154A

2. Module: Power-Saving Features

In **Section 10.0 "Power-Saving Features"**, there are two changes included.

Change 1: Example 10-1 is modified to show a condition and a note. The changes are shown below in **bold**.

EXAMPLE 10-1: PWRSAV INSTRUCTION SYNTAX

```
PWRSAV  #IDLE_MODE     ; Put the device into Idle mode
PWRSAV  #SLEEP_MODE    ; Put the device into Sleep mode(1)
```

Note 1: The use of PWRSV #SLEEP_MODE has limitations when the Flash Voltage Regulator bit, VREGSF (RCON<11>), is set to Standby mode. Refer to Section 10.2.1 "Sleep Mode" for more information.

Change 2: The fourth paragraph of **Section 10.2.1 "Sleep Mode"** is modified to include the condition where the Flash voltage regulator is placed in Standby mode. An additional example is added to show how to implement the SLEEP instruction in a 4-instruction word-aligned function. The modified text is added as follows:

For optimal power savings, the internal regulator and the Flash regulator can be configured to go into standby when Sleep mode is entered by clearing the VREGS (RCON<8>) and VREGSF (RCON<11>) bits (default configuration). However, putting the Flash Voltage Regulator in Standby mode (VREGSF = 0) when in Sleep has the effect of corrupting the prefetched instructions placed in the instruction queue. When the part wakes up, these instructions may cause undefined behavior. To remove this problem, the instruction queue must be flushed after the part wakes up. A way to flush the instruction queue is to perform a branch. Therefore, it is required to implement the SLEEP instruction in a function with 4-instruction word alignment. The 4-instruction word alignment will assure that the SLEEP instruction is always placed on the correct address to make sure the flushing will be effective. Example 10-2 shows how this is performed.

EXAMPLE 10-2: SLEEP MODE PWRSAV INSTRUCTION SYNTAX (WITH FLASH VOLTAGE REGULATOR SET TO STANDBY MODE)

```
.global     _GoToSleep
.section    .text
.align      4

_GoToSleep:

PWRSAV  #SLEEP_MODE
BRA     TO_FLUSH_QUEUE_LABEL
TO_FLUSH_QUEUE_LABEL:
RETURN
```

APPENDIX A: DOCUMENT REVISION HISTORY

Rev A Document (6/2013)

Initial release of this document; issued for silicon revision A0.

Includes silicon issues 1 (Core, CPU), 2 (Core, Program Memory), 3-4 (SPI, Frame modes), 5 (Input Capture), 6-10 (PWM), 11-12 (ADC), 13 (ECAN), 14-15 (JTAG), and 16 (QEI).

Rev B Document (9/2013)

Adds silicon issue **20. Module: "FRC"** and updates Table 2. Adds a new bulleted list in silicon issue **20. Module: "FRC"**. Updates work around section in silicon issue **20. Module: "FRC"**.

Rev C Document (10/2013)

Updates Table 1 with new revision ID, "A1". Updates Table 2.

Rev D Document (11/2013)

Adds silicon issue **21. Module: "Op Amp"** and updates Table 2.

Rev E Document (6/2014)

Replaced silicon issue **9. Module: "PWM"**. Adds silicon issue **10. Module: "PWM"**, **11. Module: "PWM"**, **12. Module: "PWM"**, **13. Module: "PWM"** and updates Table 2.

Rev F Document (9/2014)

Updates Table 1 with new revision ID, "A2". Updates Table 2 and Table 3. Adds silicon issues **22. Module: "CPU"**, **23. Module: "Output Compare"**, **24. Module: "Output Compare"**. Replaces silicon issue **6. Module: "PWM"**.

Adds data sheet clarification **1. Module: "Packaging Information"**.

Rev G Document (12/2014)

Updates the silicon issue description of **7. Module: "PWM"**, **10. Module: "PWM"**, **11. Module: "PWM"**, **12. Module: "PWM"** and **13. Module: "PWM"**. Basic issue is unchanged.

Adds new silicon issues **25. Module: "CPU"**, **26. Module: "PWM"**, **27. Module: "PWM"** and **28. Module: "ADC"**.

Adds data sheet clarification **2. Module: "Power-Saving Features"**.

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