# DAWEI XIONG (DAVID)

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## EDUCATION

**University of Illinois at Urbana-Champaign** *Aug. 2020 – Present*
*Bachelor of Computer Science —Minor in Electrical Engineering— Technical GPA: 3.70/4.0*
**Relevant coursework:** Computer Architecture, VLSI Design, Digital Signal Lab (FPGA), Embedded System, Operating System, Analog/Digital Signal Progressing
**Language:** English, Mandarin, Japanese (elementary)

## PROJECTS

**A bit-sliced RISC-V32I compliant single-cycle processor(Cadence Virtuoso Layout Suite)** *Jan 2024 - Now*
- Independently designed schematic and physical layout of a single-cycle RISC-V32I processor using Cadence Virtuoso, starting from fundamental arithmetic cells, latches, and D-type flip-flops. Implemented source/drain merging to minimize area and adhered to transistor sizing rules.
- Verified functionality through Design Rule Checking (DRC) and Layout vs Schematic (LVS) checking.

**Optimized Forward Propogation Neural Layer(CUDA)** *April. 2023 - May. 2023*
- Implemented the kernel function using parallel programming techniques including shared tiled memory, constant memory, loop unrolling etc to increase the training of a image classification problem then adjust parameters for further improvement.
- Used Nvidia Nsight-Systems and Nsight-compute to generate profiling result of the algorithm, evaluate the improvement of algorithm based on performance metrics of the kernel function and each layer.

**A Distributed Machine Learning Platform(Python)** *Aug. 2022 - Dec. 2022*
- Developed a simplified distributed file system (SDFS) based on a Gossip-style failure detection mechanism, supporting up to three simultaneous machine failures and scalable with an increasing number of servers.
- Implemented functionality to perform inference on MobileNet and MNIST models by fetching queries from SDFS and writing inference results back to the system.
- Introduced a Round Robin Scheduling algorithm to ensure fair time inference, achieving consistent query processing rates for different jobs within 20% of each other, regardless of user-specified hyperparameters such as batch size.

## RESEARCH EXPERIENCE

**ARCANA(Architechs Reimaging Computing Around New Applications)** *Sep. 2022 - Present*
- Proposed the use of Triple Modular Redundancy (TMR) as an error correction scheme in Process-in-Memory architecture based on off-the-shelf DRAM, utilizing the *Ramulator 2.0* DRAM simulator to verify feasibility under DDR5. Results indicate that TMR effectively reduces errors induced by DRAM.
- Contributed to the design of a simulator for a novel Process-in-Memory Architecture based on ReRAM, focusing on in-memory micro-arithmetic operation design and verification of Memory Processing Unit (MPU) functionalities. Introduced *SST-Merlin*, a Network on Chip (NoC) topology tool, to simulate inter-MPU communication and enhance the scalability of our design.
- Led the integration of the *Structural Simulation Toolkit (SST)* with our simulator to achieve enhanced cycle-accurate simulations, enabling manipulation of parameters such as bandwidth and link latency. Independently authored comprehensive SST integration guides for fellow researchers. Initial simulation results demonstrate that our architectural design can significantly reduce energy consumption by an order of magnitude.

## EXTRA-CURRICULAR

**RoboMaster Co-leader of the embedded development Team (C++/C/STM32)** *Aug. 2020 - Present*
- 2nd Place in RoboMaster University League North American 1v1 and 3v3 Confrontation Contest.
- Integrated chassis control algorithms for own designed standard robot based on Mecanum wheel and steering wheel using C++ and HAL functions based on STM32 board.
- Applied the AHRS algorithm to the IMU embedded in the STM32 developing board for data fusion to calculate the precise position of the gimbal.