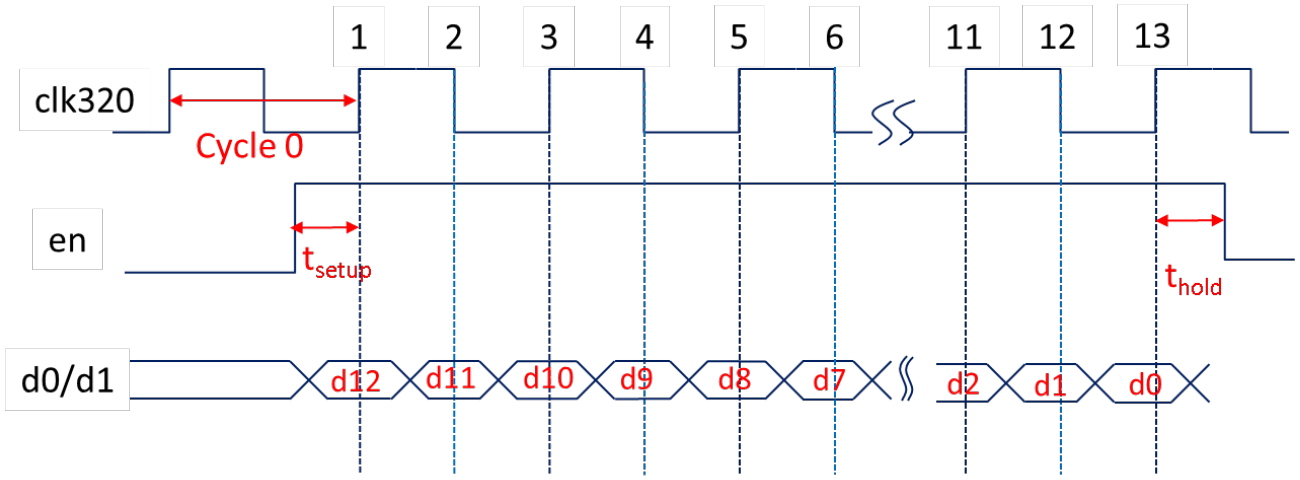
Interface between pad-trigger logic and the strip-TDS

- Source synchronization with a DDR clock (clk320 MHz) and data enable (en);
- Data line (d0 and d1) rate is: 640 Mbps;
- d0 is for BCID (12 bits), d1 is for Band-phi ID (13 bits), MSB coming out first.

The timing diagram of the protocol is shown as follows:



BCID: d[12:1]; Band_phi_ID: d[12:0]

For the above timing diagram:

1) The first bit is captured at rising edge of clk320 after “en” becomes valid.
2) A total of 13 bits (d[12:0]) will be captured via dual edges of clk320.
3) There is flexibility on width of “en”: “en” can starts valid at any time in “Cycle 0” as long as the setup time (t_{setup}) is meet; “en” can also extend until the rising edge following edge 13, but it should stay valid for at least the time of t_{hold}.

The interface inside TDS will capture the corresponding BCID and Band-phi ID from the two lines, and output this information with a trigger request.