I2C addr.	R/W	Size (byte)	Memory addr.	Bit Map
0	R/W	4	bit[31 : 0]	[31 : 20] BCID offset; [19 : 8] BCID rollover value; [7 : 4] BC clock phase, 6.25 ns step; 0 deg: 4'b0011; 90 deg : 4'b0110; 180 deg: 4'b1100; 270 deg: 4'b1001 [3 : 0] strip TDS matching window, from 25 ns to 50 ns, 6.25 ns step. 25 ns : 4'b0000; 31.25 ns: 4'b0001; 37.5 ns: 4'b0011; 43.75 ns: 4'b0111; 50 ns: 4'b1111;
1	R/W	2	bit[47 : 32]	[47 : 43] Phase of 160 MHz to VMM #1 [42 : 38] Phase of 160 MHz to VMM #0 [37 : 34] GBT SER PLL current set [33 : 32] GBT SER PLL low-pass filter resistor set
2	R/W	16	bit[175: 48]	[175: 48] disable set for channel #127-0 (MSB-LSB)
3	R/W	16	bit[303:176]	[190:176] strip TDS trigger road LUT 0 [206:192] strip TDS trigger road LUT 1 [222:208] strip TDS trigger road LUT 2 [238:224] strip TDS trigger road LUT 3 [254:240] strip TDS trigger road LUT 4 [270:256] strip TDS trigger road LUT 5 [286:272] strip TDS trigger road LUT 6 [302:288] strip TDS trigger road LUT 7
4	R/W	16	bit[431:304]	[318:304] strip TDS trigger road LUT 8 [334:320] strip TDS trigger road LUT 9 [350:336] strip TDS trigger road LUT a [366:352] strip TDS trigger road LUT b [382:368] strip TDS trigger road LUT c [398:384] strip TDS trigger road LUT d [414:400] strip TDS trigger road LUT e [430:416] strip TDS trigger road LUT f
5	R/W	16	bit[559:432]	[436: 432] delay for pad chnl #0 [444: 440] delay for pad chnl #1 [452: 448] delay for pad chnl #2 [460: 456] delay for pad chnl #3 [468: 464] delay for pad chnl #4 [476: 472] delay for pad chnl #5 [484: 480] delay for pad chnl #6 [492: 488] delay for pad chnl #7 [500: 496] delay for pad chnl #8 [508: 504] delay for pad chnl #9 [516: 512] delay for pad chnl #10 [524: 520] delay for pad chnl #11 [532: 528] delay for pad chnl #12 [540: 536] delay for pad chnl #13

				[548: 544] delay for pad chnl #14 [556: 552] delay for pad chnl #15
6	R/W	16	bit[687:560]	[564: 560] delay for pad chnl #16 [572: 568] delay for pad chnl #17 [580: 576] delay for pad chnl #18 [588: 584] delay for pad chnl #19 [596: 592] delay for pad chnl #20 [604: 600] delay for pad chnl #21 [612: 608] delay for pad chnl #22 [620: 616] delay for pad chnl #23 [628: 624] delay for pad chnl #24 [636: 632] delay for pad chnl #25 [644: 640] delay for pad chnl #26 [652: 648] delay for pad chnl #27 [660: 656] delay for pad chnl #28 [668: 664] delay for pad chnl #29 [676: 672] delay for pad chnl #30 [684: 680] delay for pad chnl #31
7	R/W	16	bit[815:688]	[692: 688] delay for pad chnl #32 [700: 696] delay for pad chnl #33 [708: 704] delay for pad chnl #34 [716: 712] delay for pad chnl #35 [724: 720] delay for pad chnl #36 [732: 728] delay for pad chnl #37 [740: 736] delay for pad chnl #38 [748: 744] delay for pad chnl #39 [756: 752] delay for pad chnl #40 [764: 760] delay for pad chnl #41 [772: 768] delay for pad chnl #42 [780: 776] delay for pad chnl #43 [788: 784] delay for pad chnl #44 [796: 792] delay for pad chnl #45 [804: 800] delay for pad chnl #46 [812: 808] delay for pad chnl #47
8	R/W	16	bit[943:816]	[820: 816] delay for pad chnl #48 [828: 824] delay for pad chnl #49 [836: 832] delay for pad chnl #50 [844: 840] delay for pad chnl #51 [852: 848] delay for pad chnl #52 [860: 856] delay for pad chnl #53 [868: 864] delay for pad chnl #54 [876: 872] delay for pad chnl #55 [884: 880] delay for pad chnl #56 [892: 888] delay for pad chnl #57 [900: 896] delay for pad chnl #58 [908: 904] delay for pad chnl #59 [916: 912] delay for pad chnl #60 [924: 920] delay for pad chnl #61

				[932: 928] delay for pad chnl #62 [940: 936] delay for pad chnl #63
9	R/W	16	bit[1071:944]	[948: 944] delay for pad chnl #64 [956: 952] delay for pad chnl #65 [964: 960] delay for pad chnl #66 [972: 968] delay for pad chnl #67 [980: 976] delay for pad chnl #68 [988: 984] delay for pad chnl #69 [996: 992] delay for pad chnl #70 [1004:1000] delay for pad chnl #71 [1012:1008] delay for pad chnl #72 [1020:1016] delay for pad chnl #73 [1028:1024] delay for pad chnl #74 [1036:1032] delay for pad chnl #75 [1044:1040] delay for pad chnl #76 [1052:1048] delay for pad chnl #77 [1060:1056] delay for pad chnl #78 [1068:1064] delay for pad chnl #79
10	R/W	16	bit[1199:1072]	[1076:1072] delay for pad chnl #80 [1084:1080] delay for pad chnl #81 [1092:1088] delay for pad chnl #82 [1100:1096] delay for pad chnl #83 [1108:1104] delay for pad chnl #84 [1116:1112] delay for pad chnl #85 [1124:1120] delay for pad chnl #86 [1132:1128] delay for pad chnl #87 [1140:1136] delay for pad chnl #88 [1148:1144] delay for pad chnl #89 [1156:1152] delay for pad chnl #90 [1164:1160] delay for pad chnl #91 [1172:1168] delay for pad chnl #92 [1180:1176] delay for pad chnl #93 [1188:1184] delay for pad chnl #94 [1196:1192] delay for pad chnl #95
11	R/W	8	bit[1263:1200]	[1204:1200] delay for pad chnl #96 [1212:1208] delay for pad chnl #97 [1220:1216] delay for pad chnl #98 [1228:1224] delay for pad chnl #99 [1236:1232] delay for pad chnl #100 [1244:1240] delay for pad chnl #101 [1252:1248] delay for pad chnl #102 [1260:1256] delay for pad chnl #103
12	R/W	4	bit[1295:1264]	[1271:1264] reset SER if equals 0x14 reset logic if equals 0x06 reset ePLL if equals 0x20 [1276:1272] {bypass_trigger, bypass_scrambler, test_frame2Router_enable, stripTDS_globaltest, PRBS_en }

				[1283:1280] prompt circuit: b3 :b0 [1287:1284] bypass prompt if equals 0xF [1295:1288] timer
13	R	16		8-bit CRC polynomial 0x97 for a total of 1296 bits [7 : 0] 8-bit CRC of memory bits [80: 0] [15 : 8] 8-bit CRC of memory bits [161: 81] [23 : 16] 8-bit CRC of memory bits [242: 162] [31 : 24] 8-bit CRC of memory bits [323: 243] [39 : 32] 8-bit CRC of memory bits [404: 324] [47 : 40] 8-bit CRC of memory bits [485: 405] [55 : 48] 8-bit CRC of memory bits [566: 486] [63 : 56] 8-bit CRC of memory bits [647: 567] [71 : 64] 8-bit CRC of memory bits [728: 648] [79 : 72] 8-bit CRC of memory bits [809: 729] [87 : 80] 8-bit CRC of memory bits [890: 810] [95 : 88] 8-bit CRC of memory bits [971: 891] [103: 96] 8-bit CRC of memory bits [1052: 972] [111:104] 8-bit CRC of memory bits [1133:1053] [119:112] 8-bit CRC of memory bits [1214:1134] [127:120] 8-bit CRC of memory bits [1295:1215]
14	R	6		[1 : 0] lock of SER (MSB), lock of ePLL (LSB) [26: 8] monitoring of strip TDS channel #0 [46:28] monitoring of strip TDS channel #64
15	R	4		[12: 0] strip TDS trigger BAND and Phi ID [27:16] strip TDS trigger BCID