ILLINOIS
Electrical & Computer Engineering
GRAINGER COLLEGE OF ENGINEERING

ECE 385 Lab Report 1

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Lab Section: Friday

0.1 Abstract

Te purpose of this lab is to implement a circuit which realizes a 2 to 1 multiplexer. We first use nand gate to simplify the circuit and then use a 2 * 4 kmap to help us design a cricuit which eliminates glitch/static hazard.

0.2 Documentation

K-Map We can build a kmap base on the input, here,

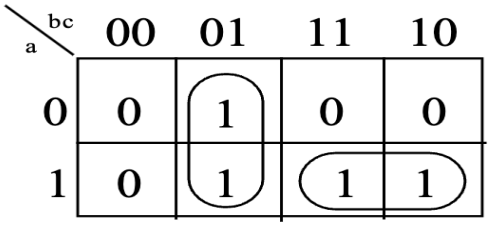


Figure 13 - Karnaugh map of 2-to-1 Multiplexer Function

Logic Equatioin We can have the logic equation,

$$Out_1 = B'C + BA$$

However, since the not gate for B will cause glitch/static hazard when input of B wire is changed, we need to add the adjacent part of the two group in order to avoid static hazard.

Logic Equatioin without static hazard We can get

$$Out_2 = AC + B'C + BA = \overline{\overline{Out_1} \wedge \overline{A}C}$$

According to SOP, we can substitute all "and" and the final "or" with nand gate.

Logic Diagram

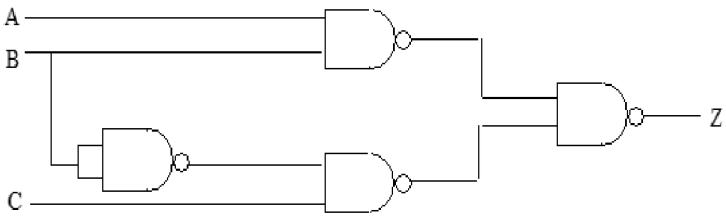


Figure 17 - Single chip implementation using one 7400 Quad 2-input NANDs.

BreadBoard View

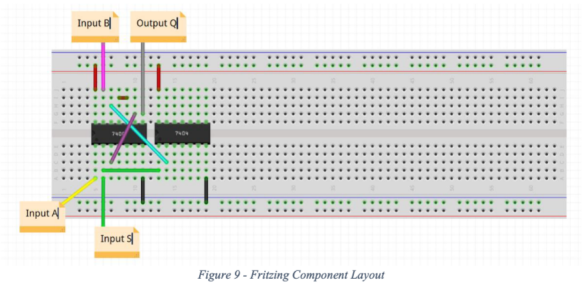


Figure 9 - Fritzing Component Layout

Logic Diagram Without Static Hazard

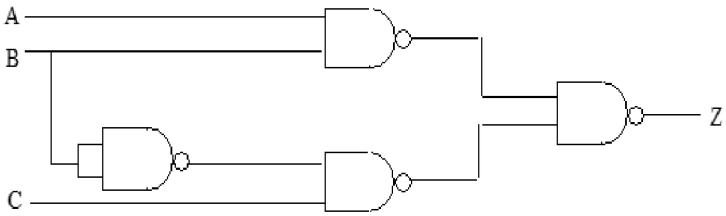
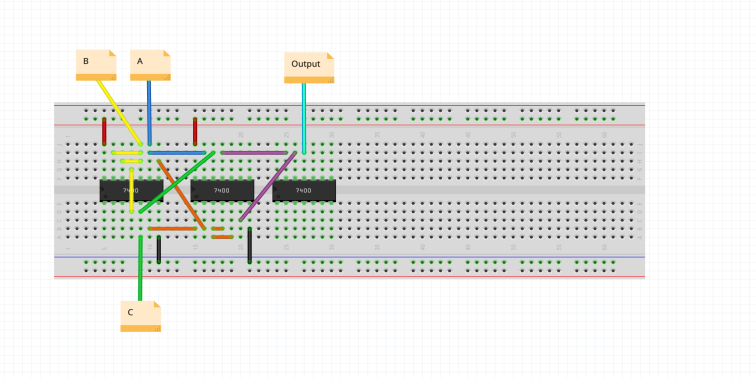
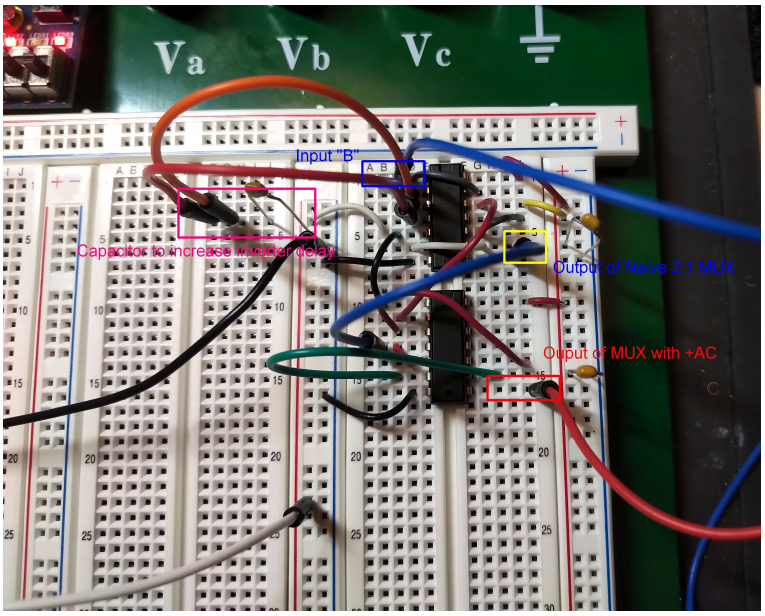


Figure 17 - Single chip implementation using one 7400 Quad 2-input NANDs.

BreadBoard View Without Static Hazard



Actual Physical Layout



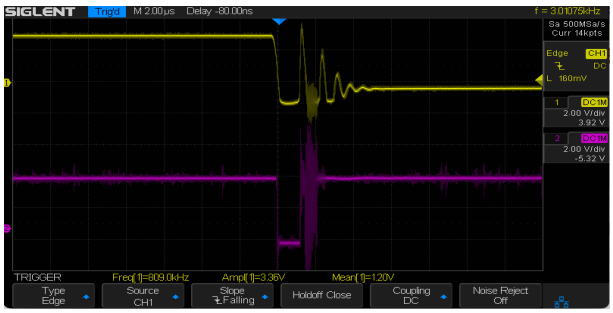
0.3 Result

I use truth table which shows the ideal output together with oscillation diagram which shows actual output on the screen. The oscillation diagram was provided by Prof. Cheng.

Truth Table

A	B	C	Z
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

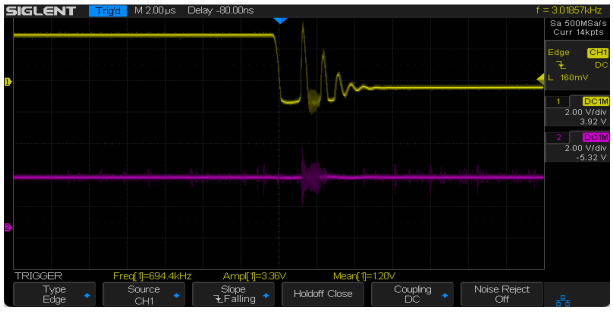
Oscillation Diagram



Truth Table Without Static Hazard

A	B	C	Z
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

Oscillation Diagram Without Static Hazard



From the diagram above, we can easily find out that adding the "extraneous" circuit protect our circuit from affecting from static hazard.

0.4 Answer Prelab Question

Not all groups may observe static hazards (why?) If you do not observe a static hazard, chain an odd number of inverters together

Because the propagation delay for single inverter is relative small. so we need to chain a number of the inverter to enlarge the delay. Odd number to ensure our desired output matches with single inverter which invert the input.

0.5 Answer Lab Question

Complete a truth table of the output. Does it respond like the circuit of part A?

From the graph, we notice the truth table are the same because they are all derived from KMap.

Describe and save the output and explain any differences between it and the results obtained in part 2.

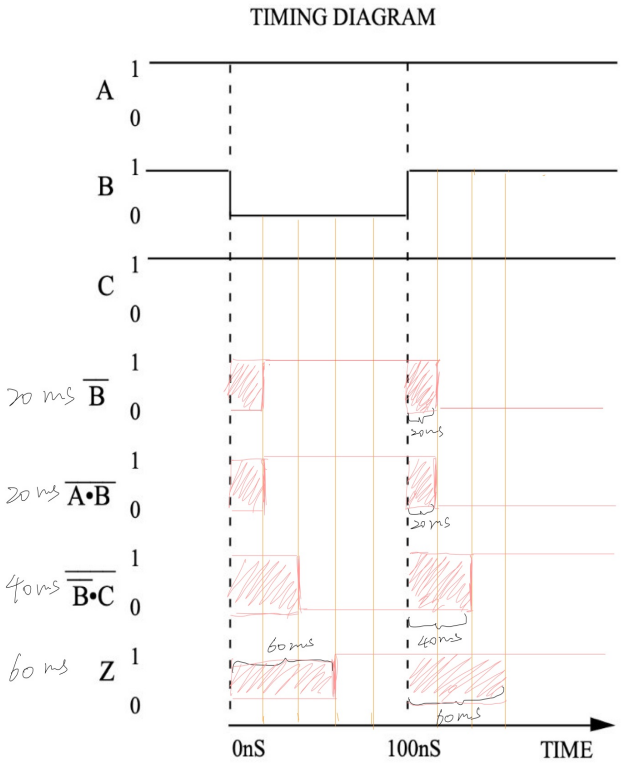
The difference is that the graph which eliminates static hazard does not have explicit drop when we change the input. The reason is, we add "extraneous" AC circuit which protect our design.

Consider the following question and explain: for the circuit of part A of the pre-lab, at which edge (rising/falling) of the input B are we more likely to observe a glitch at the output

In the falling edge. Since if we observe the rising edge with A and C both input 1. When B change from 0 to 1, The circuit output will still be 1 because the final nand will still receive two 0 input even with the propagation delay. For falling edge, when B change from 1 to 0, it will be a short time for that the final nand gate will receive two 1 input and final output will be 0.

0.6 Answer Postlab Question

Diagram



How long does it take the output Z to stabilize on the falling edge of B (in ns)? How long does it take on the rising edge (in ns)? Are there any potential glitches in the output, Z? If so, explain what makes these glitches occur

It takes 60ns for both rising and falling edge. The potensial glitch occurs in 0-60ns, the ideal output should be one, but due to the propatation delay of three nand gates, which makes the output of Z unstable, which may cause a short drop to 0.

Explain how and why the debouncer circuit given in General Guide (Figure 22) works. Specifically, what makes it behave like a switch and how the ill effect of mechanical contact bounces is eliminated?

When it connects to A, D is low, and Q is high, and G is high, so QN is low. When we switch from A to B, G gets to low immediately, no matter Q is, QN becomes high when it becomes stable. Before QN becoms stable, it maintains low, so Q is still high. Which makes the output of Q to be trustworthy when the switch is connecting to B. Avoids the bad effect causing from the switch bouceing B. Later, when QN becomes stable, QN is high, D is high, then Q is low.

0.7 General Guide Question

What is the advantage of a larger noise immunity?

It will make the circuit ore robust, for example the high/low voltage will not be easily changed to low/high voltage which will cause a logic level change.

Why is the last inverter observed rather than simply the first?

It will observe a explicit delay.

How would you calculate the noise immunity for the inverter?

If we have two or more LEDs to monitor several signals, why is it bad practice to share resistors?

If we share resistors, the only we can do is connect the LED lights in parallel, which will lower the current and lead to the inaccurate result.

0.8 Conclusion

During this lab, we have an introduction to how to use breadboard ubilding a basic circuits and use extra circuit coming from KMap to protect our cirtuict from having glitch.