OmniVision®

OV9712/OV9211 (rev 1D)

datasheet

PRODUCT SPECIFICATION

1/4" CMOS WXGA (1 megapixel) HD sensor
with OmniPixel3-HS™ technology

CMOS WXGA (1 megapixel) HD image sensor with OmniPixel3-HS™ technology

datasheet (CSP2)
PRODUCT SPECIFICATION

version 2.01
november 2013

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OmniVision Technologies is publicly traded on NASDAQ under the symbol OVTI.

applications

- cellular phones
- picture phones
- toys
- PC multimedia
- digital still cameras

features

- high sensitivity for low-light operation
- ultra low power and low cost
- automatic image control functions: automatic exposure control (AEC), automatic gain control (AGC), automatic white balance (AWB), automatic band filter (ABF), automatic black level calibration (ABLC)
- programmable controls: frame rate, AEC/AGC 16-zone size/position/weight control, mirror, flip and windowing
- image quality controls: lens correction and defective pixel canceling

- output support for raw RGB
- supports image sizes: WXGA (1280x800) and 640x400
- support for horizontal and vertical sub-sampling
- support for black sun cancellation
- standard serial camera control bus (SCCB) interface
- digital video port (DVP) parallel output interface
- embedded one-time programmable (OTP) memory
- on-chip phase lock loop (PLL)
- built-in 1.5V regulator for core

key specifications (typical)

- **active array size:** 1280 x 800
- **power supply:**
  analog: 3.0 ~ 3.6V
  core: 1.5VDC ± 5% (built-in regulator)
  I/O: 1.7 ~ 3.6V
- **power requirements:**
  active: 110 mW
  standby: 50 µA
- **temperature range:**
  operating: -30°C to 70°C junction temperature (see **table 8-2**)
  stable image: 0°C to 50°C junction temperature (see **table 8-2**)
- **output formats (10-bit):** raw RGB data
- **lens size:** 1/4"

- **lens chief ray angle:** 25° non-linear (see **figure 10-2**)
- **input clock frequency:** 6 ~ 27 MHz
- **scan mode:** progressive
- **maximum image transfer rate:**
  WXGA (1280x800): 30 fps
  640x400: 60 fps
- **sensitivity:** 3700 mV/Lux-sec
- **max S/N ratio:** 40 dB
- **dynamic range:** 69 dB @ 8x gain
- **maximum exposure interval:** 826 x t_{ROW}
- **pixel size:** 3 µm x 3 µm
- **dark current:** 20 mV/s @ 60°C junction temperature
- **image area:** 3888 µm x 2430 µm
- **package dimensions:** 5415 µm x 4415 µm

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1 signal descriptions

table 1-1 lists the signal descriptions and their corresponding pin numbers for the OV9712/OV9211 image sensor. The package information is shown in **section 9**.

table 1-1   signal descriptions (sheet 1 of 2)

pin number	signal name	pin type	description	default I/O status
A1	AVDD	power	analog power (3.0 ~ 3.6V)	
A2	AGND	ground	ground	
A3	TM	I/O	test mode input with pull-down resistor	input
A4	AVDD	power	analog power (3.0 ~ 3.6V)	
A5	AGND	ground	ground	
A6	XCLK	I/O	input clock	input
B1	VREFN	reference	reference voltage[a]	
B2	PWDN	I/O	power down input with pull-down resistor	input
B3	SIOD	I/O	SCCB data	
B4	SIOC	input	SCCB clock	
B5	VSYNC	I/O	vertical sync output	output
B6	HREF	I/O	horizontal sync output	output
C1	VREFH	reference	reference voltage[a]	
C2	Y6	I/O	DVP output bit[6]	output
C3	RSTB	I/O	reset input with pull-up resistor	input
C6	Y5	I/O	DVP output bit[5]	output
D1	Y8	I/O	DVP output bit[8]	output
D2	Y2	I/O	DVP output bit[2]	output
D3	PCLK	I/O	pixel clock output	output
D4	Y0	I/O	DVP output bit[0]	output
D5	Y3	I/O	DVP output bit[3]	output
D6	Y7	I/O	DVP output bit[7]	output
E1	DOVDD	power	power for I/O circuit (1.7 ~ 3.6V)	
E2	Y4	I/O	DVP output bit[4]	output
E3	DGND	ground	ground	

table 1-1 signal descriptions (sheet 2 of 2)

pin number	signal name	pin type	description	default I/O status
E4	Y1	I/O	DVP output bit[1]	output
E5	DVDD	power	power for digital core (1.5V)	
E6	Y9	I/O	DVP output bit[9]	output

a. should be connected to AGND using a 0.1μF capacitor

figure 1-1 pin diagram

top view
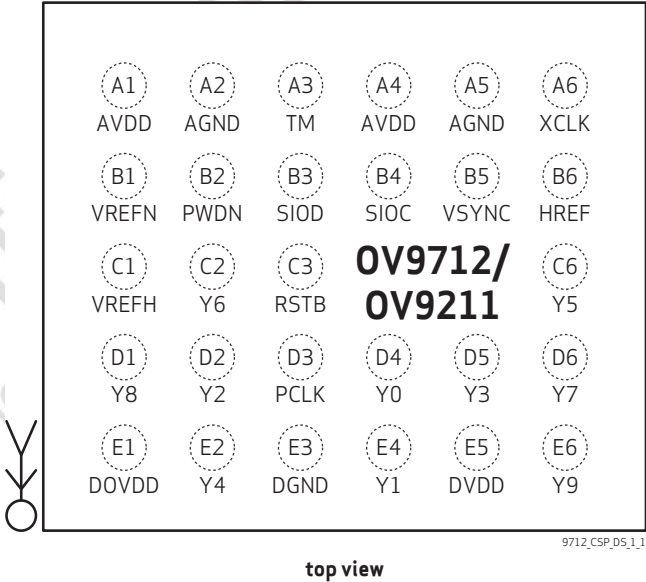
2   system level description

2.1 overview

The OV9712 (color) and the OV9211 (b&w) image sensors are low voltage and high performance quarter-inch 1 megapixel CMOS image sensor that provides the full functionality of a single-chip WXGA (1280x800) camera using OmniPixel3-HS™ technology in a small footprint package. It provides full-frame, sub-sampled, windowed 8-bit/10-bit images in raw RGB format via the digital video port (DVP).

The OV9712/OV9211 has an image array capable of operating at up to 30 frames per second (fps) in WXGA resolution with complete user control over image quality, formatting and output data transfer. All required image processing functions including exposure control, white balance, defective pixel canceling, etc., are programmable through the SCCB interface. In addition, OmniVision image sensors use proprietary sensor technology to improve image quality by reducing or eliminating common lighting/electrical sources of image contamination, such as fixed pattern noise, smearing, etc., to produce a clean, fully stable image.

The OV9712/OV9211 includes a one-time programmable (OTP) memory.

2.2 architecture

The OV9712/OV9211 sensor core generates streaming pixel data at a constant frame rate, indicated by HREF and VSYNC. Maximum pixel rate is 30 megapixels per second, corresponding to a pixel clock rate of 40~42.5 MHz. **figure 2-1** shows the functional block diagram of the OV9712/OV9211 image sensor.

The timing generator outputs clocks to access the rows of the imaging array, precharging and sampling the rows of the array sequentially. In the time between precharging and sampling a row, the charge in the pixels decreases with exposure to incident light. This is the exposure time in rolling shutter architecture.

The exposure time is controlled by adjusting the time interval between precharging and sampling. After the data of the pixels in the row has been sampled, it is processed through analog circuitry to correct the offset and multiply the data with corresponding gain. Following analog processing is the ADC which outputs a 10-bit data for each pixel in the array.

figure 2-1   OV9712/OV9211 block diagram
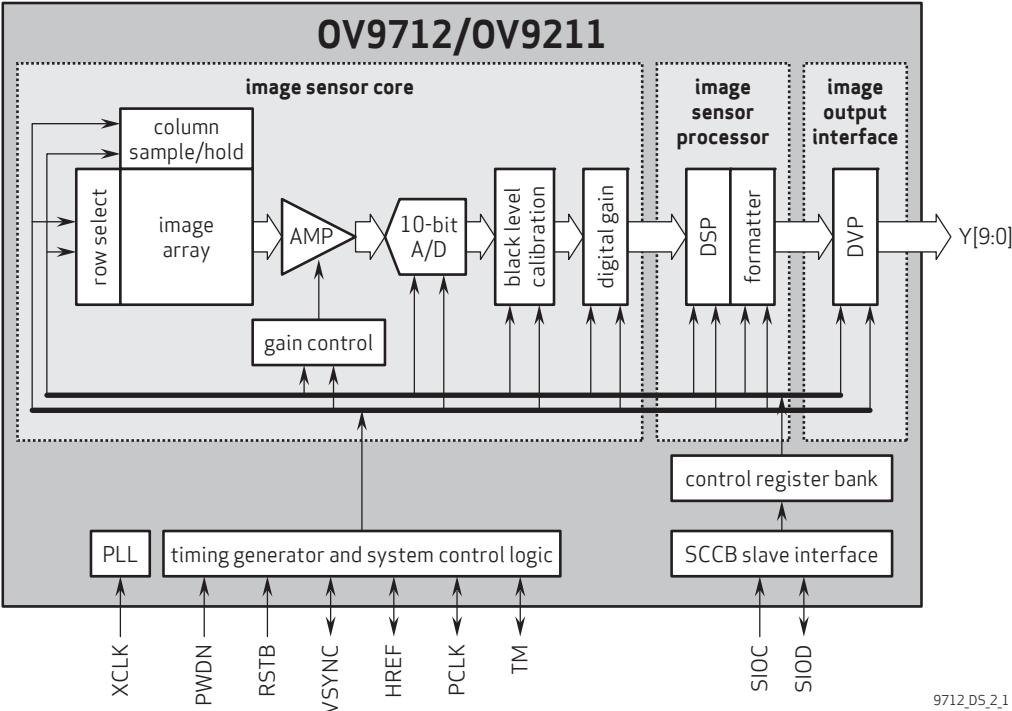
9712_DS_2_1

figure 2-2   reference design schematic
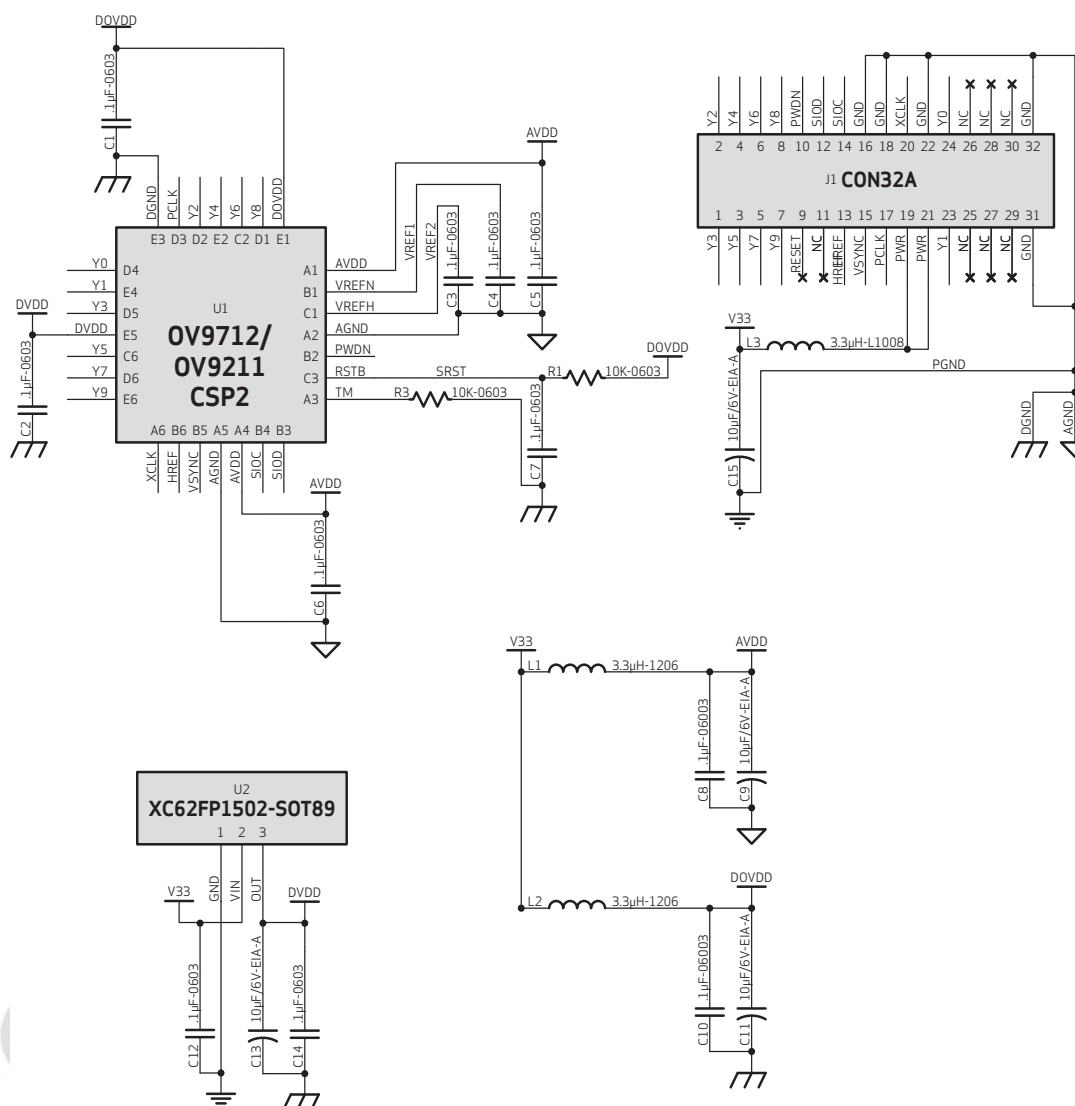
note 1 control of PWDN is required in power up and working state.

note 2 RSTB should be connected to DOVDD outside of module if unused.

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2.3 I/O control

The OV9712/OV9211 I/O pin direction and driving capability can be easily adjusted. **table 2-1** lists the driving capability and direction control registers of the I/O pins.

table 2-1   driving capability and direction control for I/O pins

function	register	description
output drive capability control	**0x5D**	Bit[5:4]: output drive capability 00: 1x 01: 2x 10: 3x 11: 4x
Y[9:0] I/O control	**0x56**[1:0], **0x55**[7:0]	input/output selection for the Y[9:0] pins: 0: input 1: output
VSYNC I/O control	**0x56**	Bit[3]: input/output selection for the VSYNC pin: 0: input 1: output
PCLK I/O control	**0x56**	Bit[2]: input/output selection for the PCLK pin: 0: input 1: output
HREF I/O control	**0x56**	Bit[4]: input/output selection for the HREF pin: 0: input 1: output

2.4 system clock control

The OV9712/OV9211 PLL allows for an input clock frequency ranging from 6~27 MHz. The PLL can be bypassed by setting register **REG5D**[6] (0x5D) to 1.

figure 2-3   system control block diagram

| REG5C[6:5] | REG5C[4:0] | REG5D[3:2] | REG11[5:0] |

XCLK → PLL pre-divider →(CLK1)→ PLL multiplier →(CLK2)→ PLL divider →(CLK3)→ system clock divider → SYSCLK
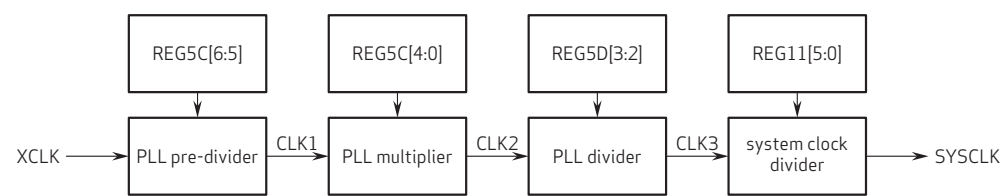
note 1 CLK1 = XCLK / PLL_pre_divider, PLL_pre_divider = REG5C[6:5] = 0X = /1, REG5C[6:5] = 10 = /2, REG5C[6:5] = 11 = /4, CLK ≥ 6 MHz

note 2 CLK2 = CLK1 × (32 - REG5C[4:0])

note 3 CLK3 = CLK2 / (REG5D[3:2] +1)

note 4 SYSCLK = CLK3 / ((REG11[5:0] +1) × 2)

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2.5 SCCB interface

The Serial Camera Control Bus (SCCB) interface controls the image sensor operation. Refer to the OmniVision Technologies Serial Camera Control Bus (SCCB) Specification for detailed usage of the serial control port.

2.6 power up sequence

Based on the system power configuration (1.8V or 3.3V for I/O power, using external DVDD or internal DVDD, the power up sequence will differ. Due to the higher power down current when using an external DVDD source, OmniVision strongly recommends cutting off all power supplies, including the external DVDD, when the sensor is not in use in the case of the external DVDD.

2.6.1 power up with internal DVDD

When powering up with the internal DVDD and SCCB access during the power ON period, the following conditions must occur:

1. when DOVDD and AVDD are turned ON, make sure DOVDD becomes stable before AVDD becomes stable
2. PWDN is active high with an asynchronized design (does not need clock)
3. PWDN must go high during the power up period
4. for PWDN to go low, power must first become stable (AVDD to PWDN ≥ 5 ms)
5. RSTB is active low with an asynchronized design
6. state of RSTB does not matter during power up period once DOVDD is stable
7. master clock XCLK should be provided at least 1 ms before host accesses the sensor's registers
8. host can access SCCB bus (if shared) during entire period. 20 ms after PWDN goes low or 20 ms after RSTB goes high if reset is inserted after PWDN goes low, the host can access the sensor's registers to initialize the sensor

figure 2-4   power up timing with internal DVDD

DOVDD first, then AVDD, and rising time is less than 5 ms
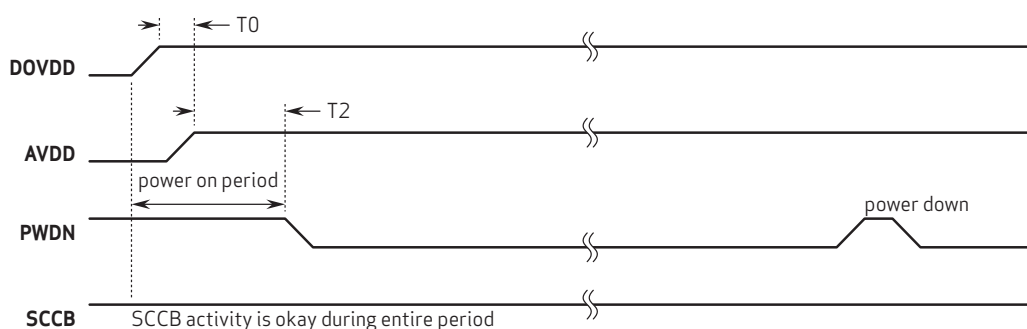
note T0 ≥ 0 ms: delay from DOVDD stable to AVDD stable
T2 ≥ 5 ms: delay from AVDD stable to sensor power up stable

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2.6.2 power up with external DVDD source

When powering up with an external DVDD source and SCCB access during the power ON period, the following conditions must occur:

1. when DOVDD and AVDD are turned ON, make sure DOVDD becomes stable before AVDD becomes stable
2. when AVDD and DVDD are turned ON, make sure AVDD becomes stable before DVDD becomes stable
3. PWDN is active high with an asynchronized design (does not need clock)
4. for PWDN to go low, power must first become stable (DVDD to PWDN ≥ 5 ms)
5. all power supplies are cut off when the camera is not in use (power down mode is not recommended
6. RSTB is active low with an asynchronized design
7. state of RSTB does not matter during power up period once DOVDD is stable
8. master clock XCLK should be provided at least 1 ms before host accesses the sensor's registers
9. host can access SCCB bus (if shared) during entire period. 20 ms after PWDN goes low or 20 ms after RSTB goes high if reset is inserted after PWDN goes high, the host can access the sensor's registers to initialize the sensor

figure 2-5   power up timing with external DVDD source

DOVDD first, then AVDD, followed by DVDD, and rising time is less than 5 ms
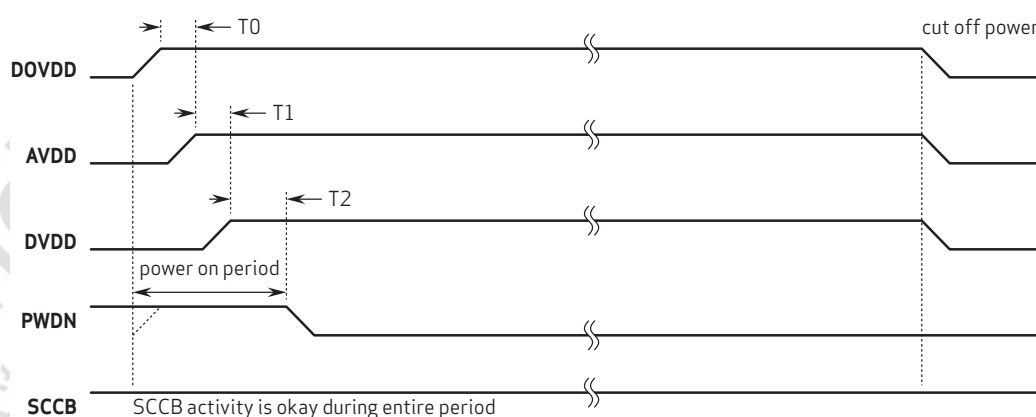
note T0 ≥ 0 ms: delay from DOVDD stable to AVDD stable
T1 ≥ 0 ms: delay from AVDD stable to DVDD stable
T2 ≥ 5 ms: delay from DVDD stable to sensor power up stable

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2.7 reset

The OV9712/OV9211 sensor includes a **RSTB** pin that forces a complete hardware reset when it is pulled low (GND). The OV9712/OV9211 clears all registers and resets them to their default values when a hardware reset occurs. A reset can also be initiated through the SCCB interface by setting register 0x12[7] to high.

The whole chip will be reset during power up. Manually applying a hard reset upon power up is recommended even though the on-chip power up reset is included. The hard reset is active low with an asynchronized design. The host reset can be inserted 1 ms after PWDN goes low. The reset pulse width should be greater than or equal to 1 ms.

2.8 power OFF

For the full sensor power OFF, all external power supplies must be turned OFF and RSTB, PWDN and XCLK pins must be pulled to low.

2.9 power down

Two methods are available to place the OV9712/OV9211 into power down mode:

- hardware power down
- SCCB software power down

To initiate hardware power down, the **PWDN** pin must be tied to high. When this occurs, the OV9712/OV9211 internal device clock is halted and all internal counters are reset.

Executing a software power down through the SCCB interface suspends internal circuit activity but does not halt the device clock. All register content is maintained in standby mode.

3 block level description

3.1 pixel array structure

The OV9712/OV9211 sensor has an image array of 1296 columns by 818 rows (1,060,128 pixels). **figure 3-1** shows a cross-section of the image sensor array.

The color filters are arranged in a Bayer pattern. The primary color BG/GR array is arranged in line-alternating fashion. Of the 1,060,128 pixels, 1,024,000 (1280x800) are active pixels and can be output. The other pixels are used for black level calibration.

The sensor array design is based on a field integration read-out system with line-by-line transfer and an electronic shutter with a synchronous pixel read-out scheme.

figure 3-1   sensor array region color filter layout
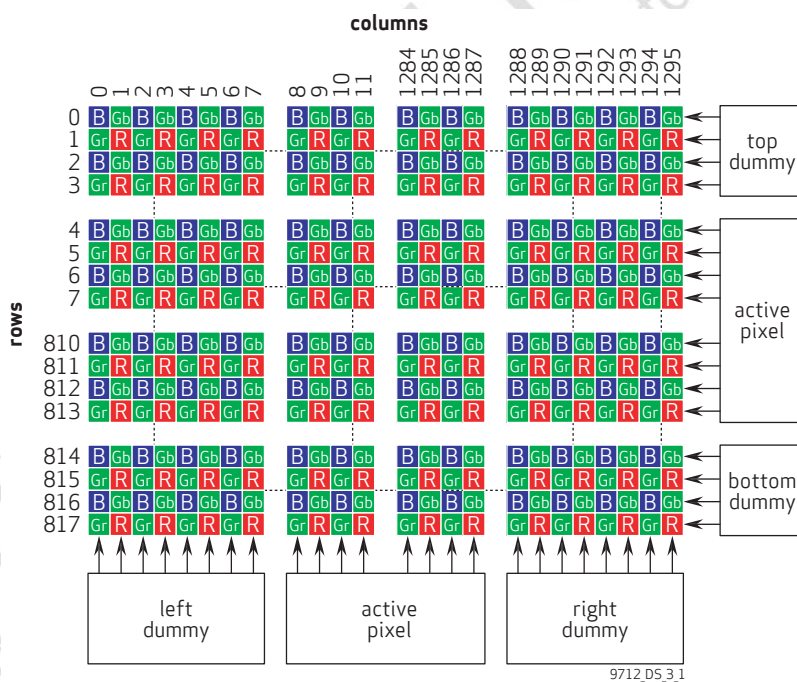
3.2 analog amplifier

When the column sample/hold circuit has sampled one row of pixels, the pixel data will shift one-by-one into an analog amplifier.

3.2.1 gain control

The amplifier gain can either be programmed by the user or controlled by the internal automatic gain control (AGC) circuit.

3.3 10-bit A/D converters

After passing through the analog amplifier, the Bayer pattern raw signal is fed to two 10-bit analog-to-digital (A/D) converters, one for the G channel and one shared by the BR channels. These A/D converters operate at speeds up to 20 MHz and are fully synchronous to the pixel rate (actual conversion rate is related to the frame rate).

4   image sensor core digital functions

4.1 mirror and flip

The OV9712/OV9211 provides mirror and flip readout modes, which respectively reverse the sensor data readout order horizontally and vertically (see **figure 4-1**). In mirror, the readout sequence of R/G or B/G is programmable. In flip, the starting line for VREF must be adjusted. Then, the DSP block will auto detect whether the pixel is in the red line or blue line and make the necessary adjustment.

figure 4-1   mirror and flip samples

| original image | mirrored image | flipped image | mirrored and flipped image |
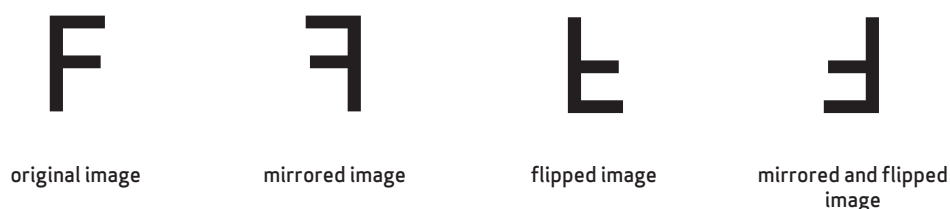
9712 DS 4 1

table 4-1   mirror and flip function control

function	register	description
mirror	0x04	Bit[7]: mirror ON/OFF select 0: mirror OFF 1: mirror ON
flip[a]	0x04	Bit[6]: flip ON/OFF select 0: flip OFF 1: flip ON

a.   When using the flip function, the starting line of VREF, {**VSTART**[7:0] (0x19), **REG03**[1:0] (0x03)}, must be adjusted.

4.2 test pattern

For testing purposes, the OV9712/OV9211 offers one kind of test pattern, color bar

figure 4-2   test pattern
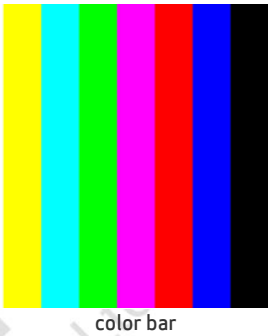
color bar

table 4-2   test pattern selection control

function	register	description
color bar (with pixel overlay)	**0x12**	Bit[1]: color bar enable 0: normal image 1: color bar with pixel overlay
color bar (without pixel overlay)	**0x97**	Bit[3]: color bar without pixel overlay 0: normal image 1: color bar enable
color bar pattern select	**0x97**	Bit[1:0]: pattern options for color bar without pixel overlay 00: color bar 1 (solid color) 01: color bar 2 (fade to gray) 10: color bar 3 11: not allowed

4.3 AEC/AGC algorithms

The auto exposure control (AEC) and auto gain control (AGC) functions allow the image sensor to adjust the image brightness to a desired range by setting the proper exposure time and gain applied to the image. Besides automatic control, exposure time and gain can be set manually from external control. The related registers are listed in **table 4-3**.

table 4-3   AEC/AGC control functions

function	register	description
AEC enable	0x13	Bit[0]: auto/manual exposure control select 0: manual 1: auto
LAEC (less than 1 row of exposure time)	{0x3C, 0x1F}	LAEC[15:8] = 0x3C[15:8] LAEC[7:0] = 0x1F[7:0]
AEC exposure time	{0x16, 0x10}	AEC[15:8] = 0x16[15:8] AEC[7:0] = 0x10[7:0]
AGC gain	0x00	Bit[7]: digital gain Bit[6:0]: analog gain
AGC enable	0x13	Bit[2]: auto/manual gain control select 0: manual 1: auto
histogram / average-based selection	0x0E	Bit[0]: AEC/AGC method select 0: average-based AEC/AGC 1: histogram-based AEC/AGC

There are two different algorithms that decide whether the current frame is too bright or too dark and determine if the exposure time/gain should increase or decrease for the next frame. One algorithm, Histogram algorithm, is based on the statistics of the percentage of high/low luminance pixels, and the other is based on the weighted-average of a frame.

4.3.1 average-based algorithm

The average-based AEC controls image luminance using registers **WPT/HisH** (0x24) and **BPT/HisL** (0x25). In average-based mode, the value of register **WPT/HisH** (0x24) indicates the high threshold value and the value of register **BPT/HisL** (0x25) indicates the low threshold value. When the target image luminance average value **YAVG** (0x2F) is within the range specified by registers **WPT/HisH** (0x24) and **BPT/HisL** (0x25), the AEC keeps the image exposure. When register **YAVG** (0x2F) is greater than the value in register **WPT/HisH** (0x24), the AEC will decrease the image exposure. When register **YAVG** (0x2F) is less than the value in register **BPT/HisL** (0x25), the AEC will increase the image exposure. Accordingly, the value in register **WPT/HisH** (0x24) should be greater than the value in register **BPT/HisL** (0x25). The gap between the values of registers **WPT/HisH** (0x24) and **BPT/HisL** (0x25) controls the image stability.

The AEC function supports both normal and fast speed selections in order to bring the image exposure into the range set by the values in registers **WPT/HisH** (0x24) and **BPT/HisL** (0x25). AEC set to normal mode will allow for single-step

increment or decrement in the image exposure to maintain the specified range. A value of "0" in register **FASTEN**[7] (0x13) will result in normal speed operation and a "1" will result in fast speed operation.

Register **VPT** (0x26) controls the fast AEC range. If the target image **YAVG** (0x2F) is greater than **VPT**[7:4] × 16, AEC will decrease by 2. If register **YAVG** (0x2F) is less than **VPT**[3:0] × 16, AEC will increase by 2.

As shown in **figure 4-3**, the AEC/AGC convergence uses two regions, the inner stable operating region and the outer control zone, which defines the convergence step size change as follows:

4.3.1.1 outside control zone

step size: $2 \times (AEC[15:0])$

t_{STEP}: $t_{ROW} \times (2 \times AEC[15:0])$

4.3.1.2 inside control zone

step size: $2 \times (AEC[15:0]) \div 16$

t_{STEP}: $t_{ROW} \times (2 \times AEC[15:0] \div 16)$

Once the current value is inside the stable operating region, the AEC/AGC value has converged.

figure 4-3　　desired convergence
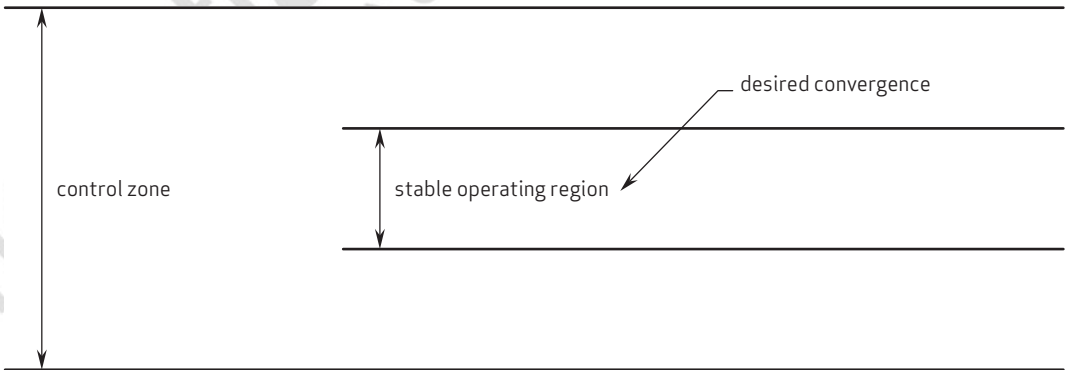
9712_DS_4_3

control zone upper limit: {**VPT**[7:4] (0x26[7:4]), 4'b0000}

control zone lower limit: {**VPT**[3:0] (0x26[3:0]), 4'b0000}

stable operating region upper limit: WPT[7:0] (0x24)

stable operating region lower limit: BPT[7:0] (0x25)

table 4-4   AEC control functions

function	register	AEC / AGC method	description
WPT/HisH	0x24	histogram-based	luminance signal / histogram high range for AEC/AGC operation
		average-based	AEC/AGC value decreases in auto mode when average luminance histogram is greater than **WPT/HisH**[7:0].
BPT/HisL	0x25	histogram-based	luminance signal / histogram low range for AEC/AGC operation
		average-based	AEC/AGC value increases in auto mode when average luminance histogram is less than **BPT/HisL**[7:0].
VPT	0x26	histogram-based	fast mode large step range thresholds - effective only in AEC/AGC fast mode Bit[7:4]: high threshold Bit[3:0]: low threshold
		average-based	AEC/AGC may change in larger steps when luminance average is greater than **VPT**[7:4] or less than **VPT**[3:0].
YAVG	0x2F		luminance average - this register will auto update. Average luminance is calculated from the B/Gb/Gr/R channel average as follows: B/Gb/Gr/R channel average = (BAVG[7:0] + GbAVG[7:0] + GrAVG[7:0] + RAVG[7:0]) × 0.25
FASTEN	0x13		Bit[7]: AEC speed select 0: normal 1: faster AEC adjustment

For the average-based AEC/AGC algorithm, the measured window is horizontally and vertically adjustable and divided into sixteen (4x4) zones (see **figure 4-4**). Each zone (or block) is 1/16th of the image. The final YAVG is the weighted average of the sixteen zones. The 4-bit weight could be n/4 where n is from 0 to 3. For more details on adjusting horizontal and vertical windows and weight for each window, refer to **section 4.3.1.3,** average luminance (YAVG).

4.3.1.3 average luminance (YAVG)

Auto exposure time calculation is based on a frame brightness average value. By properly setting AHS,AVS, AHW, and AVH as shown in **figure 4-4**, a 4x4 grid average window is defined. The average value is the weighted average of the 16 sections. **table 4-5** lists the corresponding registers.

figure 4-4   average-based window definition
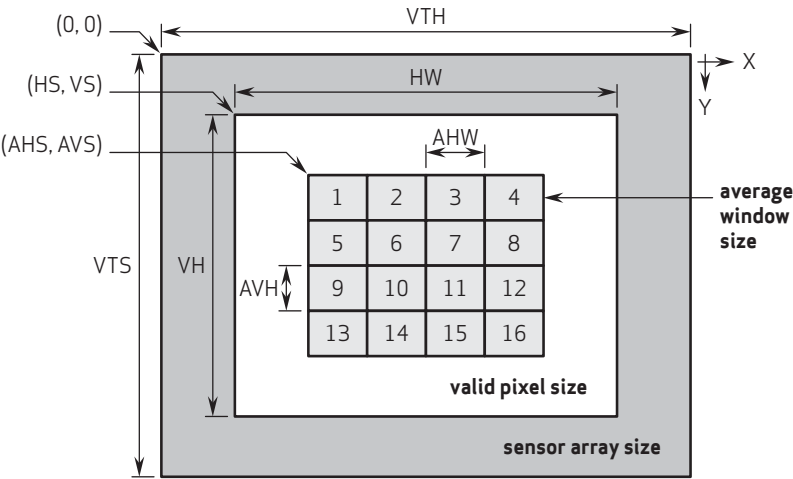
note 1   sensor array size (for WXGA, VTH=1296, VTS=818)
valid pixel size (for WXGA, VTH=1280, VTS=800)

9712_DS_4_4

table 4-5   average-based algorithm functions

function	register	description
average section weighting	0x4E~0x51	section 1 weight = 0x4E[1:0] section 2 weight = 0x4E[3:2] section 3 weight = 0x4E[5:4] section 4 weight = 0x4E[7:6] section 5 weight = 0x4F[1:0] section 6 weight = 0x4F[3:2] section 7 weight = 0x4F[5:4] section 8 weight = 0x4F[7:6] section 9 weight = 0x50[1:0] section 10 weight = 0x50[3:2] section 11 weight = 0x50[5:4] section 12 weight = 0x50[7:6] section 13 weight = 0x51[1:0] section 14 weight = 0x51[3:2] section 15 weight = 0x51[5:4] section 16 weight = 0x51[7:6]

4.3.2 histogram-based algorithm

The OV9712/OV9211 histogram-based AEC controls exposure levels based on image histogram distribution and probability.

table 4-6 histogram-based AEC algorithm adjustment controls

function	register	description
BP level	0x72	upper limit of luminance level for dark pixels
WP level	0x73	lower limit of luminance level for bright pixels
BP number	0x76	lower limit of probability for dark pixels to trigger auto AEC/AGC If dark pixel probability > BP number, AEC/AGC will increase automatically.
WP number	0x77	lower limit of probability for bright pixels to trigger auto AEC/AGC If bright pixel probability > WP number, AEC/AGC will decrease automatically.
VBP level	0x74	upper limit of luminance level for very dark pixels
VWP level	0x75	lower limit of luminance level for very bright pixels
VBP number	0x78	lower limit of probability for very dark pixels to trigger fast AEC/AGC If very dark pixel probability > BP number, AEC/AGC will increase in fast mode.
VWP number	0x79	lower limit of probability for very bright pixels to trigger fast AEC/AGC If very bright pixel probability > WP number, AEC/AGC will decrease in fast mode.

4.4 AEC/AGC steps

figure 4-5 shows how the AEC and AGC work together to obtain adequate exposure/gain based on the current environment's illumination. The upper one illustrates the non-banding operation which time unit is based on Tline. The lower one shows exposure in banding. The x-axis represents the length of exposure in time scale. In normal light circumstances, the length of exposure will fall into a range from 1 Tline to 1 Tframe. In extremely bright or dark circumstances, exposure time less than 1 Tline/Tband or greater than 1 Tframe may be required accordingly. In order to achieve the best signal-to-noise ratio (SNR), extending the exposure time is always preferred, rather than raising the analog gain, when the current illumination is getting brighter. Vice versa, under dark conditions, the action to decrease the gain is always taken prior to shortening the exposure time.

figure 4-5   darker illumination situation / brighter illumination situation
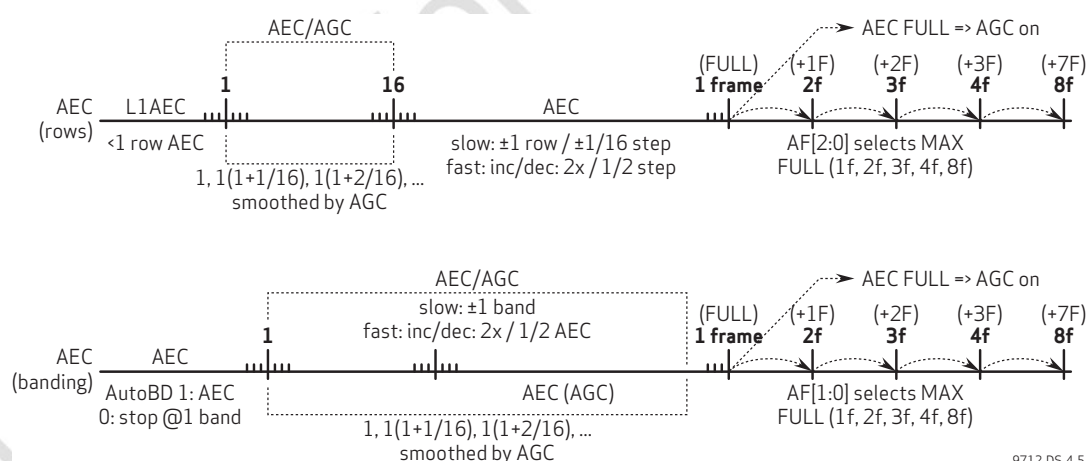
9712_DS_4_5

4.4.1 auto exposure control (AEC)

The function of the AEC is to calculate integration time of the next frame and send the information to the timing control block. Based on the statistics of previous frames, the AEC is able to determine whether the integration time should increase, decrease, fast increase, fast decrease, or remain the same.

In extremely bright situations, the LAEC activates, allowing integration time to be less than one row. In extremely dark situations, the VAEC activates, allowing integration time to be larger than one frame.

To avoid image flickering under a periodic light source, the integration time step can be adjusted as an integer multiple of the period of the light source. This new AEC step system is called banding, suggesting that the steps are not continuous but fall in some bands.

4.4.1.1 LAEC

If the integration time is only one row but the image is too bright, AEC will enter LAEC mode. Within LAEC, the integration time can be further decreased to a minimal of 1/16 row or so. LAEC ON/OFF can be set in 0x13[3].

4.4.1.2 banding mode ON with AEC

When banding mode is ON, AEC step, which is also called 'band', increments by an integer multiple of the period of light intensity. This design is to reject image flickering when light source is not steady but periodical.

For a given operating frequency, band step can be expressed in terms of row timing.

Band Step = 'period of light intensity' × 'frame rate' × 'rows per frame'.

The band steps for 50Hz and 60Hz light sources can be set in registers 0x49~0x4A.

When auto-banding is ON, if the next integration time is less than the minimal band step, banding will automatically turn OFF. It will turn ON again until the next integration time becomes larger than minimal band. If auto-banding is disabled, the minimal integration time is one minimal band. Auto-banding can be set in register 0x13[5].

4.4.1.3 banding mode OFF with AEC

When Banding is OFF, integration time increases/decreases by 1/16 of the previous step in slow mode or becomes twice/half of the previous step in fast mode.

4.4.1.4 VAEC

In extremely dark situations, the integration time must be longer than one frame.

The OV9712/OV9211 supports long integration time such as 1 frame, 2 frames, 3 frames and 7 frames. This is achieved by slowing down original frame rate and waiting for exposure. VAEC ceiling can be set in register 0x03[7:5]. VAEC can be disable by setting register 0x0E[3] to 0.

4.4.2 auto gain control (AGC)

Unlike prolonging integration time, increasing gain will amplify both signal and noise or between two gaps of banding exposure time. Thus, AGC usually starts after AEC is full. However, in same cases where adjacent AEC step changes are too large(>1/16), AGC step should be inserted in between; otherwise, the integration time will keep switching from two adjacent steps and the image flickers.

4.4.2.1 integration time between 1~16 rows

When integration time is less than 16 rows, the changes between adjacent AEC steps are larger than 1/16, which may possibly make the image oscillate between two AEC levels; thus, some AGC steps are added in between. For example, from AEC = 2 rows to AEC = 3 rows, there are 7 more AGC steps (1+ x/16, x=1~7) inserted, which ensures every step change is less than 1/16.

4.4.2.2 gain insertion between AEC banding steps

In Banding ON mode, the minimal integration time change is the period of light intensity (10ms for 50Hz, 16.67ms for 60Hz). For the first 16 band steps, since the change between adjacent steps is larger than 1/16, AGC steps are inserted to ensure image stability.

4.4.2.3 gain insertion between VAEC steps

Between VAEC steps (e.g., integration time = 1 frame and 2 frames), AGC steps are inserted to ensure no adjacent step change is larger than 1/16 (6.25%).

4.4.2.4 when AEC reaches maximum

When AEC reaches its maximum while the image is still too dark, the AGC starts to increase until the new frame average falls into the no-adjust region or the AGC reaches its maximum. The AGC maximum can be set in register 0x14[7:5].

table 4-7 histogram-based AEC/AGC reference area option

function	register	description	
LAEC ON/OFF	**0x13**	Bit[3]:	LAEC ON/OFF select 0: OFF 1: ON
VAEC ON/OFF (add frame)	**0x0E**	Bit[3]:	VAEC ON/OFF select 0: OFF 1: ON
VAEC ceiling (max integration time)	**0x03**	Bit[7:5]:	VAEC ceiling 001: 1 frame 010: 2 frames 011: 3 frames 1xx: 7 frames
VAEC active point trigger option	**0x21**	Bit[5:4]:	automatically trigger VAEC when gain is greater than: 00: 2x 01: 4x 10: 8x 11: 16x
banding filter ON/OFF	**0x13**	Bit[5]:	banding filter ON/OFF select 0: OFF 1: ON
banding filter option	**0x14**	Bit[3]:	enable AEC below banding value 0: limit the minimum exposure time to 1/100 or 1/120 second under any light conditions when banding filter is enabled 1: allow exposure time to be less than 1/100 or 1/120 second under strong light conditions when banding filter is enabled
max_band	**0x22**	Bit[5:0]:	max banding steps in terms of row exposure
banding step	**0x49~0x4A**	banding filter value BDst[9:8] = **REG4A**[1:0] BDst[7:0] = **REG49**[7:0]	

4.5 black level calibration (BLC)

The pixel array contains four optically shielded (black) rows. These rows are used to provide the data for offset cancellation algorithms (black level calibration).

Digital image processing starts with black level subtraction. The BLC algorithm estimates the offset of the black level from the data provided by black rows. These offsets of different color channels will be subtracted from values of the color pixels. If the subtraction produces a negative result for a particular pixel, the value of this pixel is set to "0." By default, BLC will be triggered when gain is changing.

table 4-8   BLC control functions

function	register	description
target	0x41	Bit[3:0]: target black level value that is used in the algorithm
BLC_R, BLC_B	0x43	Bit[7:6]: BLC line selection x0: use R/Gr channel offset for all channels 01: use B/Gb channel offset for all channels 11: use all four channel offsets
BLC always ON	0x37	Bit[2]: target black level value that is used in the algorithm BLC offsets are adjusted every frame
MBLC	0x37	Bit[3]: target black level value that is used in the algorithm Trigger BLC manually for 64 frames
R offset	{0x48[1:0], 0x44[7:0]}	BLC offset for R channel
B offset	{0x48[3:2], 0x45[7:0]}	BLC offset for B channel
Gr offset	{0x48[5:4], 0x46[7:0]}	BLC offset for Gr channel
Gb offset	{0x48[7:6], 0x47[7:0]}	BLC offset for Gb channel

4.6 digital gain

After black level subtraction, multiplication may apply to all pixel values based on an optional digital gain. By default, the sensor will use analog gain up to its maximum before applying digital gain to the pixels.

table 4-9　　digital gain control functions

function	register	description
dgain	**0x00**	Bit[7]:　range of digital gain 0:　apply digital gain only if gain ≥ 2x 1:　apply digital gain only if gain ≥ 4x

4.7 one-time programmable (OTP) memory

The OV9712/OV9211 supports 128 bits maximum one-time programmable (OTP) memory to store chip identification and manufacturing information. Contact your local OmniVision FAE for more details.

5 image sensor processor digital functions

5.1 ISP top

The main purpose of the ISP top is to integrate all sub-modules. The ISP should always be enabled.

table 5-1   ISP top registers

address	register name	default value	R/W	description
0x96	DSP_CTRL_0	1'b1	RW	Bit[0]: ISP enable 0: Disable ISP 1: Enable ISP
0x97	DSP_CTRL_1	4'h0	RW	Bit[3]: bar_en 0: Disable color bar 1: Enable color bar Bit[2]: sht_neg 0: Disable delaying the data HREF/valid clock 1: Enable delaying the data HREF/valid clock Bit[1:0]: bar_style Selects type of color bar to output
0x98	DSP_CTRL_2	0x00	RW	Bit[7:0]: pre_out_hoff[7:0] Horizontal offset of the pre_win output (valid with **DSP_CTRL_4**[2:0] (0x9A))
0x99	DSP_CTRL_3	0x00	RW	Bit[7:0]: pre_out_voff[7:0] Vertical offset of the pre_win output (valid with **DSP_CTRL_4**[5:4] (0x9A))
0x9A	DSP_CTRL_4	0x00	RW	Bit[7:6]: Reserved Bit[5:4]: pre_out_voff[9:8] Vertical offset of the pre_win output (valid with **DSP_CTRL_3**[7:0] (0x99)) Bit[3]: Reserved Bit[2:0]: pre_out_hoff[10:8] Horizontal offset of the pre_win output (valid with **DSP_CTRL_2**[7:0] (0x98))
0x9B	DSP_CTRL_5	0x04	RW	Bit[7:4]: pre_pad_vrgt Padding the column number in pre_win Bit[3:0]: pre_pad_hrgt Padding the row number in pre_win
0xD6	SC_CTRL_0	0x0C	RW	Bit[7]: Bypass DVP (default value = 1'b0) Bit[6]: Reserved (default value = 1'b0) Bit[5]: snr_rst_ctrl for DVP (default value = 1'b0) Bit[4]: snr_rst_ctrl for DSP (default value = 1'b0) Bit[3]: DVP gated clock (default value = 1'b1) Bit[2]: DSP gated clock (default value = 1'b1) Bit[1]: DVP reset (default value = 1'b0) Bit[0]: DSP reset (default value = 1'b0)

5.2 lens correction (LENC)

The LENC algorithm compensates for the illumination drop off in the corners due to the lens. Based on the radius of each pixel to the lens, the algorithm calculates a gain for each pixel and then corrects each pixel with the calculated gain to compensate for the light distribution due to the lens curvature.

For each channel, first adjust the center coordinate, LCC_X and LCC_Y. Then, for each pixel, calculate the distance r to the center. The further the distance from the center, the greater the gain should be applied to this pixel. The exact equation is:

Lens Correction Gain = ar^2 + br + 1, where a and b are coefficients chosen for the correction in which a is a positive value and b can be either positive or negative. Each channel can choose a separate a and b.

figure 5-1 shows how the LENC module works. Registers 0xA3 to 0xA8 are for blue channel control, registers 0xA9 to 0xAE are for green channel control, and registers 0xAF to 0xB4 are for red channel control.

figure 5-1   LENC description
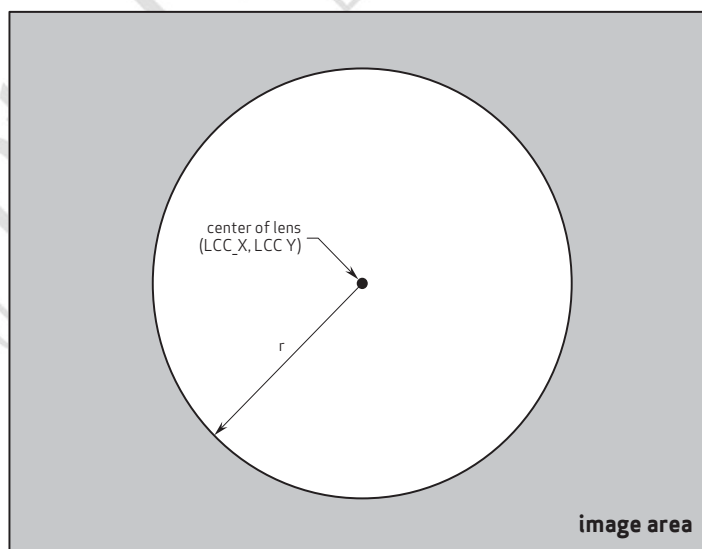
note R/G/B each channel can have different center.
R/G/B each channel applies lens correction gains separately.
r is the distance of each pixel to the center.   9712_DS_5_1

For example, in the case of B channel, the values for center, a, and b are determined as follows:

LCC_X = B_X0[10:0] = {0xA5[2:0], 0xA3[7:0]}
LCC_Y = B_Y0[9:0]   = {0xA5[5:4], 0xA4[7:0]}

$a = B\_A1[6:0] \times 2^{(-(B\_A2[3:0] + 0x08))}$
$b = B\_B1[6:0] \times 2^{(-(B\_B2[3:0] + 0x01))}$, where B_B1[7] is the sign bit.

table 5-2   LENC registers (sheet 1 of 2)

function	address	register name	description
LENC enable	0x96	**DSP_CTRL_0**	Bit[3]: LENC correction function enable 0: Disable 1: Enable
manual center operation	0xA1	**LENC_CTRL_3**	Bit[4]: Manually selects the center of the R, G, B circle
rnd_en	0xA1	**LENC_CTRL_3**	Bit[3]: Determines whether or not to round off the last two bits of LENC input data 0: Do not round off the last 2 bits 1: Round off the last 2 bits
lenc_off_man	0xA2	**LENC_CTRL_4**[7:0]	Bit[7:0]: Black level manual setting for LENC Range: 0 ~ 255
R_X0	{0xA5, 0xA3}	{**LENC_CTRL_7**[2:0], **LENC_CTRL_5**[7:0]}	LCC_X for Red Channel
R_Y0	{0xA5, 0xA4}	{**LENC_CTRL_7**[5:4], {**LENC_CTRL_6**[7:0]}	LCC_Y for Red Channel
R_A1	0xA6	**LENC_CTRL_8**	Bit[6:0]: Composed of the first group of factors used in the LENC correction of the red color channel.
R_A2	0xA8	**LENC_CTRL_10**	Bit[3:0]: Composed of the first group of factors used in the LENC correction of the red color channel.
R_B1	0xA7	**LENC_CTRL_9**	Bit[7:0]: Composed of the second group of factors used in the LENC correction of the red color channel.
R_B2	0xA8	**LENC_CTRL_10**	Bit[7:4]: Composed of the second group of factors used in the LENC correction of the red color channel.
G_X0	{0xAB, 0xA9}	{**LENC_CTRL_13**[2:0], **LENC_CTRL_11**[7:0]}	LCC_X for Green Channel
G_Y0	{0xAB, 0xAA}	{**LENC_CTRL_13**[5:4], {**LENC_CTRL_12**[7:0]}	LCC_Y for Green Channel
G_A1	0xAC	**LENC_CTRL_14**	Bit[6:0]: Composed of the first group of factors used in the LENC correction of the green color channel.
G_A2	0xAE	**LENC_CTRL_16**	Bit[3:0]: Composed of the first group of factors used in the LENC correction of the green color channel.
G_B1	0xAD	**LENC_CTRL_15**	Bit[7:0]: Composed of the second group of factors used in the LENC correction of the green color channel.

table 5-2   LENC registers (sheet 2 of 2)

function	address	register name	description
G_B2	0xAE	**LENC_CTRL_16**	Bit[7:4]: Composed of the second group of factors used in the LENC correction of the green color channel.
B_X0	{0xB1, 0xAF}	{**LENC_CTRL_19**[2:0], **LENC_CTRL_17**[7:0]}	LCC_X for Blue Channel
B_Y0	{0xB1, 0xB0}	{**LENC_CTRL_19**[5:4], {**LENC_CTRL_18**[7:0]}	LCC_Y for Blue Channel
B_A1	0xB2	**LENC_CTRL_20**	Bit[6:0]: Composed of the first group of factors used in the LENC correction of the blue color channel.
B_A2	0xB4	**LENC_CTRL_22**	Bit[3:0]: Composed of the first group of factors used in the LENC correction of the blue color channel.
B_B1	0xB3	**LENC_CTRL_21**	Bit[7:0]: Composed of the second group of factors used in the LENC correction of the blue color channel.
B_B2	0xB4	**LENC_CTRL_22**	Bit[7:4]: Composed of the second group of factors used in the LENC correction of the blue color channel.
V_skip	0xB5	**LENC_CTRL_23**	Bit[2]: Lens correction option for sub-sampling mode. This register should be set during sub-sampling. 0: Normal image output (full size and cropped image) 1: Sub-sampling output
H_skip	0xB5	**LENC_CTRL_23**	Bit[0]: Lens correction option for sub-sampling mode. This register should be set during sub-sampling. 0: Normal image output (full size and cropped image) 1: Sub-sampling output

5.2.1 LENC gain COEF

The main purpose of the LENC Gain COEF is to adjust the parameters used in LENC according to the sensor gain.

figure 5-2   LENC gain coefficient

9712_DS_5_2
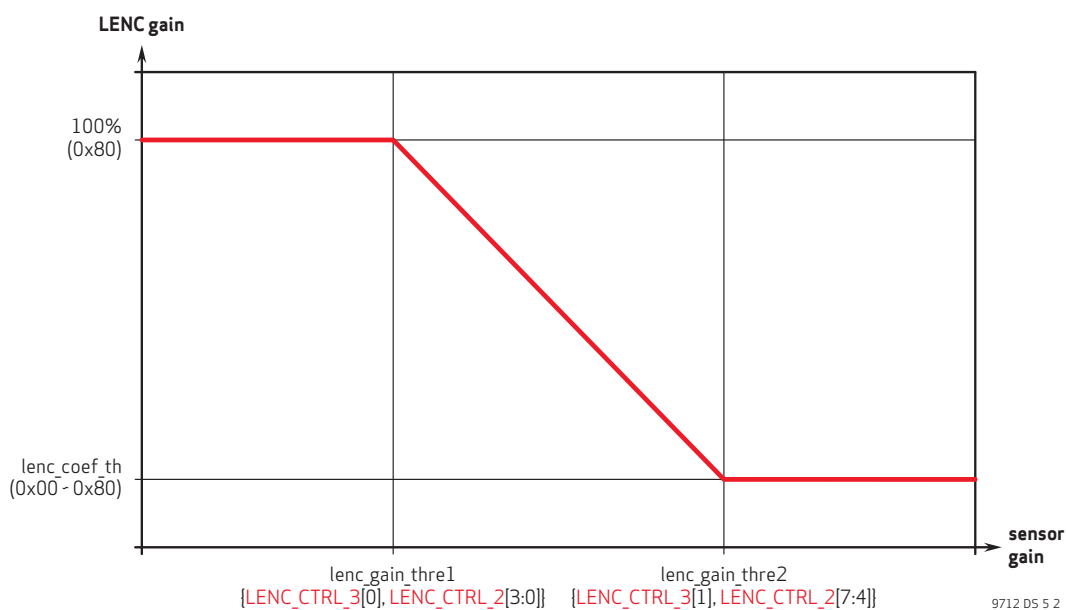
table 5-3   LENC gain COEF registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x96	DSP_CTRL_0	1'b0	RW	Bit[2]: lenc_gain_coef_en Enable the lenc_gain_coef module 0: Disable lenc_gain_coef module 1: Enable lenc_gain_coef module
0x9E	LENC_CTRL_0	0x00	RW	Bit[7:0]: def_coef_man Manual value of the lenc_coef gain (effective when **LENC_CTRL_3**[2] (0xA1) is set)
0x9F	LENC_CTRL_1	0x80	RW	Bit[7:0]: lenc_coef_th

table 5-3　　LENC gain COEF registers (sheet 2 of 2)

address	register name	default value	R/W	description	
0xA0	LENC_CTRL_2	0xF1	RW	Bit[7:4]:	lenc_gain_thre2[3:0] High threshold of the LENC gain (valid with **LENC_CTRL_3**[1] (0xA1))
				Bit[3:0]:	lenc_gain_thre1[3:0] Low threshold of the LENC gain (valid with **LENC_CTRL_3**[0] (0xA1))
0xA1	LENC_CTRL_3	0x6A	RW	Bit[2]:	def_coef_man_en Enable manual mode of the lenc_coef gain
				Bit[1]:	lenc_gain_thre2[4] High threshold of the LENC gain (valid with **LENC_CTRL_2**[7:4] (0xA0))
				Bit[0]:	lenc_gain_thre1[4] Low threshold of the LENC gain (valid with **LENC_CTRL_2**[3:0] (0xA0))

5.3 white balance control

The OV9712/OV9211 provides options for manual white balance control and auto white balance control.

5.3.1 manual white balance control

In manual white balance control mode, the user has full control of the image white balance based on different preferences. It can be easily interfaced with a backend image processor through SCCB register control.

In manual mode, the OV9712/OV9211 internal red, green, and blue channels can be fully controlled by a backend companion chip.

To enable manual white balance mode, turn OFF both 0x34[4] and 0x97[4]. Then, adjust the color gain using the following registers:

- Blue[11:0]   {0x01[7:0], 0x06[7:4]}
- Red[11:0]   {0x02[7:0], 0x06[3:0]}
- Green[11:0]   {0x05[7:4], 0x07[7:4]}

For example, blue gain = Blue[11:0] / 0x400

5.3.2 automatic white balance control

In general, the automatic white balance is done by adjusting the red, blue, and green channels to make the red, blue, and green averages equal. The automatic mode can be enabled by setting both registers 0x34[4] and 0x97[4].

The main purpose of the AWB is to provide auto white balance correction. The algorithm is based on the gray world. In other words, the mean values of red, blue and green in the image are equal.

table 5-4   white balance function related registers (sheet 1 of 2)

function	address	register name	description
AWB_options	0x38	**COM25**	Bit[4]: AWB gain write options 0: Manual white balance control 1: ISP automatically controls the white balance function
AWB_en	0x96	**DSP_CTRL_0**	Bit[4]: AWB enable 0: Disable 1: Enable
Blue	{0x01, 0x06}	{**BLUE**[7:0], **BRL**[7:4]}	AWB blue channel gain Blue[11:0] = {0x01[7:0], 0x06[7:4]} / 0x400
Red	{0x02, 0x06}	{**RED**[7:0], **BRL**[3:0]}	AWB red channel gain Red[11:0] = {0x02[7:0], 0x06[3:0]} / 0x400
Green	{0x05, 0x07}	{**GREEN**[7:4], **GL**[7:4]}	AWB green channel gain Green[11:0] = {0x05[7:4], 0x07[7:4]} / 0x400

table 5-4   white balance function related registers (sheet 2 of 2)

function	address	register name	description	
AWB_gain_en	0x96	**DSP_CTRL_0**	Bit[5]:	AWB gain enable Applies auto white balance gain according to the ISP results or manual adjustment. 0: Disable 1: Enable
AWB_fast	0xB6	**AWB_CTRL_0**	Bit[2]:	AWB fast mode enable 0: Disable 1: Enable
AWB_bias	0xB6	**AWB_CTRL_0**	Bit[1]:	AWB bias enable 0: Disable 1: Enable
AWB_bias_plus	0xB6	**AWB_CTRL_0**	Bit[0]:	AWB bias plus enable Adds AWB bias back after AWB gain is calculated 0: Disable 1: Enable
stable_range	0xB8	**AWB_CTRL_2**	Bit[7:0]:	AWB stable range 1 Stable range when computing the gain value for R, G, and B in AWB module.
stable_rangew	0xB9	**AWB_CTRL_3**	Bit[7:0]:	AWB stable range 2 Stable range after the gain value for R, G, and B is stable. AWB gain will be recalculated after the values exceed stable range 2.
AWB_frame_cnt	0xBA	**AWB_CTRL_4**	Bit[7:0]:	AWB frame count Number of frame count to apply AWB gain after AWB calculation is done.
delta	0xBB	**AWB_CTRL_5**	Bit[7:0]:	AWB delta Number of steps toward stable range.

5.4 white black pixel cancellation (WBC)

The main purpose of the WBC function is to remove the white/black pixel effect.

table 5-5   WBC registers

address	register name	default value	R/W	description
0x96	**DSP_CTRL_0**	0xF9	RW	Bit[7]: black_en Black pixel cancel function can remove the black pixels introduced because of sensor defect (default = 1'b1) Bit[6]: white_en White pixel cancel function can remove the white pixels introduced because of sensor defect (default = 1'b1)

5.5 sub-sample

DSP-CRTL_1[7] should be enabled during sub-sampling mode.

table 5-6   sub-sample registers

function	address	register name	description
SMPH_mean	0x97	**DSP_CTRL_1**	Bit[7]: SMPH mean enable (sub-sampling mode options) 0: Disable 1: Enable

5.6 YAVG

The main purpose of the YAVG function is to determine the average value of Y.

table 5-7   YAVG registers

address	register name	default value	R/W	description
0x9C	DSP_CTRL_6	0x00	RW	Bit[7:0]: blk_thresh
0x9D	DSP_CTRL_7	0xFF	RW	Bit[7:0]: wht_thresh
0xBD	YAVG_CTRL_0	0xA0	RW	Bit[7:0]: yavg_winh
0xBE	YAVG_CTRL_1	0xC8	RW	Bit[7:0]: yavg_winv
0xBF	YAVG_CTRL_2	0x00	RW	Bit[7:0]: yavg_winofh[7:0] (valid with **YAVG_CTRL_4**[2:0] (0xC1))
0xC0	YAVG_CTRL_3	0x00	RW	Bit[7:0]: yavg_winofv[7:0] (valid with **YAVG_CTRL_4**[5:4] (0xC1))
0xC1	YAVG_CTRL_4	0x00	RW	Bit[7]: yavg_win_man Bit[6]: Reserved Bit[5:4]: yavg_winofv[9:8] (valid with **YAVG_CTRL_3**[7:0] (0xC0)) Bit[3]: Reserved Bit[2:0]: yavg_winofh[10:8] (valid with **YAVG_CTRL_2**[7:0] (0xBF))

6 image sensor output interface digital functions

6.1 digital video port (DVP)

The digital video port (DVP) provides 10-bit parallel data output in all formats supported and extended features including HREF, CCIR656 format, HSYNC mode and test pattern output.

6.1.1 HREF mode

HREF mode is the default mode of the DVP (see **figure 6-1**). Each DVP_VSYNC indicates the starting of a new frame. The OV9712/OV9211 supports three types of DVP_VSYNC signals (vsync_old, vsync_new, and vsync3) as shown in **figure 6-2**). DVP_VSYNC, DVP_HREF, and DVP_PCLK can be reversed using the register settings.

figure 6-1   DVP timing
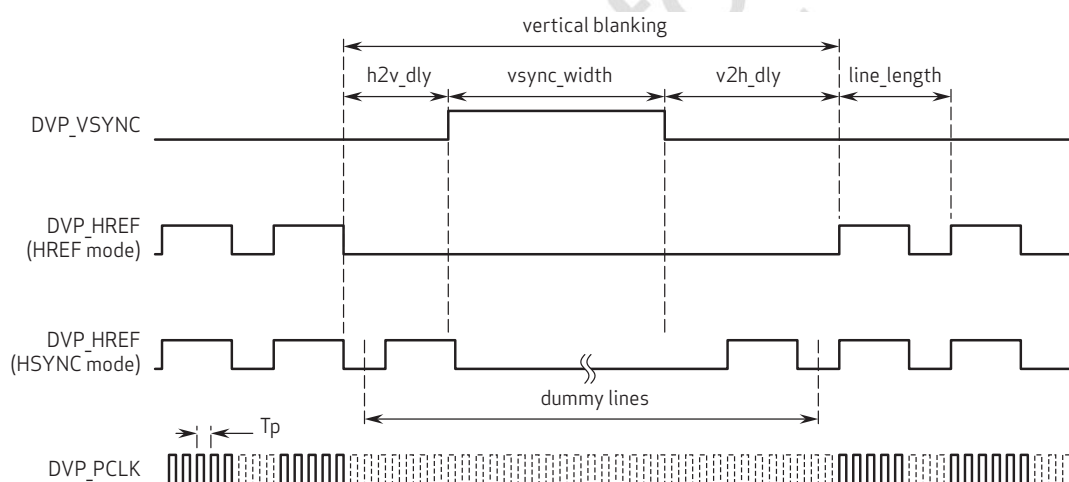
note 1 DVP_PCLK can be optionally gated when DVP_HREF is low.

note 1 typical values are: h2v_dly=256xTp, v2h_dly=16432Tp, line_length=1608Tp. these parameters are variable when setting changes.

9712_DS_6_1

figure 6-2 VSYNC timing

DVP_HREF

VSYNC_OLD
(vsync3_sel=0
and vsync_new_sel=0)

programmable
width

VSYNC_NEW
(vsync3_sel=0
and vsync_new_sel=1)

max 7 cycles
programmable
delay

max 7 cycles
programmable
delay

24-bit
programmable
delay

VSYNC3
(vsync3_sel=1)

9712_DS_6_2
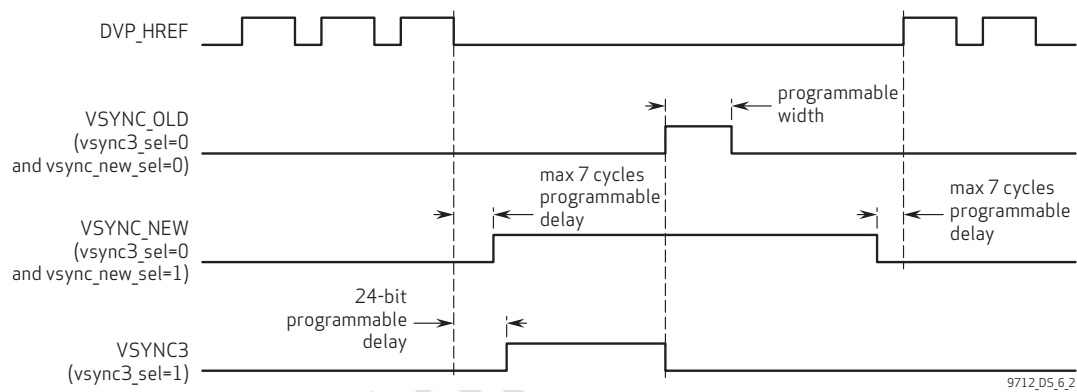
6.1.2 HSYNC mode

In this mode, the line blanking time and VSYNC to the first image line are fixed. Also, there are dummy lines when vertical blanking. The following settings are used to open HSYNC mode (see **table 6-2** for the DVP control registers).

1. Write 0xCB to 0x32 (sets hsync_en = 1)
2. Write 0xC3 to 0x21 (starts to calculate the parameters for HSYNC mode)

6.1.3 CCIR656 mode

The OV9712/OV9211 supports standard CCIR656 mode. The sync code can either be automatically generated or by setting registers 0xC3 to 0xC7. "F" of the sync code can be optionally toggled every frame. To set CCIR656 mode setting:

1. Write 0xC3 to 0xA0 (sets ccir656_en = 1)
2. Write 0xD4 to 0x23 (sets F_log_en = 1)

figure 6-3 CCIR656 timing

PCLK

PIXEL 80 10 FF 00 00 XP Dat Dat FF 00 00 XP 80 10
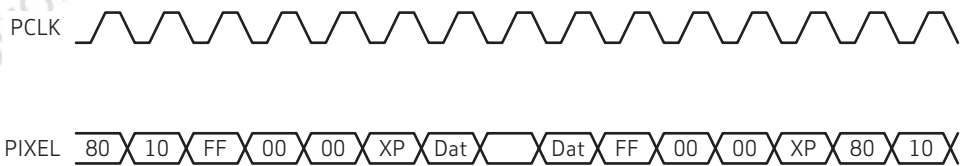
note 1

XP: {1, F, V, H, P[3:0]}	1	F	V	H	P3	P2	P1	P0	1	F	V	H	P3	P2	P1	P0
F: 0 for field 1; 1 for field 2	1	0	0	0	0	0	0	1	1	0	0	0	1	1	1
V: 0 for all else; 1 for field blanking	1	0	0	1	1	1	0	1	1	1	0	1	1	0	1	0
H: 0 for SAV; 1 for EAV	1	0	1	0	1	0	1	1	1	1	1	0	1	1	0	0
P[3:0]: protect bits	1	0	1	1	0	1	1	0	1	1	1	1	0	0	0	1

9712_DS_6_3

6.1.4 DVP timing

figure 6-4 DVP timing diagram
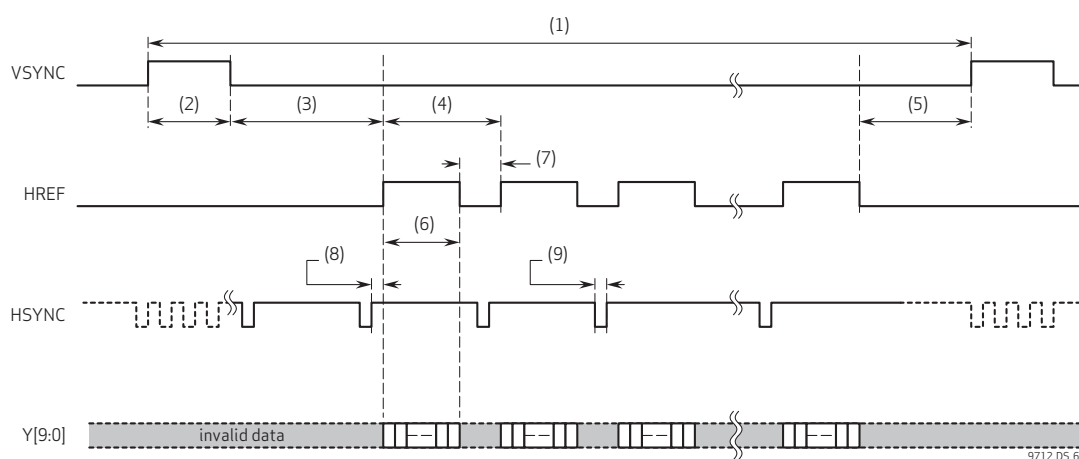
table 6-1 DVP timing specifications

mode	timing
WXGA 1280x800	(1) 1397664 tp = 828 lines (2) 33584 tp (3) 13832 tp (4) 1688 tp (5) 256 tp (6) 1280 tp (7) 408 tp (8) 274 tp (9) 48 tp where 1 pclk = 1 tp
640x400	(1) 698832 tp = 414 lines (2) 9944 tp (3) 13840 tp (4) 1688 tp (5) 256 tp (6) 1280 tp (7) 408 tp (8) 286 tp (9) 48 tp where 1 pclk = 2 tp

note
Timing values shown in **table 6-1** may vary depending upon register settings.

table 6-2 DVP control registers (sheet 1 of 4)

address	register name	default value	R/W	description
0xC2	DVP_CTRL_00	0x80	RW	Bit[7:6]: VSYNC options 00: vsync_old 01: vsync_new 10: vsync3 11: Invalid Bit[5]: pclk_gate_en Gate dvp_pclk when there is no data transfer 0: Disable 1: Enable Bit[4]: vsync_gate Gate dvp_pclk when VSYNC && pclk_gate_en 0: Disable 1: Enable Bit[3]: vsync3_w_sel 0: VSYNC3 will go low when SOF 1: Use vsync_width × 64 as vsync3_width Bit[2]: pclk_pol 1: Reverse DVP_PCLK Bit[1]: href_pol 1: Reverse DVP_HREF Bit[0]: vsync_pol 0: VSYNC=1 is frame blanking time 1: VSYNC=0 is frame blanking

table 6-2　　DVP control registers (sheet 2 of 4)

address	register name	default value	R/W	description
0xC3	DVP_CTRL_01	0x20	RW	Bit[7]: ccir656_en 　0: Disable 　1: Enable Bit[6]: sync_code_sel 　0: Auto generate sync code for CCIR656 　1: Use FS, FE, LS, LE (registers **0xC4** to **0xC7**) as sync code Bit[5]: blk_656 　0: CCIR656 data is 0x040 or 0x200 　1: CCIR656 data is 0x000 when blanking Bit[4]: eav_first 　1: CCIR656 sends EAV first Bit[3:1]: dvp_data_sequence 　000: Y9,Y8,Y7,Y6,Y5,Y4,Y3,Y2, Y1,Y0 　001: Y1,Y0,Y9,Y8,Y7,Y6,Y5,Y4, Y3,Y2 　010: Y7,Y6,Y5,Y4,Y3,Y2,Y1,Y0, Y9,Y8 　011: Reserved 　100: Y0,Y1,Y2,Y3,Y4,Y5,Y6,Y7, Y8,Y9 　101: Y8,Y9,Y0,Y1,Y2,Y3,Y4,Y5, Y6,Y7 　110: Y2,Y3,Y4,Y5,Y6,Y7,Y8,Y9, Y0,Y1 　111: Reserved Bit[0]: chg_flag Write 1 to this bit will generate change flag for HSYNC mode. This bit will auto clear. DVP will restart to calculate all timing parameters and output a frame.
0xC4	DVP_CTRL_02	0xAB	RW	Bit[7:0]: FS for CCIR656
0xC5	DVP_CTRL_03	0xB6	RW	Bit[7:0]: FE for CCIR656
0xC6	DVP_CTRL_04	0x80	RW	Bit[7:0]: LS for CCIR656
0xC7	DVP_CTRL_05	0x9D	RW	Bit[7:0]: LE for CCIR656
0xC8	DVP_CTRL_06	0x00	RW	Bit[7]: blk_tog 　1: dvp_data will toggle when blanking Bit[6]: vsync_width_sel 　0: Use vsync_widthx64 as VSYNC width 　1: Select 4x line length as VSYNC width Bit[5:3]: h2v_dly VSYNC to HREF delay for vsync_new Bit[2:0]: v2h_dly HREF to VSYNC delay for vsync_new
0xC9	DVP_CTRL_07	0x80	RW	Bit[7:0]: vsync_width_l vsync_width_real = vsync_width × 64

table 6-2   DVP control registers (sheet 3 of 4)

address	register name	default value	R/W	description
0xCA	DVP_CTRL_08	0x20	RW	Bit[7:6]: vsync_width_h Bit[5:4]: sof2h_dly_offset Bit[3]: ddr_phase 0: First pixel is at rising edge 1: First pixel is at falling edge Bit[2]: Test pattern options 0: 10-bit 1: 8-bit Bit[1:0]: Test pattern mode 00: No test pattern 01: 1, 2, 4, 8,... 10: 1, 1, 2, 2,...
0xCB	DVP_CTRL_09	0xA6	RW	Bit[7]: sof_rst_en 1: DVP state machine will be reset by SOF Bit[6:5]: chg_sel for recalculating DVP timing for HSYNC mode 00: Select SNR change and manual change (manual change flag is in register **DVP_CTRL_01**[0] (0xC3)) 01: Select auto detect change and manual change 10: Manually set change Bit[4]: hsync_en 1: Enable HSYNC mode (see **figure 6-1**) Bit[3]: hsync_dvp_en 1: v2h_dly, h2v_dly and line_length are fixed for each frame (see **figure 6-1**) Bit[2]: hsync_1st_en 0: Mask the first frame when in HSYNC mode Bit[1:0]: line_length_sel 00: Select line_length_snr 01: Select line_length_reg 10: Select line_length_auto
0xCC	DVP_CTRL_0A	0x40	RW	Bit[7:4]: FIFO_BUF size Bit[3:0]: dmy_line_nu Use CCIR656 first dummy line number to generate VSYNC
0xCD	DVP_CTRL_0B	0x00	RW	Bit[7:0]: eof2v_dly[23:16]
0xCE	DVP_CTRL_0C	0x01	RW	Bit[7:0]: eof2v_dly[15:8]
0xCF	DVP_CTRL_0D	0x00	RW	Bit[7:0]: eof2v_dly[7:0]
0xD0	DVP_CTRL_0E	0xFF	RW	Bit[7:0]: line_length[15:8]
0xD1	DVP_CTRL_0F	0xFF	RW	Bit[7:0]: line_length[7:0]

table 6-2   DVP control registers (sheet 4 of 4)

address	register name	default value	R/W	description
0xD2	DVP_CTRL_10	0xFF	RW	Bit[7:0]: clip_max[9:2] DVP output data should be less than or equal to clip_max (valid with **DVP_CTRL_12**[1:0] (0xD4))
0xD3	DVP_CTRL_11	0x00	RW	Bit[7:0]: clip_min[9:2] DVP output data should be larger than or equal to clip_min (valid with **DVP_CTRL_12**[3:2] (0xD4))
0xD4	DVP_CTRL_12	0x03	RW	Bit[5]: f_tog_en 1: ccir_f will toggle every frame Bit[4]: ddr_en 1: DVP will output DDR clock Bit[3:2]: clip_min[1:0] (valid with **DVP_CTRL_11**[7:0] (0xD3)) Bit[1:0]: clip_max[1:0] (valid with **DVP_CTRL_10**[7:0] (0xD2))

7   register tables

The following tables provide descriptions of the device control registers contained in the OV9712/OV9211. For all registers enable/disable bits, ENABLE = 1 and DISABLE = 0. The device slave addresses are 0x60 for write and 0x61 for read.

7.1 system control [0x00 - 0x95]

table 7-1   system control registers (sheet 1 of 12)

address	register name	default value	R/W	description
0x00	GAIN	0x00	RW	AGC Gain Control This AGC register combines analog gain and digital gain Bit[7]: Digital gain 0: Apply digital gain only if gain ≥ 2x 1: Apply digital gain only if gain ≥ 4x Bit[6:0]: Analog gain
0x01	BLUE	0x40	RW	B Channel Offset MSBs for AWB (LSBs in register **BRL**[7:4] (0x06))
0x02	RED	0x40	RW	R Channel Offset MSBs for AWB (LSBs in register **BRL**[3:0] (0x06))
0x03	REG03	0x02	RW	Register 03 Bit[7:5]: VAEC ceiling 000: 1 frame 010: 2 frames 011: 3 frames 1xx: 7 frames Bit[4]: Reserved Bit[3:2]: Sensor vertical output size LSBs (MSBs in register **AVsize** (0x1A)) Bit[1:0]: Sensor vertical output start point LSBs (MSBs in register **VSTART** (0x19))
0x04	REG04	0x00	RW	Register 04 Bit[7]: Mirror Bit[6]: Vertical flip Bit[5:1]: Reserved Bit[0]: Group latch enable
0x05	GREEN	0x00	RW	G Channel Offset MSBs for AWB (LSBs in register **GL** (0x07))

table 7-1   system control registers (sheet 2 of 12)

address	register name	default value	R/W	description
0x06	BRL	0x00	RW	Bit[7:4]: B channel offset LSBs for AWB (MSBs in register **BLUE** (0x01)) Bit[3:0]: R channel offset LSBs for AWB (MSBs in register **RED** (0x02))
0x07	GL	0x00	RW	Bit[7:4]: G channel offset LSBs for AWB (MSBs in register **GREEN** (0x05)) Bit[3:0]: Reserved
0x08	REG08	0x00	RW	Bit[7:4]: H window size offset between sensor output and DSP output Bit[3:0]: V window size offset between sensor output and DSP output
0x09	COM2	0x00	RW	Common Control 2 Bit[7:5]: Reserved Bit[4]: Chip sleep mode Bit[3]: Reset sensor timing when mode changes Bit[2:0]: Reserved
0x0A	PIDH	0x97	R	Product ID MSBs (read only)
0x0B	PIDL	0x11	R	Product ID LSBs (read only)
0x0C	COM3	0x00	RW	Common Control 3 Bit[7:1]: Reserved Bit[0]: Single frame output
0x0D	COM4	0x01	RW	Common Control 4 Bit[7]: Reserved Bit[6]: Freeze AEC Bit[5]: Initiate BLC calculation manually Bit[4:2]: Reserved Bit[1]: Manual mode for tp level exposure Bit[0]: AEC step control 0: AEC max increasing step less than vertical black 1: AEC max increasing step has no limit

table 7-1   system control registers (sheet 3 of 12)

address	register name	default value	R/W	description
0x0E	COM5	0x40	RW	Common Control 5 Bit[7]: Reserved Bit[6]: BLC line selection 　　0: Electrical BLC 　　1: Optical BLC Bit[5:4]: Reserved Bit[3]: VAEC ON/OFF 　　0: OFF 　　1: ON Bit[2:1]: Reserved Bit[0]: AEC/AGC algorithm selection 　　0: Average-based 　　1: Histogram-based
0x0F	COM6	0x00	RW	Common Control 6 Bit[7:0]: Reserved
0x10	AEC	0x9A	RW	Automatic Exposure Control[7:0] (MSBs in register **AECH** (0x16))
0x11	CLK	0x00	RW	Clock Rate Control Bit[7:6]: Reserved Bit[5:0]: Clock divider SysClk = CLK3 / (decimal value of CLK[5:0] + 1) / 2 (see **figure 2-3**)
0x12	COM7	0x40	RW	Common Control 7 Bit[7]: SRST 　　1: Initiates soft reset. All registers are set to factory default values after which the chip resumes normal operation Bit[6]: VT2 Down sample mode vertical timing Bit[5:2]: Reserved Bit[1]: Array color bar enable Bit[0]: HT2 Down sample mode horizontal timing

table 7-1 system control registers (sheet 4 of 12)

address	register name	default value	R/W	description
0x13	COM8	0x85	RW	Common Control 8 Bit[7]: AEC speed selection 0: Normal 1: Faster AEC adjustment Bit[6]: AEC step selection Bit[5]: Banding filter ON/OFF selection 0: OFF 1: ON Bit[4]: Reserved Bit[3]: LAEC ON/OFF select 0: OFF 1: ON Bit[2]: AGC auto/manual control selection Bit[1]: Reserved Bit[0]: Exposure auto/manual control selection 0: Manual 1: Auto
0x14	COM9	0x10	RW	Common Control 9 Bit[7:5]: AGC gain ceiling 000: 2x analog gain 001: 4x analog gain 010: 8x analog gain 011: 16x analog gain 100: 16x analog gain plus 2x digital gain Bit[4]: Reserved Bit[3]: Enable AEC below banding value 0: Limit the minimum exposure time to 1/100 or 1/120 second under any light conditions when banding filter is enabled 1: Allow exposure time to be less than 1/100 or 1/120 second under strong light conditions when banding filter is enabled Bit[2]: Reserved Bit[1]: Enable frame drop function Bit[0]: Reserved

table 7-1 system control registers (sheet 5 of 12)

address	register name	default value	R/W	description

0x15	COM10	0x00	RW	Common Control 10
				Bit[7]: HSYNC swap
				    0: HSYNC
				    1: HREF
				Bit[6]: HREF pin output swap
				    0: HREF
				    1: HSYNC
				Bit[5:4]: Reserved
				Bit[3]: HREF polarity
				    0: Output positive HREF
				    1: Output negative HREF for valid data
				Bit[2]: Reserved
				Bit[1]: VSYNC polarity
				    0: Positive
				    1: Negative
				Bit[0]: HSYNC polarity
				    0: Positive
				    1: Negative

0x16	AECH	0x01	RW	Automatic Exposure Control[15:8] (LSBs in register **AEC** (0x10))
0x17	HSTART	0x26	RW	Sensor Horizontal Output Start Point MSBs (LSBs in register **REG32**[2:0] (0x32))
0x18	AHsize	0xA2	RW	Sensor Horizontal Output Size MSBs (LSBs in register **REG32**[5:3] (0x32))
0x19	VSTART	0x01	RW	Sensor Vertical Output Start Point MSBs (LSBs in register **REG03**[1:0] (0x03))
0x1A	AVsize	0xC8	RW	Sensor Vertical Output Size MSBs (LSBs in register **REG03**[3:2] (0x03))
0x1B	PSHIFT	0x81	RW	Pixel Shift
0x1C	MIDH	0x7F	R	Manufacturer ID Byte – High
0x1D	MIDL	0xA2	R	Manufacturer ID Byte – Low
0x1E	COM11	0x00	RW	Common Control 11 Bit[7:0]: Reserved
0x1F	REG1F	0x00	RW	LSBs for Tp Level Exposure Control when exposure is less than one line (MSBs in register **COM28** (0x3C))
0x20	COM12	0x00	RW	Common Control 12 Bit[7:0]: Reserved

table 7-1　system control registers (sheet 6 of 12)

address	register name	default value	R/W	description
0x21	COM13	0x03	RW	Common Control 13 Bit[7:6]:　Reserved Bit[5:4]:　Automatically trigger VAEC when gain is greater than: 　00:　2x 　01:　4x 　10:　8x 　11:　16x Bit[3:0]:　Reserved
0x22	COM14	0x00	RW	Common Control 14 Bit[7:6]:　Reserved Bit[5:0]:　Maximum smooth banding steps in terms of row exposure
0x23	COM15	0x00	RW	Common Control 15 Bit[7:0]:　Reserved
0x24	WPT	0x60	RW	Luminance Signal High Range for AEC/AGC Operation
0x25	BPT	0x55	RW	Luminance Signal Low Range for AEC/AGC Operation
0x26	VPT	0x92	RW	Fast Mode Large Step Range Thresholds – effective only in AEC/AGC fast mode
0x27	COM16	0x00	RW	Common Control 16 Bit[7:0]:　Reserved
0x28	COM17	0x00	RW	Common Control 17 Bit[7:0]:　Reserved
0x29	COM18	0x00	RW	Common Control 18 Bit[7:0]:　Reserved
0x2A	REG2A	0x9B	RW	Horizontal Tp Counter End Point LSBs (MSBs in register **REG2B** (0x2B))
0x2B	REG2B	0x06	RW	Horizontal Tp Counter End Point MSBs (LSBs in register **REG2A** (0x2A))
0x2C	COM19	0x50	RW	Common Control 19 Bit[7:0]:　Reserved
0x2D	REG2D	0x00	RW	LSBs for Automatically Inserted Dummy Lines in Night Mode (MSBs in register **REG2E** (0x2E))
0x2E	REG2E	0x00	RW	MSBs for Automatically Inserted Dummy Lines in Night Mode (LSBs in register **REG2D** (0x2E))
0x2F	YAVG	0x00	RW	Luminance Average Value

table 7-1   system control registers (sheet 7 of 12)

address	register name	default value	R/W	description
0x30	REG30	0x08	RW	HSYNC Start Point
0x31	REG31	0x20	RW	HSYNC Stop Point
0x32	REG32	0x01	RW	Register 32 Bit[7:6]: Reserved Bit[5:3]: Sensor horizontal output size length LSBs (MSBs in register **AHsize** (0x18)) Bit[2:0]: Sensor horizontal output start point LSBs (MSBs in register **HSTART** (0x17))
0x33~ 0x36	RSVD	–	–	Reserved
0x37	COM24	0x02	RW	Common Control 24 Bit[7:4]: Reserved Bit[3]: Trigger BLC manually for 64 frames Bit[2]: BLC select 0: BLC triggered by gain change 1: BLC is always ON, meaning BLC offsets are adjusted every frame Bit[1:0]: Reserved
0x38	COM25	0x10	RW	Common Control 25 Bit[7:5]: Reserved Bit[4]: AWB_gain write options 0: ISP controls white balance function 1: Manual white balance control Bit[3:0]: Reserved
0x39~ 0x3B	RSVD	–	–	Reserved
0x3C	COM28	0x00	RW	MSBs for Tp Level Exposure Control when exposure is less than one line (LSBs in register **REG1F** (0x1F))
0x3D	RENDL	0x3C	RW	R Counter End Point LSBs (MSBs in register **RENDH** (0x3E))
0x3E	RENDH	0x03	RW	R Counter End Point MSBs (LSBs in register **RENDL** (0x3E))
0x3F~ 0x40	RSVD	–	–	Reserved

table 7-1   system control registers (sheet 8 of 12)

address	register name	default value	R/W	description
0x41	REG41	0x82	RW	Register 41 Bit[7]: BLC window enable Bit[6:4]: Reserved Bit[3:0]: BLC target base
0x42	REG42	0x14	RW	Register 42 Bit[7:0]: Reserved
0x43	REG43	0xC0	RW	Register 43 Bit[7:6]: BLC line selection 00: Not used 01: Only selects red line as BLC line 10: Only selects blue line as BLC line 11: Selects both blue line and red line as BLC line Bit[5:0]: Reserved
0x44	ROFFS	–	R	LSBs for BLC Offset of R Channel (MSBs in register **HOFFS**[1:0] (0x48))
0x45	BOFFS	–	R	LSBs for BLC Offset of B Channel (MSBs in register **HOFFS**[3:2] (0x48))
0x46	GrOFFS	–	R	LSBs for BLC Offset of Gr Channel (MSBs in register **HOFFS**[5:4] (0x48))
0x47	GbOFFS	–	R	LSBs for BLC Offset of Gb Channel (MSBs in register **HOFFS**[7:6] (0x48))
0x48	HOFFS	–	R	Bit[7:6]: MSBs for BLC offset of Gb channel (LSBs in register **GbOFFS** (0x47)) Bit[5:4]: MSBs for BLC offset of Gr channel (LSBs in register **GrOFFS** (0x46)) Bit[3:2]: MSBs for BLC offset of B channel (LSBs in register **BOFFS** (0x45)) Bit[1:0]: MSBs for BLC offset of R channel (LSBs in register **ROFFS** (0x44))
0x49	REG49	0x00	RW	Banding Step LSBs (MSBs in register **REG4A**[1:0] (0x4A))
0x4A	REG4A	0xD0	RW	Register 4A Bit[7:2]: Reserved Bit[1:0]: Banding step MSBs (LSBs in register **REG49** (0x49))
0x4B~0x4D	RSVD	–	–	Reserved

table 7-1 system control registers (sheet 9 of 12)

address	register name	default value	R/W	description

0x4E	REG4E	0x55	RW	16-Zone Y Average Select
				Bit[7:6]: Zone 4
				  00: Not allowed
				  01: Weight x1
				  10: Weight x2
				  11: Weight x4
				Bit[5:4]: Zone 3
				  00: Not selected
				  01: Weight x1
				  10: Weight x2
				  11: Weight x4
				Bit[3:2]: Zone 2
				  00: Not allowed
				  01: Weight x1
				  10: Weight x2
				  11: Weight x4
				Bit[1:0]: Zone 1
				  00: Not allowed
				  01: Weight x1
				  10: Weight x2
				  11: Weight x4

0x4F	REG4F	0x55	RW	16-Zone Y Average Select
				Bit[7:6]: Zone 8
				  00: Not allowed
				  01: Weight x1
				  10: Weight x2
				  11: Weight x4
				Bit[5:4]: Zone 7
				  00: Not allowed
				  01: Weight x1
				  10: Weight x2
				  11: Weight x4
				Bit[3:2]: Zone 6
				  00: Not allowed
				  01: Weight x1
				  10: Weight x2
				  11: Weight x4
				Bit[1:0]: Zone 5
				  00: Not allowed
				  01: Weight x1
				  10: Weight x2
				  11: Weight x4

table 7-1   system control registers (sheet 10 of 12)

address	register name	default value	R/W	description
0x50	REG50	0x55	RW	16-Zone Y Average Select Bit[7:6]: Zone 12 　00: Not allowed 　01: Weight x1 　10: Weight x2 　11: Weight x4 Bit[5:4]: Zone 11 　00: Not allowed 　01: Weight x1 　10: Weight x2 　11: Weight x4 Bit[3:2]: Zone 10 　00: Not allowed 　01: Weight x1 　10: Weight x2 　11: Weight x4 Bit[1:0]: Zone 9 　00: Not allowed 　01: Weight x1 　10: Weight x2 　11: Weight x4
0x51	REG51	0x55	RW	16-Zone Y Average Select Bit[7:6]: Zone 16 　00: Not allowed 　01: Weight x1 　10: Weight x2 　11: Weight x4 Bit[5:4]: Zone 15 　00: Not allowed 　01: Weight x1 　10: Weight x2 　11: Weight x4 Bit[3:2]: Zone 14 　00: Not allowed 　01: Weight x1 　10: Weight x2 　11: Weight x4 Bit[1:0]: Zone 13 　00: Not allowed 　01: Weight x1 　10: Weight x2 　11: Weight x4
0x52~ 0x54	RSVD	–	–	Reserved

table 7-1 system control registers (sheet 11 of 12)

address	register name	default value	R/W	description
0x55	REG55	0xFF	RW	Data Pins In/Out Control (0: input; 1: output) Bit[7]:　　Y7 Bit[6]:　　Y6 Bit[5]:　　Y5 Bit[4]:　　Y4 Bit[3]:　　Y3 Bit[2]:　　Y2 Bit[1]:　　Y1 Bit[0]:　　Y0
0x56	REG56	0x1F	RW	In/Out Control (0: input; 1: output) Bit[7:5]:　Reserved Bit[4]:　　HREF Bit[3]:　　VSYNC Bit[2]:　　PCLK Bit[1]:　　Y9 Bit[0]:　　Y8
0x57	REG57	0x00	RW	Register 57 Bit[7:5]:　Reserved Bit[4:2]:　DSP output horizontal size LSBs (MSBs in register **REG59** (0x59)) Bit[1:0]:　DSP output vertical size LSBs (MSBs in register **REG58** (0x58))
0x58	REG58	0xC8	RW	DSP Output Vertical Size MSBs (LSBs in register **REG57**[1:0] (0x57))
0x59	REG59	0xA0	RW	DSP Output Horizontal Size MSBs (LSBs in register **REG57**[4:2] (0x57))
0x5A~0x5B	RSVD	–	–	Reserved
0x5C	REG5C	0x59	RW	Register 5C Bit[7]:　　Reserved Bit[6:5]:　PLL pre-divider 　　　　　0x:　÷ 1 　　　　　10:　÷ 2 　　　　　11:　÷ 4 Bit[4:0]:　PLL_d 　　　　　PLL multiplier 　　　　　CLK2 = CLK1 × (32 – PLL_d) 　　　　　(see **figure 2-3**)

table 7-1   system control registers (sheet 12 of 12)

address	register name	default value	R/W	description
0x5D	REG5D	0xC4	RW	Register 5D Bit[7]: Reserved Bit[6]: Bypass PLL Bit[5:4]: Output drive capability control 00: 1x 01: 2x 10: 3x 11: 4x Bit[3:2]: PLL_sel PLL divider control CLK3 = CLK2 / (PLL_sel + 1) (see **figure 2-3**) Bit[1:0]: Reserved
0x5E~ 0x71	RSVD	–	–	Reserved
0x72	REG72	0x60	RW	Upper Limit of Luminance Level for B Pixels
0x73	REG73	0x49	RW	Lower Limit of Luminance Level for W Pixels
0x74	REG74	0x40	RW	Upper Limit of Luminance Level for VB pixels
0x75	REG75	0xE0	RW	Lower Limit of Luminance Level for VW pixels
0x76	REG76	0xC0	RW	Lower Limit of Probability for B Pixels to Trigger Auto AEC/AGC If B pixel probability > **REG76**, AEC/AGC will increase automatically
0x77	REG77	0xC0	RW	Lower Limit of Probability for W Pixels to Trigger Auto AEC/AGC If W pixel probability > **REG77**, AEC/AGC will increase automatically
0x78	REG78	0xFF	RW	Lower Limit of Probability for B Pixels to Trigger Fast AEC/AGC If B pixel probability > **REG78**, AEC/AGC will increase in fast mode
0x79	REG79	0xFF	RW	Lower Limit of Probability for W Pixels to Trigger Fast AEC/AGC If W pixel probability > **REG79**, AEC/AGC will increase in fast mode
0x7A~ 0x95	RSVD	–	–	Reserved

7.2 DSP control [0x96 - 0xFF]

table 7-2   DSP control registers (sheet 1 of 13)

address	register name	default value	R/W	description
0x96	DSP_CTRL_0	0xF9	RW	DSP Control 0 Bit[7]: Black pixel correction enable 0: Disable 1: Enable Bit[6]: White pixel correction enable 0: Disable 1: Enable Bit[5]: AWB gain enable 0: Disable 1: Enable Bit[4]: AWB enable 0: Disable 1: Enable Bit[3]: Lens correction enable 0: Disable 1: Enable Bit[2]: Lens correction gain coefficient enable 0: Disable 1: Enable Bit[1]: Reserved Bit[0]: ISP enable 0: Disable 1: Enable
0x97	DSP_CTRL_1	0x80	RW	DSP Control 1 Bit[7]: smph_mean Enable computation of mean value Bit[6:4]: Reserved Bit[3]: bar_en Enable/disable color bar output Bit[2]: sht_neg Enable delay of data HREF/valid clock Bit[1:0]: bar_style Select type of color bar to output
0x98	DSP_CTRL_2	0x00	RW	DSP Control 2 Bit[7:0]: pre_out_hoff[7:0] Horizontal offset of the pre_win output (valid with **DSP_CTRL_4**[2:0] (0x9A))
0x99	DSP_CTRL_3	0x00	RW	DSP Control 3 Bit[7:0]: pre_out_voff[7:0] Vertical offset of the pre_win output (valid with **DSP_CTRL_4**[5:4] (0x9A))

table 7-2   DSP control registers (sheet 2 of 13)

address	register name	default value	R/W	description
0x9A	DSP_CTRL_4	0x00	RW	DSP Control 4 Bit[7:6]: Reserved Bit[5:4]: pre_out_voff[9:8] Vertical offset of the pre_win output (valid with **DSP_CTRL_3**[7:0] (0x99)) Bit[3]: Reserved Bit[2:0]: pre_out_hoff[10:8] Horizontal offset of the pre_win output (valid with **DSP_CTRL_2**[7:0] (0x98))
0x9B	DSP_CTRL_5	0x04	RW	DSP Control 5 Bit[7:4]: pre_pad_vrgt Padding the column number in pre_winc Bit[3:0]: pre_pad_hrgt Padding the row number in pre_win
0x9C	DSP_CTRL_6	0x00	RW	DSP Control 6 Bit[7:0]: blk_thresh Black threshold used in YAVG
0x9D	DSP_CTRL_7	0xFF	RW	DSP Control 7 Bit[7:0]: wht_thresh White threshold used in YAVG
0x9E	LENC_CTRL_0	0x00	RW	LENC Control 0 Bit[7:0]: det_coef_man Manual value of the LENC gain coefficient
0x9F	LENC_CTRL_1	0x80	RW	LENC Control 1 Bit[7:0]: lenc_coef_th
0xA0	LENC_CTRL_2	0xF1	RW	LENC Control 2 Bit[7:4]: lenc_gain_thre2[3:0] High threshold of the LENC gain (valid with **LENC_CTRL_3**[1] (0xA1)) Bit[3:0]: lenc_gain_thre1[3:0] Low threshold of the LENC gain (valid with **LENC_CTRL_3**[0] (0xA1))

table 7-2   DSP control registers (sheet 3 of 13)

address	register name	default value	R/W	description
0xA1	LENC_CTRL_3	0x0D	RW	LENC Control 3 Bit[7:5]: Reserved Bit[4]: center_man Manually selects center of R, G, B circle Bit[3]: md_en Signal indicating if the result is rounded off Bit[2]: det_coef_man_en Enable manual mode of the LENC gain coef Bit[1]: lenc_gain_thre2[4] High threshold of the LENC gain (valid with **LENC_CTRL_2**[7:4] (0xA0)) Bit[0]: lenc_gain_thre1[4] Low threshold of the LENC gain (valid with **LENC_CTRL_2**[3:0] (0xA0))
0xA2	LENC_CTRL_4	0x00	RW	LENC Control 4 Bit[7:0]: lenc_off_man[7:0] Black level manual setting for LENC. Range from 0 to 255.
0xA3	LENC_CTRL_5	0x80	RW	LENC Control 5 Bit[7:0]: R_X0[7:0] R_X0 is the horizontal center position in red color channels. It should be fixed as the horizontal position of the image which comes from the middle of the lens, so it is usually set as the horizontal position of the middle pixel of each image. Range from 0 to 1296. Valid with **LENC_CTRL_7**[2:0] (0xA5).
0xA4	LENC_CTRL_6	0x90	RW	LENC Control 6 Bit[7:0]: R_Y0[7:0] R_Y0 is the vertical center position in red color channels. It should be fixed as the vertical position of the image which comes from the middle of the lens, so it is usually set as the vertical position of the middle pixel of each image. Range from 0 to 800. Valid with **LENC_CTRL_7**[5:4] (0xA5).

table 7-2   DSP control registers (sheet 4 of 13)

address	register name	default value	R/W	description
0xA5	LENC_CTRL_7	0x12	RW	LENC Control 7 Bit[7:6]: Reserved Bit[5:4]: R_Y0[9:8] Valid with **LENC_CTRL_6**[7:0] (0xA4) Bit[3]: Reserved Bit[2:0]: R_X0[9:8] Valid with **LENC_CTRL_5**[7:0] (0xA3)
0xA6	LENC_CTRL_8	0x22	RW	LENC Control 8 Bit[7]: Reserved Bit[6:0]: R_A1 Composed of the first group of factors used in the LENC correction of the red color channels.
0xA7	LENC_CTRL_9	0xC2	RW	LENC Control 9 Bit[7:0]: R_B1 Composed of the second group of factors used in the LENC correction of the red color channels.
0xA8	LENC_CTRL_10	0x87	RW	LENC Control 10 Bit[7:4]: R_B2 Composed of the second group of factors used in the LENC correction of the red color channels. Bit[3:0]: R_A2 Composed of the first group of factors used in the LENC correction of the red color channels.
0xA9	LENC_CTRL_11	0x80	RW	LENC Control 11 Bit[7:0]: G_X0[7:0] G_X0 is the horizontal center position in green color channels. It should be fixed as the horizontal position of the image which comes from the middle of the lens, so it is usually set as the horizontal position of the middle pixel of each image. Range from 0 to 1296. Valid with **LENC_CTRL_13**[2:0] (0xAB).

table 7-2 DSP control registers (sheet 5 of 13)

address	register name	default value	R/W	description
0xAA	LENC_CTRL_12	0x90	RW	LENC Control 12 Bit[7:0]: G_Y0[7:0] G_Y0 is the vertical center position in green color channels. It should be fixed as the vertical position of the image which comes from the middle of the lens, so it is usually set as the vertical position of the middle pixel of each image. Range from 0 to 800. Valid with **LENC_CTRL_13**[5:4] (0xAB).
0xAB	LENC_CTRL_13	0x12	RW	LENC Control 13 Bit[7:6]: Reserved Bit[5:4]: G_Y0[9:8] Valid with **LENC_CTRL_12**[7:0] (0xAA) Bit[3]: Reserved Bit[2:0]: G_X0[9:8] Valid with **LENC_CTRL_11**[7:0] (0xA9)
0xAC	LENC_CTRL_14	0x22	RW	LENC Control 14 Bit[7]: Reserved Bit[6:0]: G_A1 Composed of the first group of factors used in the LENC correction of the green color channels.
0xAD	LENC_CTRL_15	0xC2	RW	LENC Control 15 Bit[7:0]: G_B1 Composed of the second group of factors used in the LENC correction of the green color channels.
0xAE	LENC_CTRL_16	0x87	RW	LENC Control 16 Bit[7:4]: G_B2 Composed of the second group of factors used in the LENC correction of the green color channels. Bit[3:0]: G_A2 Composed of the first group of factors used in the LENC correction of the green color channels.

table 7-2   DSP control registers (sheet 6 of 13)

address	register name	default value	R/W	description
0xAF	LENC_CTRL_17	0x80	RW	LENC Control 17 Bit[7:0]: B_X0[7:0] B_X0 is the horizontal center position in blue color channels. It should be fixed as the horizontal position of the image which comes from the middle of the lens, so it is usually set as the horizontal position of the middle pixel of each image. Range from 0 to 1296. Valid with **LENC_CTRL_19**[2:0] (0xB1).
0xB0	LENC_CTRL_18	0x90	RW	LENC Control 18 Bit[7:0]: B_Y0[7:0] B_Y0 is the vertical center position in blue color channels. It should be fixed as the vertical position of the image which comes from the middle of the lens, so it is usually set as the vertical position of the middle pixel of each image. Range from 0 to 800. Valid with **LENC_CTRL_19**[5:4] (0xB1).
0xB1	LENC_CTRL_19	0x12	RW	LENC Control 19 Bit[7:6]: Reserved Bit[5:4]: B_Y0[9:8] Valid with **LENC_CTRL_18**[7:0] (0xB0) Bit[3]: Reserved Bit[2:0]: B_X0[9:8] Valid with **LENC_CTRL_17**[7:0] (0xAF)
0xB2	LENC_CTRL_20	0x22	RW	LENC Control 20 Bit[7]: Reserved Bit[6:0]: B_A1 Composed of the first group of factors used in the LENC correction of the blue color channels.
0xB3	LENC_CTRL_21	0xC2	RW	LENC Control 21 Bit[7:0]: B_B1 Composed of the second group of factors used in the LENC correction of the blue color channels.

table 7-2   DSP control registers (sheet 7 of 13)

address	register name	default value	R/W	description
0xB4	LENC_CTRL_22	0x87	RW	LENC Control 22 Bit[7:4]: B_B2 Composed of the second group of factors used in the LENC correction of the blue color channels. Bit[3:0]: B_A2 Composed of the first group of factors used in the LENC correction of the blue color channels.
0xB5	LENC_CTRL_23	0x00	RW	LENC Control 23 Bit[7:3]: Reserved Bit[2]: v_skip[1:0] Bit[1]: Reserved Bit[0]: h_skip[1:0]
0xB6	AWB_CTRL_0	0x07	RW	AWB Control 0 Bit[7:4]: Reserved Bit[3]: awb_off_man_en Enable manual AWB bias 0: From sensor_bias 1: From AWB_off_man Bit[2]: awb_fast AWB in fast mode Bit[1]: awb_bias_on Enable the AWB bias 0: Disable 1: Enable Bit[0]: awb_bias_plus Decides if the AWB_bias is added back when the AWB_gain is finished
0xB7	AWB_CTRL_1	0x00	RW	AWB Control 1 Bit[7:0]: awb_off_man Manual value of the AWB_bias
0xB8	AWB_CTRL_2	0x04	RW	AWB Control 2 Bit[7:0]: stable_range Stable range when computing the gain value for R, G, and B in the AWB module
0xB9	AWB_CTRL_3	0x08	RW	AWB Control 3 Bit[7:0]: stable_rangew Range after the gain for R, G, and B is stable
0xBA	AWB_CTRL_4	0x00	RW	AWB Control 4 Bit[7:0]: awb_frame_cnt After AWB, AWB can output the gain for R, G, and B

table 7-2   DSP control registers (sheet 8 of 13)

address	register name	default value	R/W	description
0xBB	AWB_CTRL_5	0x20	RW	AWB Control 5 Bit[7:0]: awb_delta
0xBC	WBC_CTRL_0	0x68	RW	WBC Control 0 Bit[7:0]: Reserved
0xBD	YAVG_CTRL_0	0xA0	RW	YAVG Control 0 Bit[7:0]: yavg_winh
0xBE	YAVG_CTRL_1	0xC8	RW	YAVG Control 1 Bit[7:0]: yavg_winv
0xBF	YAVG_CTRL_2	0x00	RW	YAVG Control 2 Bit[7:0]: yavg_winofh[7:0] (valid with **YAVG_CTRL_4**[2:0] (0xC1))
0xC0	YAVG_CTRL_3	0x00	RW	YAVG Control 3 Bit[7:0]: yavg_winofv[7:0] (valid with **YAVG_CTRL_4**[5:4] (0xC1))
0xC1	YAVG_CTRL_4	0x00	RW	YAVG Control 4 Bit[7]: yavg_win_man Bit[6]: Reserved Bit[5:4]: yavg_winofv[9:8] (valid with **YAVG_CTRL_3**[7:0] (0xC0)) Bit[3]: Reserved Bit[2:0]: yavg_winofh[10:8] (valid with **YAVG_CTRL_2**[7:0] (0xBF))

table 7-2   DSP control registers (sheet 9 of 13)

address	register name	default value	R/W	description
0xC2	DVP_CTRL_00	0x80	RW	Bit[7:6]: VSYNC options 00: vsync_old 01: vsync_new 10: vsync3 11: Invalid Bit[5]: pclk_gate_en Gate dvp_pclk when there is no data transfer 0: Disable 1: Enable Bit[4]: vsync_gate Gate dvp_pclk when VSYNC && pclk_gate_en 0: Disable 1: Enable Bit[3]: vsync3_w_sel 0: VSYNC3 will go low when SOF 1: Use vsync_width × 64 as vsync3_width Bit[2]: pclk_pol 1: Reverse DVP_PCLK Bit[1]: href_pol 1: Reverse DVP_HREF Bit[0]: vsync_pol 0: VSYNC=1 is frame blanking time 1: VSYNC=0 is frame blanking

table 7-2   DSP control registers (sheet 10 of 13)

address	register name	default value	R/W	description

0xC3	DVP_CTRL_01	0x20	RW	DVP Control 01
				Bit[7]: ccir656_en
				   0: Disable
				   1: Enable
				Bit[6]: sync_code_sel
				   0: Auto generate sync code for CCIR656
				   1: Use FS, FE, LS, LE (registers **0xC4** to **0xC7**) as sync code
				Bit[5]: blk_656
				   0: CCIR656 data is 0x040 or 0x200
				   1: CCIR656 data is 0x000 when blanking
				Bit[4]: eav_first
				   1: CCIR656 sends EAV first
				Bit[3:1]: dvp_data_sequence
				   000: Y9,Y8,Y7,Y6,Y5,Y4,Y3,Y2 Y1,Y0
				   001: Y1,Y0,Y9,Y8,Y7,Y6,Y5,Y4, Y3,Y2
				   010: Y7,Y6,Y5,Y4,Y3,Y2,Y1,Y0, Y9,Y8
				   011: Reserved
				   100: Y0,Y1,Y2,Y3,Y4,Y5,Y6,Y7, Y8,Y9
				   101: Y8,Y9,Y0,Y1,Y2,Y3,Y4,Y5, Y6,Y7
				   110: Y2,Y3,Y4,Y5,Y6,Y7,Y8,Y9, Y0,Y1
				   111: Reserved
				Bit[0]: chg_flag
				   Write 1 to this bit will generate change flag for HSYNC mode. This bit will auto clear. DVP will restart to calculate all timing parameters and output a frame.

0xC4	DVP_CTRL_02	0xAB	RW	DVP Control 02 Bit[7:0]: FS for CCIR656
0xC5	DVP_CTRL_03	0xB6	RW	DVP Control 03 Bit[7:0]: FE for CCIR656
0xC6	DVP_CTRL_04	0x80	RW	DVP Control 04 Bit[7:0]: LS for CCIR656
0xC7	DVP_CTRL_05	0x9D	RW	DVP Control 05 Bit[7:0]: LE for CCIR656

table 7-2 DSP control registers (sheet 11 of 13)

address	register name	default value	R/W	description

0xC8	DVP_CTRL_06	0x00	RW	DVP Control 06
				Bit[7]: blk_tog
				  1: dvp_data will toggle when blanking
				Bit[6]: vsync_width_sel
				  0: Use vsync_widthx64 as VSYNC width
				  1: Select 4x line length as VSYNC width
				Bit[5:3]: h2v_dly
				  VSYNC to HREF delay for vsync_new
				Bit[2:0]: v2h_dly
				  HREF to VSYNC delay for vsync_new

0xC9	DVP_CTRL_07	0x80	RW	DVP Control 07 Bit[7:0]: vsync_width_l vsync_width_real =vsync_width × 64

0xCA	DVP_CTRL_08	0x20	RW	DVP Control 08
				Bit[7:6]: vsync_width_h
				Bit[5:4]: sof2h_dly_offset
				Bit[3]: ddr_phase
				  0: First pixel is at rising edge
				  1: First pixel is at falling edge
				Bit[2]: Test pattern options
				  0: 10-bit
				  1: 8-bit
				Bit[1:0]: Test pattern mode
				  00: No test pattern
				  01: 1, 2, 4, 8,...
				  10: 1, 1, 2, 2,...

table 7-2   DSP control registers (sheet 12 of 13)

address	register name	default value	R/W	description
0xCB	DVP_CTRL_09	0xA6	RW	DVP Control 09 Bit[7]: sof_rst_en 1: DVP state machine will be reset by SOF Bit[6:5]: chg_sel for recalculating DVP timing for HSYNC mode 00: Select SNR change and manual change (manual change flag is in register **DVP_CTRL_01**[0] (0xC3)) 01: Select auto detect change and manual change 10: Manually set change Bit[4]: hsync_en 1: Enable HSYNC mode (see **figure 6-1**) Bit[3]: hsync_dvp_en 1: v2h_dly, h2v_dly and line_length are fixed for each frame (see **figure 6-1**) Bit[2]: hsync_1st_en 0: Mask the first frame when in HSYNC mode Bit[1:0]: line_length_sel 00: Select line_length_snr 01: Select line_length_reg 10: Select line_length_auto
0xCC	DVP_CTRL_0A	0x40	RW	DVP Control 0A Bit[7:4]: FIFO_BUF size Bit[3:0]: dmy_line_nu Use CCIR656 first dummy line number to generate VSYNC
0xCD	DVP_CTRL_0B	0x00	RW	DVP Control 0B Bit[7:0]: eof2v_dly[23:16]
0xCE	DVP_CTRL_0C	0x01	RW	DVP Control 0C Bit[7:0]: eof2v_dly[15:8]
0xCF	DVP_CTRL_0D	0x00	RW	DVP Control 0D Bit[7:0]: eof2v_dly[7:0]
0xD0	DVP_CTRL_0E	0xFF	RW	DVP Control 0E Bit[7:0]: line_length[15:8]
0xD1	DVP_CTRL_0F	0xFF	RW	DVP Control 0F Bit[7:0]: line_length[7:0]

table 7-2   DSP control registers (sheet 13 of 13)

address	register name	default value	R/W	description
0xD2	DVP_CTRL_10	0xFF	RW	DVP Control 10 Bit[7:0]: clip_max[9:2] DVP output data should be less than or equal to clip_max (valid with **DVP_CTRL_12**[1:0] (0xD4))
0xD3	DVP_CTRL_11	0x00	RW	DVP Control 11 Bit[7:0]: clip_min[9:2] DVP output data should be larger than or equal to clip_min (valid with **DVP_CTRL_12**[3:2] (0xD4))
0xD4	DVP_CTRL_12	0x03	RW	DVP Control 12 Bit[5]: f_tog_en 1: ccir_f will toggle every frame Bit[4]: ddr_en 1: DVP will output DDR clock Bit[3:2]: clip_min[1:0] (valid with **DVP_CTRL_11**[7:0] (0xD3)) Bit[1:0]: clip_max[1:0] (valid with **DVP_CTRL_10**[7:0] (0xD2))
0xD5	RSVD	–	–	Reserved
0xD6	SC_CTRL_0	0x0C	RW	SC Control 0 Bit[7]: Bypass DVP Bit[6]: Reserved Bit[5]: snr_rst_dvp Bit[4]: snr_rst_dsp Bit[3]: dvp_sclk_gate Bit[2]: dsp_sclk_gate Bit[1]: dvp_rst Bit[0]: dsp_rst
0xD7~ 0xFF	RSVD	–	–	Reserved

8 operating specifications

8.1 absolute maximum ratings

table 8-1 absolute maximum ratings

parameter		absolute maximum rating[a]
ambient storage temperature		-40°C to +125°C
supply voltage (with respect to ground)	V_{DD-A}	4.5V
	V_{DD-IO}	4.5V
electro-static discharge (ESD)	human body model	2000V
	machine model	200V
all input/output voltages (with respect to ground)		-0.3V to V_{DD-IO} + 1V
I/O current on any input or output pin		± 200 mA
peak solder temperature (10 second dwell time)		245°C

a. exceeding the absolute maximum ratings shown above invalidates all AC and DC electrical specifications and may result in permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

8.2 functional temperature

table 8-2 functional temperature

parameter	range
operating temperature[a]	-30°C to +70°C junction temperature
stable image temperature[b]	0°C to 50°C junction temperature

a. sensor functions but image quality may be noticeably different at temperatures outside of stable image range

b. image quality remains stable throughout this temperature range

8.3 DC characteristics

table 8-3 DC characteristics (-30°C < T_J < 70°C)

symbol	parameter	min	typ	max	unit
supply					
V_{DD-A}	supply voltage (analog)	3.0	3.3	3.6	V
V_{DD-D}	supply voltage (digital core)	1.425	1.5	1.575	V
V_{DD-IO}	supply voltage (digital I/O)	1.7	1.8	3.6	V
I_{DD-A}			22	30	mA
I_{DD-D}	active (operating) current		6	10	mA
I_{DD-IO}			8	14	mA
$I_{DDS-SCCB}$	standby current[a]		250	600	µA
$I_{DDS-PWDN}$			50	100	µA
digital inputs (typical conditions: AVDD = 3.3V, DVDD = 1.5V, DOVDD = 1.8V)					
V_{IL}	input voltage LOW			0.54	V
V_{IH}	input voltage HIGH	1.26			V
C_{IN}	input capacitor			10	pF
digital outputs (standard loading 25 pF)					
V_{OH}	output voltage HIGH	1.62			V
V_{OL}	output voltage LOW			0.18	V
serial interface inputs					
V_{IL}^{b}	SIOC and SIOD	-0.5	0	0.54	V
V_{IH}^{b}	SIOC and SIOD	1.26	1.8	2.3	V

a. standby current is measured at room temperature

b. based on DOVDD = 1.8V.

8.4 AC characteristics

table 8-4   AC characteristics (T_A = 25°C, V_{DD-A} = 2.8V)

symbol	parameter	min	typ	max	unit
ADC parameters					
B	analog bandwidth		30		MHz
DLE	DC differential linearity error		0.5		LSB
ILE	DC integral linearity error		1		LSB
	settling time for hardware reset			<1	ms
	settling time for software reset			<1	ms
	settling time for resolution mode change			<1	ms
	settling time for register setting			<300	ms

table 8-5   timing characteristics

symbol	parameter	min	typ	max	unit
oscillator and clock input					
f_{OSC}	frequency (XCLK)	6	24	27	MHz
t_r, t_f	clock input rise/fall time			5 (10[a])	ns

a.   if using the internal PLL

9 mechanical specifications

9.1 physical specifications

figure 9-1 package specifications

top view
(bumps down)

bottom view
(bumps up)

center of BGA (die) = center of the package

side view
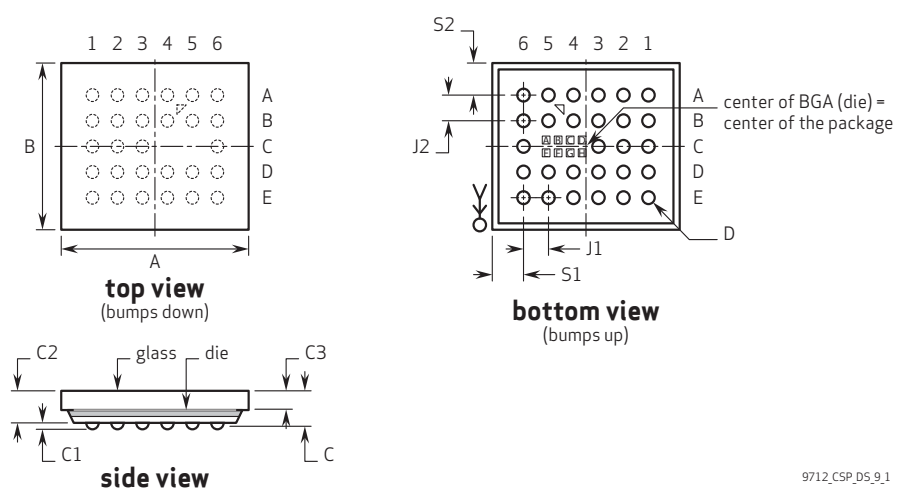
9712_CSP_DS_9_1

table 9-1 package dimensions

parameter	symbol	min	typ	max	unit
package body dimension x	A	5390	5415	5440	µm
package body dimension y	B	4390	4415	4440	µm
package height	C	845	905	965	µm
ball height	C1	150	180	210	µm
package body thickness	C2	680	725	770	µm
thickness of glass surface to wafer	C3	425	445	465	µm
ball diameter	D	320	350	380	µm
total pin count	N		28		
pin count x-axis	N1		6		
pin count y-axis	N2		5		
pins pitch x-axis	J1		800		µm
pins pitch y-axis	J2		750		µm
edge-to-pin center distance along x	S1	678	708	738	µm
edge-to-pin center distance along y	S2	678	708	738	µm

9.2 IR reflow specifications

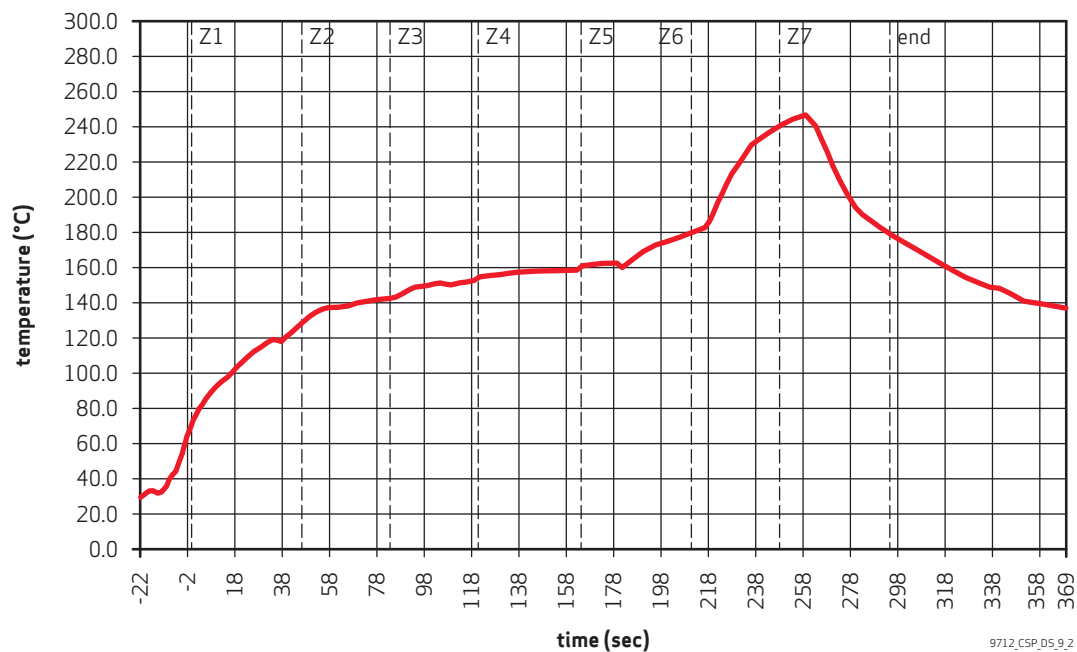**figure 9-2**   IR reflow ramp rate requirements

note

The OV9712/OV9211 uses a lead-free package.

table 9-2   reflow conditions

condition	exposure
average ramp-up rate (30°C to 217°C)	less than 3°C per second
> 100°C	between 330 - 600 seconds
> 150°C	at least 210 seconds
> 217°C	at least 30 seconds (30 ~ 120 seconds)
peak temperature	245°C
cool-down rate (peak to 50°C)	less than 6°C per second
time from 30°C to 245°C	no greater than 390 seconds

10 optical specifications

10.1 sensor array center

figure 10-1   sensor array center

top view
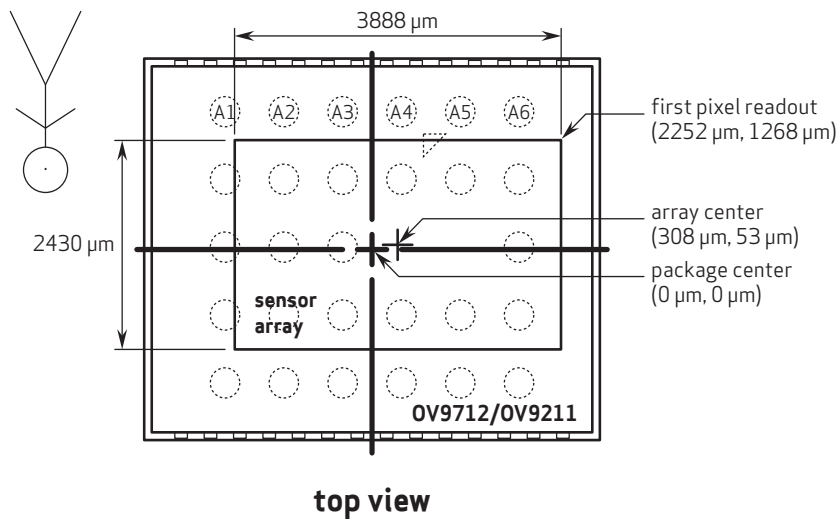
note 1 this drawing is not to scale and is for reference only.

note 2 as most optical assemblies invert and mirror the image, the chip is typically mounted with pins A1 to A6 oriented down on the PCB.

9712_CSP_DS_10_1

10.2 lens chief ray angle (CRA)

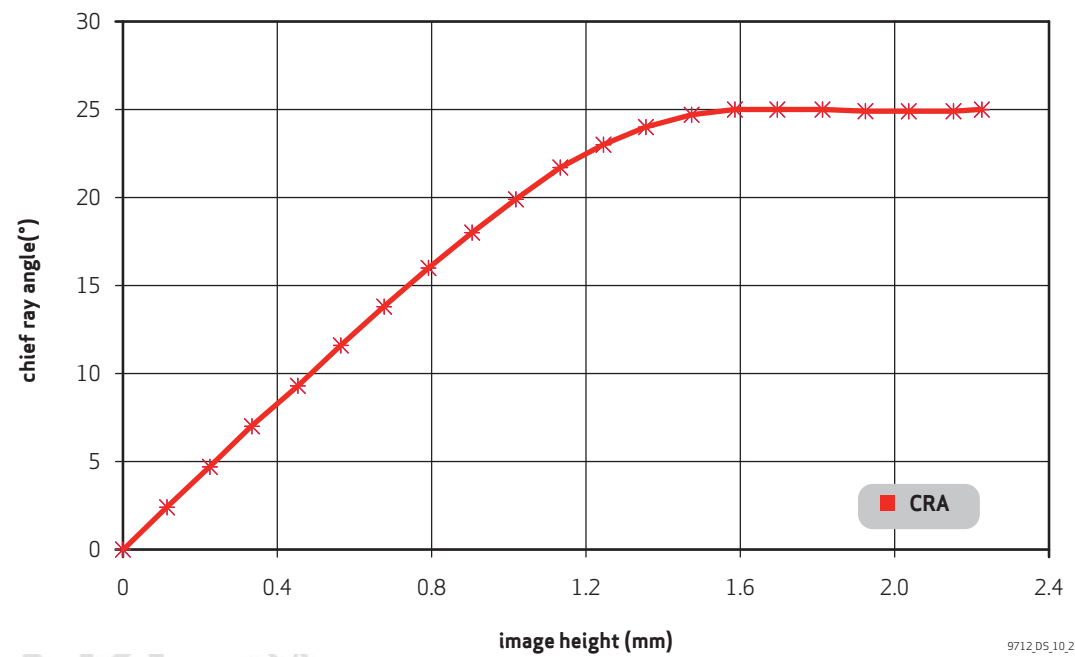**figure 10-2**   chief ray angle (CRA)

9712_DS_10_2

table 10-1   CRA versus image height plot (sheet 1 of 2)

field (%)	image height (mm)	CRA (degrees)
0.00	0.000	0.0
0.05	0.113	2.4
0.10	0.226	4.7
0.15	0.340	7.0
0.20	0.453	9.3
0.25	0.566	11.6
0.30	0.679	13.8
0.35	0.792	16.0
0.40	0.906	18.0
0.45	1.019	19.9
0.50	1.132	21.6

table 10-1   CRA versus image height plot (sheet 2 of 2)

field (%)	image height (mm)	CRA (degrees)
0.55	1.245	23.0
0.60	1.358	24.0
0.65	1.472	24.7
0.70	1.585	25.0
0.75	1.698	25.0
0.80	1.811	25.0
0.85	1.924	24.9
0.90	2.038	24.9
0.95	2.151	24.9
1.00	2.264	25.0

revision history

version 2.0   10.18.2013

- initial release

version 2.01   11.20.2013

- in table 7-1, changed register addresses from 0x74 to 0x76, 0x75 to 0x77, 0x76 to 0x74, 0x77 to 0x75, updated register names to reflect changes to register addresses, and changed default value for updated registers, register 0x74 from 0xC0 to 0x40, register 0x75 from 0xC0 to 0xE0, register 0x76 from 0xE0 to 0xC0, register 0x77 from 0xE0 to 0xC0

defining the future of digital imaging™

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