GMA301 ±6g Tri-Axial Digital Accelerometer

General Introduction

GMA 301 is a digital accelerometer and ±6g tri-axial embedded with 10-bit ADC. The functions are strengthening for motion applications like smart phone and tablet on smart connected devices. GMA301 integrate a sensing element and a conditioning CMOS IC in a compact 3×3×1 mm^3 package. The sensing element is a MEMS device. The CMOS IC provides interrupt signals and digital interface with build-in functions.

Features

- Tri-axial digital accelerometer with ±6g dynamic range
- 10 bit ADC embedded with I2C (slave address 0x18h with 7-bit format) digital interface supporting 400kHz high-speed mode.
- Flexible sampling rate from below 1 to 100Hz
- Temperature sensor for internal compensation and capable of digital output
- Operation voltage:
  - Analog Voltage: +1.8V~ +3.6V
  - Digital Voltage: +1.8V ~ +3.3V
- Power consumption:
  - Normal mode : typical 140uA at 100Hz ODR
  - Standby mode: typical 8uA
- Special low-power mode with current consumption below 60uA
- One interrupt pin as the selectable polarity with open-drain option and data-ready signal
- 3mm × 3mm × 1mm DFN package
- 5000g shock tolerance
- 10-pin DFN package with lead-free
- RoHS compliance

Applications

Smart user interface, gaming, motion detection

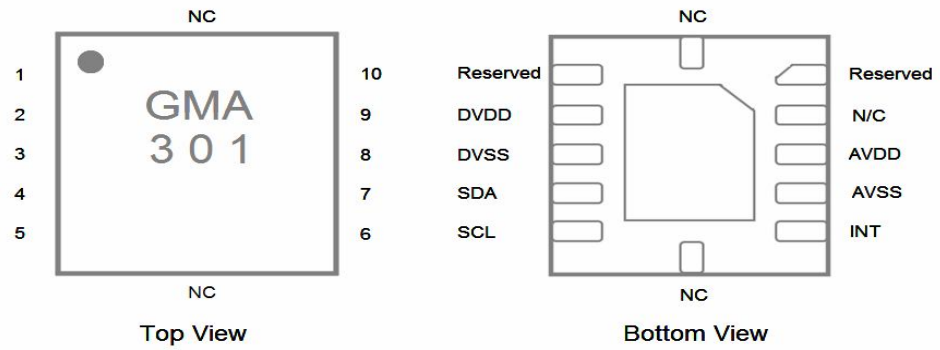


Figure 1 : GMA301

Figure 1: GMA301 Package Types

Specifications

Table 1: Pin Descriptions

Pin#	Pin Name	Description	Pin#	Pin Name	Description
1	NC	No connection inside	6	SCL	I2C serial clock
2	Reserved	Open	7	SDA	I2C serial data
3	AVDD	Analog power, 1.8~3.6V	8	DGND	Digital ground
4	AGND	Analog ground	9	DVCC	Digital power, 1.8~3.3V
5	INT	Interrupt signal	10	Reserved	Open

Example Functional Block Diagram

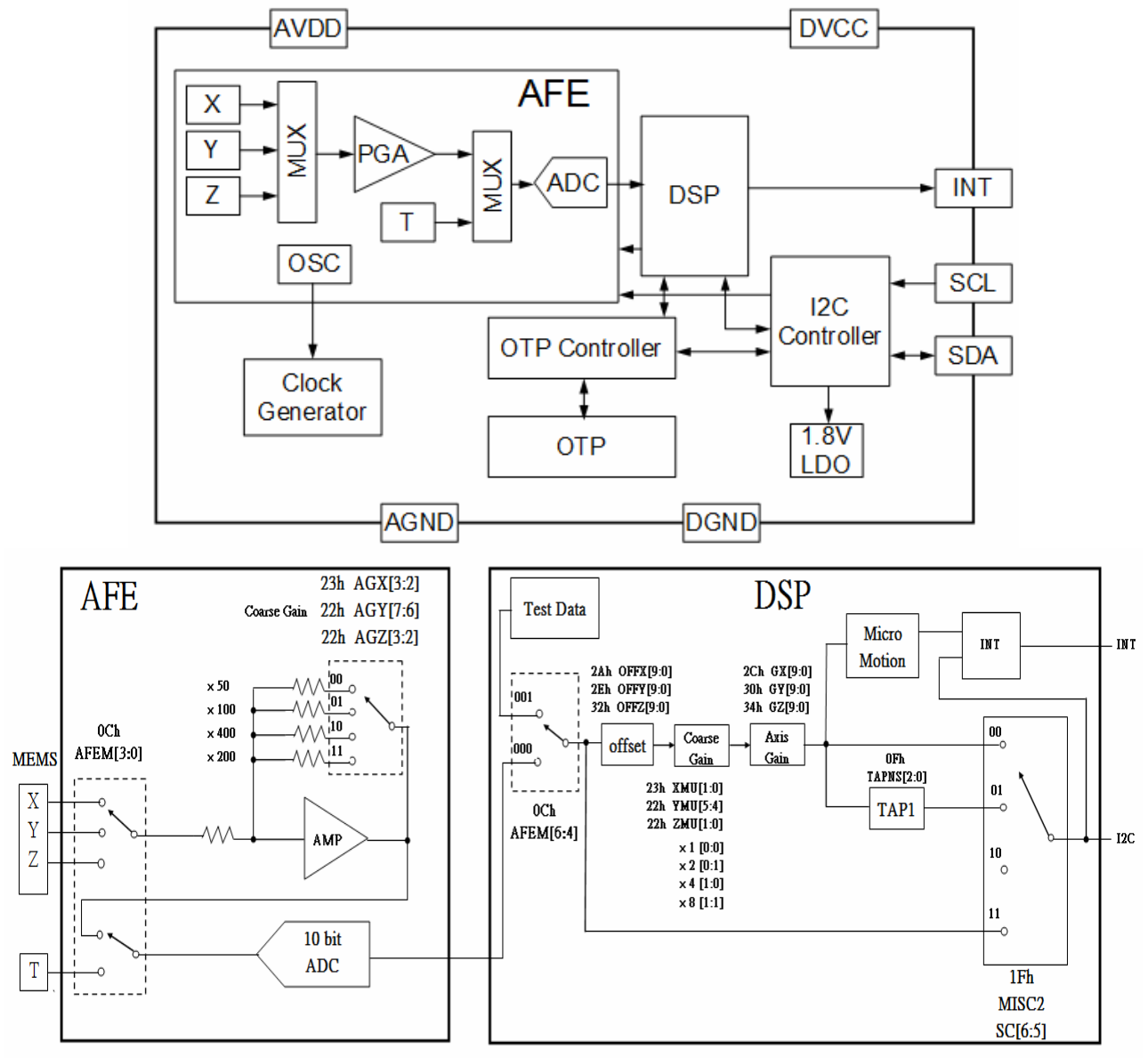


Figure 2: Block Diagram of GMA301

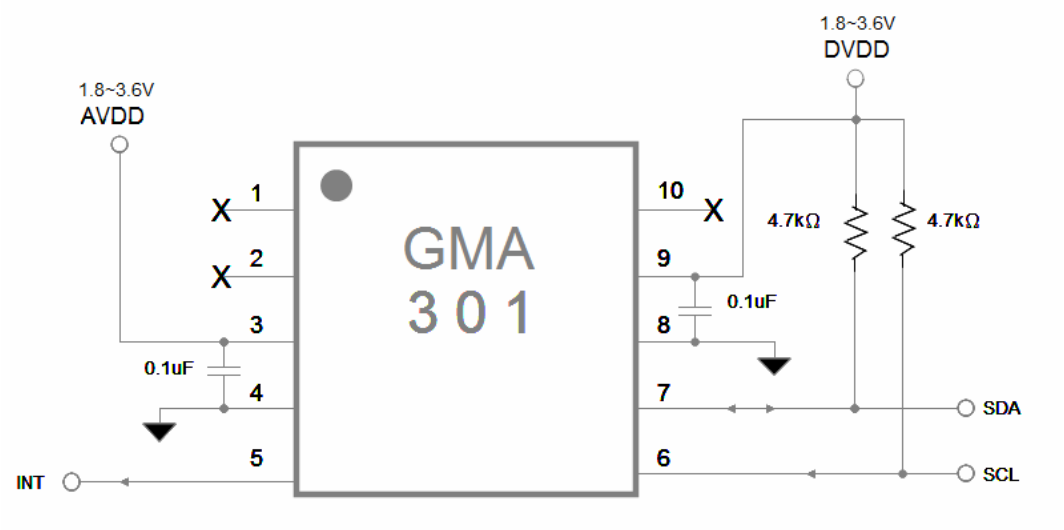


Figure 3: I2C Connection

Table 2: General Specification

Analog voltage V_{op} = 3V, environment temperature T_a = 25°C if not specified otherwise

Parameter	Conditions	Min.	Typ.	Max.	Unit
Analog Voltage Vop (AVDD)	T_a = -40°C ~ +85°C	1.8	3.0	3.6	V
Digital Voltage (DVCC)	T_a = -40°C ~ +85°C	1.8	—	3.3	V
Normal operating current	ODR = 100 Hz ODR = 50 Hz ODR = 25 Hz ODR = 12.5 Hz ODR = 6.25 Hz ODR = 3.125 Hz ODR = 1.5625 Hz ODR = 0.78125 Hz	—	140 120 110 105 104 103 102 100	—	uA
Low-power mode operating current	ODR = 12.5 Hz ODR = 6.25 Hz ODR = 3.125 Hz ODR = 1.5625 Hz ODR = 0.78125 Hz	—	60 50 43 35 30	—	uA
Standby current		—	8	15	uA
Dynamic range		—	±6	—	g
Sensitivity		61	64※	67	LSB/g
Zero-g offset, calibrated		—	±60	—	mg
Sensitivity to temp. dependency	T_a = -40°C ~ +85°C	—	±0.08	—	%/°C
Zero-g offset temp. dependency	T_a = -40°C ~ +85°C	—	±2	—	mg/°C
Nonlinearity		—	±2	—	%FS
Cross axis sensitivity		—	2	—	%
Noise		—	1.1	—	mg/√Hz
Operation temperature		-40	—	+85	°C
Storage temperature		-40	—	+125	°C

※ The apparent sensitivity for 10-bit ADC on ±6g dynamic range is 64 LSB/g.

Maximum Ratings

Table 3: Absolute Maximum Rating

Parameter	Rating
V_{op}-GND	-0.3 ~ 4 V
Any other pin voltage	GND-0.3 to V_{op}+0.3 V
Temperature Range (Storage)	−40°C to +125°C
ESD	2KV (HBM)
Mechanical Shock (unpowered)	5,000 g for 0.2ms
Freefall on concrete surface	1.5 m

Note: Stress above the absolute maximum rating as listed in Table 3 may cause permanent damage to the device

General Operation

Initialization

GMA 301 is a special sensing element when power-on will go to standby mode. Before that, we must take some initialization steps to start the unit for operations. Please used below the recommended steps to set GMA301 to the normal operation mode are shown as a typical example.

For other operation mode, please change the respective register setting as shown in the next section “Operation Modes”.

Step1. Read the STADR register (12h) and check the value should be 0x55h. If not, the sensor isn't connected or I2C communication is incorrect.

Step2. Write 0x52 to the PD register (21h). This will set the RST bit which reset the sensor.

Step3. Write the 5-byte sequence, 0x02, 0x12, 0x02, 0x82 and 0x02, to the ACTR register (00h) in one I2C transaction. This will download OTP data into internal parameter registers and enable internal clock then clear the data path.

Step4. Write 0x28 to the MISC2 register (1Fh). This will set the OSCAEN bit to enable oscillator for correct clock timing and selected calibrated data as output.

Step5. Write 0x8F to the AFEM(0Ch) register. This will enable X, Y, Z, T data conversion in high speed.

Step6. Write 0x06 to the ACTR(00h) register. The state will transfer from standby to active to begin sensor data conversion and output.

General Operation

Interrupt setup

Step1. Write 0x02 to the ACTR(00h) register to enable registers data write.

Step2. Setting MISC1 register (11h) to match hardware interrupt pin requirement if needed.

Step3. Write 0x00 to INTC register (0Eh). This will disable all interrupts.

Step4. Write 0x28 to MISC2 register (1Fh). This will disable micro motion interrupt.

Step5. Setting SKTH register (38h) for shake threshold. If uses shake as interrupt, please jump to Step9.

Step6. Setting SKTM register (39h) for micro motion threshold.

Step7. Read data from 12h ~ 19h for latching reference data of micro motion.

Step8. Write 0x38 to MISC2 register (1Fh). This will enable micro motion interrupt..

Step9. Wait at least 1ms to wait the micro motion be set.

Step10. Read first STAINT register (1Ch) then INTSTS register (1Dh) to clear interrupt status.

Step11. Setting INTC register (0Eh) to enable which axes to generate interrupt then interrupt function works now.

Step12. Write 0x06 to the ACTR(00h) register. The sensor will transfer from standby to active.

Operation Modes

There are three operation modes for general usage: normal, low-power and standby. The register setting for respective modes are shown in the following table.

No1. Normal mode:

▲Output data rate: 0.78125Hz up to 100 Hz.

This mode is recommended for general applications, especially for those require faster output data rate.

No2. Low-power mode:

▲Output data rate: 0.78125 Hz up to 12.5 Hz.

This mode has special consideration for conserving power. For data rate less than 12.5 Hz, we can use this low-power mode to save power consumption.

No3. Standby mode:

This mode will put the sensor in sleeping. The register values will be kept as long as the power is connected.

Operation modes and register settings

Operation Mode	ACTR (00h)	AFEN (0Ch[7])	CCK (0Dh[3:0])
Normal	0x06	b'1	b'0000
Low-Power	0x06	b'0	b'0100
Standby	0x00	b'0	b'0100

ODR Support Range and Output Date Rate Register Setting Value

	Output Data Rate (ODR), Hz							
	0.78125	**1.5625**	**3.125**	**6.25**	**12.5**	**25**	**50**	**100**
Support range	Normal Mode ODR Range							
	Low-power Mode ODR Range							
CKSEL (0Dh[7:0])	0x04	0x14	0x24	0x34	0x44	0x50	0x60	0x70

User Register Map

Table 4: User Register Map Table

Register Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Type	Default Value
00h	ACTR[7:0]								R/W	02h
01~0Bh	**Reserved**								—	—
0Ch	AFEN	**Reserved**			EN_Z	EN_Y	EN_X	EN_T	R/W	0Fh
0Dh	ODR[3:0]				**Reserved**				R/W	70h
0Eh	INTG	**Reserved**	INTDA	INTZ	INTY	INTX	**Reserved**		R/W	00h
0Fh	**Reserved**				Not used	TAP1[2:0]			R/W	00h
10h	**Reserved**								—	—
11h	RTEN	**Reserved**				AUTOT	INTA	INTD	R/W	05h
12h	STADR[7:0]								R	55h
13h	DAOW	DRDY	INT	**Reserved**					R	00h
14h	DX[7:0]								R	N/A
15h	DX[9]	DX[9]	DX[9]	DX[9]	DX[9]	DX[9]	DX[9:8]		R	N/A
16h	DY[7:0]								R	N/A
17h	DY[9]	DY[9]	DY[9]	DY[9]	DY[9]	DY[9]	DY[9:8]		R	N/A
18h	DZ[7:0]								R	N/A
19h	DZ[9]	DZ[9]	DZ[9]	DZ[9]	DZ[9]	DZ[9]	DZ[9:8]		R	N/A
1Ah	DT[7:0]								R	N/A
1Bh	DT[9]	DT[9]	DT[9]	DT[9]	DT[9]	DT[9]	DT[9:8]		R	N/A
1Ch	STAINT[7:0]								R	AAh
1Dh	Not used	DRDY	SHK	SHKZ	SHKY	SHKX	**Reserved**		R	N/A
1Eh	**Reserved**								—	—
1Fh	**Reserved**	SC[1:0]		MMEN	OSCAEN	**Reserved**			R/W	00h
20h	**Reserved**								—	—
21h	Not used					PD_BG	RST	PD_LDO	R/W	50h
22~37h	**Reserved**								—	—
38h	SKTH[7:0]								R/W	53h
39h	SKTM[7:0]								R/W	13h
3A~3F	**Reserved**								—	—

Description of Registers

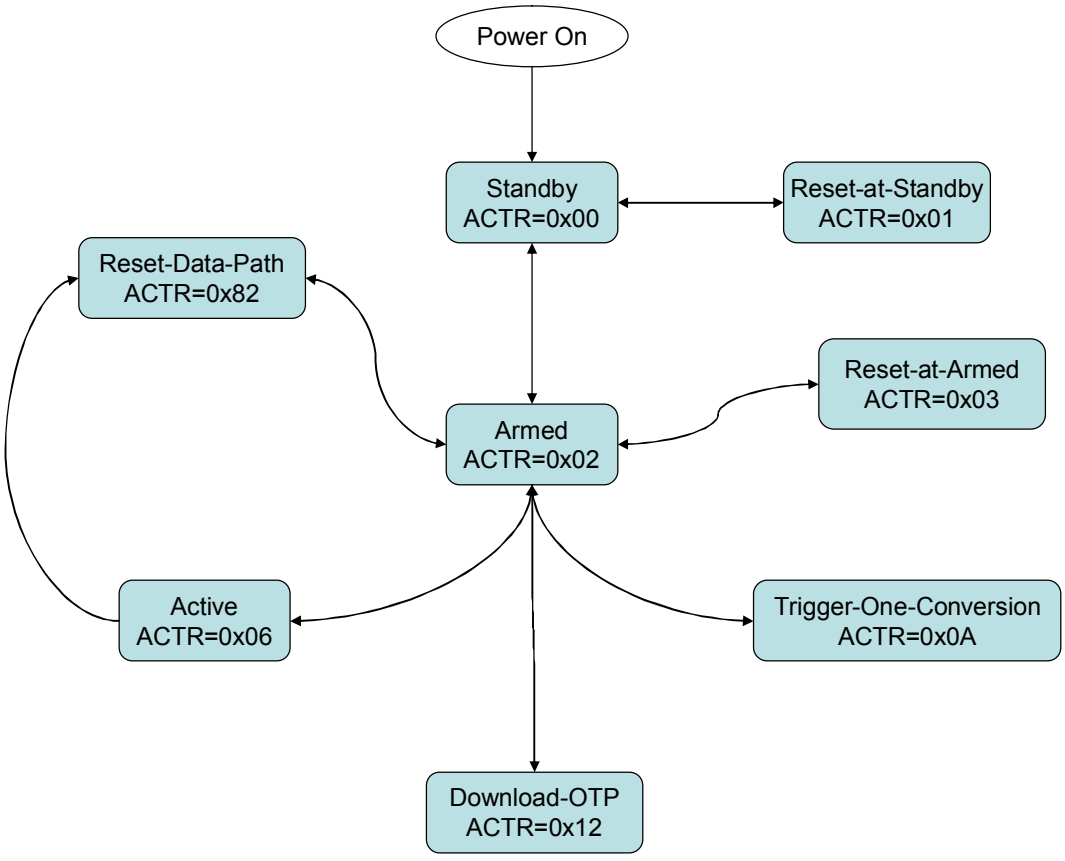
ACTR: action register

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Type	Default
00h	ACTR[7:0]								R/W	02h

Bit set to the ACTR register will trigger the following actions:

Bit Set	Action
ACTR[0]	Reset at standby
ACTR[1]	Enable armed state
ACTR[2]	Enable active state for normal/low power mode
ACTR[3]	Trigger one conversion
ACTR[4]	Download OTP data into internal parameter registers
ACTR[5]	Reserved
ACTR[6]	Reserved
ACTR[7]	Reset DSP data path

State Transition Diagram



AFEM : AFE mode register

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Type	Default
0Ch	AFEN	**Reserved**			EN_Z	EN_Y	EN_X	EN_T	R/W	0Fh

EN_T: enable T conversion for AFE, active high.

EN_X: enable X conversion for AFE, active high.

EN_Y: enable Y conversion for AFE, active high.

EN_Z: enable Z conversion for AFE, active high.

For normal operation, EN_T, EN_X, EN_Y, and EN_Z should be set to high.

AFEN set 0: AFE will be automatically power down after completion of each conversion. This is for the special low power mode for output data rate 12.5 Hz and below.

AFEN set 1: For normal mode operation or the data rate larger than 12.5Hz.

CKSEL : clock selection register

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Type	Default
0Dh	ODR[3:0]				**Reserved**				R/W	70h

ODR [3:0] is used to select output data rate. The output data rate is set to 100Hz by default.

ODR[3:0]	Output Data Rate (Hz)
0000	0.78125
0001	1.5625
0010	3.125
0011	6.25
0100	12.5
0101	25
0110	50
0111	100
1000~1111	Reserved

INTC: interrupt control register

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Type	Default
0Eh	INTG	Reserved	INTDA	INTZ	INTY	INTX	Reserved		R/W	00h

Bit Set	Description
INTC[0]	Reserved
INTC[1]	Reserved
INTC[2]	X axis interrupt enable
INTC[3]	Y axis interrupt enable
INTC[4]	Z axis interrupt enable
INTC[5]	Data ready interrupt enable.
INTC[6]	Reserved
INTC[7]	Global mask for INTC[5:0]. Set to 1 to disable INTC[5:0].

TAPNS: tap number register

Address	bit7	bit6	bit5	Bit4	bit3	bit2	bit1	bit0	Type	Default
0Fh	**Reserved**				Not used	TAP1[2:0]			R/W	00h

TAP1: TAP1 is to set the tap number of the first decimation filter, which can be further processed to reduce some noise before through I2C interface.

As shown the value in the following table.

TAP1	Tap Number
000	No filter
001	2
010	4
011	8
100	16
101	32

MISC1: miscellaneous option register 1

Address	bit7	bit6	bit5	Bit4	bit3	bit2	bit1	bit0	Type	Default
11h	RTEN	**Reserved**				AUTOT	INTA	INTD	R/W	05h

INTD: Interrupt Driving Configuration

INTD	Description
0	INT are configured to open-drain
1	INT are configured to push-pull

INTA: Interrupt Active Logic Configuration

INTA	Description
0	INT are configured to active low
1	INT are configured to active high

AUTOT: Auto T Configuration

AUTOT	Description
0	Disable T in the auto I2C read address
1	Enable T in the auto I2C read address

RTEN: read-trigger mode

RTEN	Description
0	Read-trigger mode is disabled
1	Read-trigger mode is enabled

Once read-trigger mode is enabled, every reading of data output will trigger a new conversion.

STADR: data output start read register

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Type	Default
12h	STADR								R	55h

SATADR is the first register to read for I2C data output transaction. The value is fixed to 55h.

For the XYZ data output, set 11h (MISC1) AUTOT to 0 and data must be read from 12h (STADR) to 19h within one I2C transaction. With AUTOT set to 0, the internal I2C address pointer will rewind to 12h (STADR) after reading 19h.

For the XYZ and T data output, set 11h (MISC1) AUTOT to 1 and data must be read from 12h (STADR) to 1Bh within one I2C transaction. With AUTOT set to 1, the internal I2C address pointer will rewind to 12h (STADR) after reading 1Bh.

TILT: tilt and data status register

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Type	Default
13h	DAOW	DRDY	INT	**Reserved**					R	00h

DRDY: data ready status

DRDY	Description
0	Data is not ready
1	Conversion is done and data is ready for output

DAOW: data over-written status

DAOW	Description
0	No data over-written
1	Data over-written occur

INT: Interrupt flag

INT	Description
0	No Interrupt happened
1	Interrupt has been happened

Data registers

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Type	Default
14h	DX[7:0]								R	N/A
15h	DX[9]	DX[9]	DX[9]	DX[9]	DX[9]	DX[9]	DX[9:8]		R	N/A
16h	DY[7:0]								R	N/A
17h	DY[9]	DY[9]	DY[9]	DY[9]	DY[9]	DY[9]	DY[9:8]		R	N/A
18h	DZ[7:0]								R	N/A
19h	DZ[9]	DZ[9]	DZ[9]	DZ[9]	DZ[9]	DZ[9]	DZ[9:8]		R	N/A
1Ah	DT[7:0]								R	N/A
1Bh	DT[9]	DT[9]	DT[9]	DT[9]	DT[9]	DT[9]	DT[9:8]		R	N/A

Acceleration and temperature output values can be read from the data registers. The data output is encoded to a 10-bit value and stored across two bytes. Data representation is 2'b complement, i.e. MSB (bit 9) is the sign bit with 1 representing negative value. The sign extension is completed automatically.

The acceleration sensing has dynamic range of ±6g with apparent sensitivity of 64LSB/g. The central data output value (00h) stands for 0g.

STAINT: interrupt status start read register

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Type	Default
1Ch	STAINT[7:0]								R	AAh

STAINT is the first register to read for interrupt status transaction. The value is fixed to 0xAAh.

INTSTS: Interrupt status

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Type	Default
1Dh	No used	DRDY	SHK	SHKZ	SHKY	SHKX	**Reserved**		R	N/A

SHKX: Shake or micro motion in X-direction.

SHKY: Shake or micro motion in Y-direction.

SHKZ: Shake or micro motion in Z-direction.

SHK: Shake or micro motion in X or Y or Z direction.

DRDY: Data ready for reading.

Data of 1Dh can NOT be read directly. It should be read 1Ch first then 1Dh.

After the registers are read, the data in 1Dh will be cleared to 0x00.

Once interrupt has been taken then data of 1Dh should be cleared.

If the data of 1Dh does NOT clear then the interrupt will be always exist on INT output pin.

MISC2: miscellaneous option register 2

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Type	Default
1Fh	Reserved	SC[1:0]		MMEN	OSCAEN	Reserved			R/W	00h

OSCAEN: Enable oscillator calibration

OSCAEN	Description
0	Disenable oscillator calibration
1	Enable oscillator calibration

MMEN: Enable Micro motion detection

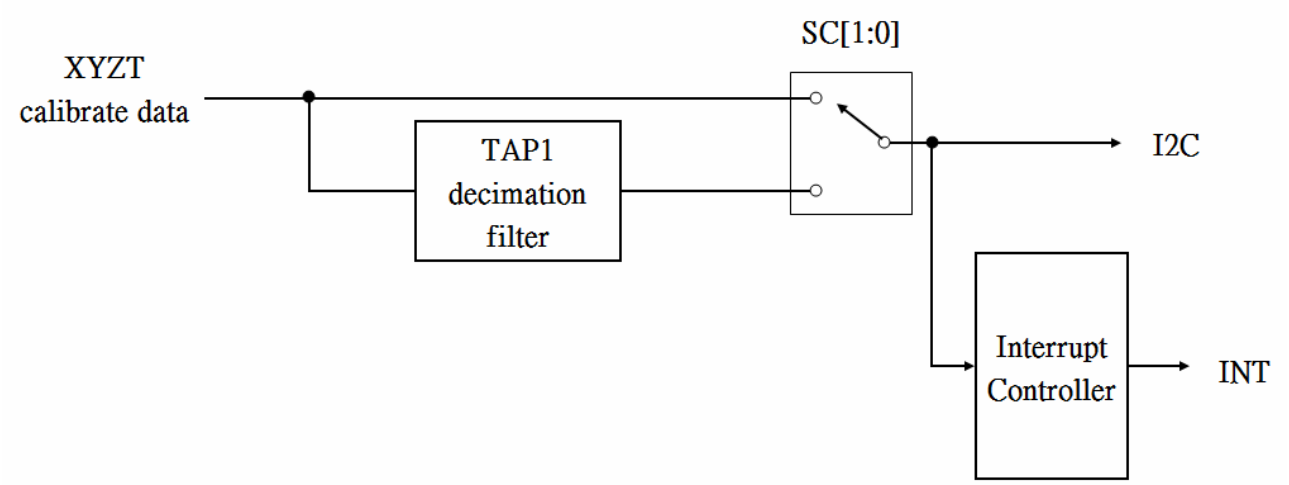
MMEN	Description
0	Disenable micro motion detection
1	Enable micro motion detection

Before set MMEN bit, please read 12h ~ 19h to latch the reference data as micro motion detection.

After MMEN bit be set then any read of 12h ~ 19h would NOT be latched again as reference data of micro motion.

SC: Select data output channel

SC[1:0]	Description
00	Select the decimation filter as output
01	Select the calibrated data as output
10	Reserved
11	Reserved



PD: power down control

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Type	Default
21h	Not used					PD_BG	RST	PD_LDO	R/W	50h

PD_LDO: Power down digital LDO

PD_LDO	Description
0	Normal operation
1	Digital LDO power down

RST: Reset

RST	Description
0	Normal operation
1	Reset core logics

PD_BG: Power down band gap LDO circuit

PD_BG	Description
0	Normal operation
1	Bypass AVDD to AFE module directly

NOTE: The PD_BG only uses in the AVDD power input < 2.0V

SKTH: Threshold of shake

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Type	Default
38h	SKTH[7:0]								R/W	53h

For GMA301 64 LSB/g, the values of SKTH * 4 is the real LSB to compare with.

For example, if the value of SKTH set to 0x10h then threshold of shake is 0x10h * 4 = 0x40h = 64 LSB.

GMA301 will issue an interrupt once these axes which are larger than 64 LSB (1g).

SKTM: Threshold of micro motion

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Type	Default
39h	SKTM[7:0]								R/W	13h

For GMA301 64 LSB/g, the values of SKTM * 4 is the real LSB to compare with.

For example, if the value of SKTM set to 0x01h then threshold of shake is 0x01h * 4 = 0x04h = 4 LSB.

GMA301 will issue an interrupt once these axes which are larger than latched reference data of micro motion plus 4 LSB.

Please refer to the 1Fh MMEN setting for latched reference data of micro motion.

Digital Interface

GMA301 provides an I2C digital interface and an interrupt signal to communicate with the outside system. The interrupt signal INT has output options to be configured to open-drain or push-pull. The active level can be further set to low or high. Please refer to the MISC1 (11h) register description for details.

I2C Interface

The I2C interface is designed with clock speed up to 400 kHz, with the 7-bit I2C device address fixed at **0x18**.

The I2C bus takes master clock through SCL pin and exchanges serial data via SDA. SDA is bidirectional (input/output) with open-drain. Both must be connected externally to DVCC via a pull-up resistor.

The I2C interface supports multiple read and write. When using multiple read/write, generally the internal I2C address pointer will automatically increase by 1 for the next access. But exceptions to this general rule are highlighted in the following table. For example, a multiple write to 00h (ACTR) will write multiple byte sequence to 00h. This will make state transition easily.

Multiple R/W	Current Address	Next Address
Write	00h	00h
Write	03h	00h
Read	19h	1Ah @ 11h AUTOT=1
Read	19h	12h @ 11h AUTOT=0
Read	1Bh	12h
Read	1Eh	14h
Read	1Fh	1Fh
Read	20h	20h
Read	21h	21h
Others	Address	Address+1

I2C Access Format

Data transfer begins by bus master indicating a start condition (ST) of a falling edge on SDA when SCL is high. Stop condition (SP) also indicated by bus master is a rising edge on SDA when SCK is high.

After a start condition, the 7-bit slave address + RW bit must be sent by master. If the slave address does not match with GMA301, there is no acknowledge and the following data transfer will not affect GMA301. If the slave address corresponds to GMA301, it will acknowledge by pulling SDA to low and the SDA line is let free enabling the data transfer. The master should let the SDA high (no pull down) and generate a high SCL pulse for GMA301 acknowledge.

Table 5: I2C access format

Single Write

ST	Slave Address + RW	A	Reg Address	A	Data	A	SP

Multiple Write

ST	Slave Address + RW	A	Reg Address	A	Data	A	Data	NA	SP

Single Read

ST	Slave Address + RW	A	Reg Address	A	SR	Slave Address + RW	A
Data	NA	SP					

Multiple Read

ST	Slave Address + RW	A	Reg Address	A	SR	Slave Address + RW	A
Data	A	Data	NA	SP			

Master to Slave Slave to Master

A = acknowledge (SDA Low)
NA = not acknowledge (SDA High)
ST = START condition
SR = repeated START condition
SP = STOP condition

I2C Specifications

Table 6: I2C Timing Specification

Parameter	Symbol	Minimum	Typical	Maximum	Unit
SCL clock frequency	SCL	—	—	400	kHz
Clock low period	t_{LOW}	1.2	—	—	µs
Clock high period	t_{HIGH}	0.6	—	—	µs
Bus free to new start	t_{BUF}	1.2	—	—	µs
Start hold time	$t_{HD.STA}$	0.6	—	—	µs
Start setup time	$t_{SU.STA}$	0.6	—	—	µs
Data-in hold time	$t_{HD.DAT}$	0	—	—	µs
Data-in setup time	$t_{SU.DAT}$	100	—	—	ns
Stop setup time	$t_{SU.STO}$	0.6	—	—	µs
Data-out hold time	t_{DH}	50	—	—	ns

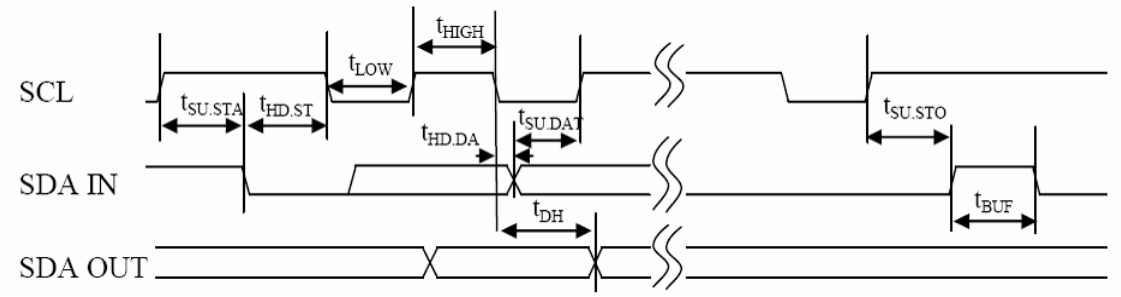


Figure 4: I2C Timing Diagram

Package

Outline Dimension

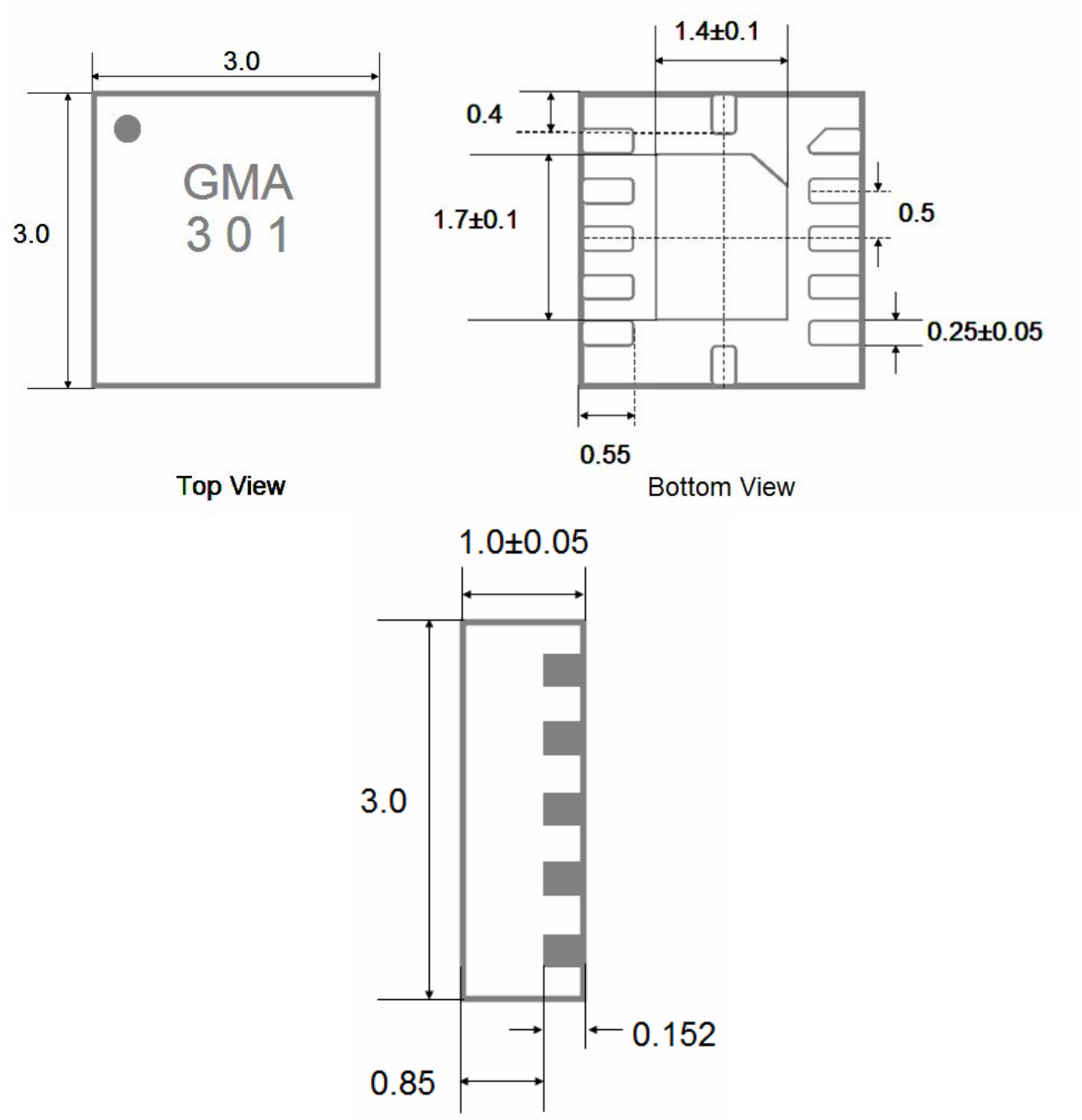


Figure 5: Package Outline Dimension

Axes Orientation

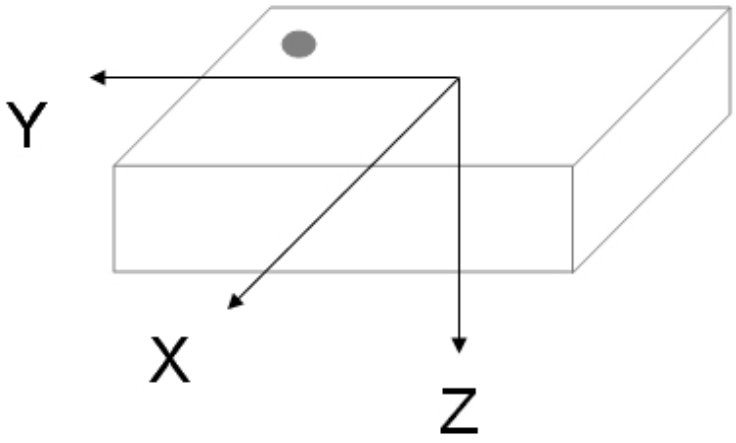


Figure 6: Axes Orientation of GMA301

RoHS Compliance

GMEMS DFN sensors are compliant with Restrictions on Hazardous Substances (RoHS), having halide free molding compound (green) and lead-free terminations. Reflow profiles applicable to those processes can be used successfully for soldering the devices.

Surface Mounting Information

The accelerometer is a delicate device that is sensitive to the mechanical and thermal stress. Proper PCB board design and well-executed soldering processes are crucial to ensure consistent performance. A recommended land pad layout can be found in the Figure 7.

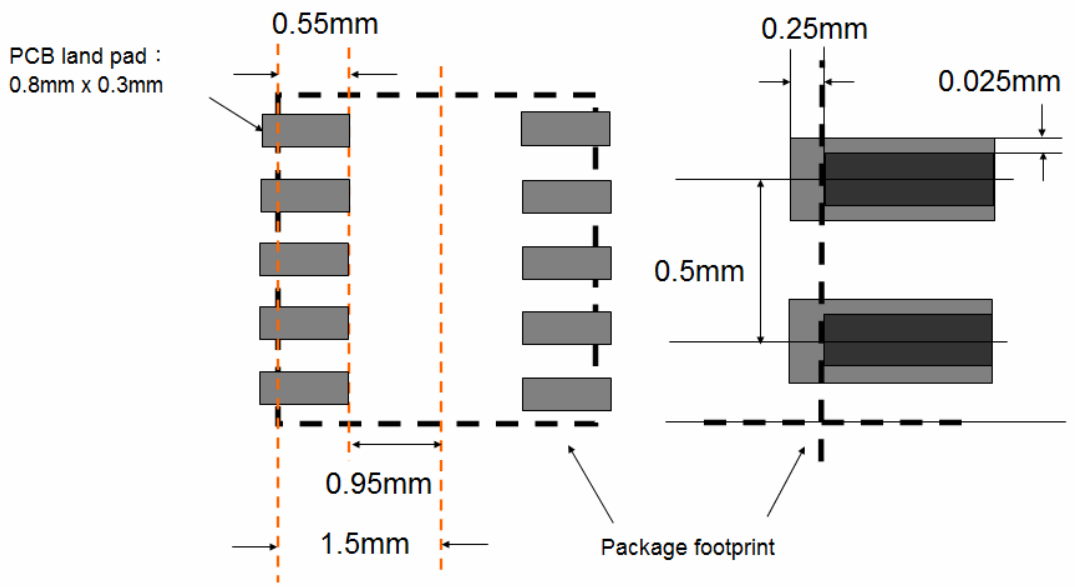


Figure 7: Layout Recommendation for PCB Land Pad

Document History and Modification

Revision No.	Description	Date
Preliminary V0.2	First preliminary release for customer review	2014/1/27
Preliminary V0.3	Second preliminary release for customer review	2014/7/23
Preliminary V0.5	5th preliminary release for customer review. It adds the interrupt registers.	2014/8/12
Preliminary V0.5.1	Modified interrupt setup steps.	2014/8/15
Preliminary V0.5.2	Modified Surface Mounting Information	2014/10/20