General Description:

JX-H42 is an HD CMOS image sensor designed with a superior 3.0µm pixel with excellent low-light sensitivity and low dark current performance. It features a 60fps native high definition (HD) 720p video capability for camera applications in PC multimedia, security, and entertainment devices.

The JX-H42 consists of a 1296x732 active pixel sensor (APS) array with an on-chip 10-bit ADC, programmable gain control (PGA), and correlated double sampling (CDS) to significantly reduce fixed pattern noise (FPN). The sensor also has many standard programmable and automatic functions. It has both the industry compliant DVP parallel and MIPI CSI2 serial interfaces. The external host controller can access this device through a standard serial interface.

It is available in wafer-level packaged CSP.

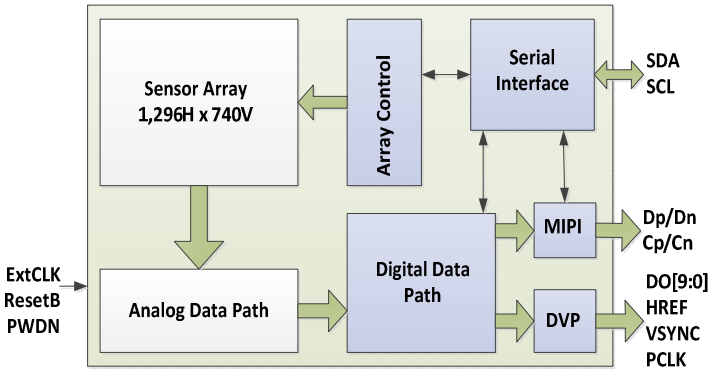
Features:

- Automatic functions:
  - o AEC – Automatic Exposure Control
  - o AGC – Automatic Gain Control
  - o ABLC – Automatic Black Level Calibration
- Programmable controls:
  - o Gain, exposure, frame rate and size
  - o Image mirror and flip
  - o Window panning and cropping
  - o I2C slave ID
- Output formats:
  - o DVP parallel interface
  - o MIPI CSI2 1 Lane
- Data formats:
  - o 10-bit RAW RGB
- Others
  - o 50/60Hz flick noise cancellation
  - o Register group write capability
  - o Frame synchronization
  - o Black sun spot cancellation

Key Specifications:

Optical format		1/4”
Active Pixels		1296H x 732V
Pixel size		3.0 x 3.0 µm
Color filter array		RGB Bayer pattern
Chief Ray Angle		17.5 degrees linear
Shutter type		Electronic rolling shutter
Maximum Frame Rate		60fps
Supply voltage	**Digital**	2.6 – 3.0V (2.8V nominal)
	Analog	2.6 – 3.0V (2.8V nominal)
	I/O	1.7 – 3.0V
Power consumption	**Active**	TBD mA
	Standby	< TBD µA
Output Formats		10-bit RGB Raw Data
Sensitivity		TBD mV/lux-sec
Max SNR		TBD db
Dynamic Range		TBD db
Dark Current		<TBD mV/sec @ 45C
Operating temperature		-20C to 70C
Storage temperature		-30C to 85C

Functional Block:



Component Order Information:

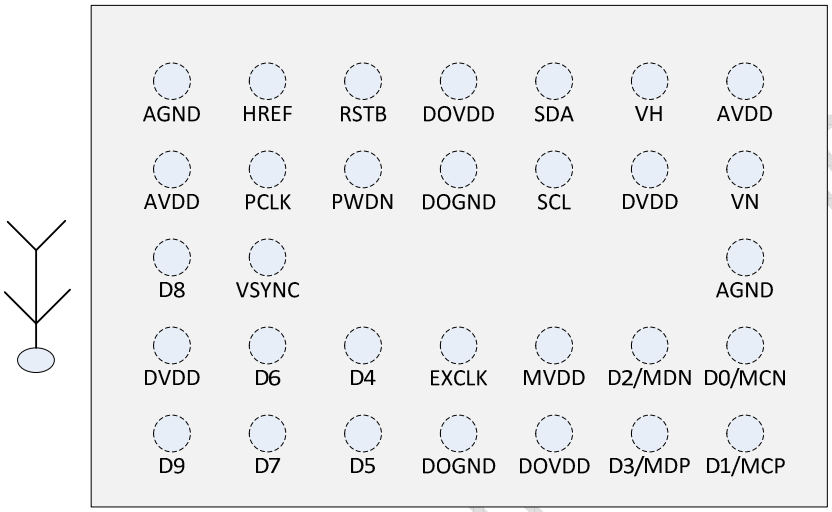
Part Number	Description
JX-H42-C1	CSP

Contents

Pin Diagram:

JX-H42's pin diagram is shown in Figure 1 and each pin's description is shown in Table 1:

Figure 1. H42's Top View CSP Pin Diagram



JX-H42 CSP Top View

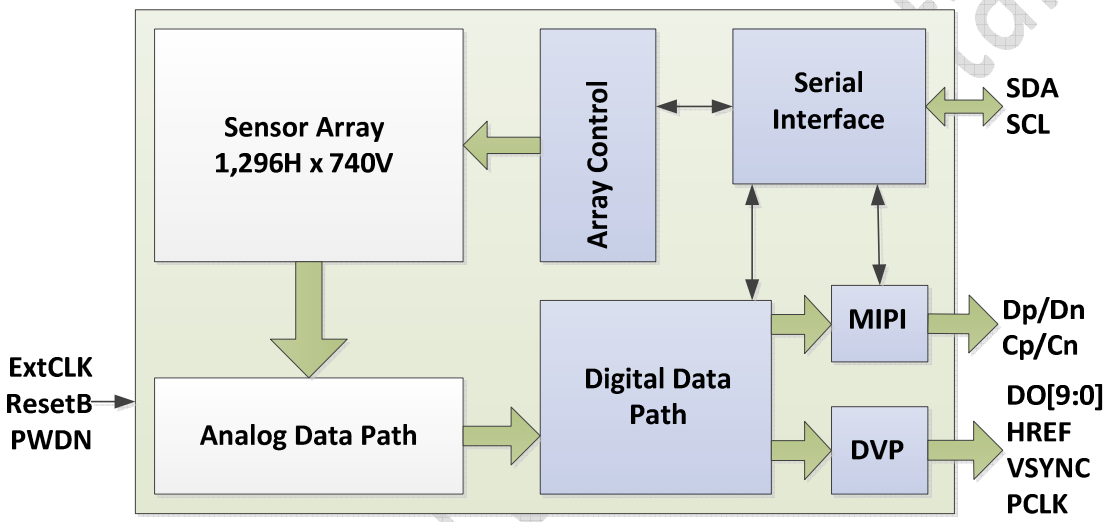
Table 1: Pin Description

Pin number	Pin name	Pin type	Description
A1	AGND	Supply	Analog ground
A2	HREF	I/O	Line data valid signal output.
A3	RSTB	Input	System synchronize reset when driven low, it resumes normal operation with all configuration register set to factory default
A4	DOVDD	Supply	Digital I/O supply voltage.
A5	SDA	I/O	Serial data, pull to DOVDD with a 4.3k Ω resistor
A6	VH	reference	Internal analog reference.
A7	AVDD	Supply	Analog supply voltage.
B1	AVDD	Supply	Analog supply voltage.
B2	PCLK	I/O	Pixel clock.
B3	PWDN	Input	Chip power down initiate pin. High active.
B4	DOGND	Supply	Digital I/O ground
B5	SCL	I	Serial interface clock input.
B6	DVDD	Supply	Digital core supply voltage.
B7	VN	Reference	Internal analog reference.
C1	D8	I/O	DVP data output bit 8.
C2	VSYNC	I/O	Vertical synchronize signal, drive high when last frame end and drive low before next frame start. Also can be programmed as frame synchronize input
C3			
C4			
C5			
C6			
C7	AGND	Supply	Analog ground
D1	DVDD	Supply	Digital core supply voltage.
D2	D6	I/O	DVP data output bit 6.
D3	D4	I/O	DVP data output bit 4.
D4	EXCLK	Input	System clock input.
D5	MVDD	Supply	MIPI block supply voltage, connect to DVDD pin.
D6	D2/MDN	I/O	DVP data output bit 2 or MIPI data lane negative output.
D7	D0/MCN	I/O	DVP data output bit 0 or MIPI clock lane negative output.
E1	D9	I/O	DVP data output bit 9.
E2	D7	I/O	DVP data output bit 7.
E3	D5	I/O	DVP data output bit 5.
E4	DOGND	Supply	Digital I/O ground
E5	DOVDD	Supply	Digital I/O supply voltage.
E6	D3/MDP	I/O	DVP data output bit 3 or MIPI data lane positive output.
E7	D1/MCP	I/O	DVP data output bit 1 or MIPI clock lane positive output.

Functional Overview:

The JX-H42 is a progressive-scan CMOS image sensor. It has an on-chip, phase-locked loop (PLL) to generate internal clocks from a single master input clock running between 6 and 54MHz. Its analog data process and digital data process can handle up to 70Mp/s at corresponding pixel clock 70MHz. Figure 2 illustrates a block diagram of the sensor.

Figure 2. Functional Block Diagram



User can access and program JX-H42 sensor internal registers through the two-wire serial bus. The core of the sensor is a 1296x732 active-pixel array. The timing and control circuitry sequences through the rows of the array, resetting and then reading each row in turn. In the time interval between resetting and reading that row, the pixels in the row integrate the incident light. The exposure is controlled by varying the time interval between reset and readout. Once a row has been read, the data from the columns is sequenced through an analog signal path to apply gain and analog signal to digital signal converter (ADC). The ADC output passes through a digital processing path for black level calibration. Then the data will output though a DVP port or MIPI CSI-2 standard interface.

Pixel Array Format:

The JX-H42 pixel array consists of a 1296-column by 740-row matrix of pixels addressed by column and row. The address (column 0, row 0) represents the upper-right corner of the entire array (please refer to Figure 3 for Pixel array structure). The first 8 rows are optical black row for black level calibration, and outside of the 1280x720 active pixels are several boundary pixels: 6 rows on top, 6 rows below, 8 columns on the right and 8 columns on the left. The detailed pixel array arrangement and default read out direction is noted in the Figure 4.

Figure 3: Pixel array structure

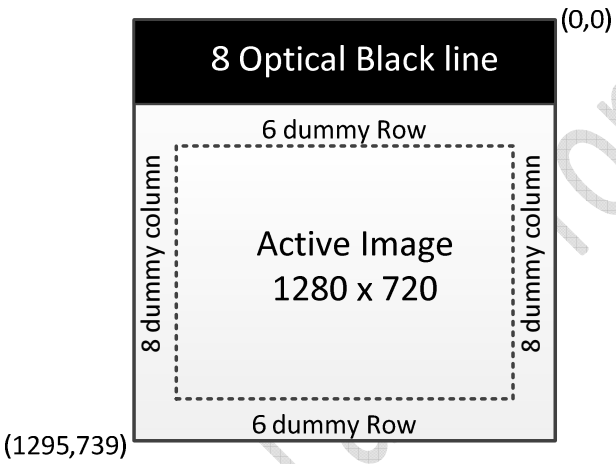
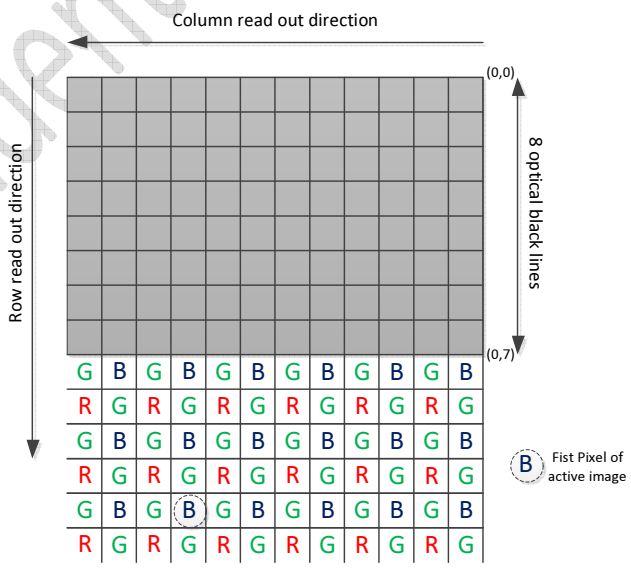


Figure 4: Pixel array detail with default read out direction.



Data Output Format:

The output images are divided into frames, which are further divided into lines. By default, the sensor produces 720 lines (rows) of 1280 columns each. The VSYNC and HREF signals indicate the boundaries between frames and lines, respectively. PCLK can be used as a clock to latch the data. For each PCLK cycle, one 10-bit pixel data outputs on the D[9:0] pins (Figure 5). The pixel data is valid when HREF signal is asserted. The VSYNC signal indicates frame end and new frame start. JX-H42 default frame timing is illustrated as figure 6.

Figure 5: row data output timing

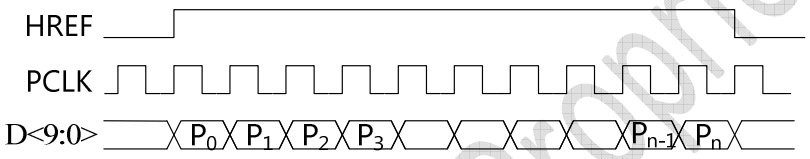
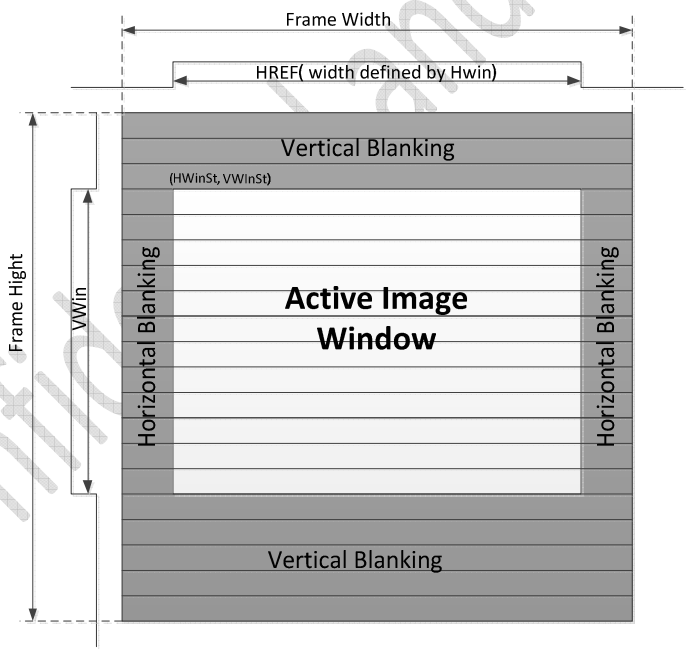


Figure 6: Default frame timing



As shown above in figure 5, a line (row) period can be calculated as Trow = Frame_width * Tpclk, and frame rate can be calculated as fps=1/(Frame_hight * Trow).

As default configuration, VSYNC, PCLK and Data are all valid at PCLK rising edge. For user convenience, JX-H42 provides register bits to control HREF, VSYNC and PCLK polarity. In addition, PCLK also have adjustable delay control.

For pixel Bayer pattern data output, several settings can have effect on pixel output sequences. These registers include HWIn_St, VWin_St, HAddr_St, Mirror, V_Flip. Please consult your SOI AE for further information.

Sensor Luminance Control:

JX-H42 has built-in automatic luminance control capability. The main purpose for luminance control is to get proper image level through exposure and gain adjustment. There are 3 configurations described below:

1) 50/60Hz flick noise cancelling (also known as banding filter). When this feature is turned on, user needs to set the line equivalents of 1/100s or 1/120s, exposure will attempt to stay within n/100s or n/120s boundaries (where "n" is an integer number). The gap between each step will be filled with gain. If the light is too strong, exposure will continuously adjust to under 1/100s or 1/120 boundary conditions. Under this condition, the moving or fixed light bands may still be observed by user.

2) Auto frame rate adjustment. For some extreme low light condition, JX-H42 provides the option to automatically slow down the frame rate to adjust exposure to a proper image level. The lowest frame rate is 1/8.

3) Partial line exposure. Exposure is usually line-based operation, but for some extreme high brightness condition such as outdoor sunny environment, JX-H42 provides another option to allow exposure be lowered to below one line period. The minimum exposure time at this condition can be a few microsecond.

Test Pattern Output:

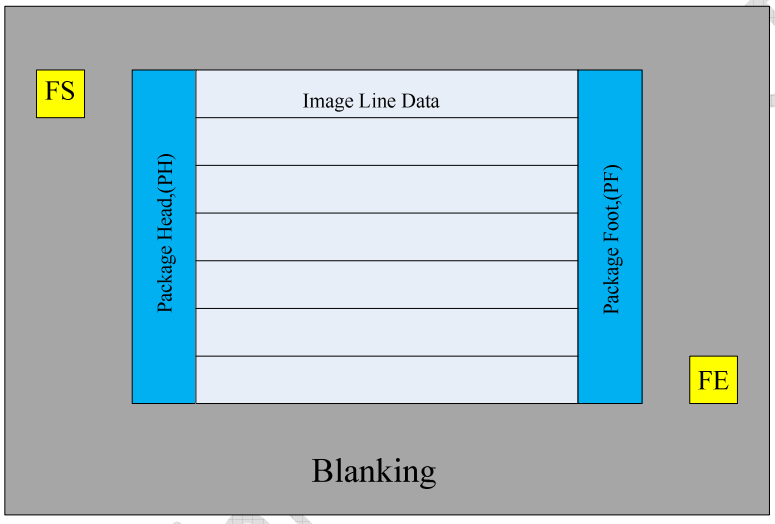
JX-H42 can output test patterns as described below:

1) Walking "1" test pattern: for most sensor module connectivity test, JX-H42 provides walking "1" test pattern.

MIPI interface:

JX-H42 support MIPI CSI-2 compliant interface. It has one pair of differential clock lane and one pair of differential data lane. JX-H42 can output raw8 or raw10 mode through MIPI interface. In raw8 mode, only 8 MSBs of 10-bit data will output and user needs to set MIPI clock speed at 8x parallel port pixel clock. In raw10 mode, user needs to set MIPI PHY clock as 10x parallel port pixel clock.

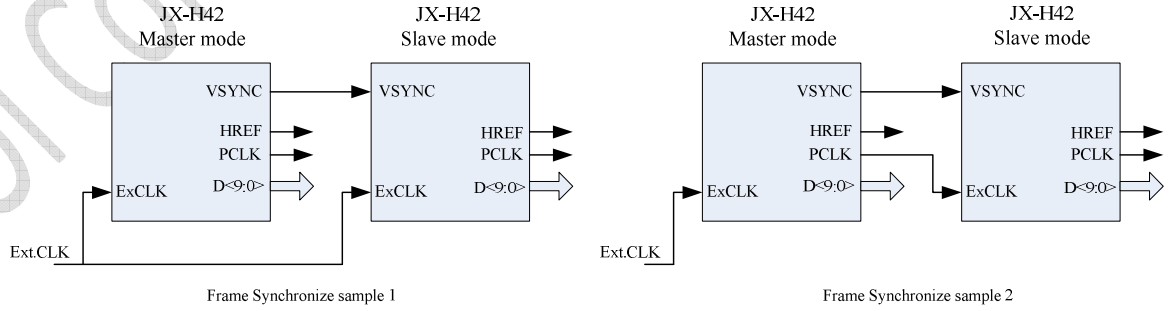
Figure 7: MIPI interface frame timing



Frame Synchronization:

JX-H42 provides the capability of frame synchronization. By setting VSYNC pin as input and enable frame-sync option, JX-H42 will work as slave device and synchronized with an external VSYNC. If all master devices and slave devices use same timing setting, all devices frame timing mismatch will be less than few pixel clocks. Figure 8 shows 2 ways to realize frame synchronization.

Figure 8: Frame Synchronization illustration



In the above 2 frame synchronize configurations, sample 2 will have more accurate synchronization than sample 1 because the slave device will have exactly same pixel clock as the master.

Serial Interface:

The serial interface is a two-wire bi-directional bus. Both wires (Serial Clock -SCL and Serial Data - SDA) are connected to DOVDD via a pull-up resistor, and when the bus is free both lines are high. The two-wire serial interface defines several different transmission stages as follows:

- A start bit
- The slave device 7-bit address
- An (No) acknowledge bit coming from slave
- An 8-bit or 16-bit message (address and/or data)
- A stop bit (or another 8bit or 16bit message in multiple Read/Write access)

Figure 9: I2C Timing chart

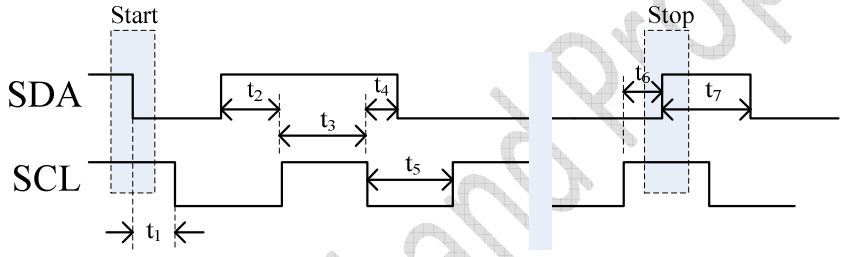
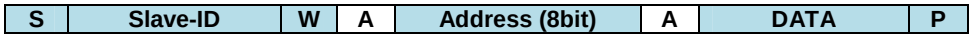


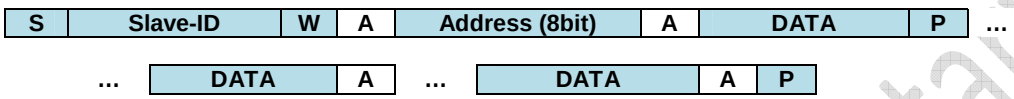
Table 2: I2C timing characteristic

Symbol	Description	Min	Max	Units
	SCL clock frequency	0	400k	Hz
t1	Hold time for START condition	0.6	-	µs
t2	Data setup time	160	-	ns
t3	High period of the SCL clock	0.6	-	µs
t4	Data hold time	0	0.9	µs
t5	Low period of the SCL clock	1.3	-	µs
t6	Setup time for STOP condition	0.6	-	µs
t7	Bus free time between STOP and START condition	1.3	-	µs
	Rise time for both SDA and SCL signals		300	ns
	Fall time for both SDA and SCL signals		300	ns
Cb	Capacitive load for each bus line		400	pF

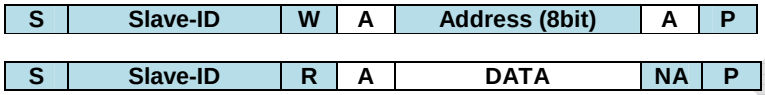
Single Write Mode operation



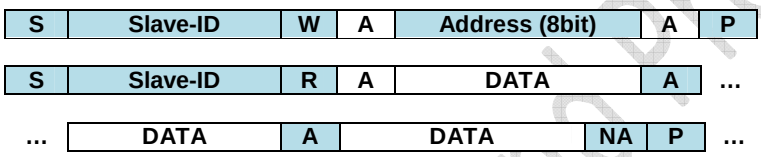
Multiple Write Mode (Register address is increased automatically) operation



Single Read Mode operation



Multiple Read Mode (Register address is increased automatically) operation



S: start conditions, A: acknowledge bit, NA: no acknowledge, DATA: 8 bit data, P: stop condition
JX-H42 slave ID is programmable, default is 0x60/61 for write and read. User can program DVP data bit<9:8> for other configuration. The slave ID program table is list below:

D[9]	D[8]	Read/Write
X	X	60/61
X	Pull high	64/65
Pull high	X	68/69
Pull high	Pull high	6C/6D

.

Register Group Write Function:

JX-H42 provides register group write function, user can pre-load address and data from register 0xC0 to 0xFF, then trigger this function by setting SYS[3], normally JX-H42 will auto write back group register content at next vertical blanking period and reset SYS[3]. JX-H42 can update up to 32bytes of registers.

User can always monitor SYS[3] to make sure group write procedure is finished or not.

Electrical Characteristics:

Table 3. Absolute maximum ratings

Symbol	Descriptions	Absolute maximum rating	Units
V_{DD-IO}	I/O Digital Power	4.5	V
V_{DD-A}	Analog Power	4.5	V
V_{DD-D}	Core Digital Power	4.5	V
V_I	Input voltages	-0.3v to V_{DD-IO} + 1V	V
T_{AS}	Ambient Storage Temperature	-40 ~ 125	ºC

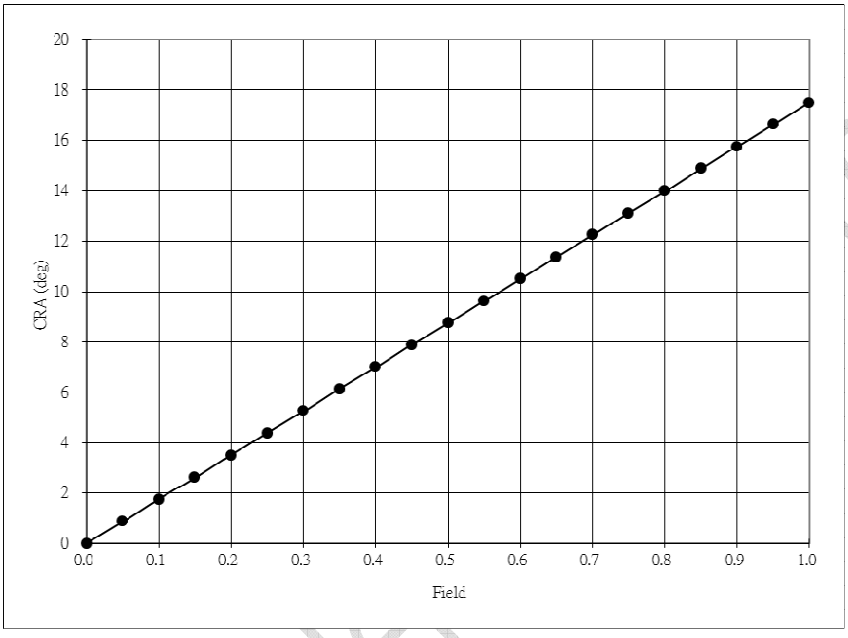
Table 4. DC Characteristics (0°C ≤ TA ≤ 85°C, Voltages referenced to GND)

Symbol	Descriptions	Max	Typ	Min	Units
supply					
V_{DD-IO}	Supply voltage (DOVDD)	3.0	1.8	1.7	V
V_{DD-A}	Supply voltage (AVDD)	3.0	2.8	2.6	V
V_{DD-D}	Supply voltage (DVDD)	3.0	2.8	2.6	V
Digital Inputs					
V_{IL}	Input voltage LOW	0.2* V_{DD-IO}	-	-	V
V_{IH}	Input voltage HIGH			0.7*V_{DD-IO}	V
C_{IN}	Input capacitor	10			pF
Digital Outputs (loading 20pF)					
V_{OH}	Output voltage HIGH			V_{DD-IO} – 0.2	V
V_{OL}	Output voltage LOW	0.2			V
Power consumption					
I_{DD-IO}	Supply current (V_{DD-IO}=2.8V@30fps SXGA without digital I/O loading)		TBD		mA
I_{DD-A}	Supply current (V_{DD-A}=2.8V@30fps SXGA)		TBD		mA
I_{DD-D}	Supply current (V_{DD-D}=2.8V@30fps SXGA)		TBD		mA
I_{STBY}	Standby current without external clock		TBD		uA

CRA Specifications:

JX-H42 is designed with a linear chief ray angle curve as shown in Figure 10. The shifting of the color filter and microlenses on the sensor is critical to accommodate the ever shorter height of the camera module as well as minimizing shading at the corner of the image.

Figure 10. CRA Curve for JX-H42



Field	CRA
0.00	0.000
0.05	0.875
0.10	1.750
0.15	2.625
0.20	3.500
0.25	4.375
0.30	5.250
0.35	6.125
0.40	7.000
0.45	7.875
0.50	8.750
0.55	9.625
0.60	10.500
0.65	11.375
0.70	12.250
0.75	13.125
0.80	14.000
0.85	14.875
0.90	15.750
0.95	16.625
1.00	17.500

Mechanical Specifications:

JX-H42 is available in CSP packaged component. Figure 11 shows top view and bottom view of the CSP component. Table 5 shows the nominal dimensions for the packaged chip.

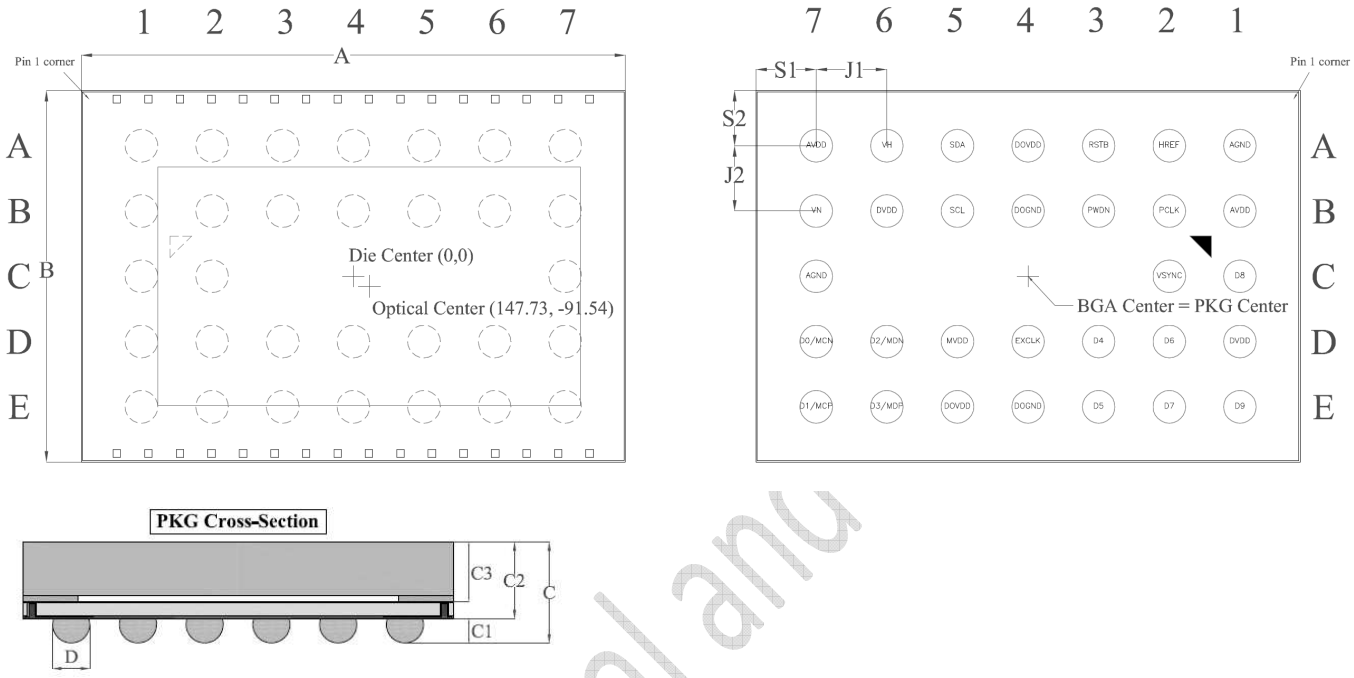


Figure 11. CSP Top, Bottom, Side View

Table 5. Dimensions for JX-H42 CSP package (in mm)

Unit : um

Package Dimension				
Parameter	Symbol	Nominal	Min.	Max.
Package Body Dimension X	A	5009	4979	5039
Package Body Dimension Y	B	3416	3386	3446
Package Height	C	768	738	798
Ball Height	C1	183	163	203
Package Body Thickness	C2	585	565	605
Thickness from top glass surface to wafer	C3	445	431	459
Ball Diameter	D	250	225	275
Total Pin Count	N	31	-	-
Pin Pitch X axis	J1	650	-	-
Pin Pitch Y axis	J2	600	-	-
Edge to Ball Center Distance along X	S1	554.5	524.5	584.5
Edge to Ball Center Distance along Y	S2	508	478	538

CSP Module Schematic (Reference):

Figure 12 shows a reference schematic for CSP module.

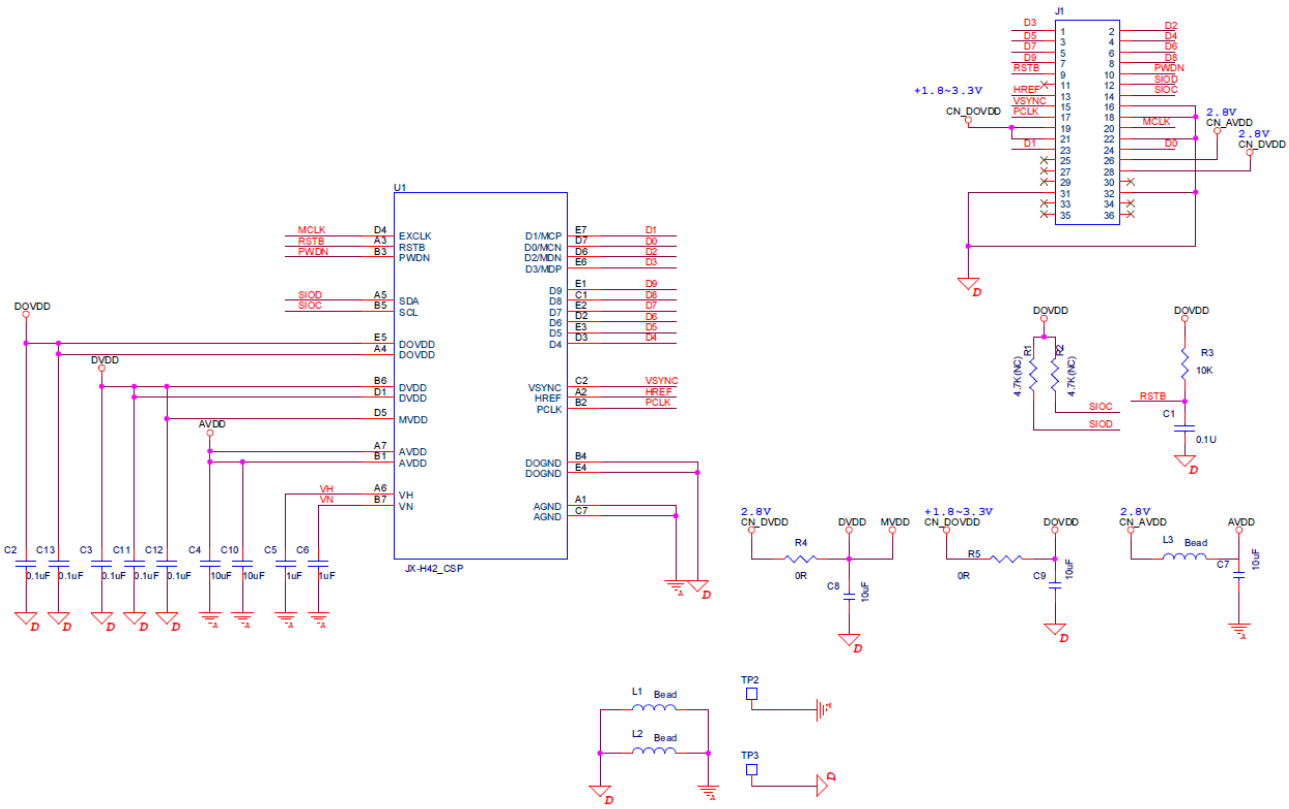


Figure 12. Reference schematic for H22 CSP module

Register Descriptions:

Address (Hex)	Register Name	Default (Hex)	R/W	Description
00	PGA	00	RW	Programmable gain, valid value: 0 to 3F. Total gain = (2^PGA[6:4])*(1+PGA[3:0]/16)
01	EXP	FF	RW	Exposure line LSBs, EXP[7:0]
02	EXP	00	RW	Exposure line MSBs, EXP[15:8]. Exposure time is defined by EXP[15:0] at line period base. T_{EXP}=EXP[15:0]*T_{Row}
03	PLEXP	FF	RW	Partial line exposure LSBs, PLEXP[7:0].
04	PLEXP	FF	RW	Partial line exposure MSBs, PLEXP[15:8]. Partial line exposure should be valid only when EXP[15:0] = 01'h. Partial line exposure time is defined by PLEXP[15:0] at pixel clock period base. T_{PLEXP} = PLEXP[15:0]*T_{PCLK}
05-08				RSVD
09		00	RW	Version control number
0A	PIDH	A0	R	Product ID MSBs.
0B	PIDL	42	R	Product ID LSBs.
0C	DVP1	40	RW	DVP control 1. DVP1[7]: reserved. DVP1[6]: Sensor sun spot elimination control, "1": disable sun spot elimination, "0": enable sun spot elimination. DVP1[5:2]: RSVD DVP[1:0]: DVP test mode control: "00": normal DVP data, "01": walking "1" test pattern output, "10", "11": RSVD
0D	DVP2	50	RW	DVP control 2. DVP2[7:3]: RSVD DVP2[2]: PAD drive capability. "0": min, "1": max. DVP2[1:0]: Digital gain control, "00": no digital gain, "01" or "10": 2x, "11": 4x digital gain.
0E	PLL1	1C	RW	PLL control 1. PLL1[7]: PLL bypass selection. "1": PLLclk = Input clock/PLL_Pre_Ratio. "0": see PLL2[3:0]. PLL1[6:4]: reserved. PLL1[3]: PLL mipi clock and mipi pixel clock ratio selection, "0": ration 8:1, "1": ration 10:1. PLL1[2]: rsvd. PLL1[1:0]: PLL pre-divider ratio. PLL_Pre_Ratio = (1 + PLL[1:0])
0F	PLL2	09	RW	PLL control 2. PLL2[7:4]: Mipi clock divider. Mipiclk = VCO/(1+PLL2[7:4]) PLL2[3:0]: PLL clock divider. PLLclk = VCO/(1+PLL2[3:0])
10	PLL3	1E	RW	PLL control 3. PLL VCO multiplier. VCO = Input clock*PLL3[7:0]/PLL_Pre_Ratio
11	CLK	80	RW	Digital system clock control

				CLK[7]: System clock option. “1”: system clock use PLLclk directly. “0”: see system clock equation below. CLK[6]: system clock digital doubler on/off selection. “1”: on, “0”: off CLK[5:0]: system clock divide ratio. *Equation:* When CLK[5:0] > 0: System clock = PLLclk *(1+CLK[6])/(2*CLK[5:0]) When CLK[5:0] = 0: System clock = PLLclk*(1+CLK[6])/2
12	SYS	00	RW	System status set up SYS[7]: Soft reset initialize, “1”: initial system reset, it will reset whole sensor to factory default status, and this bit will clear after reset. SYS[6]: Sleep mode on/off selection, “1”: sensor into sleep mode. No data output and all internal operation stops. SYS[5]: mirror image on/off, “1”: mirrored image output, “0”: normal image output SYS[4]: flip image on/off, “1”: flipped image output, “0”: normal image output. SYS[3]: Group write trigger. “1”: system will write reg0xC0 to 0xFF content to proper register. This bit will clear after group write. “0”: inactive group write function. SYS[2:0]: reserved.
13	LCCtrl1	87	RW	Luminance control register 1. LCCtrl1[7:5]: Gain ceiling at auto mode. “000”: maximum 2x analog gain, “001”: 4x, “010”: 8x, “011”: 16x. “100”: 32x, “101”: 64x, “111” & “101”: not applicable. LCCtrl1[4]: reserved. LCCtrl1[3]: Group latch function control, “0”: register group latch valid only at VSYNC period. “1”: register group latch immediately at group latch trigger set. LCCtrl1[2]: Banding filter on/off selection. “1”: on. “0”: off LCCtrl1[1]: partial line exposure on/off, “1”: enable exposure less than one line period. “0”: minimum exposure time is one line period. LCCtrl1[0]: automatic luminance control on/off selection, “0”: auto, “1”: manual
14	LCCtrl2	80	RW	Luminance Control register 2. LCCtrl2[7:0]: Image luminance average expect target.
15	LCCtrl3	44	RW	Luminance Control register 3 LCCtrl3[7:4]: auto Luminance control adjustment trigger range. LCCtrl3[3:0]: auto luminance control stable range
16	LCCtrl4	C0	RW	Luminance control register 4 LCCtrl[7:0]: Luminance control high threshold
17	LCCtrl5	40	RW	Luminance control register 5 LCCtrl[7:0]: Luminance control low threshold
18	LCCtrl6	99	RW	Luminance control register 6 LCCtrl6[7:0]: Banding filter minimum exposure line LSBs, Band [7:0]
19	LCCtrl17	00	RW	Luminance control register 7 LCCtrl7[7:6]: DVP PCLK output delay control. LCCtrl7[5]: manually gain apply option, “0”: manual gain will apply at next VSYNC, “1”: manual gain will delay 1 frame to apply. LCCtrl7[4:2]: Auto Frame rate ceiling control. “000”: disable auto frame rate adjust. “001”: max frame rate down 1/2, “010”: 1/3, “011”:1/4, “100”: 1/5; “101”: 1/6; “110”: 1/7; “111”: 1/8. LCCtrl7[1:0]: Banding filter minimum exposure line MSBs, Band[9:8].
1A	LCCtrl8	80	RW	RSVD
1B	LCCtrl9	49	RW	RSVD
1C	LCCtrl10	00	R	Luminance control register 10 LCCtrl10[7:0]: image average luminance value.
1D	DVP3	00	RW	DVP control 3 DVP3[7:0]: GPIO direction control for data output port D[7:0].

1E	DVP4	00	RW	DVP control 4 DVP4[7]: PCLK output polarity control. DVP4[6]: HREF output polarity control. DVP4[5]: VSYNC output polarity control. DVP4[4]: PCLK pin GPIO control. DVP4[3]: HREF pin GPIO control DVP4[2]: VSYNC pin GPIO control. DVP4[1:0]: DVP D[9:8] pin GPIO control.
1F	DVP5	00	RW	DVP control 5 DVP5[7:2]: reserved. DVP4[1]: Frame sync function on/off selection, “0”: disable frame sync. “1”: enable frame sync. DVP4[0]: BLC function manually trigger on/off, “0”: disable manually BLC trigger mode, “1”: enable manually trigger mode .
20	FrameW	40	RW	Sensor frame time width LSBs, FrameW[7:0]
21	FrameW	06	RW	Sensor frame time width MSBs, FrameW[15:8] FrameW[15:0]: sensor frame width. T_{Row} = FrameW[15:0] * T_{PCLK}
22	FrameH	EE	RW	Sensor frame time high LSBs, FrameH[7:0]
23	FrameH	02	RW	Sensor frame time high MSBs, FrameH[15:8] FrameH[15:0]: sensor frame high. Sensor frame rate is defined as Fpclk / (FrameW*FrameH). Fpclk: frequency of pixel clock.
24	HWin	00	RW	Image horizontal output window width LSBs: Hwin[7:0]
25	Vwin	D0	RW	Image vertical output window high LSBs: Vwin[7:0]
26	HVWin	25	RW	Image output window horizontal and vertical MSBs. { Vwin[11:8],Hwin[11:8]}
27	HwinSt	34	RW	Image horizontal output window start position LSBs. HwinSt[7:0]
28	VwinSt	0D	RW	Image vertical output window start position LSBs. VwinSt[7:0]
29	HVWinSt	01	RW	Image output window horizontal and vertical start position MSBs. {VwinSt[11:8],HwinSt[11:8]}
2A-2B			RW	RSVD
2C	SenHASt	00	RW	Sensor physical column shift start address LSBs, SenHASt[7:0], each bit represent 2 pixels
2D	SenVSt	00	RW	Sensor physical vertical start address, LSBs. SenVSt[7:0], each bit represent 4 lines
2E	SenVEnd	B9	RW	Sensor physical vertical end address, LSBs. SenVEnd[7:0] , each bit represent 4 lines
2F	SenVadd	00	RW	Sensor vertical address settings. SenVadd[7:6]: RSVD SenVadd[5]: horizontal clock selection, “0”: normal, “1”: use half frequency clock as horizontal counter clock, if this bit set, need reduce all horizontal timing, window value in half to keep same timing with normal setting SenVadd[4]: RSVD SenVadd[3:2]: SenVEnd[9:8] SenVadd[1:0]: SenVSt[9:8]
30-35				RSVD
36	VS_Pos0	00	RW	VSYNC position LSBs ,VS_Pos [7:0]
37	VS_Pos1	40	RW	VSYNC position MSBs and VSYNC width. VS_Pos1[7:4]: VSYNC width in lines.; VS_Pos1[3:0]: VSYNC position MSBs , VS_Pos [11:8]

38	VaveSt	37	RW	Vertical average double count line start point.
39	VaveWid	92	RW	Vertical average double count line number.
3A-48				RSVD
49	BLC_TGT	04	RW	Black level calibration target level. BLC_TGT[7]: BLC offset polarity control. “0”: BLC target offset is positive. “1”: negative. BLC_TGT[6:0]: Black level calibration target level
4A	BLCCtrl	03	RW	BLC control BLCCtrl[7:4]: BLC highest bits for B/Gb/Gr/R channel, {B[10],Gb[10],Gr[10],R[10]} BLCCtrl[3:2]: BLC trigger frames. Only valid at trigger mode. “00”: BLC trigger 4 frames, “01”: 3 frames, “10”: 2 frame s, “11”: 1 frames. BLCCtrl[1]: BLC action option. “0”: Sensor do BLC only when triggered. “1”: always do BLC. BLCCtrl[0]: auto BLC function on/off selection. “0”: sensor stop calculate black value. “1”: sensor calculates black value automatically.
4B	BLC_B	00	RW	B channel black value LSBs. BLC_B[7:0]
4C	BLC_Gb	00	RW	Gb channel black value LSBs. BLC_Gb[7:0]
4D	BLC_Gr	00	RW	Gr channel black value LSBs. BLC_Gr[7:0]
4E	BLC_R	00	RW	R channel black value LSBs. BLC_R[7:0]
4F	BLC_H	00	RW	Black value MSBs. {BLC_R[9:8],BLC_Gr[9:8],BLC_Gb[9:8],BLC_B[9:8]}
50-69				RSVD
6A	PWC4	01	RW	Power and reference control 4 PWC4[7:4]: Black sun cancelling voltage control1 PWC4[3:0]: RSVD
6B				RSVD
6C	DPHY2	00	RW	DPHY2[7]: Mipi interface power down. DPHY2[6:0]:RSVD
6D-73				RSVD
74	Mipi5	53	RW	Mipi timing control register 5 Mipi5[7]: Mipi Sleep mode initial. Mipi should wait a complete frame than enter sleep mode. Mipi5[6]: Mipi clock land free running option. Mipi5[5:0]: reserved
75	Mipi6	2B	RW	Mipi timing control register 6 Mipi6[7:0]: Mipi output data type
76	Mipi7	40	RW	Mipi timing control register 7 Mipi7[7:0]: Mipi data lane word count value LSBs
77	Mipi8	06	RW	Mipi timing control register 8 Mipi8[7:0]: Mipi data lane word count value MSBs
78-BF				RSVD
C0	Group0	0A	RW	Group write 1st data address
C1	Group1	0A	RW	Group write 1st data value.

C2	Group2	0A	RW	Group write 2nd data address
C3	Group3	0A	RW	Group write 2nd data value.
:::	:::::::::	::	RW	::::::::::
FE	Group62	0A	RW	Group write 32nd data address
FF	Group63	0A	RW	Group write 32nd data value.

Document Revision Control

Version Number #	Date Released	Comments
R0.0	8/10/2014	Initial release of JX-H42 datasheet
R0.1	10/20/2014	Update logo, refer with H22
R0.2	11/16/2014	Update CSP info.
R1.0	11/21/2014	Update CSP, application schematic info.