视频编码解码芯片规格书
——AC5203A(B) 芯片

珠海市杰理科技有限公司

版本：**V1.0**

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AC5203A(B)硬件设计说明书 V1.0

特别注意事项

1、 LDOIN、VDDIO、USBAVDD 要求使用 3.3V(±5%范围内)供电。

2、 AVSS 不能直接在芯片处连数字 GND，需要把其定义为模拟地作处理。

3、 晶振及其他时钟的走线要尽可能短，走线切勿与其他信号线平行走线，并需用地线或电源线包裹。

4、 AVDD18 和 AVDD28 为芯片输出电压，可供给摄像头模组等使用。

1. 版本信息

日期	版本号	描述
2015.09.16	V1.0	原始版本。

2. 引脚定义

2.1 引脚分配
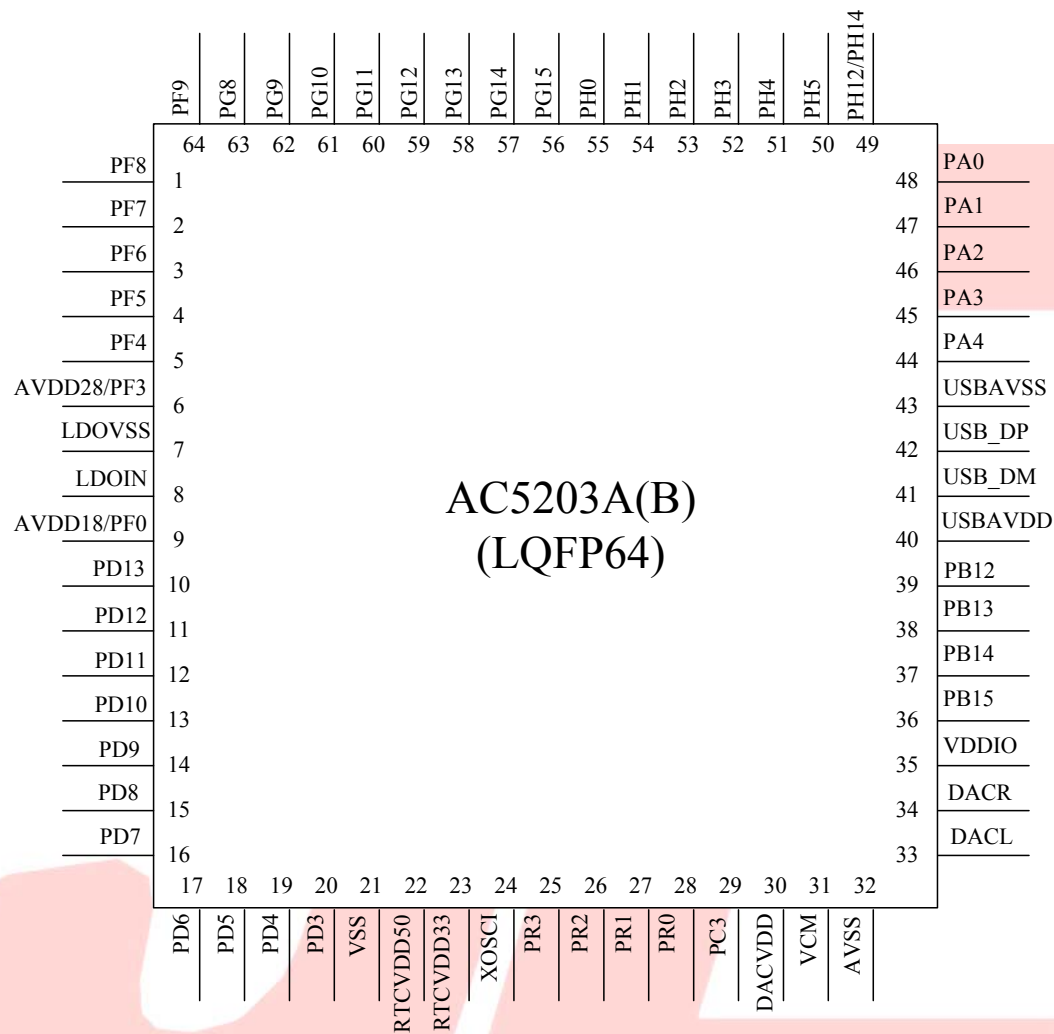
图 1   AC5203A(B) _LQFP64

2.2 引脚描述

(AC5203A/B)Pin#	Name	I/O Type	Function	Other Function
1	PF8	I/O	GPIO	SDR_BA0_B:SDRAM BA0 SENSOR1_D1_B: SENSOR1 Data 1 SD1_DAT0_A: SD Data 0 MPWM_L3_B: MOTOR PWM L3
2	PF7	I/O	GPIO	SDR_CS_BC:SDRAM CS# SENSOR1_D0_B: SENSOR1 Data 0 SD1_CLK_A: SD CLK MPWM_H2_B: MOTOR PWM H2
3	PF6	I/O	GPIO	SDR_RAS_BC:SDRAM RAS# SENSOR1_VSYNC_B: SENSOR1 Vertical Synchronization SD1_CMD_A: SD CMD MPWM_L2_B: MOTOR PWM L2
4	PF5	I/O	GPIO	SDR_CAS_BC:SDRAM CAS# SENSOR1_HSYNC_B: SENSOR1 Horizontal Synchronization SD1_DAT3_A: SD Data 3 MPWM_H1_B: MOTOR PWMH H1
5	PF4	I/O	GPIO	SDR_WE_BC:SDRAM WE# SENSOR1_CLK_B: SENSOR1 PCLK SD1_DAT2_A: SD Data 2 MPWM_L1_B: MOTOR PWMH L1
6	PF3	I/O	GPIO	UART2_RX_B: Uart2 Data In SDR_DQMH_BC: SDRAM DQ Mask High
	AVDD28	P	LDO OUT	2.8V Output
7	LDOVSS	P	Digital Ground	--
8	LDOIN	P	LDO Power In	———
9	AVDD18	P	LDO OUT	1.8V Output
	PF0	I/O	GPIO	UART2_TX_B: Uart2 Data Out SDR_DQML_BC: SDRAM DQ Mask Low
10	PD13	I/O	GPIO	SDR_A12_B:SDRAM A12 SENSOR0_D2_A: SENSOR0 Data 2
11	PD12	I/O	GPIO	SDR_A11_B:SDRAM A11 SENSOR0_D3_A: SENSOR0 Data 3
12	PD11	I/O	GPIO	SDR_A9_B:SDRAM A9 SENSOR0_D4_A: SENSOR0 Data 4 SD1_DAT1_C:SD1 Data1

13	PD10	I/O	GPIO	SDR_A8_B:SDRAM A8 SENSOR0_D5_A: SENSOR0 Data 5 SD1_DAT0_C:SD1 Data0
14	PD9	I/O	GPIO	SDR_A7_B:SDRAM A7 SENSOR0_D6_A: SENSOR0 Data 6 SD1_CLK_C:SD1 CLK
15	PD8	I/O	GPIO	SDR_A6_B:SDRAM A6 SENSOR0_D7_A: SENSOR0 Data 7 SD1_CMD_C:SD1 CMD
16	PD7	I/O	GPIO	SDR_A5_B:SDRAM A5 SENSOR0_D8_A: SENSOR0 Data 8 SD1_DAT3_C:SD1 Data3
17	PD6	I/O	GPIO	SDR_A4_B:SDRAM A4 SENSOR0_D9_A: SENSOR0 Data 9 SD1_DAT2_C:SD1 Data2
18	PD5	I/O	GPIO	UART0_RX_D: Uart0 Data In SENSOR0_VSYNC_A: SENSOR0 Vertical Synchronization IIC_SDA_A:IIC SDA
19	PD4	I/O	GPIO	UART0_TX_D: Uart0 Data Out SENSOR0_HSYNC_A: SENSOR0 Horizontal Synchronization IIC_SCL_A:IIC SCL
20	PD3	I/O	GPIO	SENSOR0_CLK_A: SENSOR0 PCLK
21	VSS	P	Digital Ground	--
22	RTCVDD50	P	RTC Power	--
23	RTCVDD33	P	RTC Power	--
24	XOSCI	I/O	RTC 32K OSC In	--
25	PR3	I/O	RTCIO	RTC32K OSC OUT
26	PR2	I/O	RTCIO	ADC12:ADC Input Channel 12
27	PR1	I/O	RTCIO	ADC13:ADC Input Channel 13
28	PR0	I/O	RTCIO	
29	PC3	I/O	GPIO	VPP UART1_RX_A: Uart1 Data In PWM3:TIMER3 PWM Output
30	DACVDD	P	DAC Power	--
31	VCM	P	VCM	--
32	AVSS	P	Analog Gound	--

33	DACL	O	DAC Left Channel	DACL
34	DACR	O	DAC Right Channel	DACR
35	VDDIO	P	IO Power	--
36	PB15	I/O	GPIO	UART3_RX_B: Uart3 Data In MIC LADC5
37	PB14	I/O	GPIO	UART3_TX_B: Uart3 Data Out AMUX0R: Simulator Channel 0 Right IIC_SDA_B:IIC SDA WAKEUP9: Port Wakeup LADC4
38	PB13	I/O	GPIO	AVOUT: AV Output WAKEUP8: Port Wakeup LADC3 PWM1:TIMER1 PWM Output
39	PB12	I/O	GPIO	AMUX0L: Simulator Channel 0 Left SENSOR0_D0_B: SENSOR0 Data 0 IIC_SCL_B:IIC SCL
40	USBAVDD	P	USB Power	--
41	USB_DM	I/O	HUSB DM	--
42	USB_DP	I/O	HUSB DP	--
43	USBAVSS	P	USB Ground	--
44	PA4	I/O	GPIO	ADC1:ADC Input Channel 1 SPI0_CLK_A:SPI0 Clock SFC_CLK:SFC Clock SD0_DAT0_A: SD Data 0
45	PA3	I/O	GPIO	SPI0_DO(0)_A:SPI0 DO(Data 0) SFC_DO(0):SFC DO(Data 0) SD0_DAT2_A: SD Data 2
46	PA2	I/O	GPIO	ADC0:ADC Input Channel 0 IIC_SCL_A:IIC SCL SPI0_DAT2_A:SPI0 Data2 SFC_DAT2:SFC Data2 SD0_CLK_A: SD CLK
47	PA1	I/O	GPIO	IIC_SDA_C:IIC SDA SPI0_DI(1)_A:SPI0 DI(Data 1) SFC_DI(1): SFC_Data 1 SD0_CMD_A: SD CMD
48	PA0	I/O	GPIO	SPI0_CS_A :SPI0 Chip Select SFC_CS :SFC Chip Select

49	PH14	I/O	GPIO	UART1_TX_C: Uart1 Data Out ADC6:ADC Input Channel 6 CLKOUT1: Clock Out 1 WAKEUP14: Port Wakeup
	PH12	I/O	GPIO	UART0_TX_C: Uart0 Data Out ALNK_MCK:AUDIO LIN MASTER CLK PWM2:TIMER2 PWM Output LVD: LVD Test Pin
50	PH5	I/O	GPIO	LCD_VSYNC: LCD Vertical Synchronization UART1_RX_B: Uart1 Data In SPI1_DI_A :SPI1 Data In LCD_SEG21:LCD SEG Output21
51	PH4	I/O	GPIO	LCD_HSYNC:LCD Horizontal Synchronization SPI1_DO_A :SPI1 Data Out LCD_SEG20:LCD SEG Output20 EMI_RD:EMI Read
52	PH3	I/O	GPIO	LCD_DEN:LCD Data Enable EMI_WR:EMI Write SPI1_CLK_A:SPI1 Clock LCD_SEG19:LCD SEG Output19
53	PH2	I/O	GPIO	LCD_DCLK:LCD Data CLK UART1_TX_B: Uart1 Data Out LCD_SEG18:LCD SEG Output18
54	PH1	I/O	GPIO	LCD_DAT17:LCD Data17 UART2_RX_D: Uart2 Data In ADC5:ADC Input Channel 5 LCD_SEG17:LCD SEG Output17 Timer2:TIMER2 Clock In WAKEUP11: Port Wakeup OSCO:OSC Out
55	PH0	I/O	GPIO	LCD_DAT16:LCD Data16 UART2_TX_D: Uart2 Data Out ADC4:ADC Input Channel 4 LCD_SEG16:LCD SEG Output16 WAKEUP10: Port Wakeup OSCI:OSC In
56	PG15	I/O	GPIO	LCD_DAT15:LCD Data15 EMI_D15:EMI Data15 LCD_SEG15:LCD SEG Output15

57	PG14	I/O	GPIO	LCD_DAT14:LCD Data14 EMI_D14:EMI Data14 LCD_SEG14:LCD SEG Output14
58	PG13	I/O	GPIO	LCD_DAT13:LCD Data13 EMI_D13:EMI Data13 SD0_DAT1_D: SD Data 1 LCD_SEG13:LCD SEG Output13
59	PG12	I/O	GPIO	LCD_DAT12:LCD Data12 EMI_D12:EMI Data12 SD0_DAT0_D: SD Data 0 LCD_SEG12:LCD SEG Output12
60	PG11	I/O	GPIO	LCD_DAT11:LCD Data11 EMI_D11:EMI Data11 SD0_CLK_D: SD Clock LCD_SEG11:LCD SEG Output11
61	PG10	I/O	GPIO	LCD_DAT10:LCD Data10 EMI_D10:EMI Data10 SD0_CMD_D: SD Command LCD_SEG10:LCD SEG Output10
62	PG9	I/O	GPIO	LCD_DAT9:LCD Data9 EMI_D9:EMI Data9 SD0_DAT3_D: SD Data 3 LCD_SEG9:LCD SEG Output9
63	PG8	I/O	GPIO	LCD_DAT8:LCD Data8 EMI_D8:EMI Data8 SD0_DAT2_D: SD Data 2 LCD_SEG8:LCD SEG Output8
64	PF9	I/O	GPIO	SDR_BA1_B:SDRAM BA1 SENSOR1_D2_B: SENSOR1 Data 2 SD1_DAT1_A: SD Data 1 MPWM_H3_B: MOTOR PWM H3

（★说明：1、P----Power Supply   2、I----Input   3、O----Output   4、I/O----Bi-direction）

3. 电气特性

3.1 I/O 输入、输出高低逻辑特性

IO 输入特性						
符号	参数	最小	典型	最大	单位	测试条件
V_{IL}	Low-Level Input Voltaget	-0.3	–	0.3*VDDIO	V	VDDIO = 3.3V
V_{IH}	High-Level Input Voltage	0.7*VDDIO	–	VDDIO+0.3	V	VDDIO = 3.3V
输出特性						
V_{OL}	Low-Level Output Voltaget	–	–	0.33	V	VDDIO = 3.3V
V_{OH}	High-Level Output Voltaget	2.7	–	–	V	VDDIO = 3.3V

3.2 I/O 输出能力、上下拉电阻特性

Port 口	输出能力	上拉电阻	下拉电阻	备注
PA0 – PA4 PB12 - PB15 PD3 - PD13 PF0 PF3 – PF9 PH12 PH14	强驱：24mA 弱驱： 8mA	10K	60K	---
PG8 – PG15 PH0 – PH5	强驱：24 mA 弱驱：8mA（片内串接200Ω电阻）	10K	60K	---
PC3	8 mA(无强弱驱之分)	10K	60K	---
PR0 – PR3	8mA（片内串接200Ω电阻）	10K	60K	RTC 模块需供电
AVDD18	电压可调：1.5V-1.9V （电流约为60 mA）	---	---	LDOIN=3.3V
AVDD28	电压可调：2.7V-3.1V （电流约为100 mA）	---	---	LDOIN=3.3V

（★说明：上下拉电阻的精度约为±20%）

3.3 DAC 特性

符号	参数	最小	典型	最大	单位	测试条件
SNR	Signal to Noise Ratio		86		dB	1KHz，SR=44.1K，静音文件，CR=192Kbps
THD+N	Total Harmoni Distortion+Noise		-78		dB	(-1.5db) 1KHz，SR=44.1K，CR=192Kbps

4. 封装规格

4.1 LQFP-64PIN 封装图

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.60
A1	0.05	—	0.20
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.17	—	0.25
b1	0.16	0.18	0.20
c	0.13	—	0.18
c1	0.12	0.127	0.14
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
eB	8.10	—	8.25
e	0.40BSC		
L	0.40	—	0.65
L1	1.00BSC		
θ	0	—	7°
L/F载体尺寸 (mil)	160*160		
	210*210		