Version:0.2

WQVGA(240x432) driver for LTPS

1. General Description

The D54E4PA7551B is a driver for LTPS panel with timing controller, RAM, internal 5V booster.

Realizing WIDE-QVGA (WQVGA) display with one chip is possible with this driver just adding gate control circuits and its HV power circuit in LTPS panel.

For the portable system like a cellular phone which needs to switch the display performance, this driver adopts the software commands to control the functions like standby other than Normal display operation to minimize the power consumption of the mobile device.

120 channel source output ports are embedded and the display data levels are outputted in the order of programming by SSD method (Shared Source Driving).

The display data is written to internal RAM from external controller so that the 64 gray-level driving per color is available.

2. Features

- Panel driving
  - 120 source output (SX1~SX120), 6SSD(Shared Source Driving) method
  - 260 thousand color (6 bit = 64 gray color)
  - Output pitch : straight array : 56um(min), source : 67um
  - vertical 320 ~ 432 line selectable
  - panel control signal generation (gate driver / SSD switch, panel booster control signals)
  - Precharge ON / OFF by command
  - SSD driving sequence selection.
  - inversion of left / right / up / down

- Interface
  - CPU I/F : Parallel I/F I80 system / BUS-width 18/16/9/8 bit selection available.

- Internal EEPROM

  16-bit built-in EEPROM for VCOM (VCOMH, VCOML) set

  Internal EEPROM for manufacture (Trimming for MagnaChip use, it is forbidden for users)

- Others
  - RAM control : internal RAM 1,866,240-bit (240x432x18-bit) = 233,280-byte

    Window access, partial display, screen scroll mode
  - Standby mode (RAM and register data are kept during Standby mode)
  - Auto Sequence by command (Standby IN and Standby OUT function)
  - Noise canceller on RESET line (discarded less than 2us)
  - internal oscillator 1.15 MHz ± 8%

- Low power consumption function
  - ・1 or 2-screen partial display + scan skip mode on non display partial area.
  - ・refresh rate control with 60 Hz and 30 Hz
  - ・driving power control for channel AMP by register setting

- Power circuits to drive LCD
  - ・2 or 3 times booster(1)
    Controlled by register setting and the output detecting method circuits are adopted.
    Output voltage range: 4.7 ~ 5.4 V / 100mV step controllable
    Load current: 2mA
    Power for source driver
    Regulator for gamma circuits: 4.6 ~ 5.3 V / 100 mV step controllable
  - ・2 or 3 times booster(2)
    Controlled by register setting and the output detecting method circuits are adopted.
    Output voltage range: 4.7 ~ 5.4V / 100 mV step controllable
    Load current: 2mA
    Power for Panel control level shifters
    Power for VCOM related circuits

- VCOM driver (3 kinds of driving is possible)
  VCOMH-VCOML switching method
  VCOM-GND DC bias method
  DC method
  VCOMH regulator: 3~5V (depends on VGM voltage) / 20mV step controllable
  VCOML/COMDC regulator: 0.2~ 3.2 V / 20mV step

- Power
  - ・analog power = 2.7V~3.4V
  - ・IO power = 1.6~3.4V

- Gray output
  - ・Fixed gamma method (independent blue gamma)
  - ・6-bit DAC

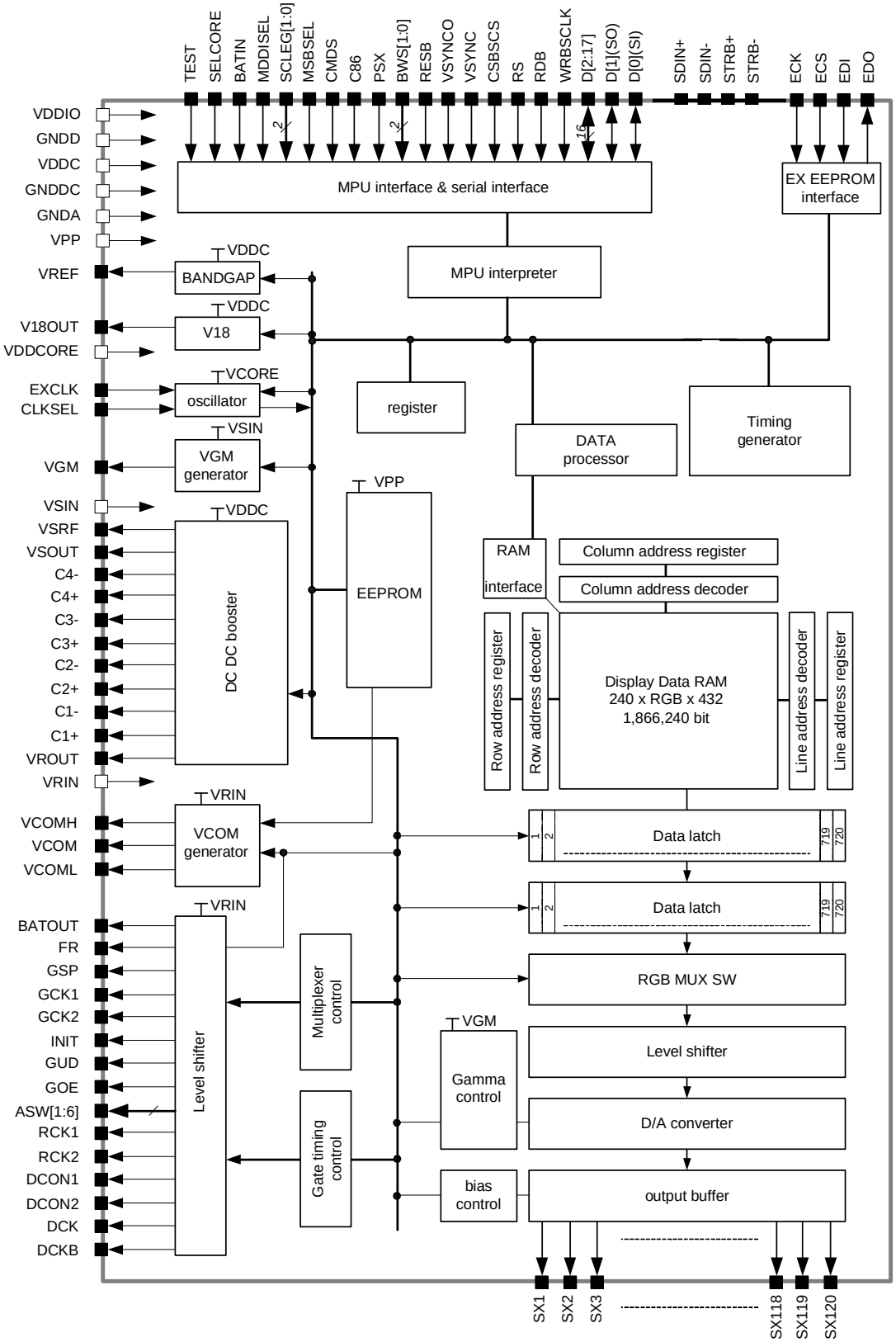
- Source driver ability
  - ・source load : R=5kΩ、C=30pF
  - ・settling time : 2.5us (Max)
  - ・variation : 15mV（middle gray）

- Operating temperature : -30 to +85°C

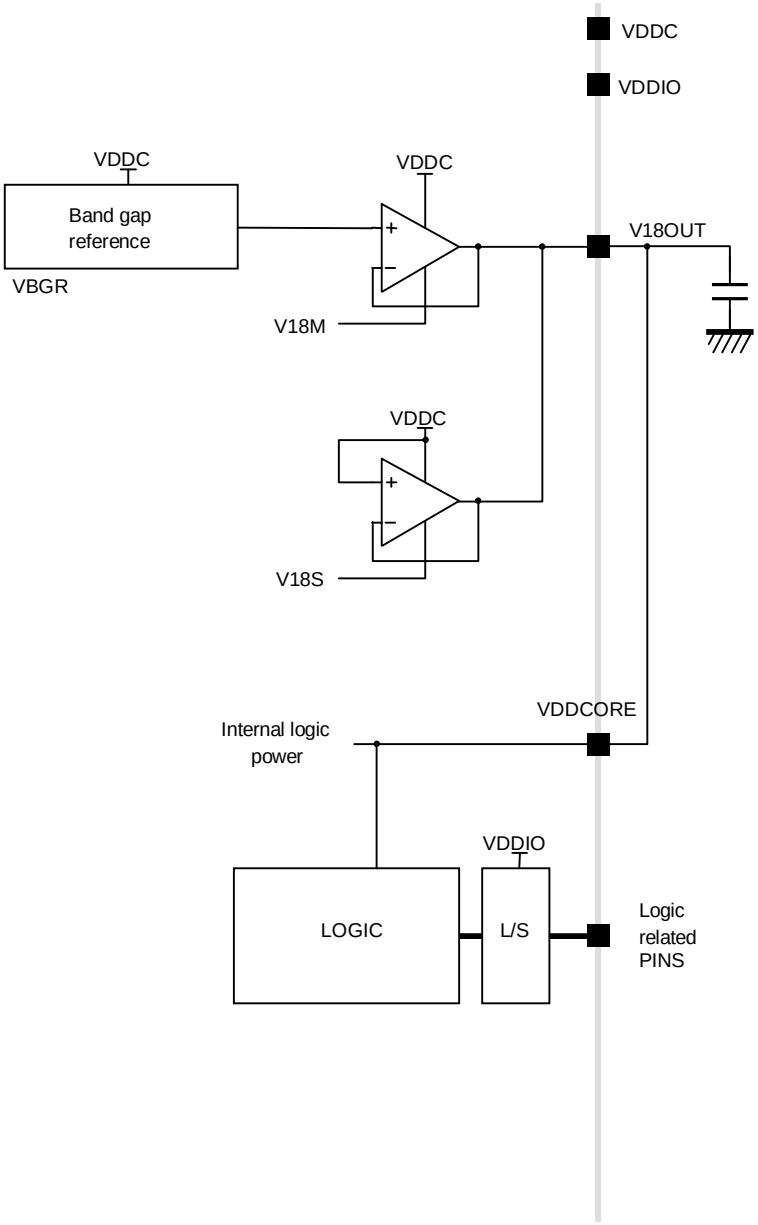
- Package : Bare Chip / Bumped chip
- CMOS technology (P-type silicon substrate)

3. Block diagram

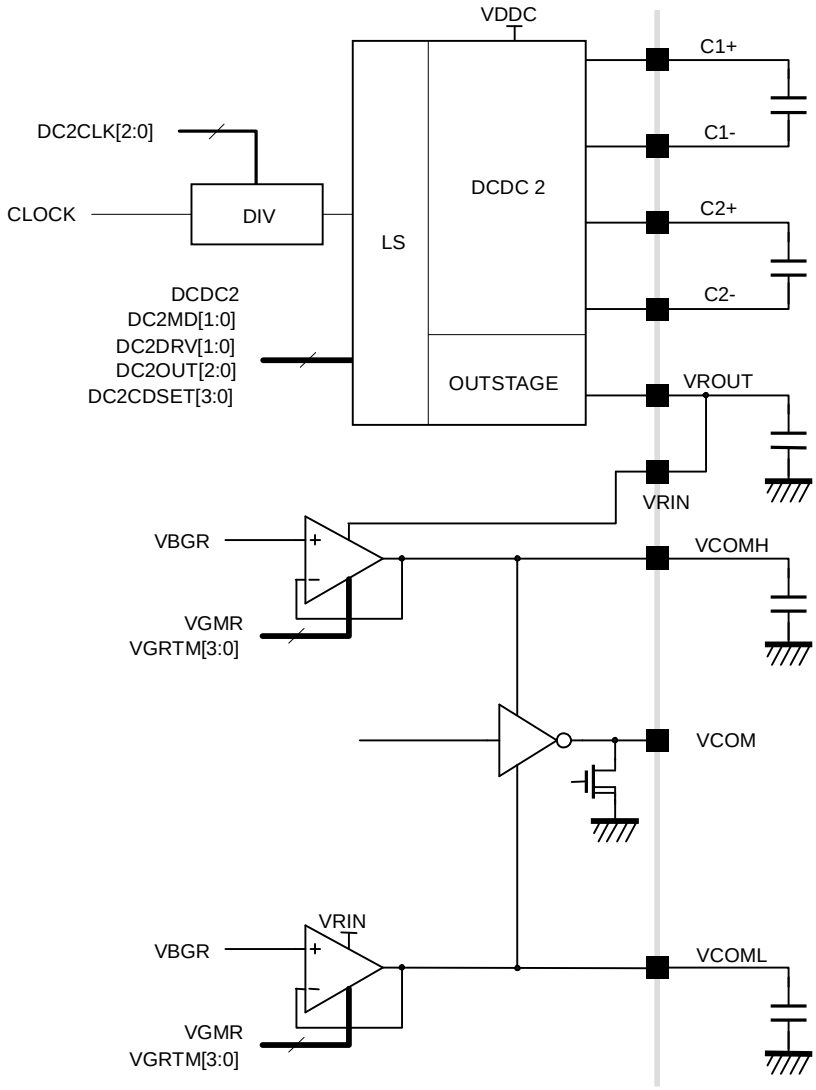
3.1. Top block diagram



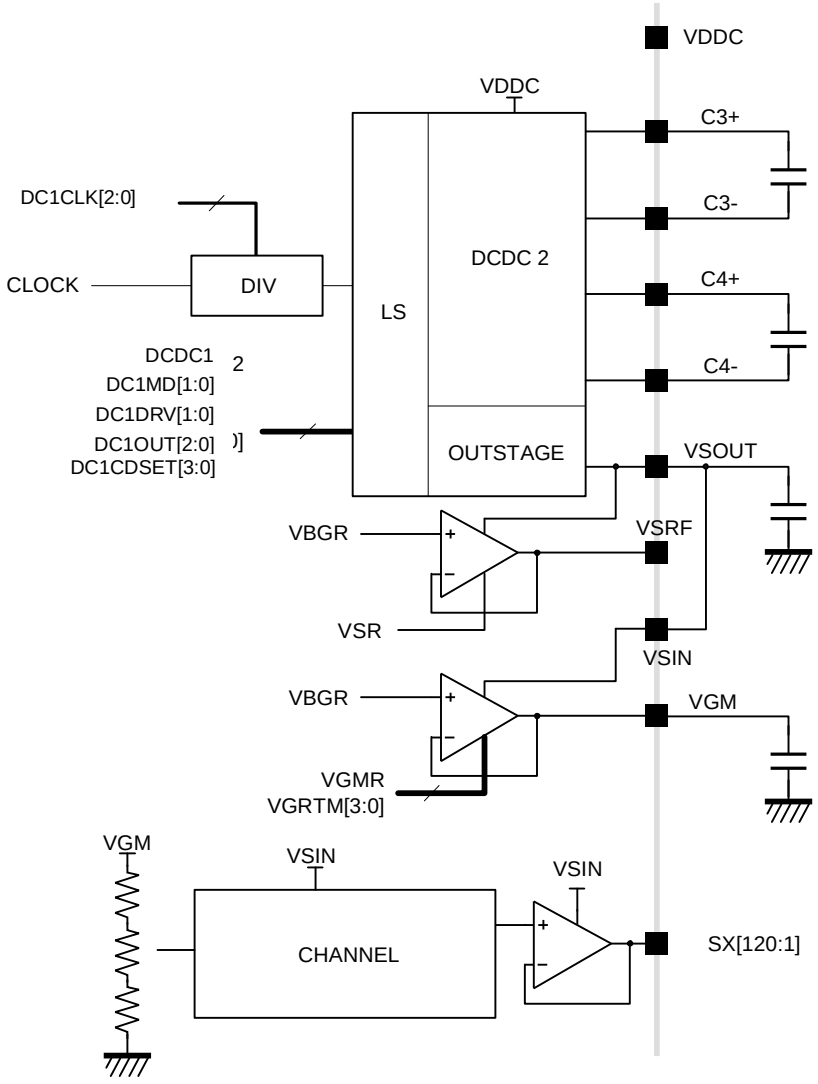
3.2. Block Diagram of Power circuits (1)



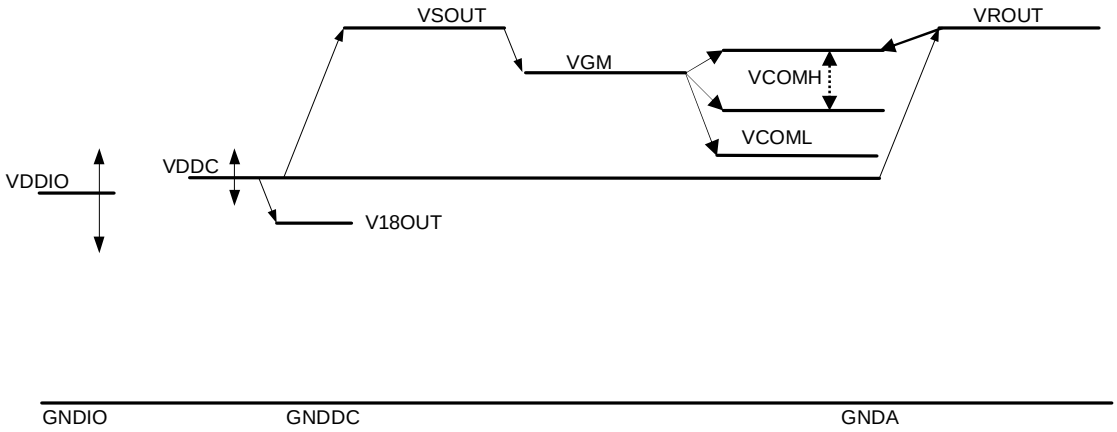
3.3. Block Diagram of Power circuits (2)



3.4. Block diagram of Power circuits (3)

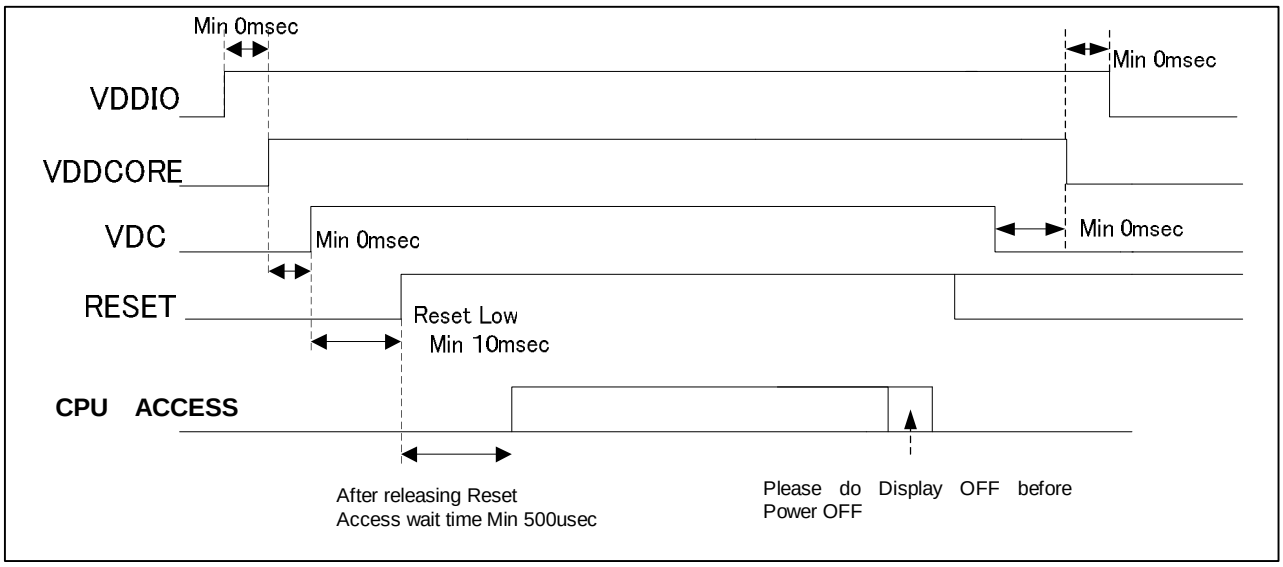


3.5. Chart of Power structure



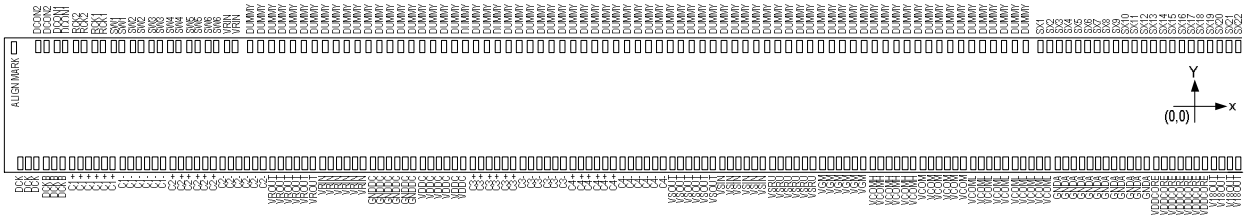
Notice) VCOMH 0.5×VGM≦VCOMH≦1.208×VGM and VCOMH≦VROUT-0.2

3.6. Power On/Off Timing Chart



4. PAD assignment

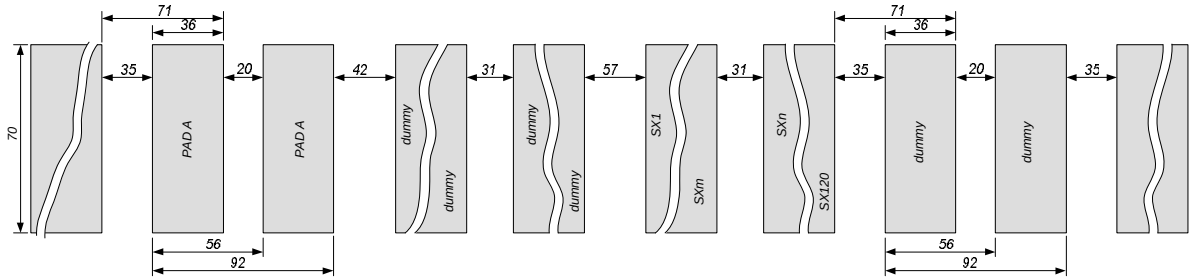
All of PAD position and/or shape information described in this section are viewed from TOP (PAD) side.



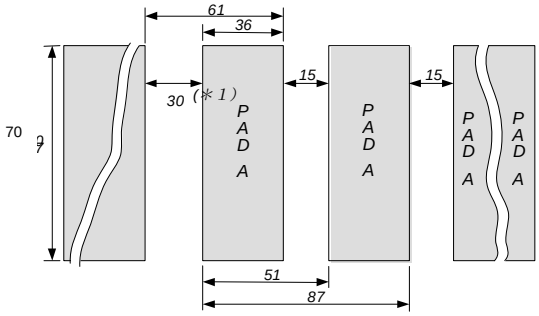
PAD assignment (Left side of Chip PAD view)

※ Dummy PADs are opened electrically.

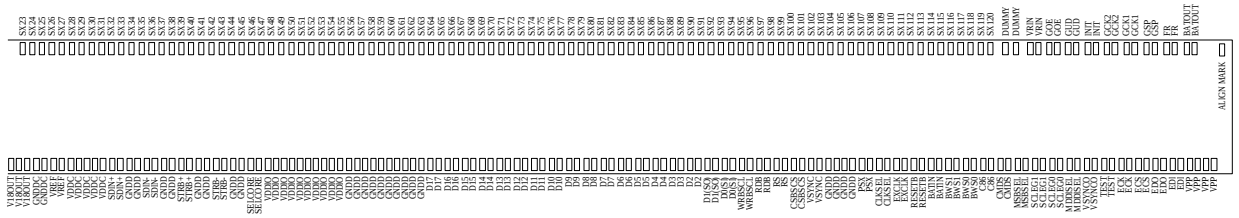
Bump size and space of drive side



Bump size and space of interface side



(*1) Space only between VREF and VDDC is 30um.



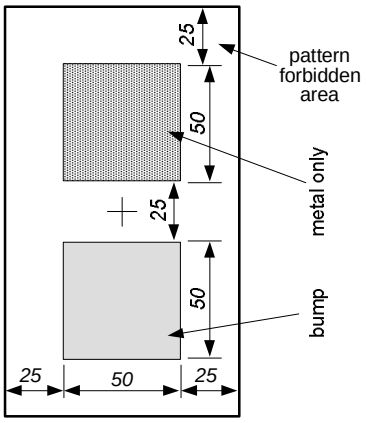
PAD assignment (Right side of Chip PAD view)

D54E4PA7551 PAD DIMENSIONS

UNIT: um

ITEMS	REMARK / PAD NO.	SIZE	
		X	Y
Chip size	With scribe lane (110 um)	16,110	1,710
	Without scribe lane	16,000	1,600
	After sawing (typical)	16,060	1,660
PAD pitch / space (bump)	Drive pads pitch	20,31,42,57(see Page8)	
	Interface pads	15,25,30(see Page8)	
PAD open size (2 open/1 bump)	Driver sides	7	56
	Interface sides	7	56
PAD size(bump)	Driver sides	36	70
	Interface sides	36	70
BUMP height	All pads	15	

ALIGN MARK DESIGN



align mark

Align marks coordinates

LEFT TOP – center coordinates X = -7934, Y = 695.5

RIGHT TOP – center coordinates X = 7934, Y = 695.5

5. PADs coordinates

Chip size 16,060×1,660㎛ (without SL, chip center = 0:0)

PAD No.	Pin name	X(㎛)	Y(㎛)	PAD No.	Pin name	X (㎛)	Y (㎛)	PAD No.	Pin name	X ((m)	Y ((m)
1	DCK	-7782	-730	51	VDDC	-5142	-730	101	VGM	-2512	-730
2	DCK	-7731	-730	52	VDDC	-5091	-730	102	VGM	-2461	-730
3	DCK	-7680	-730	53	VDDC	-5040	-730	103	VGM	-2410	-730
4	DCKB	-7619	-730	54	VDDC	-4989	-730	104	VCOMH	-2349	-730
5	DCKB	-7568	-730	55	C3+	-4928	-730	105	VCOMH	-2298	-730
6	DCKB	-7517	-730	56	C3+	-4877	-730	106	VCOMH	-2247	-730
7	C1+	-7456	-730	57	C3+	-4826	-730	107	VCOMH	-2196	-730
8	C1+	-7405	-730	58	C3+	-4775	-730	108	VCOMH	-2145	-730
9	C1+	-7354	-730	59	C3+	-4724	-730	109	VCOMH	-2094	-730
10	C1+	-7303	-730	60	C3+	-4673	-730	110	VCOM	-2033	-730
11	C1+	-7252	-730	61	C3-	-4612	-730	111	VCOM	-1982	-730
12	C1+	-7201	-730	62	C3-	-4561	-730	112	VCOM	-1931	-730
13	C1-	-7140	-730	63	C3-	-4510	-730	113	VCOM	-1880	-730
14	C1-	-7089	-730	64	C3-	-4459	-730	114	VCOM	-1829	-730
15	C1-	-7038	-730	65	C3-	-4408	-730	115	VCOM	-1778	-730
16	C1-	-6987	-730	66	C3-	-4357	-730	116	VCOML	-1717	-730
17	C1-	-6936	-730	67	C4+	-4296	-730	117	VCOML	-1666	-730
18	C1-	-6885	-730	68	C4+	-4245	-730	118	VCOML	-1615	-730
19	C2+	-6824	-730	69	C4+	-4194	-730	119	VCOML	-1564	-730
20	C2+	-6773	-730	70	C4+	-4143	-730	120	VCOML	-1513	-730
21	C2+	-6722	-730	71	C4+	-4092	-730	121	VCOML	-1452	-730
22	C2+	-6671	-730	72	C4+	-4041	-730	122	VCOML	-1401	-730
23	C2+	-6620	-730	73	C4-	-3980	-730	123	VCOML	-1350	-730
24	C2+	-6569	-730	74	C4-	-3929	-730	124	VCOML	-1299	-730
25	C2-	-6508	-730	75	C4-	-3878	-730	125	VCOML	-1248	-730
26	C2-	-6457	-730	76	C4-	-3827	-730	126	GNDA	-1187	-730
27	C2-	-6406	-730	77	C4-	-3776	-730	127	GNDA	-1136	-730
28	C2-	-6355	-730	78	C4-	-3725	-730	128	GNDA	-1085	-730
29	C2-	-6304	-730	79	VSOUT	-3664	-730	129	GNDA	-1034	-730
30	C2-	-6253	-730	80	VSOUT	-3613	-730	130	GNDA	-983	-730
31	VROUT	-6192	-730	81	VSOUT	-3562	-730	131	GNDA	-932	-730
32	VROUT	-6141	-730	82	VSOUT	-3511	-730	132	GNDA	-881	-730
33	VROUT	-6090	-730	83	VSOUT	-3460	-730	133	GNDA	-830	-730
34	VROUT	-6039	-730	84	VSOUT	-3409	-730	134	GNDA	-779	-730
35	VROUT	-5988	-730	85	VSIN	-3348	-730	135	GNDA	-728	-730
36	VROUT	-5937	-730	86	VSIN	-3297	-730	136	GNDA	-677	-730
37	VRIN	-5876	-730	87	VSIN	-3246	-730	137	GNDA	-626	-730
38	VRIN	-5825	-730	88	VSIN	-3195	-730	138	VDDCORE	-565	-730
39	VRIN	-5774	-730	89	VSIN	-3144	-730	139	VDDCORE	-514	-730
40	VRIN	-5723	-730	90	VSIN	-3093	-730	140	VDDCORE	-463	-730
41	VRIN	-5672	-730	91	VSRU	-3032	-730	141	VDDCORE	-412	-730
42	VRIN	-5621	-730	92	VSRU	-2981	-730	142	VDDCORE	-361	-730
43	GNDDC	-5560	-730	93	VSRU	-2930	-730	143	VDDCORE	-310	-730
44	GNDDC	-5509	-730	94	VSRU	-2879	-730	144	VDDCORE	-259	-730
45	GNDDC	-5458	-730	95	VSRU	-2828	-730	145	V18OUT	-198	-730
46	GNDDC	-5407	-730	96	VSRU	-2777	-730	146	V18OUT	-147	-730
47	GNDDC	-5356	-730	97	VGM	-2716	-730	147	V18OUT	-96	-730
48	GNDDC	-5305	-730	98	VGM	-2665	-730	148	V18OUT	-45	-730
49	VDDC	-5244	-730	99	VGM	-2614	-730	149	V18OUT	6	-730
50	VDDC	-5193	-730	100	VGM	-2563	-730	150	V18OUT	57	-730

** The dummy port is opened electrically.*

chip size 16,060×1,660μm (without SL, chip center = 0:0)

PAD No.	Pin name	X(μm)	Y(μm)	PAD No.	Pin name	X (μm)	Y (μm)	PAD No.	Pin name	X (μm)	Y (μm)
151	V18OUT	108	-730	201	D16	2823	-730	251	CLKSEL	5613	-730
152	GNDD	169	-730	202	D16	2874	-730	252	CLKSEL	5664	-730
153	GNDD	220	-730	203	D15	2935	-730	253	EXCLK	5725	-730
154	VREF	281	-730	204	D15	2986	-730	254	EXCLK	5776	-730
155	VREF	332	-730	205	D14	3047	-730	255	RESETB	5837	-730
156	VDDC	398	-730	206	D14	3098	-730	256	RESETB	5888	-730
157	VDDC	449	-730	207	D13	3159	-730	257	BATIN	5949	-730
158	VDDC	500	-730	208	D13	3210	-730	258	BATIN	6000	-730
159	VDDC	551	-730	209	D12	3271	-730	259	BWS1	6061	-730
160	VDDC	602	-730	210	D12	3322	-730	260	BWS1	6112	-730
161	SDIN+	663	-730	211	D11	3383	-730	261	BWS0	6173	-730
162	SDIN+	714	-730	212	D11	3434	-730	262	BWS0	6224	-730
163	GNDD	775	-730	213	D10	3495	-730	263	C86	6285	-730
164	GNDD	826	-730	214	D10	3546	-730	264	C86	6336	-730
165	SDIN-	887	-730	215	D9	3607	-730	265	CMDS	6397	-730
166	SDIN-	938	-730	216	D9	3658	-730	266	CMDS	6448	-730
167	GNDD	999	-730	217	D8	3719	-730	267	MSBSEL	6509	-730
168	GNDD	1050	-730	218	D8	3770	-730	268	MSBSEL	6560	-730
169	STRB+	1111	-730	219	D7	3831	-730	269	SCLEG1	6621	-730
170	STRB+	1162	-730	220	D7	3882	-730	270	SCLEG1	6672	-730
171	GNDD	1223	-730	221	D6	3943	-730	271	SCLEG0	6733	-730
172	GNDD	1274	-730	222	D6	3994	-730	272	SCLEG0	6784	-730
173	STRB-	1335	-730	223	D5	4055	-730	273	MDDISEL	6845	-730
174	STRB-	1386	-730	224	D5	4106	-730	274	MDDISEL	6896	-730
175	GNDD	1447	-730	225	D4	4167	-730	275	VSYNCO	6957	-730
176	GNDD	1498	-730	226	D4	4218	-730	276	VSYNCO	7008	-730
177	SELCORE	1559	-730	227	D3	4279	-730	277	TEST	7069	-730
178	SELCORE	1610	-730	228	D3	4330	-730	278	TEST	7120	-730
179	VDDIO	1671	-730	229	D2	4391	-730	279	ECK	7181	-730
180	VDDIO	1722	-730	230	D2	4442	-730	280	ECK	7232	-730
181	VDDIO	1773	-730	231	D1	4503	-730	281	ECS	7293	-730
182	VDDIO	1824	-730	232	D1	4554	-730	282	ECS	7344	-730
183	VDDIO	1875	-730	233	D0	4615	-730	283	EDO	7405	-730
184	VDDIO	1926	-730	234	D0	4666	-730	284	EDO	7456	-730
185	VDDIO	1977	-730	235	WRBSCL	4727	-730	285	EDI	7517	-730
186	VDDIO	2028	-730	236	WRBSCL	4778	-730	286	EDI	7568	-730
187	VDDIO	2079	-730	237	RDB	4839	-730	287	VPP	7629	-730
188	VDDIO	2130	-730	238	RDB	4890	-730	288	VPP	7680	-730
189	GNDD	2191	-730	239	RS	4951	-730	289	VPP	7731	-730
190	GNDD	2242	-730	240	RS	5002	-730	290	VPP	7782	-730
191	GNDD	2293	-730	241	CSBSCS	5063	-730	291	DCON2	-7782	730
192	GNDD	2344	-730	242	CSBSCS	5114	-730	292	DCON2	-7726	730
193	GNDD	2395	-730	243	VSYNC	5175	-730	293	DCON1	-7655	730
194	GNDD	2446	-730	244	VSYNC	5226	-730	294	DCON1	-7599	730
195	GNDD	2497	-730	245	GNDD	5287	-730	295	RCK2	-7528	730
196	GNDD	2548	-730	246	GNDD	5338	-730	296	RCK2	-7472	730
197	GNDD	2599	-730	247	GNDD	5389	-730	297	RCK1	-7401	730
198	GNDD	2650	-730	248	GNDD	5440	-730	298	RCK1	-7345	730
199	D17	2711	-730	249	PSX	5501	-730	299	SW1	-7274	730
200	D17	2762	-730	250	PSX	5552	-730	300	SW1	-7218	730

** The dummy port is opened electrically.*

chip size 16,060×1,660㎛ (without SL, chip center = 0:0)

PAD No.	Pin name	X((m)	Y((m)	PAD No.	Pin name	X ((m)	Y ((m)	PAD No.	Pin name	X ((m)	Y ((m)
301	SW2	-7147	730	351	dummy	-3832	730	401	SX16	-456	730
302	SW2	-7091	730	352	dummy	-3765	730	402	SX17	-389	730
303	SW3	-7020	730	353	dummy	-3698	730	403	SX18	-322	730
304	SW3	-6964	730	354	dummy	-3631	730	404	SX19	-255	730
305	SW4	-6893	730	355	dummy	-3564	730	405	SX20	-188	730
306	SW4	-6837	730	356	dummy	-3497	730	406	SX21	-121	730
307	SW5	-6766	730	357	dummy	-3430	730	407	SX22	-54	730
308	SW5	-6710	730	358	dummy	-3363	730	408	SX23	13	730
309	SW6	-6639	730	359	dummy	-3296	730	409	SX24	80	730
310	SW6	-6583	730	360	dummy	-3229	730	410	SX25	147	730
311	VRIN	-6512	730	361	dummy	-3162	730	411	SX26	214	730
312	VRIN	-6456	730	362	dummy	-3095	730	412	SX27	281	730
313	dummy	-6378	730	363	dummy	-3028	730	413	SX28	348	730
314	dummy	-6311	730	364	dummy	-2961	730	414	SX29	415	730
315	dummy	-6244	730	365	dummy	-2894	730	415	SX30	482	730
316	dummy	-6177	730	366	dummy	-2827	730	416	SX31	549	730
317	dummy	-6110	730	367	dummy	-2760	730	417	SX32	616	730
318	dummy	-6043	730	368	dummy	-2693	730	418	SX33	683	730
319	dummy	-5976	730	369	dummy	-2626	730	419	SX34	750	730
320	dummy	-5909	730	370	dummy	-2559	730	420	SX35	817	730
321	dummy	-5842	730	371	dummy	-2492	730	421	SX36	884	730
322	dummy	-5775	730	372	dummy	-2425	730	422	SX37	951	730
323	dummy	-5708	730	373	dummy	-2358	730	423	SX38	1018	730
324	dummy	-5641	730	374	dummy	-2291	730	424	SX39	1085	730
325	dummy	-5574	730	375	dummy	-2224	730	425	SX40	1152	730
326	dummy	-5507	730	376	dummy	-2157	730	426	SX41	1219	730
327	dummy	-5440	730	377	dummy	-2090	730	427	SX42	1286	730
328	dummy	-5373	730	378	dummy	-2023	730	428	SX43	1353	730
329	dummy	-5306	730	379	dummy	-1956	730	429	SX44	1420	730
330	dummy	-5239	730	380	dummy	-1889	730	430	SX45	1487	730
331	dummy	-5172	730	381	dummy	-1822	730	431	SX46	1554	730
332	dummy	-5105	730	382	dummy	-1755	730	432	SX47	1621	730
333	dummy	-5038	730	383	dummy	-1688	730	433	SX48	1688	730
334	dummy	-4971	730	384	dummy	-1621	730	434	SX49	1755	730
335	dummy	-4904	730	385	dummy	-1554	730	435	SX50	1822	730
336	dummy	-4837	730	386	SX1	-1461	730	436	SX51	1889	730
337	dummy	-4770	730	387	SX2	-1394	730	437	SX52	1956	730
338	dummy	-4703	730	388	SX3	-1327	730	438	SX53	2023	730
339	dummy	-4636	730	389	SX4	-1260	730	439	SX54	2090	730
340	dummy	-4569	730	390	SX5	-1193	730	440	SX55	2157	730
341	dummy	-4502	730	391	SX6	-1126	730	441	SX56	2224	730
342	dummy	-4435	730	392	SX7	-1059	730	442	SX57	2291	730
343	dummy	-4368	730	393	SX8	-992	730	443	SX58	2358	730
344	dummy	-4301	730	394	SX9	-925	730	444	SX59	2425	730
345	dummy	-4234	730	395	SX10	-858	730	445	SX60	2492	730
346	dummy	-4167	730	396	SX11	-791	730	446	SX61	2559	730
347	dummy	-4100	730	397	SX12	-724	730	447	SX62	2626	730
348	dummy	-4033	730	398	SX13	-657	730	448	SX63	2693	730
349	dummy	-3966	730	399	SX14	-590	730	449	SX64	2760	730
350	dummy	-3899	730	400	SX15	-523	730	450	SX65	2827	730

** The dummy port is opened electrically.*

chip size 16,060×1,660μm (without SL, chip center = 0:0)

PAD No.	Pin name	X(μm)	Y(μm)	PAD No.	Pin name	X (μm)	Y (μm)	PAD No.	Pin name	X (μm)	Y (μm)
451	SX66	2894	730	501	SX116	6244	730				
452	SX67	2961	730	502	SX117	6311	730				
453	SX68	3028	730	503	SX118	6378	730				
454	SX69	3095	730	504	SX119	6445	730				
455	SX70	3162	730	505	SX120	6512	730				
456	SX71	3229	730	506	dummy	6583	730				
457	SX72	3296	730	507	dummy	6639	730				
458	SX73	3363	730	508	VRIN	6710	730				
459	SX74	3430	730	509	VRIN	6766	730				
460	SX75	3497	730	510	GOE	6837	730				
461	SX76	3564	730	511	GOE	6893	730				
462	SX77	3631	730	512	GUD	6964	730				
463	SX78	3698	730	513	GUD	7020	730				
464	SX79	3765	730	514	INIT	7091	730				
465	SX80	3832	730	515	INIT	7147	730				
466	SX81	3899	730	516	GCK2	7218	730				
467	SX82	3966	730	517	GCK2	7274	730				
468	SX83	4033	730	518	GCK1	7345	730				
469	SX84	4100	730	519	GCK1	7401	730				
470	SX85	4167	730	520	GSP	7472	730				
471	SX86	4234	730	521	GSP	7528	730				
472	SX87	4301	730	522	FR	7599	730				
473	SX88	4368	730	523	FR	7655	730				
474	SX89	4435	730	524	BATOUT	7726	730				
475	SX90	4502	730	525	BATOUT	7782	730				
476	SX91	4569	730								
477	SX92	4636	730								
478	SX93	4703	730								
479	SX94	4770	730								
480	SX95	4837	730								
481	SX96	4904	730								
482	SX97	4971	730								
483	SX98	5038	730								
484	SX99	5105	730								
485	SX100	5172	730								
486	SX101	5239	730								
487	SX102	5306	730								
488	SX103	5373	730								
489	SX104	5440	730								
490	SX105	5507	730								
491	SX106	5574	730								
492	SX107	5641	730								
493	SX108	5708	730								
494	SX109	5775	730								
495	SX110	5842	730								
496	SX111	5909	730								
497	SX112	5976	730						Align mark center coordinates		
498	SX113	6043	730						Left top	-7934	695.5
499	SX114	6110	730						Right top	7934	695.5
500	SX115	6177	730								

** The dummy port is opened electrically.*

6. PADS and Functions

No.	Items	Name	I/O	Description	Power
1	Host related ports	BWS1	I	BUS width select.	VDDIO
2		BWS0	I	BUS width select.	
3		PSX	I	Use this pin connected to "L"level.	
4		C86	I	I/F select. (L: I80 system CPU mode, H : setting forbidden)	
5		CMDS	I	RS function select (L: Display RAM/Address Data, H: Address Data)	
6		MSBSEL	I	Parallel BUS MSB bit setting (L: DB17=MSB, DB0=LSB, H: DB0=MSB, DB17=LSB)	
7		RS	I	Display RAM/ Address Data select (Address/Data selection)	
8		CSBSCS	I	CPU BUS chip select	
9		RDB	I	Read (Enable)	
10		WRBSCLK	I	CPU BUS write signal	
11		DB17	I/O	Data BUS	
12		DB16			
13		DB15			
14		DB14			
15		DB13			
16		DB12			
17		DB11			
18		DB10			
19		DB9			
20		DB8			
21		DB7			
22		DB6			
23		DB5			
24		DB4			
25		DB3			
26		DB2			
27		DB1			
28		DB0			
29		SCLEG1	I	Tie to "L"level or “H”level.	
30		SCLEG0	I	Tie to "L"level or “H”level.	
31		SDIN+	-	Tie to GNDDC.	VDDC
32		SDIN-	-	Tie to GNDDC.	
33		STRB+	-	Use this pin open.	
34		STRB-	-	Use this pin open.	
35		MDDISEL	I	Tie to "L"level.	VDDIO
36	System related	RESB	I	System reset Reset is needed whenever recover from standby mode	VDDIO
37		BATIN	I	LCD control input pin (unused: Tie to “ H ” Level)	
38		EXCLK	I	Clock input （unused : Tie to H or L)	
39		CLKSEL	I	Input clock select(L: internal CR oscillator/ H:EXCLK)	
40	Display control related	VSYNC	I	External VSYNC (Enable/Disable is disignated by register) Unused: Tie to H or L	
41		VSYNCO	O	Output port for internal VSYNC signal (active H).	

No.	Items	Name	I/O	Description	Power
42	Panel control related	BATOUT	O	LCD control output signal	VRIN
43		FR		Timing signal of VCOM	
44		GSP		Gate control signal (Gate start pulse)	
45		GCK1,2		Gate control signal(Gate clock)s , 2 ports	
46		GOE		Gate control signal(Gate output enable signal)	
47		GUD		Gate control signal(Gate Scan direction UP or DOWN)	
48		INIT		LCD panel initialize	
49		ASW[1:6]		Source driver selection signals for panel, 6 ports	
50		DCON1		Control signal for internal power of panel (charge)	
51		DCON2		Control signal for internal power of panel (discharge)	
52		RCK1		Control signal for internal power circuitry of panel (booster clock and etc)	
53		RCK2			
54		DCK			
55		DCKB			
56	Source outputs	SX[1:120]	O	Output of source driver	VSIN
57	Dummy	ECK	O	Dummy Pin. (recommend : OPEN)	VDDIO
58		ECS	O	Dummy Pin. (recommend : OPEN)	
59		EDO	O	Dummy Pin. (recommend : OPEN)	
60		EDI	I	Dummy Pin. (Tie to “L” Level)	
61	Power related	VDDCORE	Power	Power for digital : 1.7~1.9V	-
62		VDDIO	Power	Power for IO: 1.6V~3.4V	-
63		VDDC	Power	Analog power: 2.7V~3.4V	-
64		V18OUT	Power	Internal 1.8V regulator output	VDDC
65		SELCORE	Power	Digital 1.8V select. （L:external input, H: internal 1.8V regulator）	VDDIO
66		GNDD	Power	Digital GND	-
67		GNDA	Power	Analog GND	-
68		GNDDC	Power	Booster GND	-
69		VPP	Power	Power for internal OTP when write in.(Except for write in, keep this pin open).	-
70	COM related	VCOMH	Power	Output port for VCOMH (3~5V)	VRIN
71		COM	Power	Common AC output port	VCOMH
72		VCOML	Power	VCOML regulator output (0.2~3.2V)	VRIN
73	DCDC related	VROUT	Power	Booster output port for panel and panel control circuits (4.7~5.4V)	VDDC
74		VRIN	Power	VR input port	-
75		C1+	Power	Capacitor + port for generation VR	-
76		C1-	Power	Capacitor - port for generation VR	-
77		C2+	Power	Capacitor + port for generation VR	-
78		C2-	Power	Capacitor - port for generation VR	-
79		VSOUT	Power	Booster output port for gamma and source block (4.7~ 5.4V)	VDDC
80		VSIN	Power	VS input port	-
81		C3+	Power	Capacitor + port for generation VS	-
82		C3-	Power	Capacitor - port for generation VS	-
83		C4+	Power	Capacitor + port for generation VS	-
84		C4-	Power	Capacitor - port for generation VS	-
85	Regulator related	VGM	Power	Regulator output of gamma (4.6~5.3V)	VSIN
86		VSRF	Power	Regulator output of source (spare circuit)	VSIN
87		VREF	Power	Reference output ports	VDDC
88	TEST	TEST		Test pin (OPEN or L)	VDDIO

7. CPU Interface

7. 1 General description

CPU control LCD by accessing register and display RAM. Interface for accessing is parallel interface. This IC supports the two access methods of parallel interface by the treatment of RS port.

- BUS width, Bit length is selectable.
  Parallel I/F BUS widths are selectable from 18, 16, 9, 8 bit.
- Register values and display RAM data are able to Read / Write.
- This IC supports I80 system CPU.

7.2 I / O Port

The explanations of the ports related CPU I / F.

Table 7.1 : CPU interface ports Table.

Port symbol	Port Name	I/O	explanation
BWS[1:0]	BUS width select	I	BUS width select
RSX	Mode select	I	H : Setting forbidden.
			L : Use this pin fix to L.
C86	Interface mode	I	H : Setting forbidden.
			L : I80 system CPU interface
RS	Data / Register select	I	Data, Register
CSB	Chip select	I	Chip select
RDB	Read	I	Read clock
WRBSCLK	Write	I	Write clock
DB[17:0]	Data BUS	I/O	Data BUS
SCLEG [1:0]	Unused input pin	I	This input pin can not be use. Use this pin keep “ L ” or “ H ” .
CMDS	RS function select	I	H : Address data

7.3 Register list related CPU interface

Explanation of Internal register related CPU interface.

Table 7.2 Register list of CPU interface.

ADR	Bit	Symbol	Description	Reflection	Default
01H	D2	BTSEL	This register set six-bit 3-times Data transfer using by DB[5:0] or DB[7:2].	AO	00H
	D1	DTX2	This register select the transfer method of 1pixel Data number.(Refer to Table 7.7 Transfer method).		
	D0	DTX1			
02H	D0	RREN	This register select the read operation in CMDS=0(RS function : Display RAM/Command/Data). <RREN=0> Write operation <RREN=1> Read operation At RREN=1, only this register can be write operation.	AO	00H
03H	-	RAMDT	Effectively at only CMDS=1. This function effective by accessing this address and Data has no mean. (RS function : In Index/ Data, read / write display RAM data).	AO	00H

7.4 Function/Operation

7.4.1 Select BUS-width / Bit-length

The pins related BUS-selection, BUS-width and BUS-length are PSX, BSW[1:0] and CMDS.

- The BUS-width of parallel I/F can be select 18,16, 9 and 8 bit.
- The BUS-width can be select by BSW0 and BSW1.
- Please use by PSX pin fix “L”.
- Notice of changing pin state in operation.
  In case of switching CMDS, BWS0, BWS1 and C86, do not CPU access.
  The operation is not guaranteed.

Table 7.3 BUS-width select of CPU interface

PSX	BWS0	BWS1	CMDS	Mode	CSB	RS	RDB	WRB	C86	DB[17:16]	DB[15:9]	DB[8]	DB[7:0]
L	L	L	X	18bit parallel	CSB	RS	RDB	WRB	C86	DB[17:0]			
	L	H		16bit parallel	CSB	RS	RDB	WRB	C86	Hi-Z	DB[15:0]		
	H	L		9bit parallel	CSB	RS	RDB	WRB	C86	Hi-Z	Hi-Z	DB[8:0]	
	H	H		8bit parallel	CSB	RS	RDB	WRB	C86	Hi-Z	Hi-Z	Hi-Z	DB[7:0]

X : Don’t care
Hi-Z : High impedance

7.4.2 RS port function

Explanation the kind of access by setting RS port.
The contents of access by setting RS port are change by each CMDS setting.

Table7.4 RS function table

PSX	CMDS	RS Function	
L	L	H	Access to display RAM
		L	Access to Index(*1) and its Register.
	H	H	Access to display RAM or Register (*3)
		L	Access to Index(Register) (*2) (*3)

(*1) Index indicate Register's address.
In this spec, borth word of Index and address can be use by circumstances of the expression, the meaning of these words indicate same in all.

(*2) When you access to Index 02_H、03_H, you can appoint the contents of the next data.02_H indicate register value、03_H indicate display RAM data (register function)

(*3) The access to display RAM can be permit after accessing to RAMDT in Index 03_H.

7.4.3 CPU parallel I/F mode

This LSI support I80 system CPU.

C86=L : I80 system CPU mode. C86=H : Do not use in this condition.

Table 7.5 Explanation of C86pin setting

C86	Mode	RDB(E)	WPB (RWB)	BWS0	BWS1	DB[17:16]	DB[15:9]	DB[8]	DB[7:0]
L	I80 - system CPU	RDB	WRB	L	L	DB[17:0]			
				L	H	Hi-Z	DB[15:0]		
				H	L	Hi-Z	Hi-Z	DB[8:0]	
				H	H	Hi-Z	Hi-Z	Hi-Z	DB[7:0]

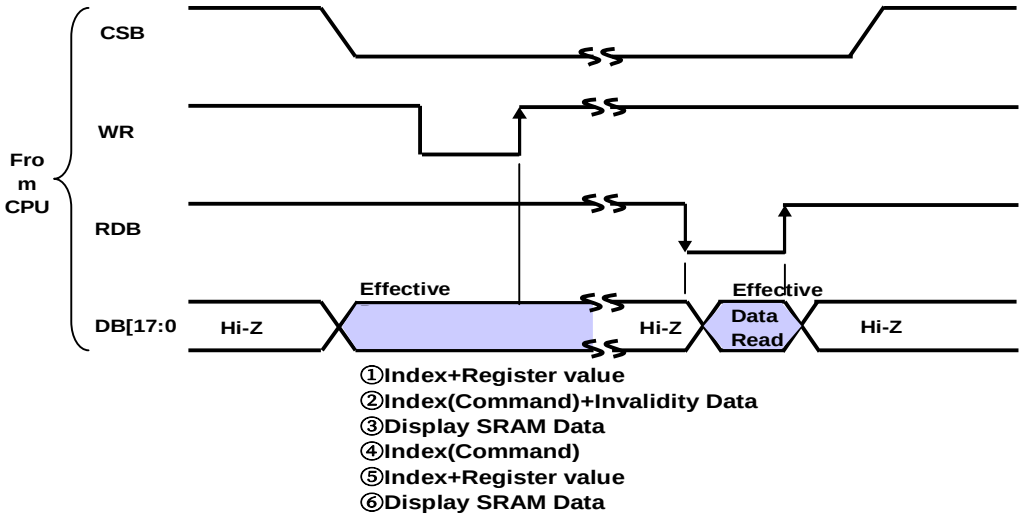
I80-system CPU can read / write operation in following Table.

Table 7.6 I80-system CPU Read / Write operation.

I80-system CPU		Function
RDB	WRB	
L	H	Read operation
H	L	Write operation

• **I80-system parallel I/F**

At the time of parallel data transfer select, the data write to this device on rising time of WRB signal. The timing between BUS and the rise position of WRB clock is refer to AC timing. The data output to data BUS during RDB signal is Low.



Because content is different, please refer to an access method and the content by a case from case ① to ⑥.

7.4.4 Data writing to display RAM

- The data bit number of 1 pixel are 8, 9, 12, 16, 18bit. And data transfer mode are 3 kinds of 1-time, 2-times, 3-times.
- Data transfer number of 1 pixel can be select using register DTX1,DTX2.
- Regarding to Data format, please refer to " Write data format (CPU→Display RAM)".

PSX	BWS0	BWS1	CMDS	Mode	DTX1	DTX2	Data number of 1pixel	Data transfer method of 1pixel
L	L	L	L	18 bit parallel	X	X	18 bit	18 bit 1time transfer
	L	H		16 bit parallel	X	L	18 bit	16 bit+2 bit 2times transfer
						H	16 bit	16 bit 1time transfer
	H	L		9bit parallel	L	L	18 bit	9 bit +9 bit 2times transfer
					L	H	16 bit	8 bit +8 bit 2times transfer
					H	L	12 bit	8 bit +4 bit 2times transfer
					H	H	9 bit	9bit 1time transfer
	H	H		8bit parallel	L	L	18 bit	6 bit+6 bit +6 bit 3times transfer (*1)
					L	H	16 bit	8 bit +8 bit 2 times transfer
					H	L	12 bit	8 bit +4 bit 2 times transfer
					H	H	8 bit	8 bit 1time transfer
	L	L	H	18 bit parallel	L	L	18 bit	18 bit 1times transfer
					L	H	16 bit	8 bit +8 bit 2times transfer
					H	L	18 bit	16 bit +2 bit 2 times transfer
					H	H	16 bit	16 bit 1time transfer
	L	H		16 bit parallel	L	L	18 bit	16 bit +2 bit 2 times transfer
					L	H	16 bit	16 bit 1 time transfer
					H	L	18 bit	6 bit +6 bit +6 bit 3times transfer (*1)
					H	H	16 bit	8 bit + 8 bit 2 times transfer
	H	L		9bit parallel	L	L	18 bit	9 bit +9 bit 2 times transfer
					L	H	16 bit	8 bit + 8 bit 2 times transfer
					H	L	12 bit	8 bit +4 bit 2 times transfer
					H	H	9 bit	9bit 1time transfer
	H	H		8bit parallel	L	L	18 bit	6 bit +6 bit +6 bit 3times transfer
					L	H	16 bit	8 bit + 8 bit 2 times transfer
					H	L	12 bit	8 bit +4 bit 2 times transfer
					H	H	8 bit	8 bit 1time transfer

(*1) In register (BITSEL) setting is "L", 3 times Data transfer case is used by DB[5:0] (Low side BUS).
And in register (BITSEL) setting is "H", 3 times Data transfer case is used by DB[7:2] (Upper side BUS).

7.4.5 Read out data from display RAM.

In read operation, RAM data (1pixel 18 bits) can read out .
(The data supplemented by write operation read out too.)

- On 18 bit parallel mode, 18bit RAM Data is read out by 1 time CPU access.

  But, when on 18 bit parallel mode, CMDS=H and DTX1=1, 18 bit RAM Data is read out by 2 times CPU access. (16bit +2bit).

  And, when on 18 bit parallel mode,CMDS=H,DTX1=L and DTX2=H, 18bit RAM Data is read out by 3 times CPU access. (6 bit +6 bit +6 bit).

- On 16 bit parallel mode, 18 bit RAM Data is read out by 2 time CPU access. (16bit + 2bit).

  But, when on 18bit parallel mode,CMDS=H and DTX1=H, 18 bit RAM Data is read out by 3 times CPU access. (6 bit +6 bit+ 6 bit).

- On 9 bit parallel mode, 18 bit RAM data is read out by 2 times. (9 bit+ 9Bit)

- On 8 bit parallel mode, 18 bit RAM Data is read out by

  Regarding to Data format, refer to Read Data format. (Display RAM->CPU).

PSX	BWS0	BWS1	CMDS	Mode	DTX1	DTX2	RAM Data read out method	
L	L	L	L	18 bit parallel	X	X	18 bit	1 time Read out
	L	H		16 bit parallel	X	X	16 bit +2 bit	2 times Read out
	H	L		9 bit parallel	X	X	9 bit+ 9 bit	2 times Read out
	H	H		8 bit parallel	X	X	6 bit+ 6 bit+ 6bit	3 times Read out (*2)
	L	L	H	18 bit parallel	L	L	18 bit	1 time Read out
					L	H	6 bit+ 6 bit+ 6bit	3 times Read out (*2)
					H	X	16 bit +2 bit	2 times Read out
	L	H		16 bit parallel	L	X	16 bit +2 bit	2 times Read out
					H	X	6 bit+ 6 bit+ 6bit	3 times Read out (*2)
	H	L		9 bit parallel	X	X	9 bit+ 9 bit	2 times Read out
	H	H		8 bit parallel	X	X	6 bit+ 6 bit+ 6bit	3 times Read out (*2)

(*2) Register, BTSEL= L and RAM data perform the reading of three times from RAM data at 6 bits with DB[5:0](bottom 6 bits). In addition, register, BTSEL=H perform the reading of RAM data of three times of 6 bits using DB[7:2](upper part 6 bits).

7.4.6 Data Format

7.4.6.1 Write data format (CPU→Display RAM)

Table7.9 18 bit Parallel I/F (18 bit 1 time transfer)

CPU BUS data																	
1st 18bit																	
DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
RAM data																	
D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
RDATA						GDATA						BDATA					
1 Pixel																	

Table 7.10 18 bit Parallel I/F (CMDS=H,DTX1=H,DTX2=L) (16bit+2bit 2 times transfer)

CPU BUS data																	
1st 16bit																2nd 2bit	
DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	DB1	DB0
RAM data																	
D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
RDATA						GDATA						BDATA					
1 Pixel																	

Table 7.11 18 bit Parallel I/F (CMDS=H,DTX1=H, DTX2=H) (16 bit 1 time transfer)

CPU BUS data																	
1st 16bit																	
DB15	DB14	DB13	DB12	DB11	-	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	-
RAM data																	
D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
RDATA						GDATA						BDATA					
1 Pixel																	

※ Display RAM data D12,D0 are supplement from CPU BUS data DB15,DB4.

Table 7 12 18 bit Parallel I/F (CMDS=H, DTX1=L, DTX2=H) (8 bit+ 8Bit 2 times transfer)

CPU BUS data																	
1st 8bit									2nd 8bit								
DB7	DB6	DB5	DB4	DB3	-	DB2	DB1	DB0	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	-
RAM data																	
D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
RDATA						GDATA						BDATA					
1 Pixel																	

※ Display RAM data D12,D0 are supplement from CPU BUS data DB7 transferred at 1st time, DB4 transferred at 2nd time.

Table7.13 16 bit Parallel I/F (16 bit+2 bit 2 times transfer)

CPU BUS data																	
1st 16bit																2nd 2bit	
DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	DB1	DB0
RAM data																	
D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
RDATA						GDATA						BDATA					
1 Pixel																	

Table 7.14 16 bit Parallel I/F (16 bit 1 time transfer)

CPU BUS data																	
1st 16bit																	
DB15	DB14	DB13	DB12	DB11	-	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	-
RAM data																	
D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
RDATA						GDATA						BDATA					
1 Pixel																	

※Display RAM data D12,D0 are supplement from CPU BUS data DB15,DB4

Table 7.15 16 bit Parallel I/F(CMDS=H,DTX1=H, DTX2=L) (6bit+6bit+6bit 3times transfer) (BTSEL=L)

CPU BUS data																	
1st 6bit						2nd 6bit						3rd 6bit					
DB5	DB4	DB3	DB2	DB1	DB0	DB5	DB4	DB3	DB2	DB1	DB0	DB5	DB4	DB3	DB2	DB1	DB0
RAM data																	
D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
RDATA						GDATA						BDATA					
1 Pixel																	

Table 7.16 16 bit Parallel I/F(CMDS=H, DTX1=H, DTX2=L) (6bit+6bit+6bit 3times transfer) (BTSEL=H)

CPU BUS data																	
1st 6bit						2nd 6bit						3rd 6bit					
DB7	DB6	DB5	DB4	DB3	DB2	DB7	DB6	DB5	DB4	DB3	DB2	DB7	DB6	DB5	DB4	DB3	DB2
RAM data																	
D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
RDATA						GDATA						BDATA					
1 Pixel																	

Table 7.17 16 bit Parallel I/F(CMDS=H, DTX1=H, DTX2=H) (8bit+8bit 2 times transfer)

CPU BUS data																	
1st 8bit									2nd 8bit								
DB7	DB6	DB5	DB4	DB3	-	DB2	DB1	DB0	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	-
RAM data																	
D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
RDATA						GDATA						BDATA					
1 Pixel																	

※Display RAM data D12,D0 are supplement from CPU BUS data DB7 transferred at 1st time, DB4 transferred at 2nd time.

Table 7.18 9 bit Parallel I/F(9bit+9bit 2times transfer)

CPU BUS data																	
1st 9bit									2nd 9bit								
DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
RAM data																	
D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
RDATA						GDATA						BDATA					
1 Pixel																	

Table7.19 9 bit Parallel I/F(8bit+4bit 2times transfer)

CPU BUS data																	
1st 8bit									2nd 8bit								
DB7	DB6	DB5	DB4	DB3	-	DB2	DB1	DB0	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	-
RAM data																	
D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
RDATA						GDATA						BDATA					
1 Pixel																	

※Display RAM data D12,D0 are supplement from CPU BUS data DB7 transferred at 1st time, DB4 transferred at 2nd time.

Table7.20 9bit Parallel I/F (8bit+4bit 2times transfer)

CPU BUS data																	
1st 8bit												2nd 4bit					
DB7	DB6	DB5	DB4	-	-	DB3	DB2	DB1	DB0	-	-	DB3	DB2	DB1	DB0	-	-
RAM data																	
D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
RDATA						GDATA						BDATA					
1 Pixel																	

※Display RAM data D[13:12],D[7:6], D[1:0] are supplement from CPU BUS data DB[7:6] , DB[3:2] transferred at 1st time, DB[3:2] transferred at 2nd time.

Table7.21 9bit Parallel I/F (9 bit 1 time transfer)

CPU BUS data																	
1st 9bit																	
DB8	DB7	DB6	-	-	-	DB5	DB4	DB3	-	-	-	DB2	DB1	DB0	-	-	-
RAM data																	
D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
RDATA						GDATA						BDATA					
1 Pixel																	

※Display RAM data D[14:12],D[8:6], D[2:0] are supplement from CPU BUS data DB[8:0] .

Table7.22 8 bit Parallel I/F(6bit+6bit+6bit 3times transfer) (BTSEL=L)

CPU BUS data																	
1st 6bit						2nd 6bit						3rd 6bit					
DB5	DB4	DB3	DB2	DB1	DB0	DB5	DB4	DB3	DB2	DB1	DB0	DB5	DB4	DB3	DB2	DB1	DB0
RAM data																	
D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
RDATA						GDATA						BDATA					
1 Pixel																	

Table7.23 8bit Parallel I/F (6bit+ 6bit+6bit 3times transfer) (BTSEL=H)

CPU BUS data																	
1st 6bit						2nd 6bit						3rd 6bit					
DB7	DB6	DB5	DB4	DB3	DB2	DB7	DB6	DB5	DB4	DB3	DB2	DB7	DB6	DB5	DB4	DB3	DB2
RAM data																	
D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
RDATA						GDATA						BDATA					
1 Pixel																	

Table7.24 8bit Parallel I/F (8bit+8bit 2times transfer)

CPU BUS data																	
1st 8bit									2nd 8bit								
DB7	DB6	DB5	DB4	DB3	-	DB2	DB1	DB0	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	-
RAM data																	
D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
RDATA						GDATA						BDATA					
1 Pixel																	

Table7.25 8bit Parallel I/F (8 bit+4bit 2times transfer)

CPU BUS data																	
1st 8bit												2nd 4bit					
DB7	DB6	DB5	DB4	-	-	DB3	DB2	DB1	DB0	-	-	DB3	DB2	DB1	DB0	-	-
RAM data																	
D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
RDATA						GDATA						BDATA					
1 Pixel																	

※Display RAM data D[13:12],D[7:6], D[1:0] are supplement from CPU BUS data DB[7:6] , DB[3:2] transferred at 1st time, DB[3:2] transferred at 2nd time.

Table7.26 8bit Parallel I/F (8bit 1time transfer)

CPU BUS data																	
1st 8bit																	
DB7	DB6	DB5	-	-	-	DB4	DB3	DB2	-	-	-	DB1	DB0	-	-	-	-
RAM data																	
D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
RDATA						GDATA						BDATA					
1 Pixel																	

※Display RAM data D[14:12],D[8:6], D[3:0] are supplement from CPU BUS data DB[7:0] .

7.4.6.2 Read data format (Display RAM→CPU)

Table7.27 18bit Parallel I/F (18bit 1time transfer)

RAM data																	
1 Pixel																	
RDATA						GDATA						BDATA					
D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
CPU BUS data																	
1st 18bit																	
DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0

Table7.28 18bit Parallel I/F (CMDS=H,DTX1=H) (16bit+2bit 2 times transfer)

RAM data																	
1 Pixel																	
RDATA						GDATA						BDATA					
D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
CPU BUS data																	
1st 16bit																2nd 2bit	
DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	DB1	DB0

Table7.29 18bit Parallel I/F (CMDS=H,DTX1=L, DTX2=H) (6bit+6bit+6bit 3 times transfer) (BTSEL=L)

RAM data																	
1 Pixel																	
RDATA						GDATA						BDATA					
D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
CPU BUS data																	
1st 6bit						2nd 6bit						3rd 6bit					
DB5	DB4	DB3	DB2	DB1	DB0	DB5	DB4	DB3	DB2	DB1	DB0	DB5	DB4	DB3	DB2	DB1	DB0

Table7.30 18bit Parallel I/F (CMDS=H,DTX1=L, DTX2=H) (6bit+6bit+6bit 3 times transfer) (BTSEL=H)

RAM data																	
1 Pixel																	
RDATA						GDATA						BDATA					
D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
CPU BUS data																	
1st 6bit						2nd 6bit						3rd 6bit					
DB7	DB6	DB5	DB4	DB3	DB2	DB7	DB6	DB5	DB4	DB3	DB2	DB7	DB6	DB5	DB4	DB3	DB2

Table7.31 16bit Parall I/F (16bit+2bit 2 times transfer)

RAM data																	
1 Pixel																	
RDATA						GDATA						BDATA					
D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
CPU BUS data																	
1st 16bit																1st 2bit	
DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	DB1	DB0

Table7.32 16bit Parallel I/F (CMDS=H, DTX1=H) (6bit+6bit+6bit 3 times transfer) (BTSEL=L)

RAM data																	
1 Pixel																	
RDATA						GDATA						BDATA					
D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
CPU BUS data																	
1st 6bit						2nd 6bit						3rd 6bit					
DB5	DB4	DB3	DB2	DB1	DB0	DB5	DB4	DB3	DB2	DB1	DB0	DB5	DB4	DB3	DB2	DB1	DB0

Table7.33 16bit Parallel I/F(CMDS=H,DTX1=H) (6bit+6bit+6bit 3 times transfer) (BTSEL=H)

RAM data																	
1 Pixel																	
RDATA						GDATA						BDATA					
D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
CPU BUS data																	
1st 6bit						2nd 6bit						3rd 6bit					
DB7	DB6	DB5	DB4	DB3	DB2	DB7	DB6	DB5	DB4	DB3	DB2	DB7	DB6	DB5	DB4	DB3	DB2

Table7.34 9bit Parallel I/F(9bit+9bit 2 times transfer)

RAM data																	
1 Pixel																	
RDATA						GDATA						BDATA					
D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
CPU BUS data																	
1st 9bit									1st 9bit								
DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0

Table7.35 8bit Parallel I/F (6bit+6bit+6bit 3times transfer) (BTSEL=L)

RAM data																	
1 Pixel																	
RDATA						GDATA						BDATA					
D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
CPU BUS data																	
1st 6bit						2nd 6bit						3rd 6bit					
DB5	DB4	DB3	DB2	DB1	DB0	DB5	DB4	DB3	DB2	DB1	DB0	DB5	DB4	DB3	DB2	DB1	DB0

Table7.36 8bit Parallel I/F (6bit+6bit+6bit 3times transfer) (BTSEL=H)

RAM data																	
1 Pixel																	
RDATA						GDATA						BDATA					
D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
CPU BUS data																	
1st 6bit						2nd 6bit						3rd 6bit					
DB7	DB6	DB5	DB4	DB3	DB2	DB7	DB6	DB5	DB4	DB3	DB2	DB7	DB6	DB5	DB4	DB3	DB2

7.4.7 Access Sequence

7.4.7.1. Parallel I/F (PSX=L)

7.4.7.1.1 Function of RS(Display RAM／Register value) and contents of access (CMDS=L)

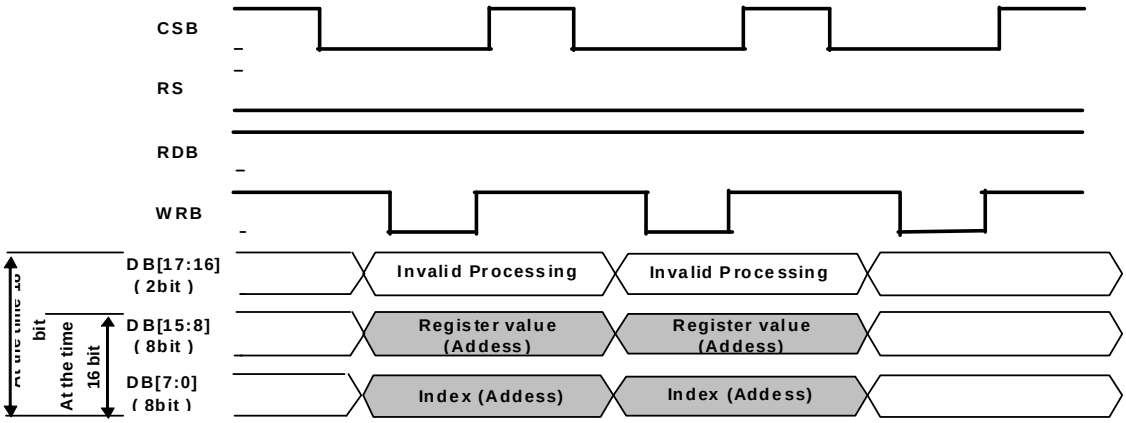
At the setting port CMDS=L, function of RS port is setting that data on CPU BUS access to register or display RAM.

1)Access of Register

16/18bit Parallel I/F

・Write operation (at the time register RREN=L)

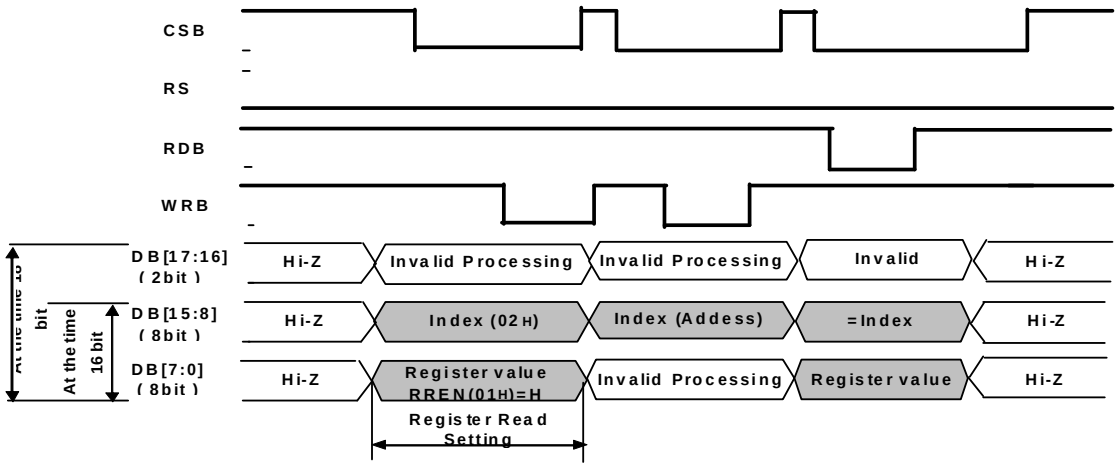
Data of DB[17:16] is invalid processing, data of DB[15:8] is Index(register address), data of DB[7:0] is register value. As below chart, Register (Include Index)can be write by 1 time access of CPU.



At the time of writing, please make CSB "H" between WRB and next WRG by all means. In IC, Data is written in synchronize at CSB.

・Read operation (Only available read at the time of register RREN=H)

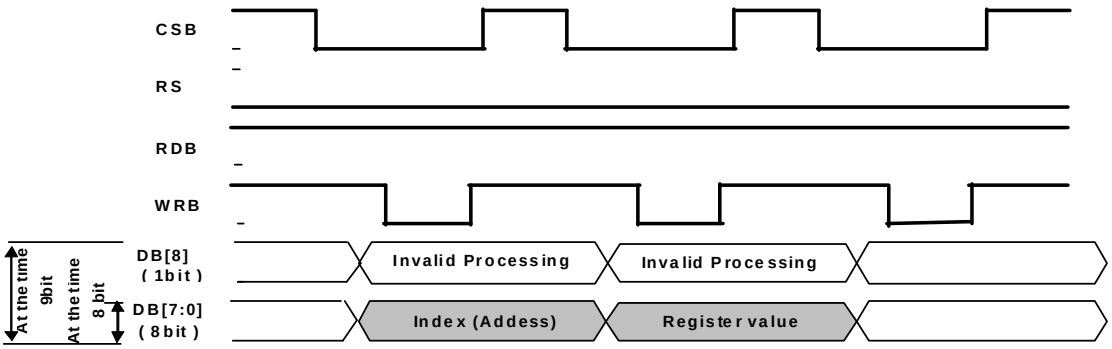
DB[15:8] is Index, DB[7:0] is register value.
After setting register RREN=H, at 1st time write Index, read operation after this write operation read out register value correspond 1st Index..



9/8bit Parallel I/F

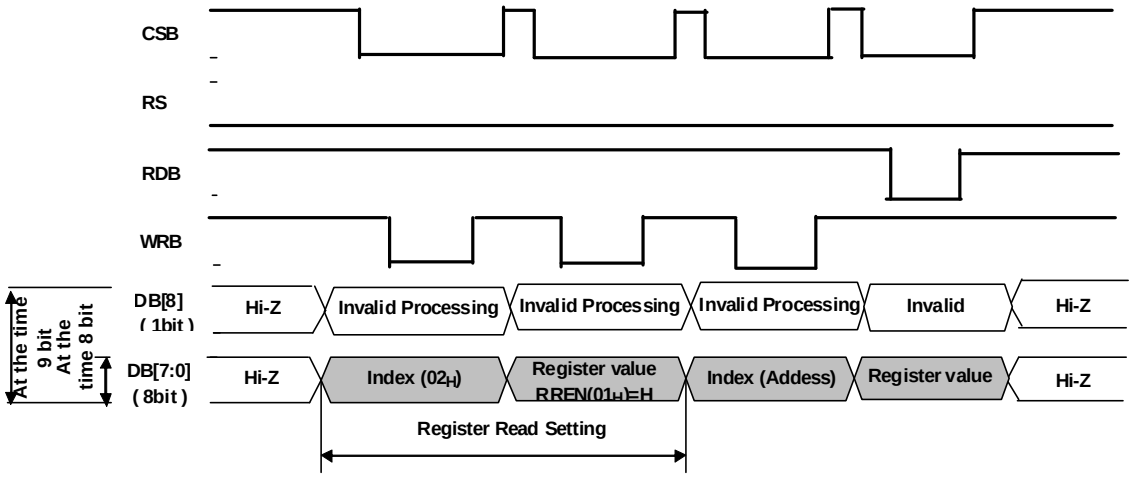
・write operation

At the time of operation setting Register RREN=L.
Index/Register value write by DB[7:0], data of DB[8] is invalid processing.
At the time of 1st write operation, write Index (Register address) and at the time of 2nd write operation, write register value corresponding 1st Index.



・Read operation (Readable only RREN=H)

DB[7:0] are Index and its register value, and DB[8]is invalid data.
After setting Index and register for RREN(RREN=H),write Index at 1st write operation and read out register value corresponding 1st write Index.



※ In the case of write operation after read operation, return RREN from H to L.
This value is not return automatically.

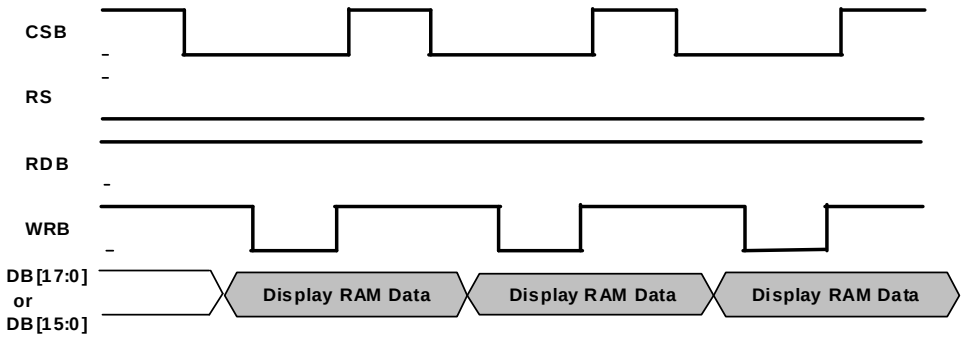
※At the time register RREN=H, writable register is only RREN.

2) Access to Display RAM

- At the time of RS=H, access to display RAM can be done.
  (03_H : RAM access can be done without Register RAMDT.)
- At the write operation, 1 pixel access can be done by select transfer times.
- At the read operation, RAM data can be read (1 pixel 18bit).

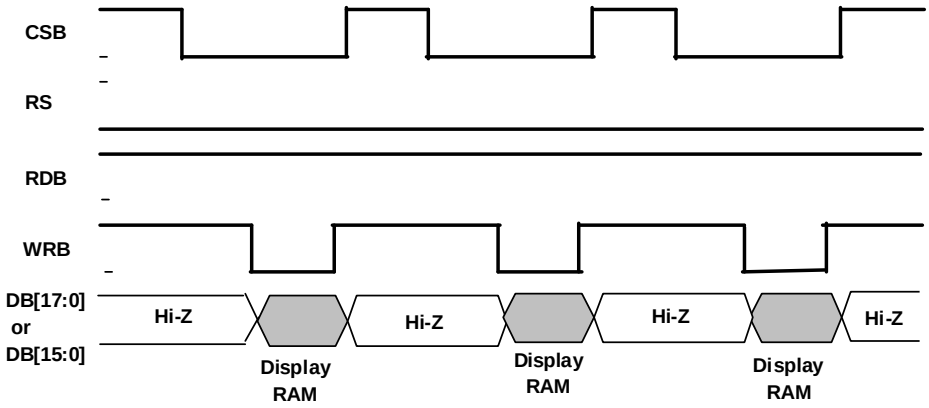
16/18bit Parallel I/F

- Write operation



At the time of 2 times transfer, register value of XA[7:0] and YA[8:0] are not change in continues writing to display RAM, and only inside counter value change(same to read out counter)(Auto increment). In the case of writing to specific address, write in Window mode or write after setting XA[7:0] and YA[8:0].

- Read operation



In the case of continues read access to display RAM, the value of XA[7:0] and YA[8:0] are not change, and only inside counter value change(same to read out counter)(Auto increment).
In the case of reading to specific address, read in Window mode or read after setting XA[7:0] and YA[8:0].

7.4.7.1.2 Function of RS(Index/Display RAM・Register value) and Contents of access (port CMDS=H)

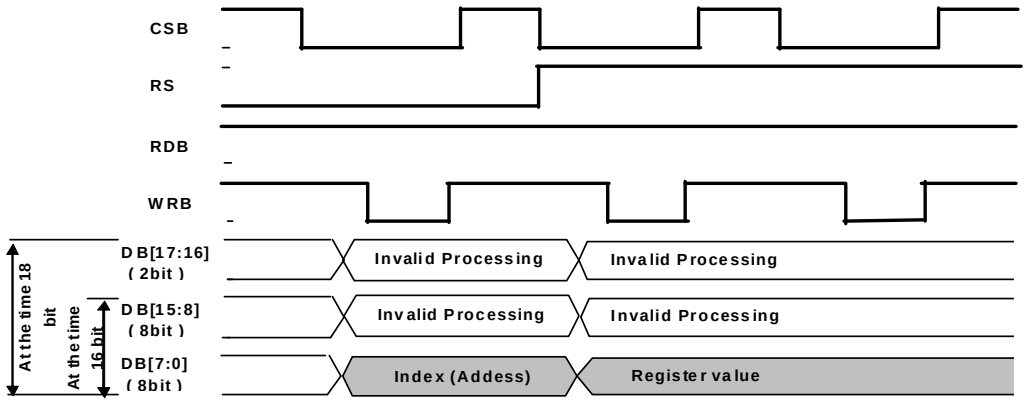
1) Access to Register

16/18bit Parallel I/F

・Write operation

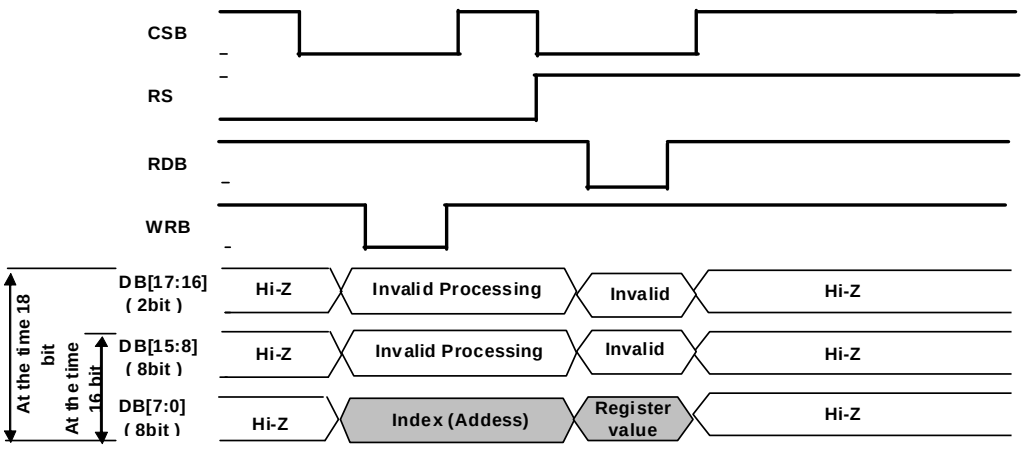
DB[7:0] is Index(Register address) or Register value and, Remaining DB[17(15):8] is invalid processing. At 1st writing, write Index and at next write register value correspond to 1st Index (Address).

(02_H：Access do regardless of register RREN. However, in the case of the designated address of the index is 03H：RAMDT, access is done to SRAM. Refer to “Access to display RAM”



・Read operation

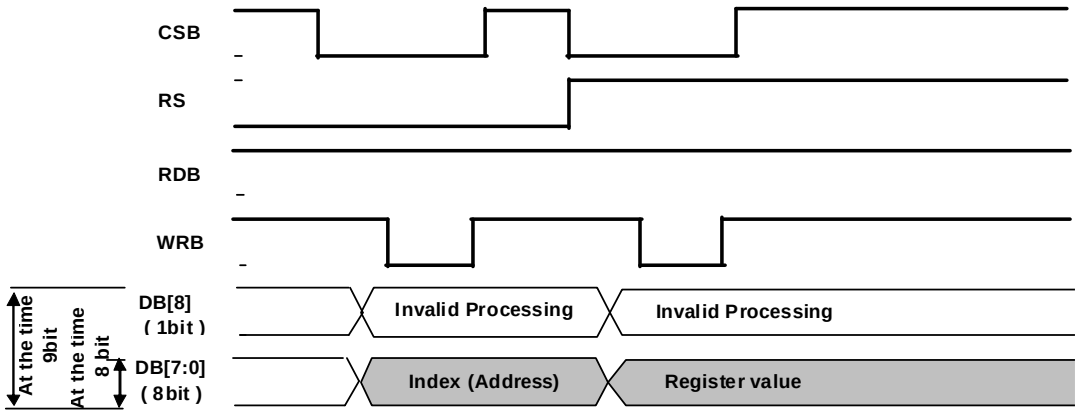
DB[7:0] is Index(Register address) or Register value and, Remaining DB[17(15):8] is invalid processing. At 1st writing, write Index and at next read time, register value correspond to 1st Index (Address) is output. (02_H：Access do regardless of register RREN.)



9/8bit Parallel I/F

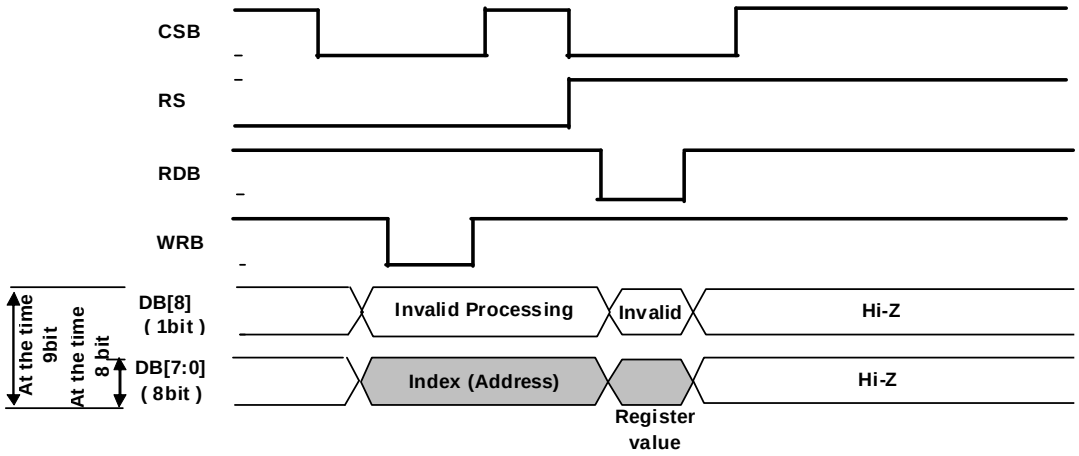
・Write operation

DB[7:0] is Index(Register address) or Register value and, Remaining DB[8] is invalid processing. At 1st writing, write Index and at next write register value correspond to 1st Index (Address). (02_H : Access to register do regardless of register RREN.)



・Read Operation

DB[7:0] is Index(Register address) or Register value and, Remaining DB[8] is invalid processing. At 1st writing, write Index (Address) and at next read time, register value correspond to 1st Index is output. (02_H : Access to register do regardless of register RREN.)

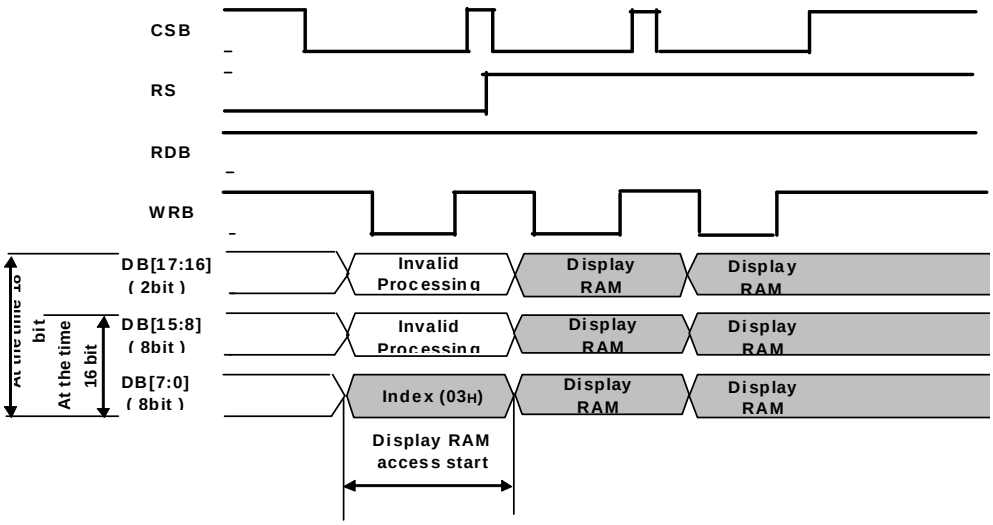


2) Access to display RAM

- By access to register RAMDT, display RAM can be read / write. (Address of display RAM are auto increment.)
- At the write operation, 1 pixel access can be done by select transfer times.
- At the read operation, RAM data can be read (1 pixel 18bit).

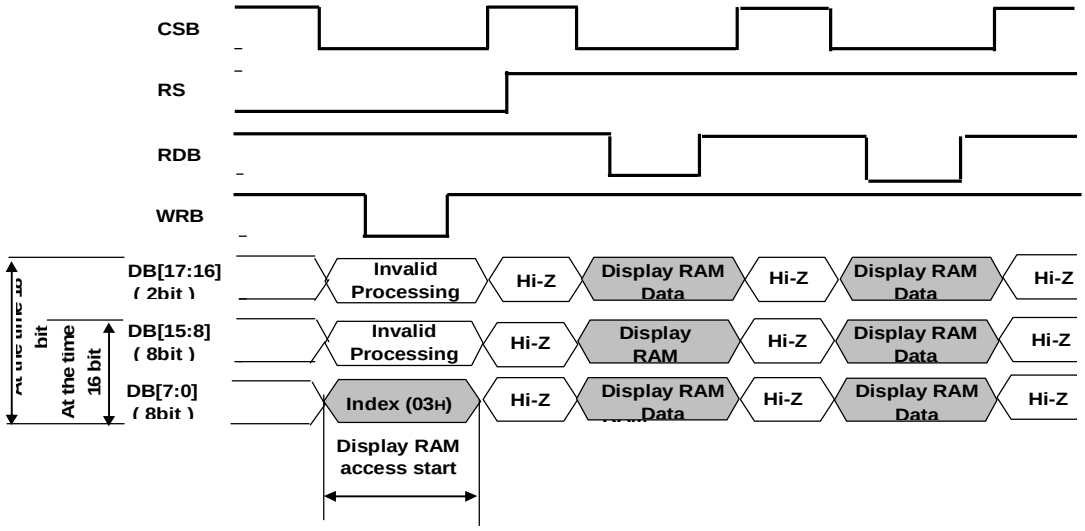
16/18bit Parallel I/F

・Write operation



※Access to Index (03H) means that the next access data become the data of the display RAM, without relations setting register value.
. Write or read operations are determined by only the signal of WRB and RDB.

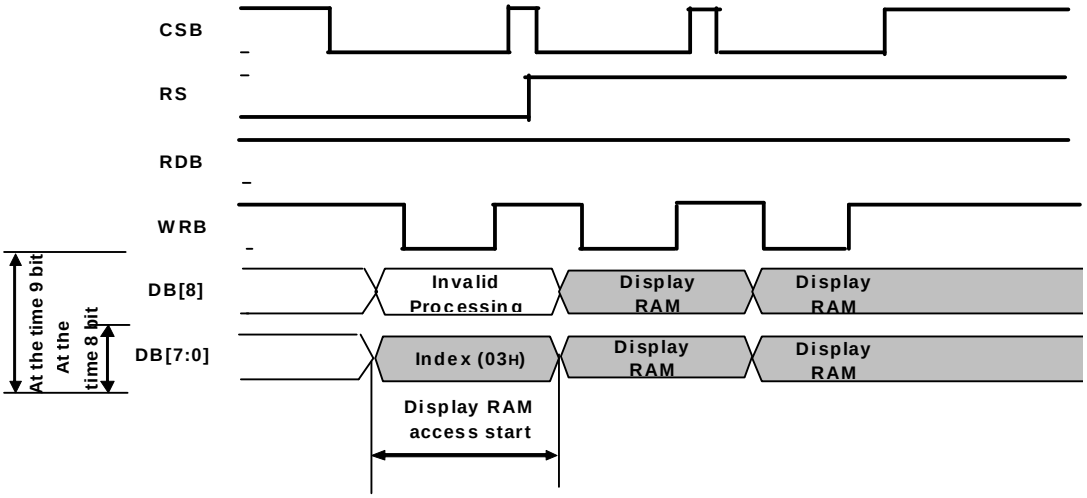
・Read operation



※Access to Index (03H) means that the next access data become the data of the display RAM, without relations setting register value.
Write or read operations are determined by only the signal of WRB and RDB.

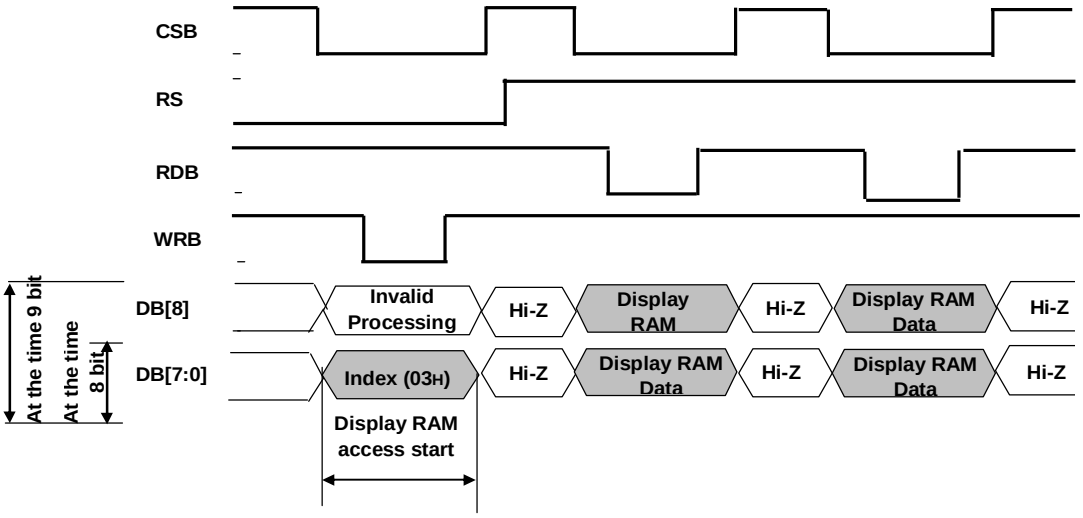
9/8bit Parallel I/F

・Write operation



※Access to Index (03H) means that the next access data become the data of the display RAM, without relations setting register value.
Write or read operations are determined by only the signal of WRB and RDB.

・Read operation



※Access to Index (03H) means that the next access data become the data of the display RAM, without relations setting register value.
Write or read operations are determined by only the signal of WRB and RDB.

8. RAM Access Specification

8.1. Size Setting

8.1.1. Register list

Register Address	Register Name	Description
10H	MPSX[7:0]	This sets the panel size（X direction line numbers）
11H,12H	MPSY[8:0]	This sets the panel size（Y direction line numbers）
13H	WXMIN[7:0]	This sets the drawing window size（X direction origin） in Window access mode
14H,15H	WYMIN[8:0]	This sets the drawing window size（Y direction origin） in Window access mode.
16H	WXMAX[7:0]	This sets the drawing window size（X direction end point） in Window access mode.
17H,18H	WYMAX[8:0]	This sets the drawing window size（Y direction end point） in Window access mode.
19H	WAS	This selects Window access mode. 0：Normal access mode 1：Window access mode

・Panel size (SRAM area) setting constraints

$1 \leqq MPSX \leqq 240$

$320 \leqq MPSY \leqq 432$

※ Exceptional operation
（The operations when the constraints above are not met.）

When setting MPSX = 0 → MPSX = 240.
When setting $241 \leqq MPSX$ → MPSX = 240.

When setting MPSY = 0 → MPSY = 432.
When setting $433 \leqq MPSY$ → MPSY = 432.

・Window access mode setting constraints

$0 \leqq WXMIN \leqq WXMAX \leqq MPSX-1$

$0 \leqq WYMIN \leqq WYMAX \leqq MPSY-1$

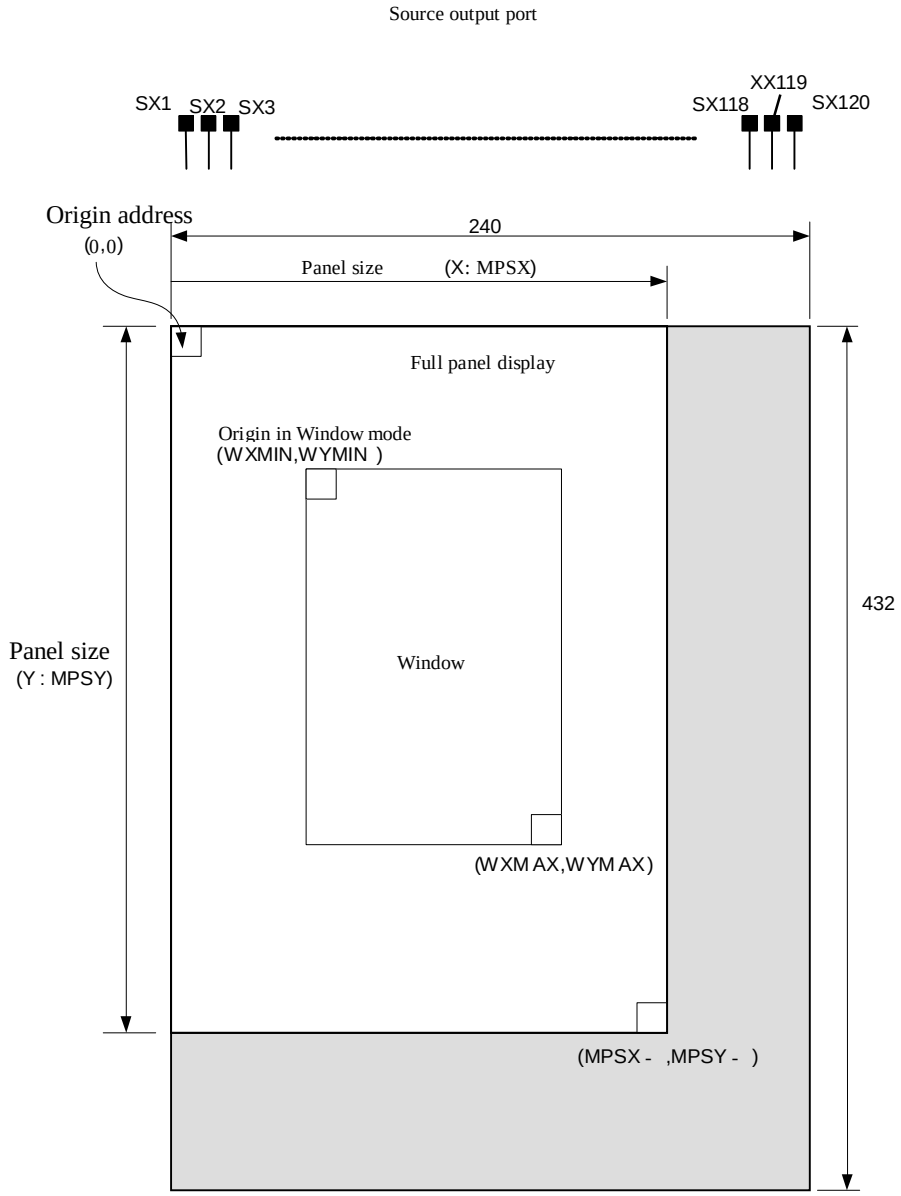
※ If the constraints above are not met, the mode doesn't make the shift to Window access mode.

・RAM Write is written RAM every time 1 pixel is written from the host. The constraints, like 2-pixel each or 8-pixel each, are not set. This is applied to all modes like Window access mode.

・When in RAM Write and RAM Read, the address will be automatically incremented. The address continues to the origin address after the end point address of (Fig.8-1).

・In Window access mode, the same operation will be done within the setting.

(Fig. 8-1) The outline drawing of the register setting related to RAM



※The mode of window access is made enable by the register WAS(index : 19H) setting.

※ Recommended setting order of Window access mode

Setting of MPSX[7:0] and MPSY[8:0]
→ Setting of WXMIN[7:0], MYMIN[8:0], WXMAX[7:0] and WYMAX[8:0]
→ Setting of WAS → (Setting of XA[7:0] and YA[8:0])
→ Acssess of the data

The pointer is moved to the origin of the window when setting the Window mode.

8.1.2. Operation of the pointer

Address	Register Name	Description
1AH	XA[7:0]	Set X-address
1BH,1CH	YA[8:0]	Set Y-address

The pointer can be moved to the arbitrary point of RAM by XA[7:0] and YA[8:0] register settings. And then RAM Write and RAM Read become possible. The pointer of RAM Write and RAM Read is in common.
The address will be automatically incremented from that point after moving the pointer. However the movement will continue to the origin address (Not XA[7:0] and XY[8:0]) when it comes to the end address.

The value set in the previous time can be read when reading XA[7:0] and YA[8:0] register values. Register value is not subordinated by the pointer. The origin point and the end point will be different from Normal Display in Window access mode.

・Setting constraints

Except in Window access mode
$0 \leqq XA \leqq MPSX-1$
$0 \leqq YA \leqq MPSY-1$

In Window access mode
$0 \leqq XA \leqq WXMAX- WXMIN$
$0 \leqq YA \leqq WYMAX- WYMIN$

※If the constraints above are not satisfied, the pointer should be returned to the origin.

・Write(Read)pointer moves only in the following 4 cases.

1. When changing XA[7:0] and YA[8:0] registers,
   → The pointer moves to（XA[7:0] and YA[8:0]）.
2. The pointer moves to the origin when resetting the hardware.
   → The pointer moves to（0,0）.
3. When setting the mode of window (Enable of WAS)
   → The pointer moves to (WXMIN[7:0],WYMIN[8:0]).
4. When accessing to ADX, ADY and index related to INC（address）
   → The pointer moves to the origin.

Register			Normal mode		Window mode	
INC	ADY	ADX	X pointer	Y pointer	X pointer	Y pointer
0	0	0	0	0	WXMIN[7:0]	WYMIN[8:0]
0	0	1	MPSX[7:0]-1	0	WXMAX[7:0]	WYMIN[8:0]
0	1	0	0	MPSY[8:0]-1	WXMIN[7:0]	WYMAX[8:0]
0	1	1	MPSX[7:0]-1	MPSY[8:0]-1	WXMAX[7:0]	WYMAX[8:0]
1	0	0	0	0	WXMIN[7:0]	WYMIN[8:0]
1	0	1	MPSX[7:0]-1	0	WXMAX[7:0]	WYMIN[8:0]
1	1	0	0	MPSY[8:0]-1	WXMIN[7:0]	WYMAX[8:0]
1	1	1	MPSX[7:0]-1	MPSY[8:0]-1	WXMAX[7:0]	WYMAX[8:0]

※ Refer to the next page,‘Memory access order’ for the direction of operation.

8.2. Memory access order

8.2.1. Register list

Address	Register Name	Description
1DH	ADX	This sets the addressing direction of X address when accessing Display RAM. 0：Normal（increment）direction 1：Inversion（decrement）direction
	ADY	This sets the addressing direction of Y address when accessing Display RAM. 0：Normal（increment）direction 1：Inversion（decrement）direction
	INC	This sets the increment direction of address when accessing Display RAM. 0：X address・increment 1：Y address・increment

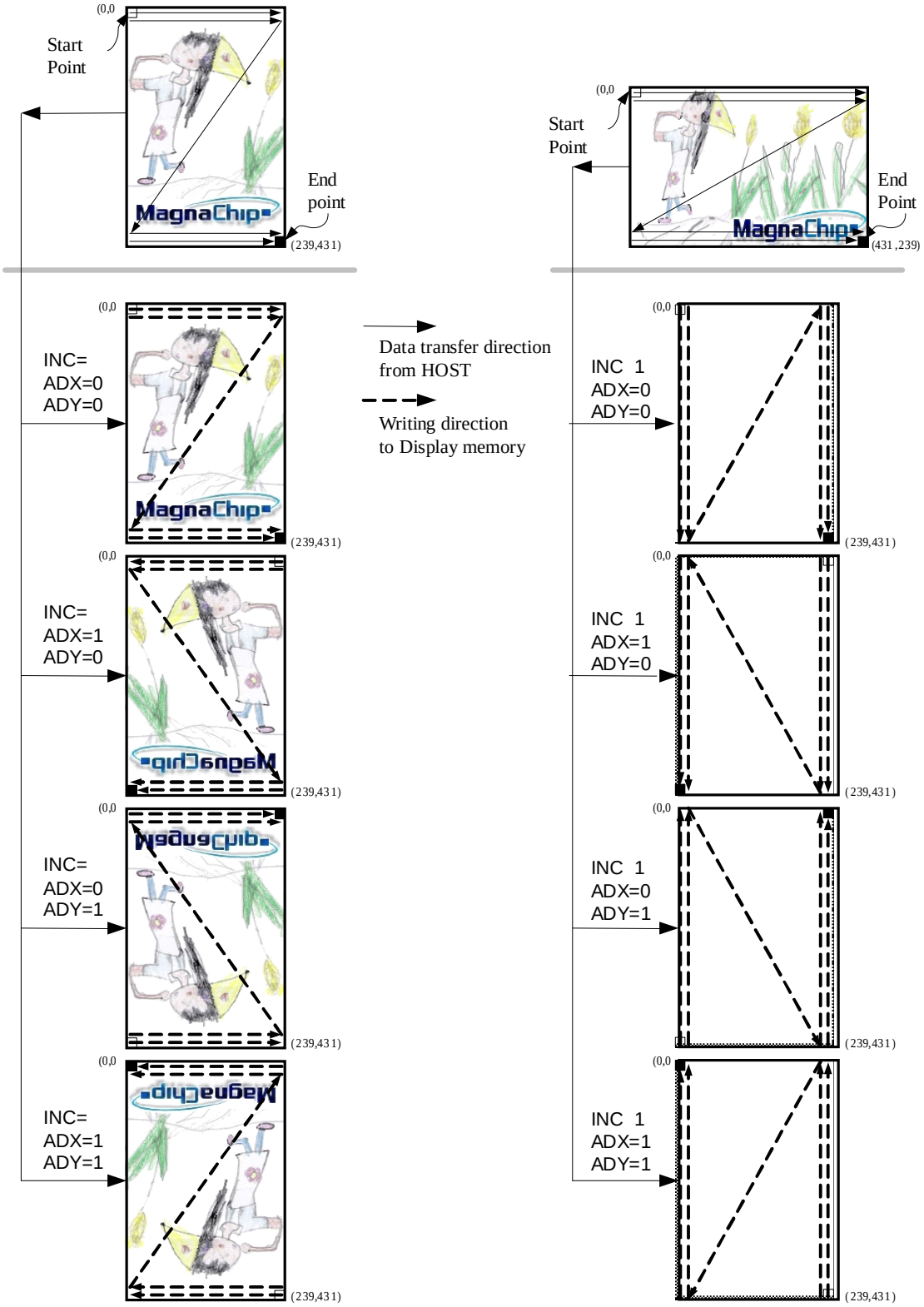
・Examples of Memory access order

The original address and Memory access order are shown below for the panel of 3×3 pixels(1～9 pixel shown below) when setting each function by ADX,ADY,INC register.
In Window access mode, the same operation is done in the setting area.

1	2	3
4	5	6
7	8	9

INC	ADY	ADX	Original address	Memory access order
0	0	0	1	1→2→3→4→5→6→7→8→9
0	0	1	3	3→2→1→6→5→4→9→8→7
0	1	0	7	7→8→9→4→5→6→1→2→3
0	1	1	9	9→8→7→6→5→4→3→2→1
1	0	0	1	1→4→7→2→5→8→3→6→9
1	0	1	3	3→6→9→2→5→8→1→4→7
1	1	0	7	7→4→1→8→5→2→9→6→3
1	1	1	9	9→6→3→8→5→2→7→4→1

(Fig.8-2) Outline Fig. of the register setting



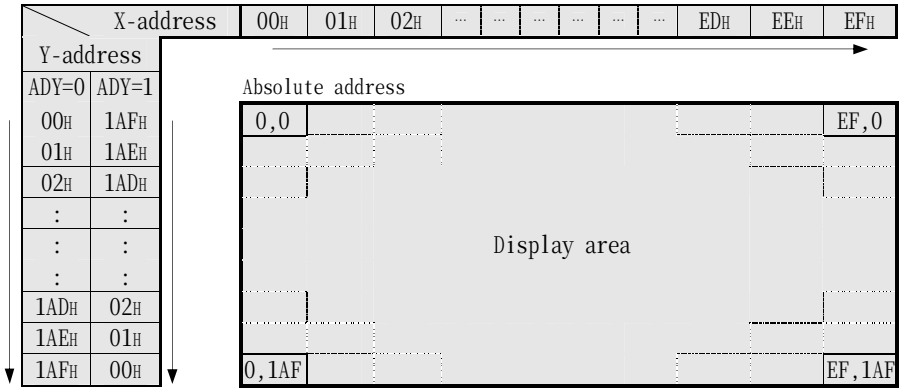
8.3. RAM Addressing

- Maximum panel size： 240 RGB×432 （MPSX[7:0]=240, MPSY[8:0]=432）

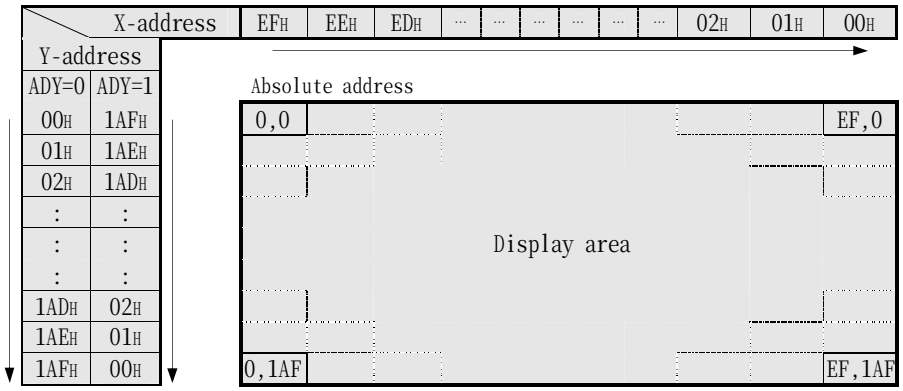
RAM Read to the panel is always executed in following order of the absolute address of RAM as the (Fig.9-3) below. However the virtual address of Write, Read and Auto increment from the host to RAM will change like X-address and Y-address in the Fig by setting ADX and ADY. Herewith flip horizontal writing and flip vertical writing in the previous page become possible. X-address and Y-address are allocated in the setting area in Window access mode.

(Fig.8-3) RAM addressing

When ADX=0,



When ADX=1,



9. Partial setting

9.1. Register list

Address	.	Description
30H	PTLON[1:0]	This selects Partial Display functions. 00：Normal Display 01：Partial Display, Display area A 10：Partial Display, Display area B 11：Partial Display, Both Display area A and Display area B.
64H	TPNREF[3:0]	Refresh frequency setting
	TREF[2:0]	Refresh frequency setting of Non-display area
36H,37H	PTLAS[8:0]	The start line of Display area A in Partial Display.
38H,39H	PTLAE[8:0]	The end line of Display area A in Partial Display.
3AH,3BH	PTLBS[8:0]	The start line of Display area B in Partial Display.
3CH,3DH	PTLBE[8:0]	The end line of Display area B in Partial Display.

・Partial-related register constraints

a: 0≦PTLAS≦PTLAE≦MPSY-1
b: 0≦PTLBS≦PTLBE≦MPSY-1

※ When PTLON=01, Partial Display will not be done if a is not satisfied.
※ When PTLON=10, Partial Display will not be done if b is not satisfied.
※ When PTLON=11, Partial Display will be done only when both a and b are satisfied.

There is no constraint for the hierarchical relation or overlapping of Display area A and Display area B.

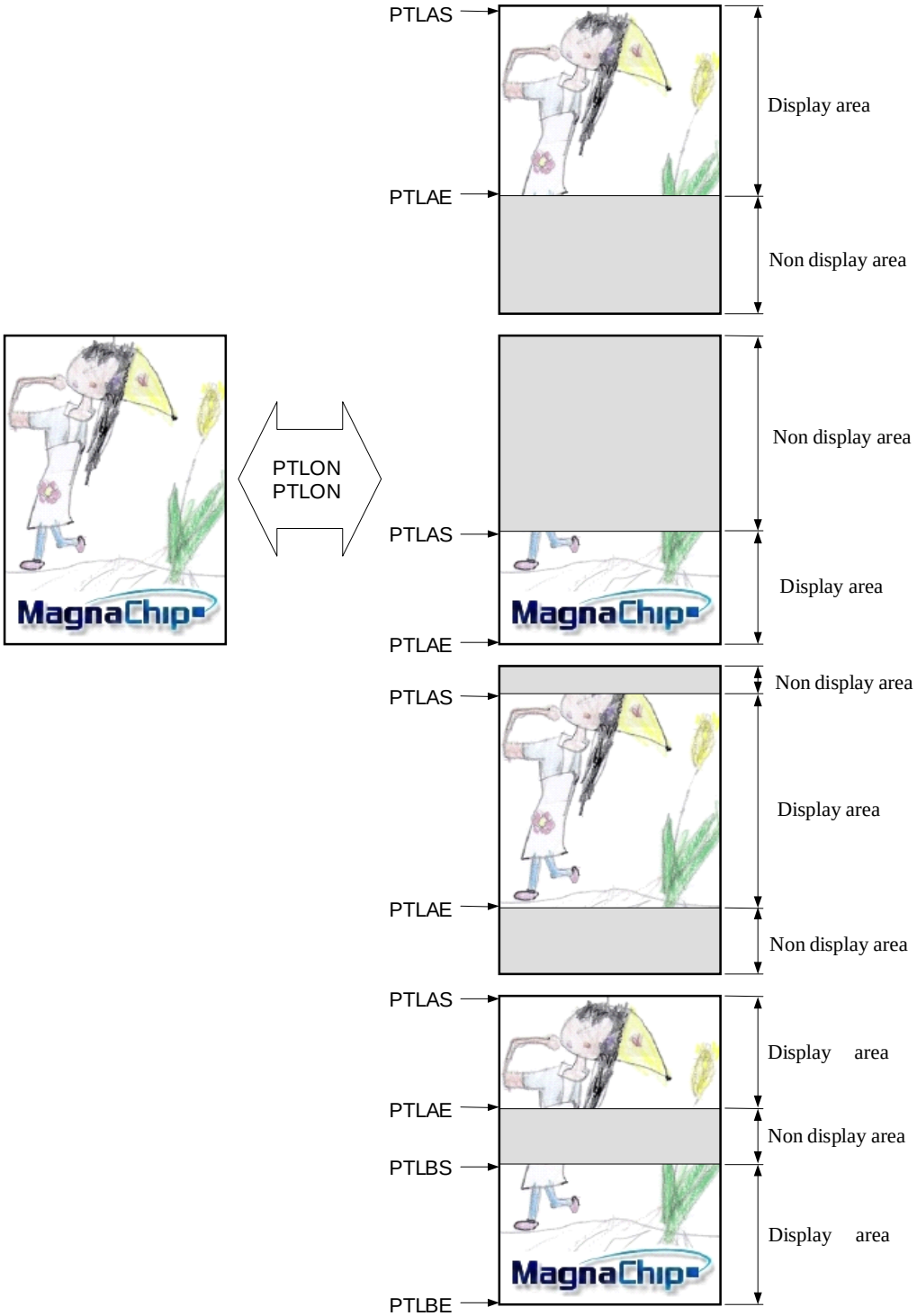
When two areas are successive or overlapped, they will be displayed as one successive area.

・Other constraints

Partial display mode and Screen scroll function have the priority order and only higher function will be displayed. Even though the higher function is in operation, the value can be entered to the register. When the higher function is OFF, the set value will be applied in Display.
Partial Display mode has higher priority than Screen scroll.

※ There is no RAM Read to any panel parts except the set area because Partial Display mode aims the electrical power saving.

(Fig.9-1) Register setting outline Fig.



※ Display area B can be set to the upper position than Display area A.

10. Screen scroll

10.1. Register list

Address	Register Name	Description
20H,21H	SSL[8:0]	This sets the start line of the scroll area in Scroll function.
22H,23H	SEL[8:0]	This sets the end line of the scroll area in Scroll function.
24H,25H	SST[8:0]	This sets the step numbers of scroll in Scroll function.

・Scroll Display is started when the value is entered to SST[8:0]register.

・ Scroll Display is the display whose upper and under sides of the image in the scroll area, set by SSL[8:0] and SEL[8:0], are connected and that image will move upward according to the number of steps already set.（Image on the display appears to move upward as the address moves downward.）, the part run off the edge from the scroll area appears from the bottom.

・When 0 is entered to SST[8:0] register, Normal Display is started.

・Scroll-related register constraints

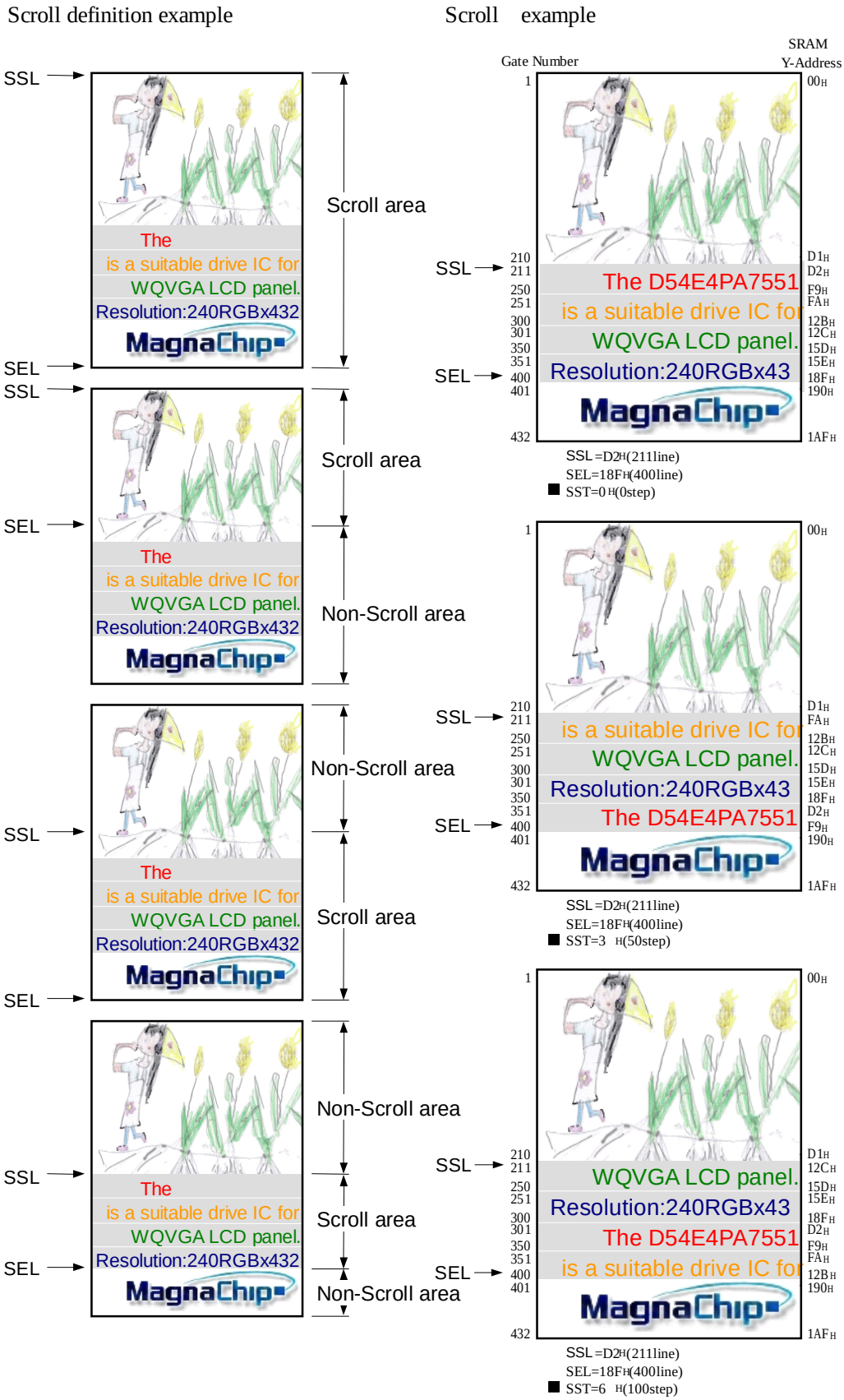
$0 \leqq SSL[8:0] < SEL[8:0] \leqq MPSY[8:0]-1$
$0 \leqq SST[8:0] < SEL[8:0] - SSL[8:0]+1$

※ When setting other than these constraints, scrolling will not be implemented.

・Other constraints

Partial display mode and Screen scroll function have the priority order and the only higher function will be displayed. Even though the higher function is in operation, the value can be entered to the register. When the higher function is OFF, the set value will be reflected in Display.
The priority of Screen scroll function is lower than Partial display mode.

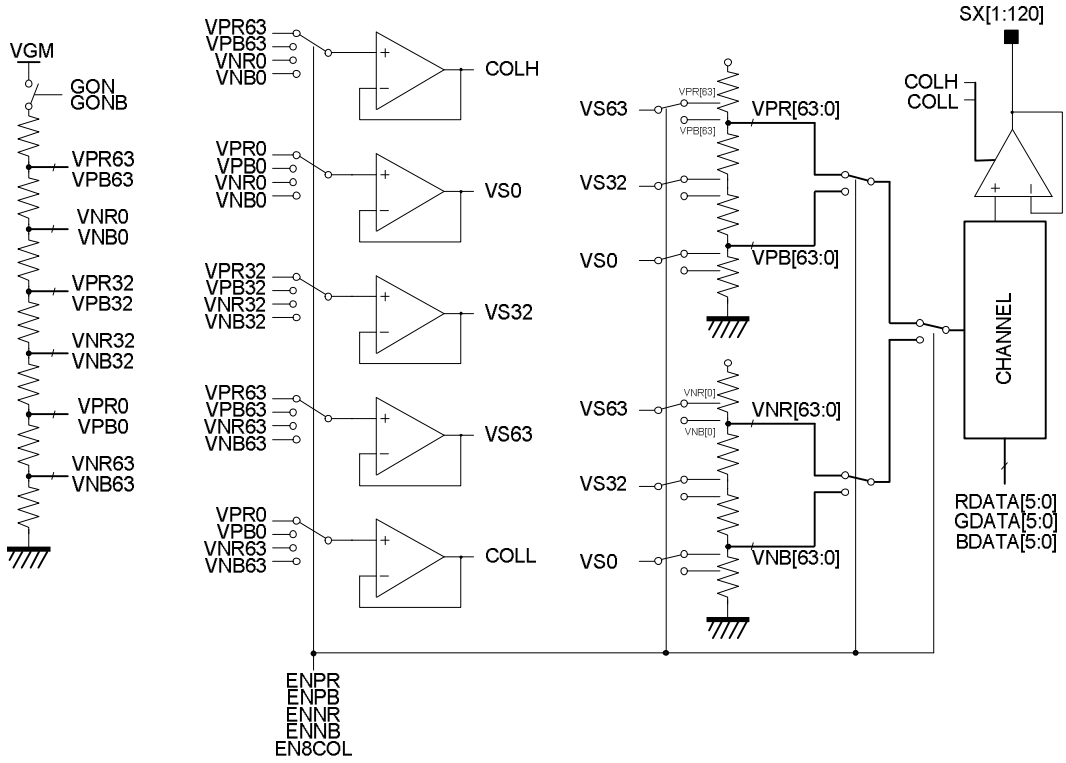
(Fig.10-1)：Register setting outline Fig.



11. Configuration of Gamma circuits

11.1. Outline

The 64-gray scale voltage is generated by the gamma resistance ratio between VGM-VGML (GND).
The Blue gamma function is available. The blue gamma is generated by selecting the same gamma resistance for Red/Green gamma's. And it actualizes the gamma function for Blue. Gamma resistance is set the positive/negative pole respectively. Gamma resistance configuration is explained below.

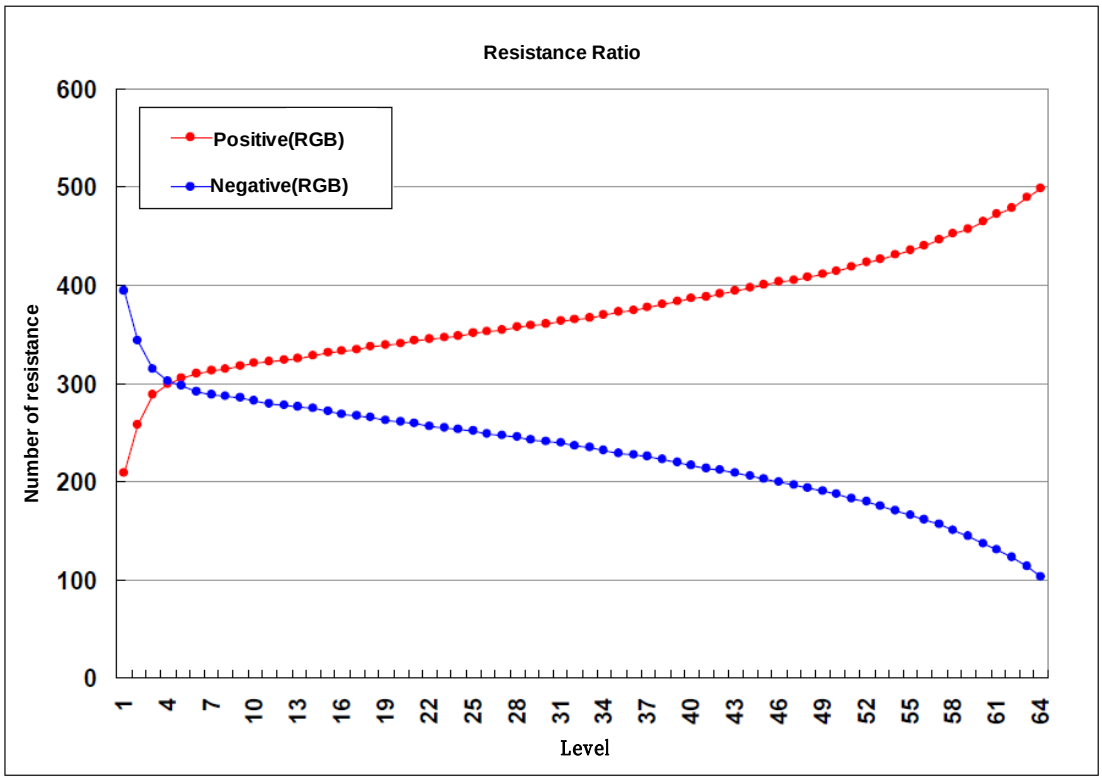


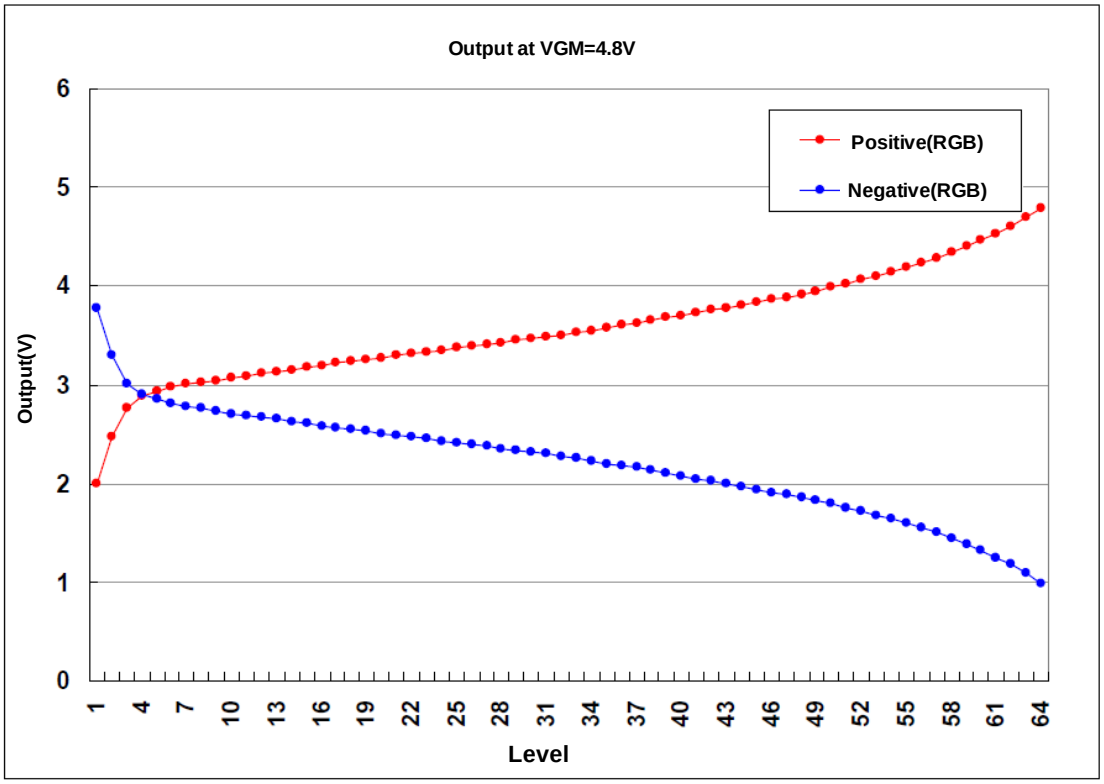
11.2. Gamma resistance ratio table

Reg/Green Gamma and Blue Gamma have some value in this case.
They have difference circuit for each and their value describe on each column.

Gray Level	Ratio of Resistance				Gray voltage at VGM=4.8V			
	Positive(VCOM=L)		Negative(VCOM=H)		Positive(VCOM=L)		Negative(VCOM=H)	
	RED/ GREEN	BLUE	RED/ GREEN	BLUE	RED/ GREEN	BLUE	RED/ GREEN	BLUE
1	208	208	394	394	1.9968	1.9968	3.7824	3.7824
2	258	258	344	344	2.4768	2.4768	3.3024	3.3024
3	288	288	314	314	2.7648	2.7648	3.0144	3.0144
4	300	300	302	302	2.8800	2.8800	2.8992	2.8992
5	305	305	297	297	2.9280	2.9280	2.8512	2.8512
6	310	310	292	292	2.9760	2.9760	2.8032	2.8032
7	313	313	289	289	3.0048	3.0048	2.7744	2.7744
8	315	315	287	287	3.0240	3.0240	2.7552	2.7552
9	317	317	285	285	3.0432	3.0432	2.7360	2.7360
10	320	320	282	282	3.0720	3.0720	2.7072	2.7072
11	322	322	280	280	3.0912	3.0912	2.6880	2.6880
12	324	324	278	278	3.1104	3.1104	2.6688	2.6688
13	326	326	276	276	3.1296	3.1296	2.6496	2.6496
14	328	328	274	274	3.1488	3.1488	2.6304	2.6304
15	331	331	271	271	3.1776	3.1776	2.6016	2.6016
16	333	333	269	269	3.1968	3.1968	2.5824	2.5824
17	335	335	267	267	3.2160	3.2160	2.5632	2.5632
18	337	337	265	265	3.2352	3.2352	2.5440	2.5440
19	339	339	263	263	3.2544	3.2544	2.5248	2.5248
20	341	341	261	261	3.2736	3.2736	2.5056	2.5056
21	343	343	259	259	3.2928	3.2928	2.4864	2.4864
22	345	345	257	257	3.3120	3.3120	2.4672	2.4672
23	347	347	255	255	3.3312	3.3312	2.4480	2.4480
24	349	349	253	253	3.3504	3.3504	2.4288	2.4288
25	351	351	251	251	3.3696	3.3696	2.4096	2.4096
26	353	353	249	249	3.3888	3.3888	2.3904	2.3904
27	355	355	247	247	3.4080	3.4080	2.3712	2.3712
28	357	357	245	245	3.4272	3.4272	2.3520	2.3520
29	359	359	243	243	3.4464	3.4464	2.3328	2.3328
30	361	361	241	241	3.4656	3.4656	2.3136	2.3136
31	363	363	239	239	3.4848	3.4848	2.2944	2.2944
32	365	365	237	237	3.5040	3.5040	2.2752	2.2752
33	367	367	235	235	3.5232	3.5232	2.2560	2.2560
34	370	370	232	232	3.5520	3.5520	2.2272	2.2272
35	373	373	229	229	3.5808	3.5808	2.1984	2.1984
36	375	375	227	227	3.6000	3.6000	2.1792	2.1792
37	377	377	225	225	3.6192	3.6192	2.1600	2.1600
38	380	380	222	222	3.6480	3.6480	2.1312	2.1312
39	383	383	219	219	3.6768	3.6768	2.1024	2.1024
40	386	386	216	216	3.7056	3.7056	2.0736	2.0736
41	389	389	213	213	3.7344	3.7344	2.0448	2.0448
42	391	391	211	211	3.7536	3.7536	2.0256	2.0256
43	394	394	208	208	3.7824	3.7824	1.9968	1.9968
44	397	397	205	205	3.8112	3.8112	1.9680	1.9680
45	400	400	202	202	3.8400	3.8400	1.9392	1.9392
46	403	403	199	199	3.8688	3.8688	1.9104	1.9104
47	405	405	197	197	3.8880	3.8880	1.8912	1.8912
48	408	408	194	194	3.9168	3.9168	1.8624	1.8624
49	411	411	191	191	3.9456	3.9456	1.8336	1.8336
50	415	415	187	187	3.9840	3.9840	1.7952	1.7952
51	419	419	183	183	4.0224	4.0224	1.7568	1.7568
52	423	423	179	179	4.0608	4.0608	1.7184	1.7184
53	427	427	175	175	4.0992	4.0992	1.6800	1.6800
54	431	431	171	171	4.1376	4.1376	1.6416	1.6416
55	436	436	166	166	4.1856	4.1856	1.5936	1.5936
56	441	441	161	161	4.2336	4.2336	1.5456	1.5456
57	446	446	156	156	4.2816	4.2816	1.4976	1.4976
58	452	452	150	150	4.3392	4.3392	1.4400	1.4400
59	458	458	144	144	4.3968	4.3968	1.3824	1.3824
60	465	465	137	137	4.4640	4.4640	1.3152	1.3152
61	472	472	130	130	4.5312	4.5312	1.2480	1.2480
62	479	479	123	123	4.5984	4.5984	1.1808	1.1808
63	489	489	113	113	4.6944	4.6944	1.0848	1.0848
64	499	499	103	103	4.7904	4.7904	0.9888	0.9888
全体比 Total	500				VGM@4.8V			

11.3. Graph of GAMMA resistance





12. VCOM Output circuit

The configurations of VCOM output using VGM as the reference and using VRIN as the power supply.

Refer to “Power supply circuits (3) Block diagram” and following“12.1 VCOM Output Voltage”.

12.1. VCOM Output Voltage

Output Voltage of VCOMH and VCOML are designated by register VCOMH(68h) and VCOML(69h).
VGM voltage works as reference voltage for VCOMH and VCOML.
The actual output voltage of VCOM and VCOML are related with VGM and both registers VCOMH(68h) and VCOML(69h).

	Min and Max value of registers	Output voltage rage	Output voltage at VGM=4.8V
VCOMH	07H～B8H	VGM×0.5～ VGM×1.208	2.40V～VRIN-0.2V（Note）
VCOML	07H～B8H	VGM×0.036～ VGM×0.744	0.20V～3.571V(Note)

Note） The output voltage which disiganated by register is different from actual output voltage.
Actual voltage is limited by following formulas.
VCOMH≦VRIN-0.2V
VCOML≧0.2V

VCOMH Output Voltage
VCOMH（V）＝VGM×[0.500+0.004×(VCOMH-07h)]

Output voltage example at VGM＝4.8V VRIN=5.1V

VCOMH[7:0]	VCOMHoutput voltage	VCOMH[7:0]	VCOMHoutput voltage
07H	2.400V	70H	4.416V
10H	2.573V	71H	4.435V
20H	2.880V	72H	4.454V
30H	3.187V	73H	4.474V
40H	3.494V	74H	4.493V
50H	3.802V	75H	4.512V
60H	4.109V	76H	4.531V
68H	4.262V	77H	4.550V
69H	4.282V	78H	4.570V
6AH	4.301V	80H	4.723V
6BH	4.320V	88H	4.877V
6CH	4.339V		
6DH	4.358V		
6EH	4.378V		
6FH	4.397V		

VCOML Output Voltage

VCOML（V）＝VGM×[0.036+0.004×(VCOML-07h)]

Output voltage example at VGM＝4.8V VRIN=5.1V

VCOML[7:0]	VCOMLoutput voltage	VCOML[7:0]	VCOMLoutput voltage
09H	0.211V	60H	1.882V
10H	0.346V	61H	1.901V
20H	0.653V	62H	1.920V
2DH	0.902V	63H	1.939V
2EH	0.922V	64H	1.958V
2FH	0.941V	65H	1.978V
30H	0.960V	66H	1.997V
31H	0.979V	67H	2.016V
32H	0.998V	68H	2.035V
33H	1.018V	69H	2.054V
34H	1.037V	6AH	2.074V
35H	1.056V	6BH	2.093V
36H	1.075V	6CH	2.112V
37H	1.094V	6DH	2.131V
40H	1.267V	70H	2.189V
50H	1.574V	80H	2.496V

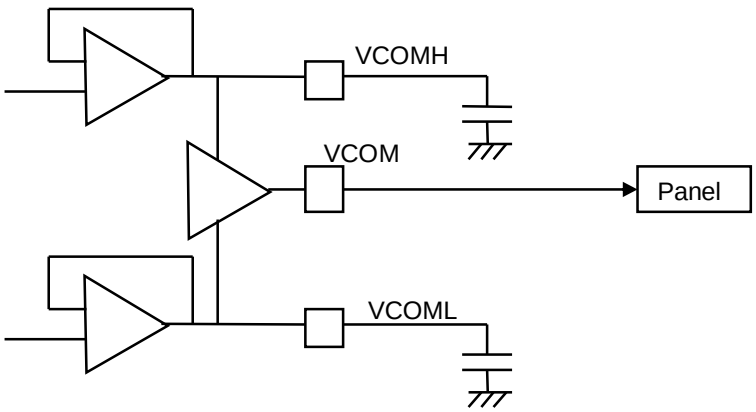
12.2. VCOM OUTPUT MODE

This VCOM output circuit has 3 kinds mode which is designated by COM_MODE[1:0](Address=6AH).

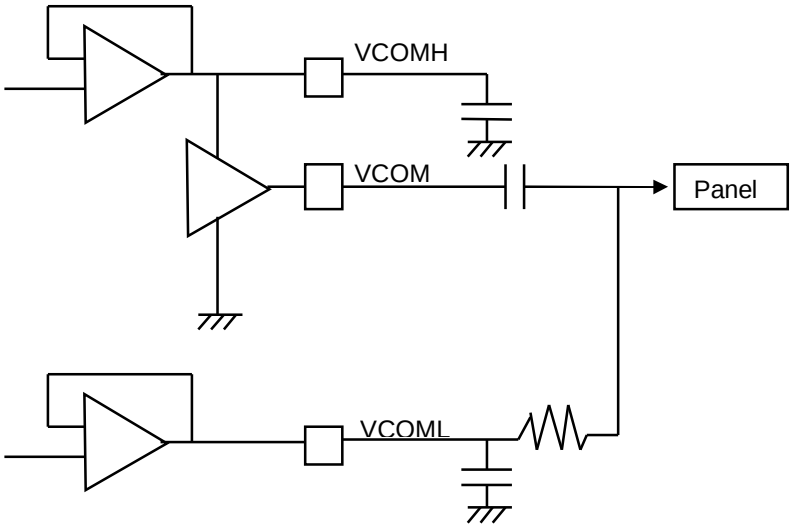
COM_MODE1	COM_MODE0	VCOM Output mode
0	0	mode 1-1
0	1	mode 1-2
1	0	mode 2
1	1	mode 3

In each mode, internal equivalent circuit and external circuit are below.
By setting COM_MODE[1:0], VCOM AMP operation change.

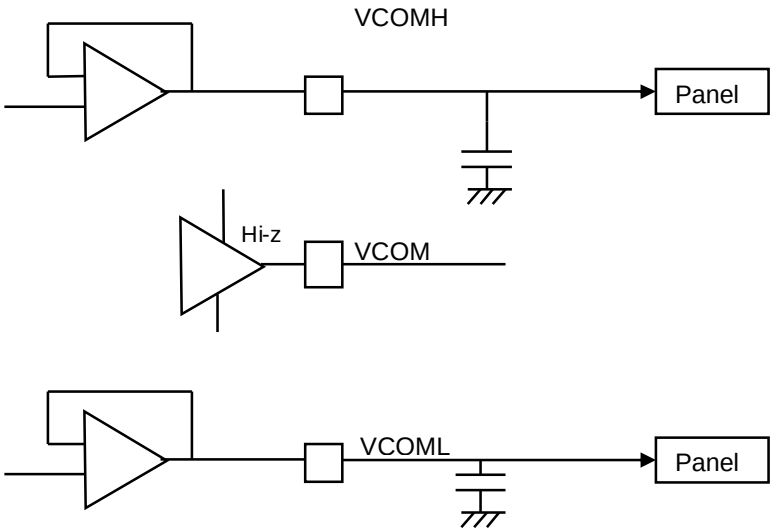
Output MODE 1-1 and 1-2 The timing of VCOM rising & falling position are difference between MODE1-1 and 1-2. Internal circuit is same.



Output mode 2



Output mode 3



13. Register map and summary

ADD	Symbol	D7	D6	D5	D4	D3	D2	D1	D0	Description	Default	Appl.
00H	NOP	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0	ID[7:0] : Device code	37	-
01H	TRFMODE	-	-	-	-	-	BTSEL	DTX2	DTX1	BTSEL : 5-bit data allocation setting DTX[2:1] : Specify the transfer mode	00	A0
02H	RREN	-	-	-	-	-	-	-	RREN	RREN : Register Read/Write selection	-	A0
03H	RAMDT	-	-	-	-	-	-	-	RAMDT	RAMDT : RAM Read/Write selection	-	A0
07H	SYSCTL	-	-	-	-	-	BATDET	OSCDIV	CRON	BAT_DET: battery detection enable OSCDIV : Built-in CR oscillation 2 frequencies dividing setting CRON : Oscillator circuit ON/OFF	01	A0
08H	MEMCTL	-	-	-	-	RBI	COL8WR	NWB	REVWR	RBI : Data exchange setting of Red/Blue COL8WR : 8-color Write NWB : Normal White/Black REVWR : Image data inversion Write	02	A0
10H	MPSX	MPSX7	MPSX6	MPSX5	MPSX4	MPSX3	MPSX2	MPSX1	MPSX0	MPSX[7:0] : PANEL X Size	F0	A0
11H	MPSY1	MPSY7	MPSY6	MPSY5	MPSY4	MPSY3	MPSY2	MPSY1	MPSY0	MPSY[8:0] : PANEL Y Size	90	A0
12H	MPSY2	-	-	-	-	-	-	-	MPSY8		01	
13H	WXMIN	WXMIN7	WXMIN6	WXMIN5	WXMIN4	WXMIN3	WXMIN2	WXMIN1	WXMIN0	WXMIN[7:0]Window mode X start point	00	A0
14H	WYMIN1	WYMIN7	WYMIN6	WYMIN5	WYMIN4	WYMIN3	WYMIN2	WYMIN1	WYMIN0	WYMIN[7:0]Window-mode Y start point	00	A0
15H	WYMIN2	-	-	-	-	-	-	-	WYMIN8			
16H	WXMAX	WXMAX7	WXMAX6	WXMAX5	WXMAX4	WXMAX3	WXMAX2	WXMAX1	WXMAX0	WXMAX[7:0] : Window mode X end point	00	A0
17H	WYMAX1	WYMAX7	WYMAX6	WYMAX5	WYMAX4	WYMAX3	WYMAX2	WYMAX1	WYMAX0	WYMAX[7:0] : Window mode Y end point	00	A0
18H	WYMAX2	-	-	-	-	-	-	-	WYMAX8			
19H	WAS	-	-	-	-	-	-	-	WAS	Window Access mode enable	00	A0
1AH	XA	XA7	XA6	XA5	XA4	XA3	XA2	XA1	XA0	XA[8:0] : RAM write X address	00	A0
1BH	YA1	YA7	YA6	YA5	YA4	YA3	YA2	YA1	YA0	YA[8:0] : RAM write Y address	00	A0
1CH	YA2	-	-	-	-	-	-	-	YA8			
1DH	RAMCTL	SCANUD (VS)					ADX (VA)	ADY (VA)	INC (VA)	SCANUD:Memory scan direction ADX : X address INC/DEC setting ADY : Y address INC/DEC setting INC : INC X/Y direction setting	00	VS A0
1EH	TVGLN	-	TVGLN6	TVGLN5	TVGLN4	TVGLN3	TVGLN2	TVGLN1	TVGLN0	TVGLN[6:0]:Display line numbers	50	VA
20H	SSL1	SSL7	SSL6	SSL5	SSL4	SSL3	SSL2	SSL1	SSL0	SSL[8:0]: Scroll start line	00	VA
21H	SSL2	-	-	-	-	-	-	-	SSL8			
22H	SEL1	SEL7	SEL6	SEL5	SEL4	SEL3	SEL2	SEL1	SEL0	SEL[8:0]: Scroll end line	00	VA
23H	SEL2	-	-	-	-	-	-	-	SEL8			
24H	SST1	SST7	SST6	SST5	SST4	SST3	SST2	SST1	SST0	SST[8:0]: Scroll step numbers SSTD: Scroll direction setting	00	VA
25H	SST2	SSTD	-	-	-	-	-	-	SST8			
30H	DSPCTL1	UD	INITON	MODE	-	PTLON1	PTLON0	-	DEN	UD: Gate scan direction INITON: LCD panel Initialization MODE: Select the register for use PTLON[1:0]: Partial Display DEN: Select the Display data	80	VS
31H	VALTRAN	-	-	-	-	-	-	-	VALG0	VALG0: Vertical synchronizing flag	00	VS
33H	DSPCTL2	-	-	-	-	-	-	DENCOL	-	DENCOL: Non-Display data color	00	VS
34H	TGCTL1	-	FROFF	SSIGOFF	GSIGOFF	GOEOFF	DCKOFF	GCKOFF	COMOFF	GSIGOFF:Gate control system output OFF control SSIGOFF:Source control system output OFF control GOEOFF: GOE output OFF control GCKOFF: GCK output OFF control COMOFF: COM output OFF control	00	A0
35H	TGCTL2	DCKINV	RCKINV	GUDINV	SSWINV	GSPINV	GOEINV	FRINV	GCKINV	DCKINV:DCK and DCKB out polarity RCKINV: RCK output polarity GUDINV: GUD output polarity SSWINV: ASW output polarity GSPINV: GSP output polarity GOEINV: GOE output polarity FRINV: FR output polarity GCKINV: GCK output polarity	00	A0
36H	PTLAS1	PTLAS7	PTLAS6	PTLAS5	PTLAS4	PTLAS3	PTLAS2	PTLAS1	PTLAS0	PTLAS[8:0] :partial area(A)start line	00	VA
37H	PTLAS2	-	-	-	-	-	-	-	PTLAS8			
38H	PTLAE1	PTLAE7	PTLAE6	PTLAE5	PTLAE4	PTLAE3	PTLAE2	PTLAE1	PTLAE0	PTLAE[8:0] :partial area(A)end line	00	VA
39H	PTLAE2	-	-	-	-	-	-	-	PTLAE8			
3AH	PTLBS1	PTLBS7	PTLBS6	PTLBS5	PTLBS4	PTLBS3	PTLBS2	PTLBS1	PTLBS0	PTLBS[8:0] :partial area(B)start line	00	VA
3BH	PTLBS2	-	-	-	-	-	-	-	PTLBS8			
3CH	PTLBE1	PTLBE7	PTLBE6	PTLBE5	PTLBE4	PTLBE3	PTLBE2	PTLBE1	PTLBE0	PTLBE[8:0] :partial area(B)end line	00	VA
3DH	PTLBE2	-	-	-	-	-	-	-	PTLBE8			
3EH	SEQCTL	-	-	-	-	-	-	AUTOFF	AUTON	AUTOFF: Auto OFF sequence start AUTON : Auto ON sequence start	00	A0
3FH	EXVSCTL	-	-	-	-	-	-	-	EXVSON	EXVSON: External VSYNC control	00	A0

ADD	Symbol	D7	D6	D5	D4	D3	D2	D1	D0	Description	Default	Appl.
40H	TPARAM1	TVBK 1LINE	TVBK GCK	TVBK GOE	TVBK COM2	TVBK COM1	TVBK COM0	TVBK SX1	TVBK SX0	TVBK1LINE: 1 line output before/after valid line TVBKGCK: Blanking GCK output TVBKGOE: Blanking GOE output TVBKCOM[2:0]:Blanking COM output TVBKSX[1:0]:Blanking source output	00	VS
42H	TVFPSIZE	-	TVFP6	TVFP5	TVFP4	TVFP3	TVFP2	TVFP1	TVFP0	TVFP[6:0]: Vertical front porch	33	VS
43H	TVBLNK	-	-	-	-	-	TVBP2	TVBP1	TVBP0	TVBP[2:0]: Vertical back porch number	01	VS
44H	THCNT	-	-	THCNT5	THCNT4	THCNT3	THCNT2	THCNT1	THCNT0	THCNT[5:0]: Horizontal scan term	09	VS
45H	TGSPWD	-	-	-	TGSPST3	TGSPST2	TGSPST1	TGSPST0	TGSPWD	TGSPST[3:0]: GSP output starting position setting TGSPWD: GSP output active width	02	VS
46H	TGCKST	-	-	-	-	TGCKST3	TGCKST2	TGCKST1	TGCKST0	TGCKST[3:0]:GCK output starting point setting	06	VS
48H	TCOMST	-	-	-	-	-	TCOMST2	TCOMST1	TCOMST0	TCOMST[2:0]:COM output position setting	01	VS
4AH	TSSWCTL1	-	-	-	FRCINV	THPCH CTL	TVBK ASW1	TVBK ASW0	SWDAREV	FRCINV: COM phase inversion setting THPCH_CTL: Horizontal pre-charge output setting TVBK_ASW[1:0]: Blanking term ASW SWDAREV: SSD output pixel inversion	00	VS
4BH	TSSWCTL2	TYPE1	TYPE0	RB	PIX	FREV1	FREV0	LREV1	LREV0	TYPE[1:0]: SSD output order setting RB: SSD output RB inversion PIX: SSD output Pixel inversion FREV[1:0]:SSD output frame inversion LREV[1:0]:SSD output line setting	00	VS
4CH	TASWST	-	-	-	TASWST4	TASWST3	TASWST2	TASWST1	TASWST0	TASWST[4:0]: AS output starting position setting	06	VS
4DH	TPCDCTL	PREST3	PREST2	PREST1	PREST0	PREWD3	PREWD2	PREWD1	PREWD0	PREST[3:0]: Pre-charge starting position setting PREWD[3:0]: Pre-charge ASW pulse width	01	VS
4FH	TPTLREF1	-	TVPTL AWS11	TVPTL AWS10	TVPTLCOM12	TVPTLCOM11	TVPTLCOM10	TVPTL SX11	TVPTL SX10	TVPTLASW1[1:0]: Partial ASW setting TVPTLCOM1[2:0]: Partial COM setting TVPTLSX1[1:0]: Partial setting	00	VS
50H	TPTLREF2	-	-	-	-	-	-	TPTL 1LINE	TPTL GOE	TPTL1LINE: Partial Non-Display output setting TPTLGOE: Partial Non-Display GOE setting	00	VS
51H	TVPTLCOM2	-	-	-	-	-	TVPTLCOM22	TVPTLCOM21	TVPTLCOM20	COM setting at Partial Mode	00	VS
52H	TASWST	-	-	-	TASWST4	TASWST3	TASWST2	TASWST1	TASWST0	TASWST[4:0] : ASW simultaneous enable start	01	VS
53H	TASWASX	-	-	-	TASWSX	TASWWD3	TASWWD2	TASWWD1	TASWWD0	TASWSX: ASW simultaneous enable source output TASWWD[2:0]: ASW simultaneous enable pulse width	01	VS
54H	TPHPARAM	-	-	-	-	-	THBKSX1	THBKSX0	TPCHLVL	THBKSX[1:0]:Blanking source output TPCHLVL:horizontal pre-charge output	02	VS
5AH	BATNZDET	-	-	-	-	-	-	BATNZDET1	BATNZDET0	BATNZDET[1:0]:batty detect period	00	A0
5BH	MPWSTEP1	MPSTP8	MPSTP7	MPSTP6	MPSTP5	MPSTP4	MPSTP3	MPSTP2	MPSTP1	Manual operation of each power step	00	A0
5CH	MPWSTEP2	-	-	-	-	-	-	MPSTP10	MPSTP9		00	A0
60H	DRVCTL1	CHGSON	LPWRON	-	COMREV	-	-	-	-	CHGSHRON:Charge share enable LPWRON:Low current control COMREV:COM output control	00	VA
61H	DRVCTL2	CHGSWD4	CHGSWD3	CHGSWD2	CHGSWD1	CHGSWD0	CHGSST2	CHGSST1	CHGSST0	CHGSWD[4:0]:Charge share period CHGSST[2:0]: Charge share start	00	VS
62H	TASW2	-	TSWWD3	TSWWD2	TSWWD1	TSWWD0	TSWSP2	TSWSP1	TSWSP0	TSWWD[3:0]:ASW pulse width TSWSP[2:0]:ASW pulse width	29	VS
63H	TRDRVB1	-	-	-	-	-	SDRVT2	SDRVT1	SDRVT0	SDRVST[2:0]:Low current drive period	00	VA
64H	TREFCTL1	-	PTLNDR3	PTLNDR2	PTLNDR1	PTLNDR0	PTLDR2	PTLDR1	PTLDR0	PTLNDR[3:0]:partial no-Display Area refresh ratio setting PTLDR[2:0]:Display area refresh ratio	00	VA
65H	TBIAS1	-	-	-	-	OBIAS3	OBIAS2	OBIAS1	OBIAS0	OBIAS[3:0]:Gamma bias current	02	A0
66H	VGAMH1	-	-	-	-	-	VGAMH2	VGAMH1	VGAMH0	VGAMH[2:0]:Gamma Amp H Voltage	03	A0
68H	VCOMH1	VCOMH7	VCOMH6	VCOMH5	VCOMH4	VCOMH3	VCOMH2	VCOMH1	VCOMH0	VCOMH[6:0]:VCOMH voltage	07	A0
69H	VCOML1	VCOML7	VCOML6	VCOML5	VCOML4	VCOML3	VCOML2	VCOML1	VCOML0	VCOML[7:0]:VCOML voltage	07	A0
6AH	COM_MODE	-	-	-	-	-	-	COMMODE1	COMMODE0	COM OUTPUT mode	02	A0
6BH	CB	-	-	-	-	-	-	CB1	CB0	For Control	02	A0
70H ↓ 76H	DRVCTL3 ↓ VGAMH2									Low current drive mode registers same function as DRVCTL1-VGAMH1		

ADD	Symbol	D7	D6	D5	D4	D3	D2	D1	D0	Description	Default	Appl.
80H	POWCTL	V18M	ANAGOFF	VSR	VGMR	VCOMR	DCDC2	DCDDC1	APWRS	V18M:1.8V core Regulator control ANAGOFF:ANALOG CONTROL VSR:source power Regulator VGMR:VGM Regulator control VCOMR:VCOM Regulator control DCDC2:DCDC2 booster control DCDC1:DCDC1 booster control APWRS:Auto sequence control	81	AO
81H	DCDCCLK	-	DC2CK2	DC2CK1	DC2CK0	-	DC1CK2	DC1CLK1	DC1CK0	DC2CK[2:0]:DCDC2 boost clock frequency DC1CK[2:0]:DCDC1 boost clock frequency	44	AO
82H	PNLCKCTL	-	-	DCKST1	DCKST0	RCKSKW1	RCKSKW0	DCKDIV1	DCKDIV0	DCST[1:0]:DCK(B) skew RCK_SKW[1:0]:GCK/RCK Skew setting DCKDIV[1:0]:DCK divide	15	AO
83H	DC1CNT	-	DC1MD1	DC1MD0	DC1DRV1	DC1DRV0	DC1OUT2	DC1OUT1	DC1OUT0	DC1MD[1:0]:DCDC1 operation mode DC1DRV[1:0]:DCDC1 drivability DC1OUT[2:0]:DCDC1 output voltage	3C	AO
84H	DC1SET	-	-	-	RD1ON	DC1SET3	DC1SET2	DC1SET1	DC1SET0	RD1ON:RDON Timing DC1SET[3:0]:DCDC1 Clock Timing	17	AO
85H	DC2CNT	-	DC2MD1	DC2MD0	DC2DRV1	DC2DRV0	DC2OUT2	DC2OUT1	DC2OUT0	DC2MD[1:0]:DCDC2 operation mode DC2DRV[1:0]:DCDC2 drivability DC2OUT[2:0]:DCDC2 output voltage	20	AO
86H	DC2SET	-	-	-	RD2ON	DC2SET3	DC2SET2	DC2SET1	DC2SET0	RD2ON:RDON Timing VDCDC2SET[3:0]:DCDC2Clock Timing	17	AO
90H	VPON1	DSTVR1	DSTVR0	PDC2ON1	PDC2ON1	PDC1ON1	PDC1ON0	PDCUP1	PDCUP0	DSTVR[1:0]:VR Start-up wait time PDC2ON[1:0]:DCDC Start-up time PDC1ON[1:0]:DCDC Start-up time PDCUP[1:0]:Panel DCS start-up time	15	AO
91H	VPON2	-	-	-	-	-	SXDISP	STDISP1	STDISP0	SXDISP:Non-Display data setting STDISP[1:0]:No-Display period	01	AO
92H	VPOFF1	-	-	EDDCON1	EDDCON0	EDCOM1	EDCOM0	EDDISP1	EDDISP0	EDDCON[1:0]:DCDC stable time EDCOM[1:0]:COM stable time EDDISP[1:0]:Display stable time	15	AO
C0	ET1CTL	-	-	-	-	-	-	EPDUSE	ET1WR	EPDUSE:VCOM EEPROM or register select ET1WR:VCOM EEPROM write	02	AO
D0	EPCOMH	EPCOMH7	EPCOMH6	EPCOMH5	EPCOMH4	EPCOMH3	EPCOMH2	EPCOMH1	EPCOMH0	VCOMH EEPROM read register	-	AO
D1	EPCOML	EPCOML7	EPCOML6	EPCOML5	EPCOML4	EPCOML3	EPCOML2	EPCOML1	EPCOML0	VCOML EEPROM read register	-	AO

(Notes)

(1) To the register set “-” in the register map, please set “0” when accessing.“0” will be read out when reading. And also to the register set“0”or“1”, please set (overwrite) that value when accessing.

(2) About the application

Application type	Symbol	Application point
Instant application	AO	It will be applied soon after the register value Write at Host interface/EEPROM interface. (However some registers require the maximum master clock to synchronization internally.)
Simultaneous application (VALGO is necessary.)	VA	The contents of VALGO system register will be applied to LCD interface simultaneously at next vertical synchronizing signal by VALGO treatment (VALGObit=“1”setting).
Simultaneous application (VALGO is not necessary.)	VS	It will be applied to the register simultaneously and automatically at the timing of Vsync.

(3) Do not access the address other than the one in the spec.

13.1. Register description

ID (Read Only)

00H	D7	D6	D5	D4	D3	D2	D1	D0
Name	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
Default	0	0	1	1	0	1	1	1

ID [7:0]: Rev. No. of D54E4PA7551B can be read out.
Writing to this register will be ignored. This operation can be used as NOP.

TRF MODE

01H	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	-	-	-	-	BTSEL	DTX2	DTX1
Default	0	0	0	0	0	0	0	0

BTSEL：Specify the bit position of the 6-bit in three times transfer mode.
'0'： DB[5:0]
'1'： DB[7:2]

DTX[1:0]：Specify the image data transfer mode.
Specify the transfer bit-width and transfer times of 1 pixel data.
Refer to" Table 7.7 Transfer mode" of "7.4.4 Writing the data to Display RAM"

RREN

02H	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	-	-	-	-	-	-	RREN
Default	-	-	-	-	-	-	-	-

RREN： Select Read/Write when CMDS='L'（command mode）.
'0'： Register write operation
'1'： Register read operation
Do NOT read out this register.
In case of set to "1", it is in Read operation, only this register can be written.

RAMDT

03H	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	-	-	-	-	-	-	RAMDT
Default	-	-	-	-	-	-	-	-

RAMDT： RAM data access command when PSX='L'（parallel I/F）& CMDS='H'（index/data mode）
The access to this access can be used for start accessing RAM.
Please refer to "2) Display RAM access" at Page 34.

SYSCTL

07H	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	-	-	-	-	BATDET	OSCDIV	CRON
Default	0	0	0	0	0	0	0	1

BATDET: Battery detecting emulation

'0'： Normal operation

'1'： Detecting operation emulation.

The same operation as an external terminal BATIN="L".

OSCDIV: OSC frequency divide control

This register is valid for the external clock mode as well.

'0'： System clock without clock divide.

'1'： Internal/External clock is divided into two for system clock.

CRON：CR oscillator control

'0'：CR oscillator disable

'1'：CR oscillator enable

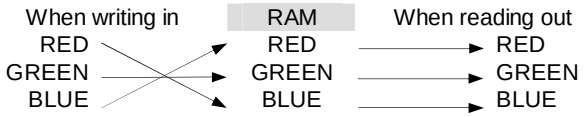
MEMCTL

08H	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	-	-	-	RBI	COL8WR	NWB	REVWR
Default	0	0	0	0	0	0	0	0

RBI：Switch the data of RED and BLUE. (Available at only write time)

'0'：Normal Write mode

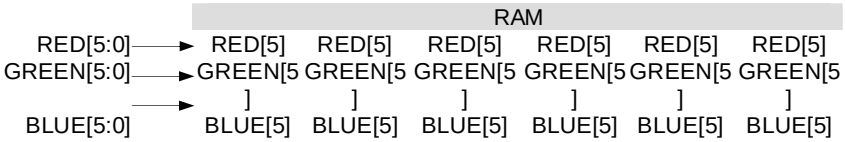
'1'：The RED data is switched to the Blue one when writing to RAM.



COL8WR：8-color data writing

'0'：Normal Write mode

'1'：8-color subtractive color processing is used when writing Display RAM.



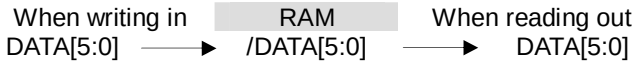
NWB： Setting of Normal White/Black

'0'：Normal Black LCD mode

'1'：Normal White LCD mode

(It will be inverted when both writing and reading the RAM data.)

There is no difference of the outer apparent operation about RAM read/write as the following fig.



REVWR：Write the inverted image data

'0'：Normal Write mode

'1'：When writing Display RAM, it writes the inverted bit data.

Inverted data will be read out when reading out because the data is inverted only when writing in.

When writing in → RAM → When reading out

DATA[5:0] → /DATA[5:0] → /DATA[5:0]

The relationship of NWB and REVWR is shown below.

NWB	REV WR	When writing in	RAM	When reading out
0	0	DATA[5:0] →	DATA[5:0]	→ DATA[5:0]
0	1	DATA[5:0] →	/DATA[5:0]	→ /DATA[5:0]
1	0	DATA[5:0] →	/DATA[5:0]	→ DATA[5:0]
1	1	DATA[5:0] →	DATA[5:0]	→ /DATA[5:0]

MPSX

10H	D7	D6	D5	D4	D3	D2	D1	D0
Name	MPSX7	MPSX6	MPSX5	MPSX4	MPSX3	MPSX2	MPSX1	MPSX0
Default	1	1	1	1	0	0	0	0

MPSX[7:0]： Set the number of pixels for X direction of the panel size.

Do not write any values other than F0H (240) as the line number of X direction is fixed in 240.

Please be aware that the value range 1≦PSX≦240 can be written in, but the value other than 240 will not be operated normally because the writing restriction as the hard ware is MPSX=240 when PSX=0 or MPSX >240.

MPSY1

11H	D7	D6	D5	D4	D3	D2	D1	D0
Name	MPSY7	MPSY6	MPSY5	MPSY4	MPSY3	MPSY2	MPSY1	MPSY0
Default	1	0	0	1	0	0	0	0

MPSY2

12H	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	-	-	-	-	-	-	MPSY8
Default	0	0	0	0	0	0	0	1

MPSY[8:0]： Set the line number of the panel size for Y direction.

Set at 320≦MPSY[8:0]≦432

When MPSY[8:0]＜320, MPSX[8:0]=320 will be set.

When MPSY[8:0]＞432, MPSY[8:0]=432 will be set.

Line number of the Display depends on this setting.

WXMIN

13H	D7	D6	D5	D4	D3	D2	D1	D0
Name	WXMIN 7	WXMIN 6	WXMIN 5	WXMIN 4	WXMIN 3	WXMIN 2	WXMIN 1	WXMIN 0
Default	0	0	0	0	0	0	0	0

WXMIN[7:0]： Set the start point of X direction in Window mode.
Write with the condition of'0≦WXMIN[7:0]≦WXMAX[7:0]'.
The window access mode does NOT work in case of violating the above prerequisite.

WYMIN1

14H	D7	D6	D5	D4	D3	D2	D1	D0
Name	WYMIN 7	WYMIN 6	WYMIN 5	WYMIN 4	WYMIN 3	WYMIN 2	WYMIN 1	WYMIN 0
Default	0	0	0	0	0	0	0	0

WYMIN2

15H	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	-	-	-	-	-	-	WYMIN 8
Default	0	0	0	0	0	0	0	0

WYMIN[8:0]： Set the start point of Y direction in Window mode.
Write with the condition of'0≦WYMIN[8:0]≦WYMAX[8:0]'.
The window access mode does NOT work in case of violating the above prerequisite.

WXMAX

16H	D7	D6	D5	D4	D3	D2	D1	D0
Name	WXMA X7	WXMA X 6	WXMA X5	WXMA X4	WXMA X3	WXMA X2	WXMA X1	WXMA X0
Default	0	0	0	0	0	0	0	0

WXMAX[7:0]： Set the ending point of X direction in Window mode.
Write with the condition of' WXMIN[7:0]≦WXMAX[7:0]≦MSPX-1'.
The window access mode does NOT work in case of violating the above prerequisite.

WYMAX1

17H	D7	D6	D5	D4	D3	D2	D1	D0
Name	WYMAX 7	WYMAX 6	WYMAX 5	WYMAX 4	WYMAX 3	WYMAX 2	WYMAX 1	WYMAX 0
Default	0	0	0	0	0	0	0	0

WYMAX2

18H	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	-	-	-	-	-	-	WYMAX 8
Default	0	0	0	0	0	0	0	0

WYMAX [8:0]: Set the end point of Y direction in Window mode.
Write with the condition of WYMIN[8:0]≦WYMAX[8:0]≦MSPY[8:0]-1'.
The window access mode does NOT work in case of violating the above prerequisite.

※ WXMIN[7:0],WXMAX[7:0],WYMIN[8:0] and WYMAX[8:0] should be set satisfying the conditions below.
0≦WXMIN[7:0]≦WXMAX[7:0]≦MSPX[7:0]-1
0≦WYMIN[8:0]≦WYMAX[8:0]≦MSPY[8:0]-1
The window access mode does NOT work in case of violating the above prerequisite even though the window access mode registers below are set.

WAS

19H	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	-	-	-	-	-	-	WAS
Default	0	0	0	0	0	0	0	0

WAS：Operation setting of Window access mode.
'0'：Start the normal access mode
'1'：Start Window access mode

Conditions
0≦WXMIN[7:0]≦WXMAX[7:0]≦MSPX[7:0]-1
0≦WYMIN[8:0]≦WYMAX[8:0]≦MSPY[8:0]-1
If'1'is written in the register when the above prerequisites are not satisfied, that writing will be ignored and "0"will be read out.

XA

1AH	D7	D6	D5	D4	D3	D2	D1	D0
Name	XA7	XA6	XA5	XA4	XA3	XA2	XA1	XA0
Default	0	0	0	0	0	0	0	0

XA[7:0]：X address for RAM Writing and Reading
This register value will not be changed even if the data is written to RAM successively.
Only the internal pointer will be changed.

YA1

1BH	D7	D6	D5	D4	D3	D2	D1	D0
Name	YA7	YA6	YA5	YA4	YA3	YA2	YA1	YA0
Default	0	0	0	0	0	0	0	0

YA2

1CH	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	-	-	-	-	-	-	YA8
Default	0	0	0	0	0	0	0	0

YA[8:0]：RAM write Y address

Read/Write of the memory is possible by specifying arbitrary RAM address by XA [7:0] and YA [8:0] register. The address of RAM pointer is increased by Read/Write operation, but the initial set value will be read out when reading this register.

Note） In WINDOW access mode, the address origin of pointer is set as (WXMIN[7:0], WXMAX[8:0]).

Note）Setting constraints are different between in Normal mode and in Window access mode.

・In Normal mode,

Other than 0≦XA[7:0]≦MPSX[7:0]-1：if XA[7:0]>MPSX[7:0]-1 → XA[7:0]=0

Other than 0≦YA[8:0]≦MPSY[8:0]-1：if YA[8:0]>MPSY[8:0]-1 → YA[8:0]=0

・ In Window access mode,

Other than 0≦XA[7:0]≦(WXMAX[7:0]-WXMIN[7:0])：

if XA[7:0]>(WXMAX[7:0]-WXMIN[7:0]) → XA[7:0]=0

Other than 0≦YA[8:0]≦(WYMAX[8:0]-WYMIN[8:0])：

if XY[8:0]>(WYMAX[8:0]-WYMIN[8:0]) → XA[8:0]=0

RAMCTL

1DH	D7	D6	D5	D4	D3	D2	D1	D0
Name	SCANUD	-	-	-	-	ADX	ADY	INC
Default	0	0	0	0	0	0	0	0

SCANUD：Set the Read out direction of Memory scan (when transferring to the panel)

‘0’：Normal direction scan

‘1’：Memory reverse order scan

When reading out the display data, the data is read out from the end point of the memory executing the flip vertical display. It is not connected to writing.

ADX, ADY and INC are the registers which are available when writing the memory.

Refer to ‘8.2. Memory access order.

ADX：Increment setting of X address

‘0’：Increment of X address

‘1’：Decrement of X address

ADY：Increment setting of Y address

‘0’：Increment of Y address

‘1’：Decrement of Y address

INC：Increment（decrement）, specify X／Y direction

‘0’：X direction increment（decrement）

‘1’：Y direction increment（decrement）

TVGLN

1EH	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	TVGLN6	TVGLN5	TVGLN4	TVGLN3	TVGLN2	TVGLN1	TVGLN0
Default	0	1	0	1	0	0	0	0

TVGLN [6:0]: Set the vertical display line number

The setting value of this register affects the scan read out address of the memory and other signals like GCK1, GCK2, GOE and ASW [1:6].

Display line number can be set within the range of 320～432 lines.
Please set the value 0≦TVGLN[6:0]≦112(D) as the display line number＝320(D) when TVGLN[6:0]=0.

If TVGLN [6:0] =112(D), the display line number=432.
Display line number =320＋TVGLN[6:0]
When setting TVGLN[6:0]＞113(D), TVGLN be set to 112(D) automatically.

SSL1

20H	D7	D6	D5	D4	D3	D2	D1	D0
Name	SSL7	SSL6	SSL5	SSL4	SSL3	SSL2	SSL1	SSL0
Default	0	0	0	0	0	0	0	0

SSL2

21H	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	-	-	-	-	-	-	SSL8
Default	0	0	0	0	0	0	0	0

SSL [8:0]: Set the start line of the scroll area.
※ When writing 0 to this register, the scroll function is OFF.
Refer to the description of'10. Scroll of screen'.
0≦SSL[8:0]＜SEL[8:0]
The scroll operation will not be executed with the conditions other than above.

SEL1

22H	D7	D6	D5	D4	D3	D2	D1	D0
Name	SEL7	SEL6	SEL5	SEL4	SEL3	SEL2	SEL1	SEL0
Default	0	0	0	0	0	0	0	0

SEL2

23H	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	-	-	-	-	-	-	SEL8
Default	0	0	0	0	0	0	0	0

SEL [8:0]: Set the end line of the scroll area.
※ Refer to the description of'10. Scroll of screen'.
0≦SSL[8:0]＜SEL[8:0]≦MPSY[8:0]-1
0≦SST[8:0]＜SEL[8:0]－SSL[8:0]+1
The scroll operation will not be executed with the conditions other than above.

SST1

24H	D7	D6	D5	D4	D3	D2	D1	D0
Name	SST7	SST6	SST5	SST4	SST3	SST2	SST1	SST0
Default	0	0	0	0	0	0	0	0

SST2

25H	D7	D6	D5	D4	D3	D2	D1	D0
Name	SSTD	-	-	-	-	-	-	SST8
Default	0	0	0	0	0	0	0	0

SST[8:0]：Scroll step number setting
SSTD：Scroll direction setting
‘0’：Forward direction scroll
‘1’：Reverse direction scroll
※Refer to the description of‘10. Scroll of screen’.
0≦SST[8:0]＜SEL[8:0]－SSL[8:0]+1
The scroll operation will not be executed with the conditions other than above.

DSPCTL1

30H	D7	D6	D5	D4	D3	D2	D1	D0
Name	UD	INITON	MODE	-	PTLON1	PTLON0	-	DEN
Default	1	0	0	0	0	0	0	1

UD：Scan direction control
‘0’：Backward direction scan Output GUD=‘L’
‘1’：Forward direction scan Output GUD=‘H’

INITON：INIT signal control
‘0’： Output‘L’by INIT terminal
‘1’： Output‘H’by INIT terminal

MODE：Low power consumption mode setting
Some registers can be set two kinds of resister settings which are the normal mode and the low power consumption mode. (60H～67H and 70H～77H)
In Low power consumption mode, the registers operate with the register value related to the low power consumption(70H～77H). And in Normal mode, the registers operate with the register value related to Normal register value (60H～67H).
‘0’：Normal mode setting
‘1’：Low power consumption mode

D4： “0”Bit
“0” MUST be set at this bit.

PTLON[1:0]：Partial mode display setting
Refer to ‘9. Partial setting.

PTLON1	PTLON0	Partial mode
0	0	Normal Display
0	1	Partial Display, Display area A
1	0	Partial Display, Display area B
1	1	Partial Display, Display area and B

DEN：Select the output data.

This register selects if RAM data is displayed or White/Black monotone color is displayed in the effective display area.

“Non-display area” is set by‘DENCOL’register (ADR=33H bit1).

‘0’：Data display of Non display setting (RAM data is not displayed.)

‘1’：Output the display data of image memory（Default, normal operation）

VALGO

31H	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	-	-	-	-	-	-	VALGO
Default	0	0	0	0	0	0	0	0

VALGO：Vertical synchronizing control is the reflection of the register value.

The data will be written in the registers which have the VAL attributes (VA and Display). The register value will be reflected at next VSYNC timing after‘1’is written to this register concurrently and this VALGO register will return to ‘0' at the same time.

DSPCTL2

33H	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	-	-	-	-	-	DENCOL	-
Default	0	0	0	0	0	0	0	0

D2 : must set to 0

DENCOL：Set the non-display color when ‘DEN’（D0 of ADR=30H）＝‘0’.

‘0’：White (in Normal White), Black (in Normal Black)

‘1’：Black (in Normal White), White (in Normal Black)

Setting of DEN=0		NWB register	
DENCOL	VCOM output	0（Normal Black）	1（Normal White）
1	L (positive pole)	V0(Black) Display (L level)	
	H (negative pole)	V0(Black) Display (H level)	
0 (Default)	L (positive pole)	V63(White) Display (H level)	
	H (negative pole)	V63(White) Display (L level)	

TGCTL1

34H	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	FROFF	SSIGOFF	GSIGOFF	GOEOFF	DCKOFF	GCKOFF	COMOFF
Default	0	0	0	0	0	0	0	0

FROFF: FR signal output control

‘0’： Normal output mode

‘1’： Output OFF FR→“L”

SSIGOFF: Source output, control the source control terminal

‘0’： Normal output mode

‘1’： Output OFF SX[1:120] is Hi-Z, ASW[6:0] becomes‘L’.

GSIGOFF：Control of Gate control signal

‘0’： Normal output mode

‘1’： Gate control signals which become all‘L’.

Gate control signals are DCON1, DCON2, INIT, ASW [6:1], GUD and GSP.

GOEOFF：GOE signal control

‘0’：Normal output mode

‘1’：GOE becomes‘L’.

DCKOFF：DCK signal control
‘0’：Normal output mode
‘1’：DCK, DCKB, RCK1 and RCK2 are fixed to‘L’.
GCKOFF：GCK signal control
‘0’：Normal output mode
‘1’：GCK1and GCK2 become‘L’.
COMOFF: COM signal control
‘0’：Normal output mode
‘1’：VCOM becomes‘L’.

TGCTL2

35H	D7	D6	D5	D4	D3	D2	D1	D0
Name	DCKINV	RCKINV	GUDINV	SSWINV	GSPINV	GOEINV	FRINV	GCKIN
Default	0	0	0	0	0	0	0	0

DCKINV：This controls the inverse output of Signal DCK and DCKB for panels.
‘0’： Normal output of DCK and DCCKB
‘1’： Inverse output of DCK and DCCK

DCKINV：This controls the inverse output of Signal RCK1 and RCK2 for panels.
‘0’： Normal output of RCK1 and RCK2
‘1’： Inverse output of RCK1 and RCK2

GUDINV：GUD output inverse control
‘0’： Normal output mode
‘1’： GUD output inversion

SSWINV：Output inverse control of ASW[6:1]
‘0’：Normal output mode
‘1’：ASW[6:1] output inversion

GSPINV：GSP inverse control
‘0’：Normal output mode
‘1’：GSP output inversion

GOEINV：GOE inverse control
‘0’：Normal output mode
‘1’：GOE output inversion

FRINV： FR inverse control
‘0’：Normal output mode, it is in-phase as COM.
‘1’：FR output inversion, it is reversed phase as COM.

GCKINV：GCK1 and 2 inverse control
‘0’：Normal output mode
‘1’：GCK1/GCK2 inverse output

PTLAS1

36H	D7	D6	D5	D4	D3	D2	D1	D0
Name	PTLAS7	PTLAS6	PTLAS5	PTLAS4	PTLAS3	PTLAS2	PTLAS1	PTLAS0
Default	0	0	0	0	0	0	0	0

PTLAS2

37H	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	-	-	-	-	-	-	PTLAS8
Default	0	0	0	0	0	0	0	0

PTLAS [8:0]: Start line setting of the partial area.

PTLAE1

38H	D7	D6	D5	D4	D3	D2	D1	D0
Name	PTLAE7	PTLAE6	PTLAE5	PTLAE4	PTLAE3	PTLAE2	PTLAE1	PTLAE0
Default	0	0	0	0	0	0	0	0

PTLAE2

39H	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	-	-	-	-	-	-	PTLAE8
Default	0	0	0	0	0	0	0	0

PTLAE [8:0]: End line setting of the partial area.

PTLBS1

3AH	D7	D6	D5	D4	D3	D2	D1	D0
Name	PTLBS7	PTLBS6	PTLBS5	PTLBS4	PTLBS3	PTLBS2	PTLBS1	PTLBS0
Default	0	0	0	0	0	0	0	0

PTLBS2

3BH	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	-	-	-	-	-	-	PTLBS8
Default	0	0	0	0	0	0	0	0

PTLBS [8:0]: Start line setting of the partial B area.

PTLBE1

3CH	D7	D6	D5	D4	D3	D2	D1	D0
Name	PTLBE7	PTLBE6	PTLBE5	PTLBE4	PTLBE3	PTLBE2	PTLBE1	PTLBE0
Default	0	0	0	0	0	0	0	0

PTLBE2

3DH	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	-	-	-	-	-	-	PTLBE8
Default	0	0	0	0	0	0	0	0

PTLBE [8:0]: End line setting of the partial B area.

Partial area line setting should satisfy the conditions below.

$0 \leqq PTLAS[8:0] < PTLAE[8:0] \leqq MPSY[8:0]-1$
$0 \leqq PTLBS[8:0] < PTLBE[8:0] \leqq MPSY[8:0]-1$

About the two conditions above, it is necessary to satisfy the conditions below because of PTLON[1:0] (D3 and D2 of DSPCTL1(ADD=30H)).

0≦PTLAS[8:0]＜PTLAE[8:0]≦MPSY[8:0]-1 when PTLON[1:0]='01'
0≦PTLBS[8:0]＜PTLBE[8:0]≦MPSY[8:0]-1 when PTLON[1:0]='10'
Both 0≦PTLAS[8:0]＜PTLAE[8:0]≦MPSY[8:0]-1
and 0≦PTLBS[8:0]＜PTLBE[8:0]≦MPSY[8:0]-1 when PTLON[1:0]='11'

The Partial mode does not work if the conditions above are not satisfied.

SEQCTL

3EH	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	-	-	-	-	-	AUTOFF	AUTON
Default	0	0	0	0	0	0	0	0

This resister executes the power-related ON/OFF sequence automatically.

AUTOFF: Auto OFF sequence execution
Auto OFF sequence is executed by setting this register to '1'.
It returns to'0'automatically after the end of the sequence.

AUTON: Auto ON sequence execution
Auto ON sequence is executed by setting this register to '1'.
It returns to'0'automatically after the end of the sequence.

EXVSCTL

3FH	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	-	-	-	-	-	-	EXVSON
Default	0	0	0	0	0	0	0	0

EXVSON: VSYNC mode setting
This mode is driven by using the external VSYNC（VSYNC terminal）.

'0'：Internal VSYNC mode
This mode uses SYNC (VSYNC, HSYC) synchronizing signals generated from internal Clock.
'1'：External VSYNC mode
This mode uses the external VSYNC to be operated. HSYNC（Display）uses the internal signal to drive. If VSYNC period and the intervals of HSYNC are not matched, the treatment of Blanking or HSYNC (Display) are reset and displayed. The external VSYNC is taken priority rather than the internal signal.

TPARAM1

40H	D7	D6	D5	D4	D3	D2	D1	D0
Name	TVBK1LINE	TVBKGCK	TVBKGOE	TVBKCOM2	TVBKCOM1	TVBKCOM0	TVBKSX1	TVBKSX0
Default	0	0	0	0	0	0	0	0

This is the register which sets the treatment of Source and Gate control-related signal within the Blanking intervals.

TVBK1LINE：Output selection of 1 line before and after the valid line
This operates the same drive as the normal output (Source, Gate control signal and so on) as a driver.
'0'：Display Black (in Normal Black), output White.(in Normal White)
'1'：Display White (in Normal Black), output Black.(in Normal White)
Normal White and Normal Black are set by'NWB'register.

TVBKGCK： Output setting of GCK terminal (GCK1, GCK2) in Vertical Blanking period
'0'：Normal output
'1'：GCK becomes the level of GND.
GCK1,GCK2='L'after'valid line＋1H'.

※GCK1 and GCK2 execute Normal operation (based on TGCKST[3:0] register) after next VSYNC falling edge (Active).

TVBKGOE：Output setting of GOE in Vertical Blanking period
'0'：Normal output（Always'H'during operation）
'1'：GOE becomes the level of GND.
GOE='L' after valid line＋1H'.
※GOE becomes 'H'(valid） right after GSP is started up and additional delay of 2-clock.

TVBKCOM[2:0]：Output setting of COM in Vertical Blanking period

TVBKCOM2	TVBKCOM1	TVBKCOM0	Output of COM
0	0	0	Normal output（alternative per 1 line）
0	0	1	It is fixed at the polarity of the last line. （However there is an inversion per frame.）
0	1	0	2 H alternative
0	1	1	4 H alternative
1	0	0	8 H alternative
1	0	1	16 H alternative
1	1	0	32 H alternative
1	1	1	64 H alternative

※ The setting especially for the partial mode is operated in priority to this register setting for the partial mode.

TVBKSX[1:0]: This is the register to set Source(SX1～SX120) output in Vertical Blanking terms.

TVBKSX1	TVBKSX0	NWB	
		0 (Normal Black)	1 (Normal White)
0	0	Black output	White output
0	1	White output	Black output
1	0	Hi-Z	
1	1	Hi-Z	

TVFPSIZE

42H	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	TVFP6	TVFP5	TVFP4	TVFP3	TVFP2	TVFP1	TVFP0
Default	0	0	1	1	0	0	1	1

TVFP[6:0]：Setting the period of Vertical front porch (Setting by HSYNC)

The values of 1～127 are set as Vertical front porch.

When setting‘0’ and ‘1’, both of them operate as the front porch operation for 1 HSYNC by the function of TVBK1LINE which outputs 1 line before and after the valid line.

TVBPSIZE

43H	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	-	-	-	-	TVBP2	TVBP1	TVBP0
Default	0	0	0	0	0	0	0	1

TVBP[2:0]：Setting the period of Vertical back porch(Setting by HSYNC)

The values of 1～7 are set as Vertical back porch.

When setting‘0’and‘1’, both of them operate as the back porch operation for 1 HSYNC by the function of TVBK1LINE which outputs 1 line before and after the valid line.

THCNT

44H	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	-	THCNT5	THCNT4	THCNT3	THCNT2	THCNT1	THCNT0
Default	0	0	0	0	1	0	0	1

THCNT[5:0]：Setting of Horizontal scanning period（Setting by the internal clock）

THCNT[5:0]						Decimal	Horizontal scanning period
0	0	0	0	0	0	0	32-clock
0	0	0	0	0	1	1	33-clock
:	:	:	:	:	:	:	:
0	0	1	0	0	1	9	41-clock（default）
0	0	1	0	1	0	10	42-clock
:	:	:	:	:	:	:	:
1	1	1	1	1	0	62	94-clock
1	1	1	1	1	1	63	95-clock

0≦THCNT[5:0]≦63D(3FH) is used as the valid data.

Horizontal scanning period becomes 32-clock when setting‘0’to this register and setting is possible within the range from 32-clock to 95-clock (when setting 3FH=63D).

Horizontal scanning period = 32+Decimal(THCNT[5:0])

THCNT=63D (3FH) is set when writing THCNT>63D (3FH), and Horizontal scanning period becomes 95-clock.

TGSPWD

45H	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	-	-	TGSPST3	TGSPST2	TGSPST1	TGSPST0	TGSPWD
Default	0	0	0	0	0	0	1	0

TGSPST[3:0]：Specify GSP output starting position（Setting by the internal clock）
Specify within the range of 0～15-clock based on the first HSYNC from VSYNC.

TGSPST[3:0]				Decimal	GSP output starting position
0	0	0	0	0	0 clock (default)
0	0	0	1	1	1-clock
0	0	1	0	2	2-clock
0	0	1	1	3	3-clock
:	:	:	:	:	:
1	1	1	0	14	14-clock
1	1	1	1	15	15-clock

TGSPWD：Active width setting of GSP output（Setting by the internal clock）
‘0’：1 HSYNC period active
‘1’：2 HSYNC period active

TGCKST

46H	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	-	-	-	TGCKST3	TGCKST2	TGCKST1	TGCKST0
Default	0	0	0	0	0	1	0	1

TGCKST[3:0]：Specify 2-start position, GCK1 and GCK2
Specify the start position of GCK1 and GCK2 within the range of 0～15-clock based on HSYNC.

TGCKST[3:0]				Decimal	Start position of GCK1 and GCK2
0	0	0	0	0	1-clock
0	0	0	1	1	1-clock
0	0	1	0	2	2-clock
0	0	1	1	3	3-clock
0	1	0	0	4	4-clock
0	1	0	1	5	5-clock（Default）
:	:	:	:	:	:
1	1	1	0	14	14-clock
1	1	1	1	15	15-clock

TCOMST

48H	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	-	-	-	-	TCOMST2	TCOMST1	TCOMST0
Default	0	0	0	0	0	0	0	1

TCOMST[2:0]：Specify the position of VCOM output
Output position of VCOM is specified 0～7-clock based on HSYNC.

TSSWCTL1

4AH	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	-	-	FRCINV	THPCHCTL	TVBLKASW1	TVBLKASW0	SWDAREV
Default	0	0	0	0	0	0	0	0

FRCINV：Inversion control of FR output（Control based on VCOM）

‘0’：In-phase output as the same as VCOM

‘1’：Reversed phase output of VCOM

THPCHCTL: Horizontal pre-charge output setting

‘0’：Pre-charge OFF

ASW [1:6] =OFF (GND). This register follows Source output=THBKSX [1:0] (D2 and D1 of ADD=54H).

‘1’：Pre-charge ON

ASW [1:6] =ON (pulse output). This register follows Source output=TPCHLVL (D0 of ADD=54H).

TVBKASW[1:0]：Operation selection in Vertical Blanking period, ASW[1:6]

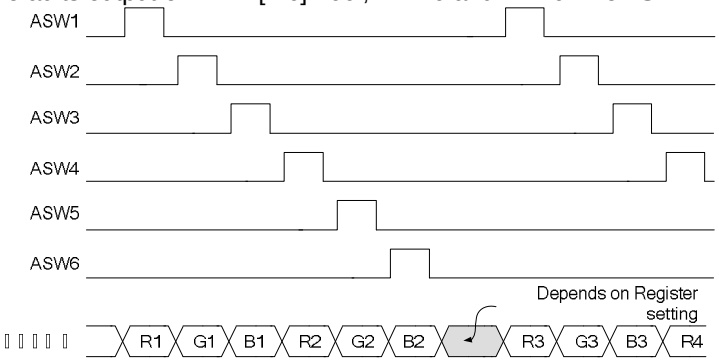
TVBKASW1	TVBKASW0	ASW[1:6] output
0	0	Normal output
0	1	Fixed to GND
1	X	ASW lump-sum ON

SWDAREV：Switching only the order of ASW[1:6] output and the source pixel output

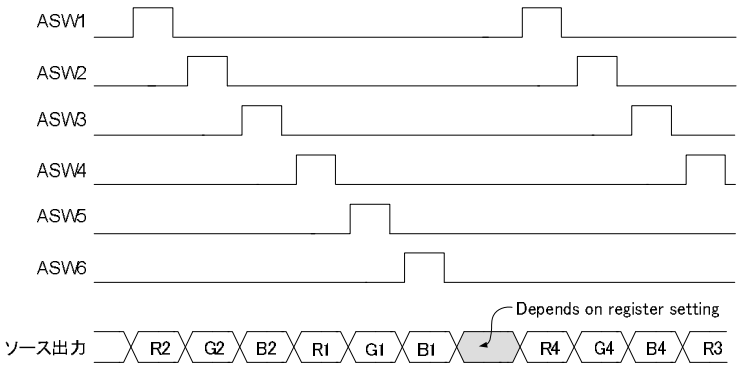
As the Fig. below, ASW [1:6] is outputted as the default setting and only Source output changes.

※ The order of ASW[1:6] is not affected.

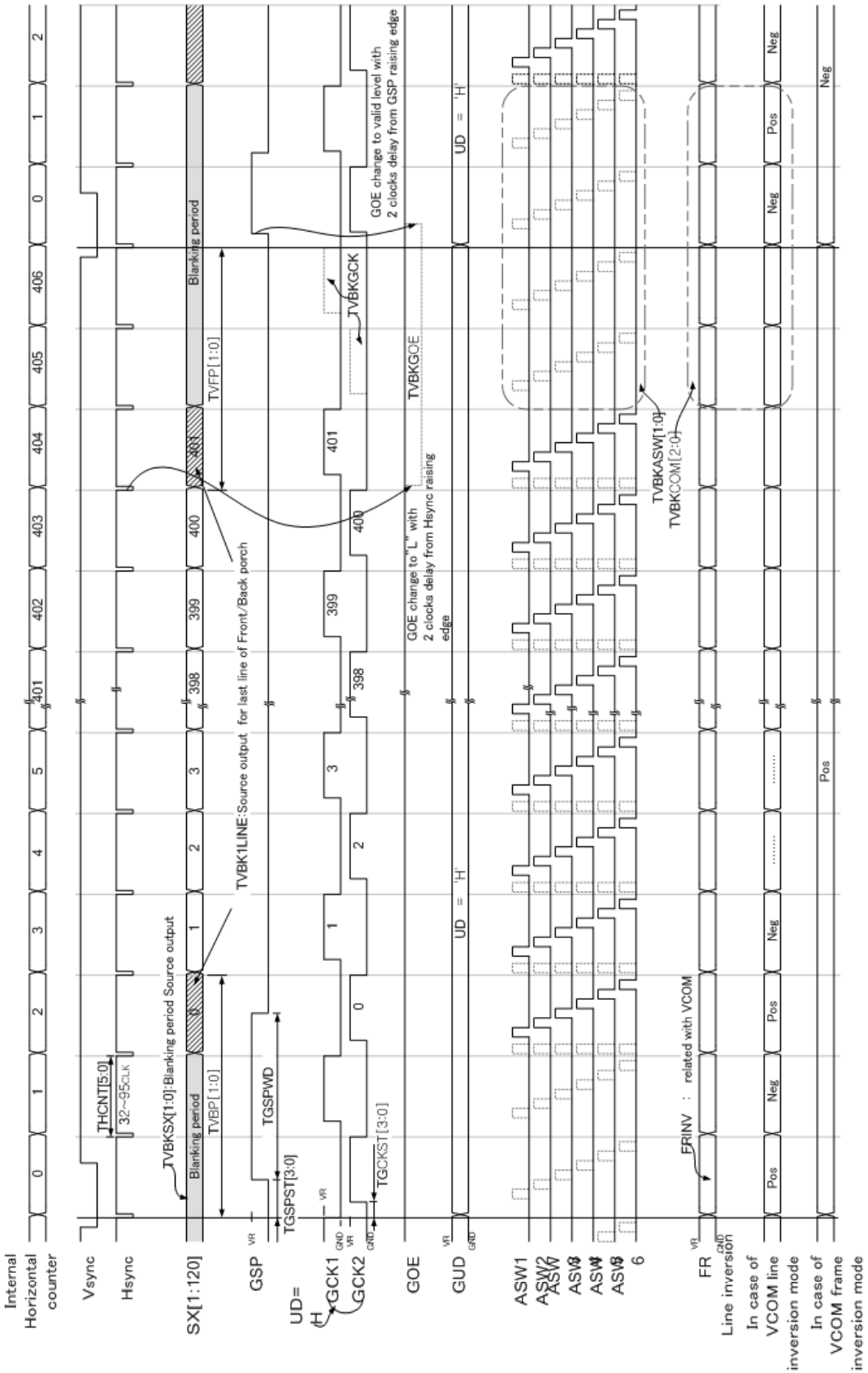
Examples of Defaults output of TYPE[1:0]=‘00’, PIX=0 and RB=0 when SWDAREV=0.



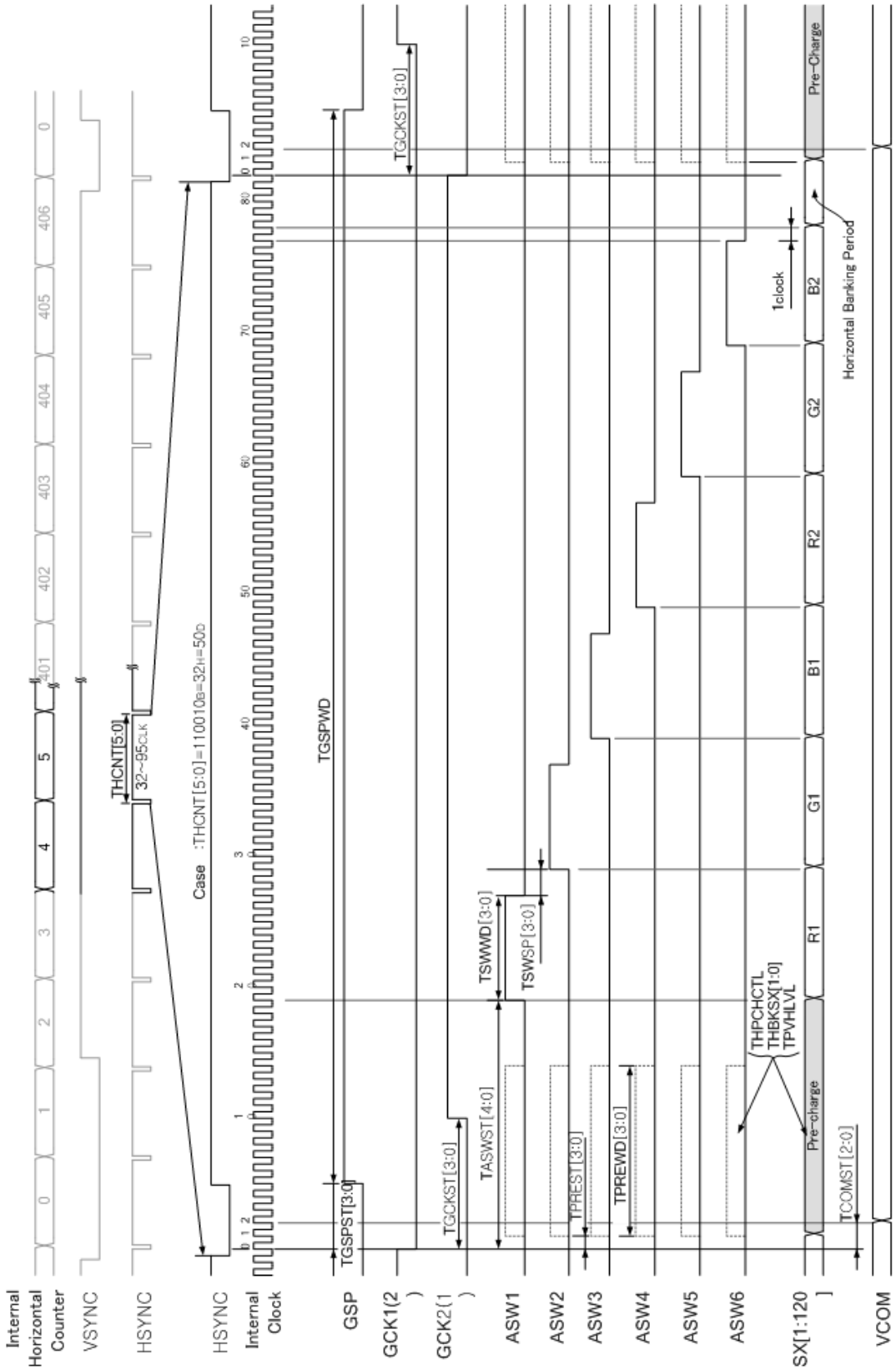
Examples of Defaults output of TYPE[1:0]=‘00’, PIX=0 and RB=0 when SWDAREV=1



※ The register which is related to Panel control timing (Normal Display). -- 1



※ The register which is related to Panel control timing (Normal Display). --- 2



TSSWCTL2

4BH	D7	D6	D5	D4	D3	D2	D1	D0
Name	TYPE1	TYPE0	RB	PIX	FREV1	FREV0	LREV1	LREV0
Default	0	0	0	0	0	0	0	0

Following registers are not the valid lines. They orders the switching based on VSYNC and HSYNC.
TYPE[1:0]：Set the output order of Source terminals, SX[1:120] and ASW[1:6] together.
RB：The function which rules the output order of Source terminals, SX[1:120] and ASW[1:6], to switch RED/BLUE.
This switches the order of RED and BLUE based on the source output order.
PIX：The function which sets the output order of Source terminals SX[1:120] and ASW[1:6] together.

PIX	RB	TYPE1	TYPE0	Output order of the source terminal SX[1:120] and ASW[1:6] → → → → → →					
0	0	0	0	R1	G1	B1	R2	G2	B2
				ASW1	ASW2	ASW3	ASW4	ASW5	ASW6
0	0	0	1	R1	R2	G1	G2	B1	B2
				ASW1	ASW4	ASW2	ASW5	ASW3	ASW6
0	0	1	0	R1	G1	B1	B2	G2	R2
				ASW1	ASW2	ASW3	ASW6	ASW5	ASW4
0	0	1	1	R1	B1	G2	R2	B2	G1
				ASW1	ASW3	ASW5	ASW4	ASW6	ASW2
0	1	0	0	B1	G1	R1	B2	G2	R2
				ASW3	ASW2	ASW1	ASW6	ASW5	ASW4
0	1	0	1	B1	B2	G1	G2	R1	R2
				ASW3	ASW6	ASW2	ASW5	ASW1	ASW4
0	1	1	0	B1	G1	R1	R2	G2	B2
				ASW3	ASW2	ASW1	ASW4	ASW5	ASW6
0	1	1	1	B1	R1	G2	B2	R2	G1
				ASW3	ASW1	ASW5	ASW6	ASW4	ASW2
1	0	0	0	R2	G2	B2	R1	G1	B1
				ASW4	ASW5	ASW6	ASW1	ASW2	ASW3
1	0	0	1	R2	R1	G2	G1	B2	B1
				ASW4	ASW1	ASW5	ASW2	ASW6	ASW3
1	0	1	0	R2	G2	B2	B1	G1	R1
				ASW4	ASW5	ASW6	ASW3	ASW2	ASW1
1	0	1	1	R2	B2	G1	R1	B1	G2
				ASW4	ASW6	ASW2	ASW1	ASW3	ASW5
1	1	0	0	B2	G2	R2	B1	G1	R1
				ASW6	ASW5	ASW4	ASW3	ASW2	ASW1
1	1	0	1	B2	B1	G2	G1	R2	R1
				ASW6	ASW3	ASW5	ASW2	ASW4	ASW1
1	1	1	0	B2	G2	R2	R1	G1	B1
				ASW6	ASW5	ASW4	ASW1	ASW2	ASW3
1	1	1	1	B2	R2	G1	B1	R1	G2
				ASW6	ASW4	ASW2	ASW3	ASW1	ASW5

FREV[1:0]：Set the output order of the source terminal SX[1:120] and ASW[1:6].
It is switched per frame.

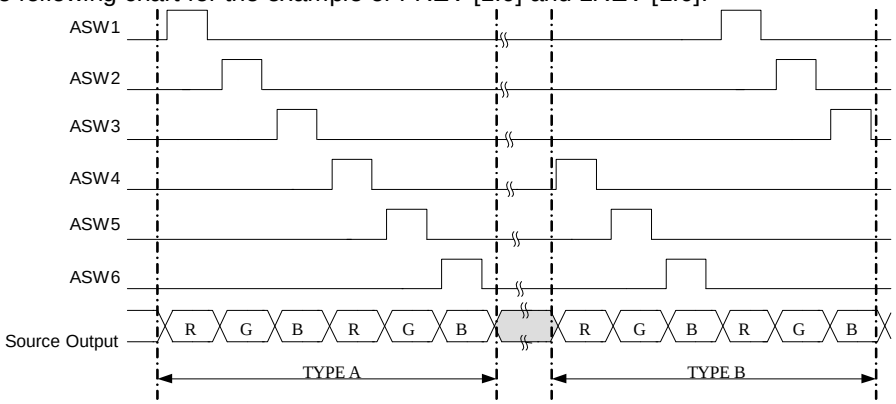
FREV1	FREV0	Source terminal SX [1:120] and ASW[1:6] order
0	X	No frame switch
1	0	Switch per frame
1	1	Switch every 2-frame

LREV[1:0]：This sets the output order of source terminals, SX[1:120] and ASW[1:6].
It will be switched per line.

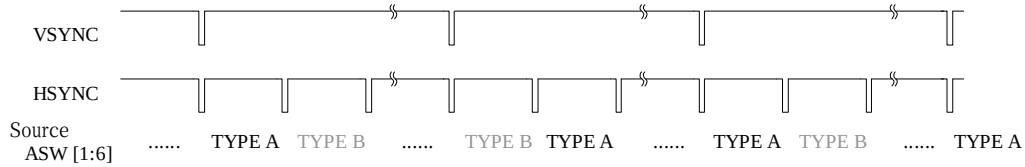
LREV 1	LREV 0	The order of Source terminals, SX [1:120] and ASW[1:6]
0	X	No line switching.
1	0	Switch per line.
1	1	Switch every 3-line.

Inversion will be executed per pixel for both the frame switching and line switching.

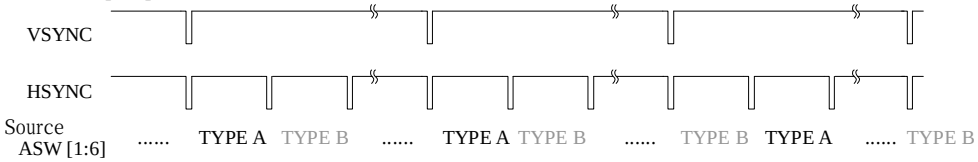
Refer to the following chart for the example of FREV [1:0] and LREV [1:0].



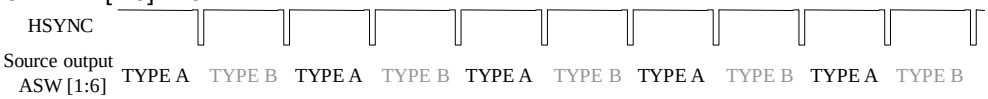
When FREV[1:0]='10'



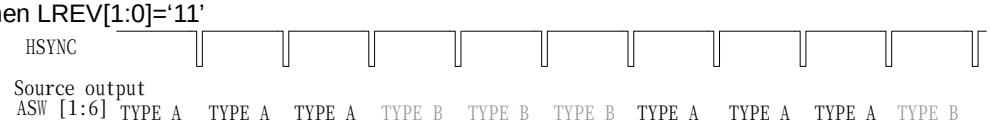
When FREV[1:0]='11'



When LREV[1:0]='10'



When LREV[1:0]='11'



TASWST

4CH	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	-	-	TASWST 4	TASWST 3	TASWST 2	TASWST 1	TASWST 0
Default	0	0	0	0	1	0	0	0

TASWST[4:0]：This specifies ASW[1:6] output starting and the source output starting position.
It can be specified from 1 to 31-clock.
※'1'will be operated when setting '0' or'1'.

TPCDCTL

4DH	D7	D6	D5	D4	D3	D2	D1	D0
Name	TPREST 3	TPREST 2	TPREST 1	TPREST 0	TPREW D3	TPREW D2	TPREW D1	TPREW D0
Default	0	0	0	0	0	0	0	1

TPREST[3:0]：This specifies the pre-charge starting position
It can be specified within 2～15-clock.
※ Either'0'or'1'does not be guaranteed.

TPREWD[3:0]：This specifies the pre-charge ASW pulse width
It can be specified within 1～15-clock
※'1'will be operated when setting '0' or'1'.

TPTLREF1

4FH	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	TPTLASW11	TPTLASW10	TVPTLCOM12	TVPTLCOM11	TVPTLCOM10	TPTLSX11	TPTLSX10
Default	0	0	0	0	0	0	0	0

There are 2 kinds of screens which are Normal screen and the partial mode screen.

It is possible to thin out the refresh frame and that rate can be selected when in the partial mode. (Refer to the register of 'TREF [2:0], TPNREF [3:0]'.)
There are three kinds of refresh control functions shown below per frame.

Display area at the refresh frame in the partial mode.
Non-Display area at the refresh frame in the partial mode.
'Display+ non-Display area at the non-refresh frame in the partial mode.

This is the register for each refresh frame control in the partial mode.
This defines the setting at the refresh frame in Non-Display area.

TPTLASW1[1:0]：This sets the operation of ASW[1:6] in the partial non-Display area at the refresh frame.

TPTLASW1[1]	TPTLASW1[0]	ASW[1:6] operation
0	0	Normal operation
0	1	Fix to GND
1	0	(*1)ASW lump-sum ON
1	1	Fix to High

(*1) Another control register will be applied for ASW lump-sum ON.

TVPTLCOM1[2:0]: This register controls COM operation at non-display area of refresh-frame

TVPTLCOM1[2:0]			COM operation
0	0	0	Normal(line inversion, default)
0	0	1	Last line polarity fix
0	1	0	2H inversion
0	1	1	4H inversion
1	0	0	8H inversion
1	0	1	16H inversion
1	1	0	32H inversion
1	1	1	64H inversion

TPTLSX[1:0]： This register sets Source output operation of Partial non-display area (the remaining area other than the display area and also one line which is right after the display area) at the refresh frame.

TPLSX1[1]	TPTLSX1[0]	Source output operation	
		NBW=0	NBW=1
0	0	Black	White
0	1	White	Black
1	X	Hi-z	

TPTLREF2

50H	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	-	-	-	-	-	TPTL1LINE	TPTLGOE
Default	0	0	0	0	0	0	0	0

This is the register for the refresh frame control in the partial mode.
Define the setting of non-Display area at the refresh frame.

TPTL1LINE：This is the setting register of the source output of the first line in non-Display area right after the Display area.

TPTL1LINE	NWB register	
	0 (Normal Black)	1 (Normal White)
0	Black output	White output
1	White output	Black output

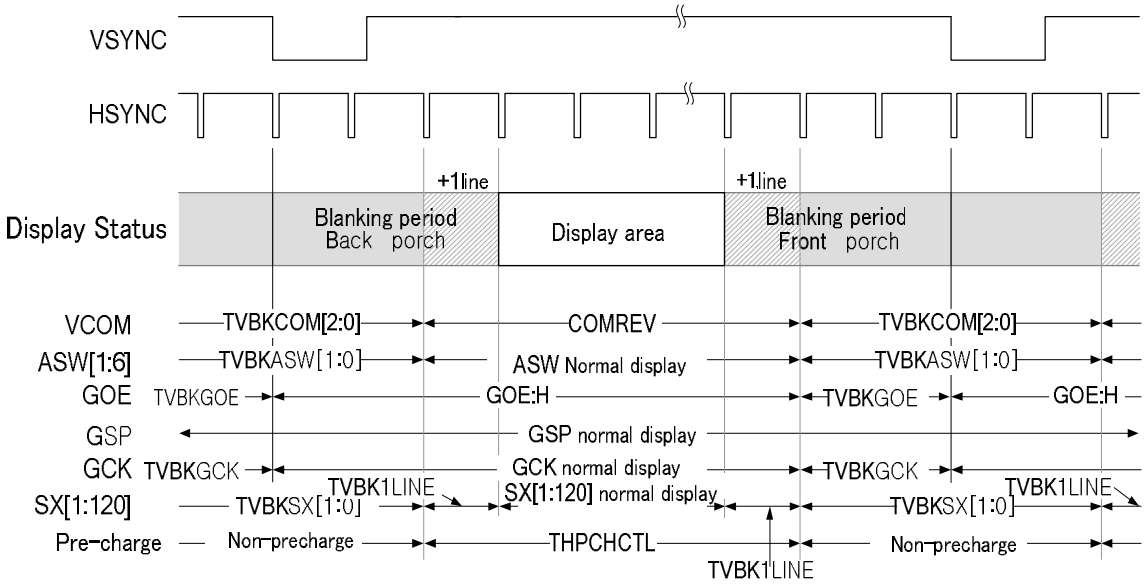
TPTLGOE：This sets GOE operation in the non-refresh frame display area except the first line right after the Display area.

‘0’： Fix GOE to H

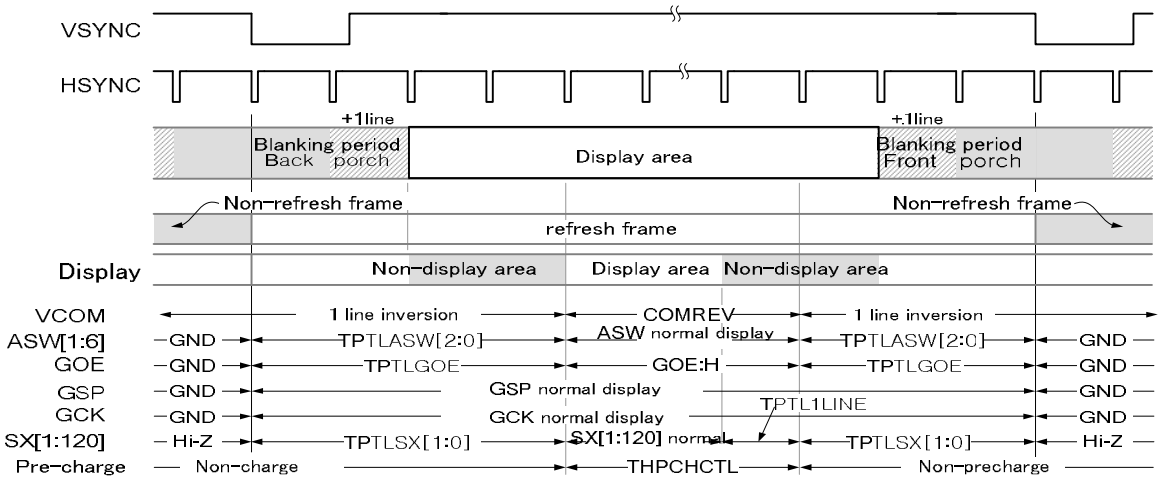
‘1’： Fix GOE to L

This register fixes to L after the second line in Non-Display area. The first line of non-Display area right after the Display area will execute Normal operation.

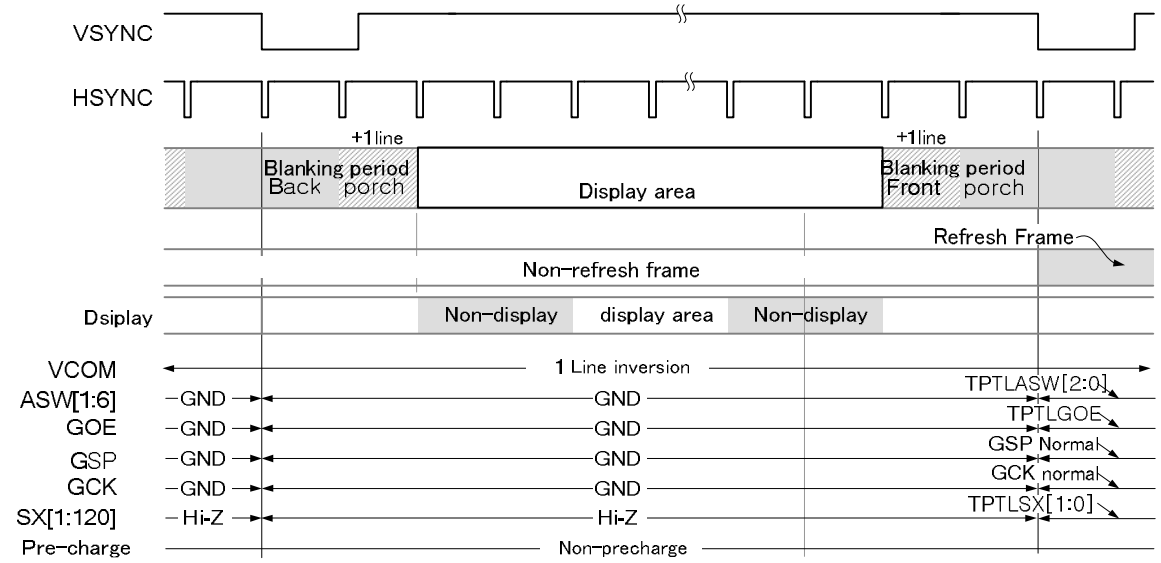
Control registers in Normal mode



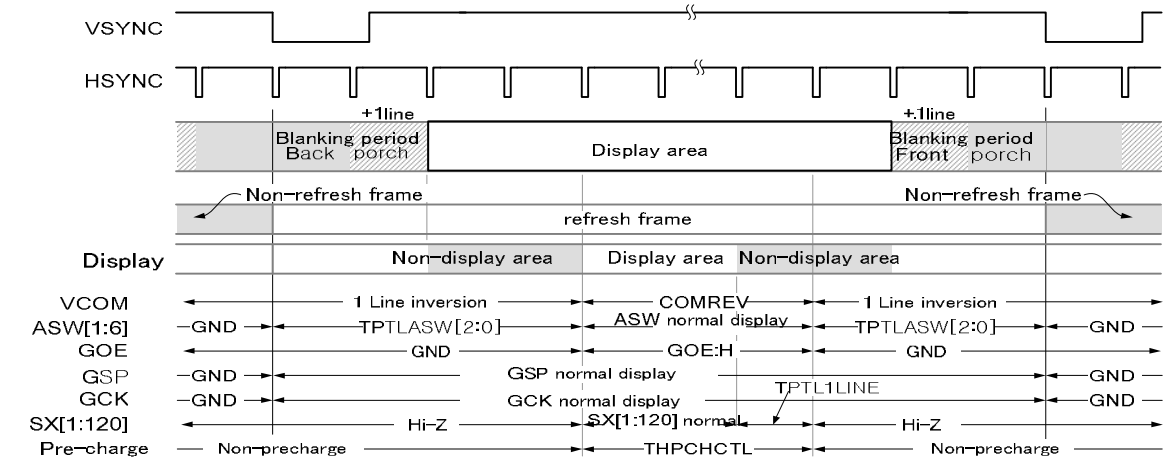
Partial mode 1 (Display/non-Display area at the refresh frame) in partial mode



Partial mode 2 (Display/non-Display area at the non-refresh frame) in partial mode



Partial mode 3 (Display area=Refresh non-Display area=non-refresh frame)



TVPTLCOM2

52H	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	-	-	TASWAST 4	TASWAST 3	TASWAST 2	TASWAST 1	TASWAST 0
Default	0	0	0	0	0	0	0	1

In Partial mode operation, this register controls COM operation at the non-display area of non-refresh frame.

TVPTLCOM2[2:0]			COM operation
0	0	0	Normal(line inversion, default)
0	0	1	Last line polarity fix
0	1	0	2H inversion
0	1	1	4H inversion
1	0	0	8H inversion
1	0	1	16H inversion
1	1	0	32H inversion
1	1	1	64H inversion

TASWAST

52H	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	-	-	TASWAST 4	TASWAST 3	TASWAST 2	TASWAST 1	TASWAST 0
Default	0	0	0	0	0	0	0	1

Operation controlled by this register will be executed in the partial non-Display area when specifying ASW lump-sum ON (when TPTLASW1[1:0]='10') in Horizontal Blanking period.

TASWAST[4:0]：Specify the start point when ASW lump-sum ON.
It can be specified within 0～31 clock.
※'1'will be operated when setting '0' or'1'.

TASWASX

53H	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	-	-	TASWASX	TASWAW D3	TASWAWD 2	TASWAWD 1	TASWAW D0
Default	0	0	0	0	0	0	0	1

Operation-related register of ASW simultaneously active in the partial non-Display area in Horizontal Blanking period.

TASWASX: Specify the source output when ASW simultaneously active.

TASWASX	NWB register	
	0 (Normal Black)	1 (Normal White)
0	Black output	White output
1	White output	Black output

TASWAWD [3:0]: These bits specify the pulse width of ASW [1:6] output when ASW simultaneously active.
It can be specified within 0～15 clock.
※'1'will be operated when setting '0' or'1'.

TPHPARAM

54H	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	-	-	-	-	THBKSX1	THBKSX0	TPCHLVL
Default	0	0	0	0	0	0	1	0

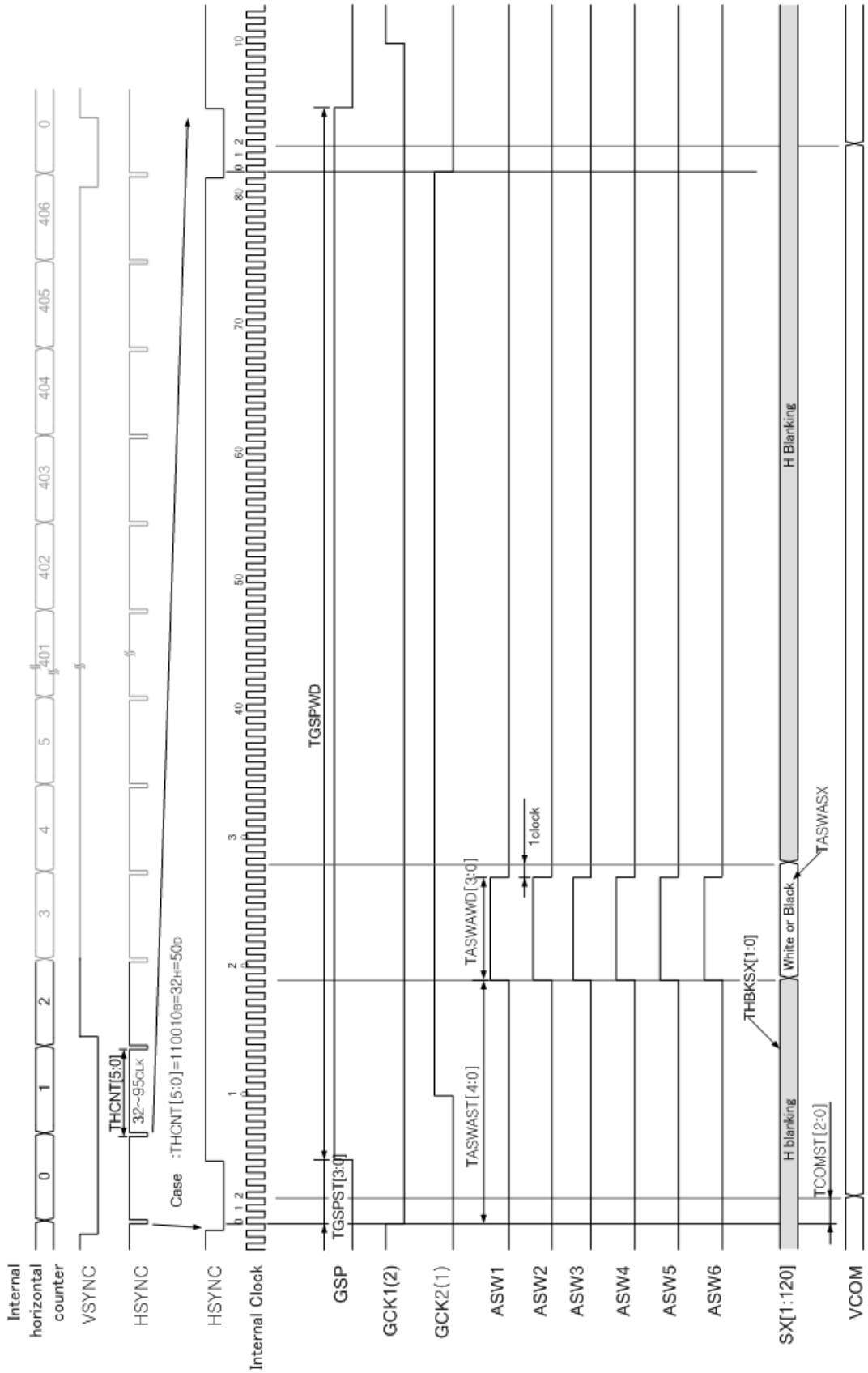
THBKSX [1:0]: Source output setting in Horizontal Blanking period

THBKSX[1]	THBKSX[0]	Source output	
		NWB=0	NWB=1
0	0	through（source last data output）	
0	1	Black output (default)	White output
1	0	White output	Black output
1	1	Hi-Z output	

TPCHLVL : Horizontal pre-charge level selection

TPCHLVL	NWB register	
	0 (Normal Black)	1 (Normal White)
0	Black output	White output
1	White output	Black output

※When Horizontal Blanking/in the partial non-Display area
Registers of the panel control timing and the relationship in ASW lump-sum ON operation



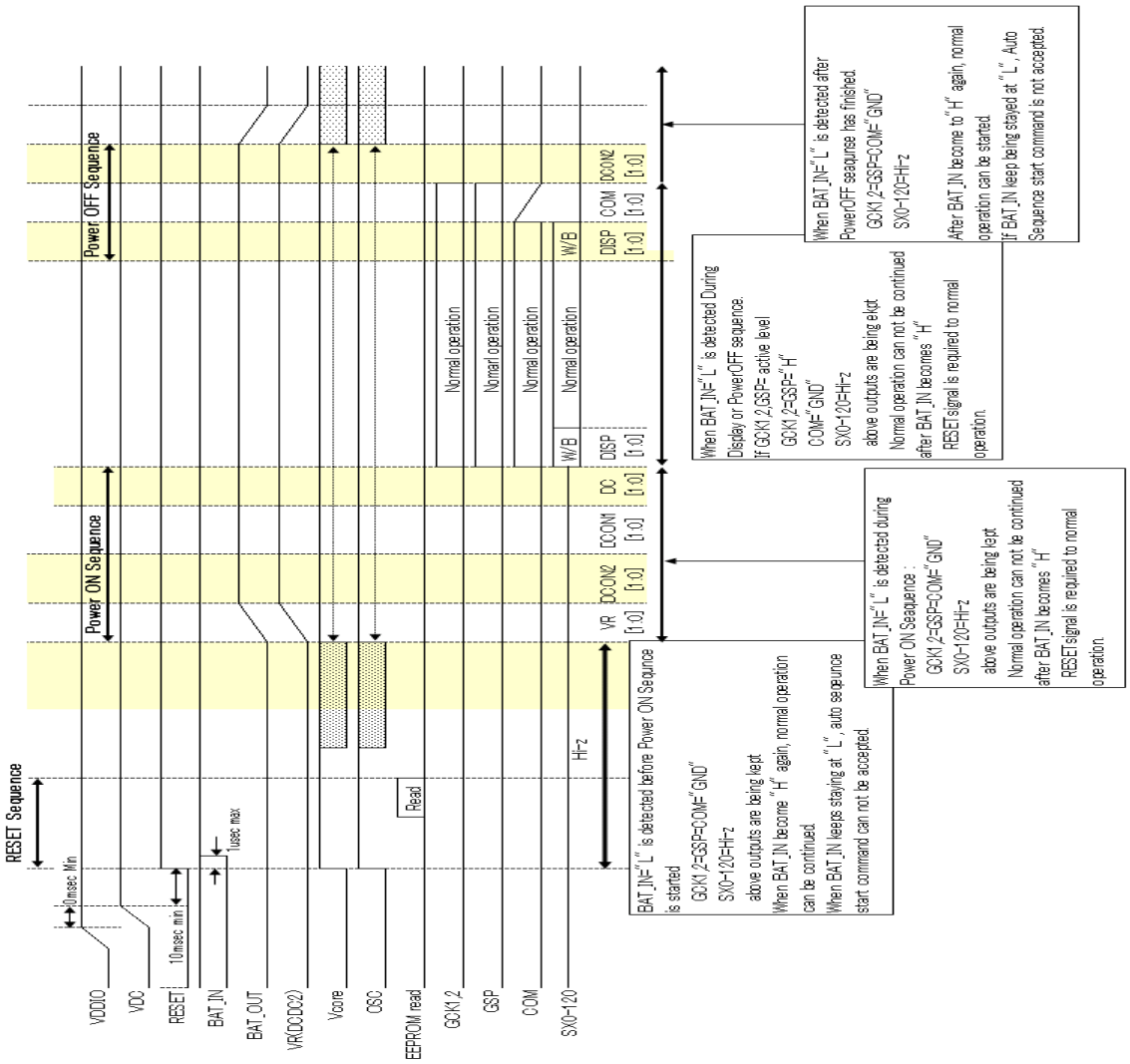
BATNZDET

5AH	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	-	-	-	-	-	BATNZDET1	BATNZDET0
Default	0	0	0	0	0	0	0	0

BATNZDET[1:0] : This register sets the valid cycle of the sample signal for Battery Detection. It samples the BATIN terminal by the clock to detect the signal if there is a battery and BATIN is considered as 'valid' if'L(valid)'is continued during the specified clock.

BATNZDET[1]	BATNZDET[0]	Source output
0	0	No Battery Detection function(Default)
0	1	Samples for 2-clock
1	0	Samples for 4-clock
1	1	Samples for 8-clock

Buttery detection will be operated as below by each timing.



MPWSTEP1

5BH	D7	D6	D5	D4	D3	D2	D1	D0
Name	MPSTP8	MPSTP7	MPSTP6	MPSTP5	MPSTP4	MPSTP3	MPSTP2	MPSTP1
Default	0	0	0	0	0	0	0	0

MPWSTEP2

5CH	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	-	-	-	-	-	MPSTP10	MPSTP9
Default	0	0	0	0	0	0	0	0

The same operation as the execution of Auto Sequence can be executed step by step by manual using this register. Each bit will operate as follows.

MPSTP1 = PSTVR [1:0] Manual Sequence start
MPSTP2 = PDC2ON [1:0]
MPSTP3 = PDC1ON [1:0]
MPSTP4 = PDCUP [1:0]
MPSTP5 = STDISP [1:0]
MPSTP6 = Normal Operation
MPSTP7 = EDDISP [1:0] Auto OFF Sequence start
MPSTP8 = EDCOM [1:0]
MPSTP9 = EDDCCON [1:0]
MPSTP10 = Standby

It is necessary to set one by one bit in order to take steps. And also'0'Write is necessary when finishing. Auto ON → display → Auto OFF are treated as one sequence. Therefore write order will be as follows.

Example) 00_0000_0001B → 00_0000_0011B → 00_0000_0111B → 00_0000_1111B → 00_0001_1111B → 00_0001_1111B →00_0011_1111B → 00_0111_1111B → 00_1111_1111B → 01_1111_1111B → 11_1111_1111B → 00_0000_0000B

MODE(D5) register of DSPCTL1 (ADR=30H) selects which register value is applied until TCOMDC1(69H) and TCOMDC2(79H) after this register.

MODE='0' (Normal mode) The register ADR=6XH is applied.
MODE='1' (Low power consumption mode) The register ADR=7XH is applied.

DRVCTL1 Selected by MODE(D5)register of DSPCTL1 (ADR=30H)

60H	D7	D6	D5	D4	D3	D2	D1	D0
Name	CHGSON	LPWRON	-	COMREV	-	-	-	-
Default	0	0	0	0	0	0	0	0

DRVCTL3

70H	D7	D6	D5	D4	D3	D2	D1	D0
Name	CHGSONL	LPWRONL	-	COMREV	-	-	-	-
Default	0	0	0	0	0	0	0	0

CHGSON : Charge share function ON/OFF setting
'0' : Charge share OFF
'1' : Charge share ON
When turning ON Charge share function, the register to set the timing of that Charge share will select Normal mode setting or Low consumption current mode setting(by MODE register of DSPCTL1) and executes Charge share function.

LPWRON : This sets the Low current drive mode (approx.75% (TBD)) related to the source and the gamma.
'0' : Low current drive OFF

'1'：Low current drive ON

COMREV：This sets the cycle of VCOM signal inversion
'0'：Line inversion
'1'：Frame inversion

DRVCTL2 Select by MODE(D5)register of DSPCTL1
（ADR=30H）

61H	D7	D6	D5	D4	D3	D2	D1	D0
Name	CHGSW D4	CHGSW D3	CHGSW D2	CHGSW D1	CHGSW D0	CHGSS T2	CHGSS T1	CHGSS T0
Default	0	0	0	0	0	0	0	0

DRVCTL4

71H	D7	D6	D5	D4	D3	D2	D1	D0
Name	CHGSW DL4	CHGSW DL3	CHGSW DL2	CHGSW DL1	CHGSW DL0	CHGSS TL2	CHGSS TL1	CHGSS TL0
Default	0	0	0	0	0	0	0	0

CHGSWD[4:0]：Charge share period setting
This sets the Charge share active period from 1 to 31 clocks.
※'1'will be operated when setting'0'or'1'.
CHGSST[2:0]：Charge share start setting
This sets Charge share starting position from 1 to 7 clocks.
※'1'will be operated when setting'0'or'1'.

TASW2 Selected by MODE(D5) register of DSPCTL1（ADR=30H）

62H	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	TSWWD 3	TSWWD 2	TSWWD 1	TSWWD 0	TSWSP 2	TSWSP 1	TSWSP 0
Default	0	0	0	0	0	0	0	0

TASW3

72H	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	TSWWD L3	TSWWD L2	TSWWD L1	TSWWD L0	TSWSP L2	TSWSP L1	TSWSP L0
Default	0	0	0	0	0	0	0	0

TSWWD[3:0]：This sets 'H' pulse width of ASW[1:6].
This Specifies from 1 to 15-clocks.
※In case of setting'0'or'1', it works as "1".

TSWSP[2:0]：This sets the pulse width of ASW[1:6].
This Specifies from 1 to 7-clocks.
※In case of setting'0'or'1', it works as "1".

TSDRVT1 Selected by MODE(D5) register of DSPCTL1
（ADR=30H）

63H	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	-	-	-	-	SDRVT2	SDRVT1	SDRVT0
Default	0	0	0	0	0	0	0	0

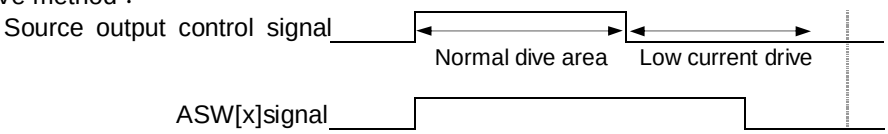
TSDRVT2

73H	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	-	-	-	-	SDRVTL2	SDRVTL1	SDRVTL0
Default	0	0	0	0	0	0	0	0

SDRVT[3:0] : This specifies Low current drive starting position of the source output.
This is available when the register of LPWRON (ADR=60H) is enable.
This specifies Normal drive area before switching to the Low current drive.

RDRVB2	RDRVB1	RDRVB0	Normal drive period
0	0	0	1-clock
0	0	1	1.5-clock
0	1	0	2-clock
0	1	1	2.5-clock
1	0	0	3-clock
1	0	1	3.5-clock
1	1	0	4-clock
1	1	1	4.5-clock

Drive method :



TREFCTL1 Selected by MODE(D5)register of DSPCTL1 (ADR=30H)

64H	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	PTLNDR3	PTLNDR2	PTLNDR1	PTLNDR0	PTLDR2	PTLDR1	PTLDR0
Default	0	0	0	0	0	0	0	0

TREFCTL2

74H	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	PTLNDRL3	PTLNDRL2	PTLNDRL1	PTLNDRL0	PTLDRL2	PTLDRL1	PTLDRL0
Default	0	0	0	0	0	0	0	0

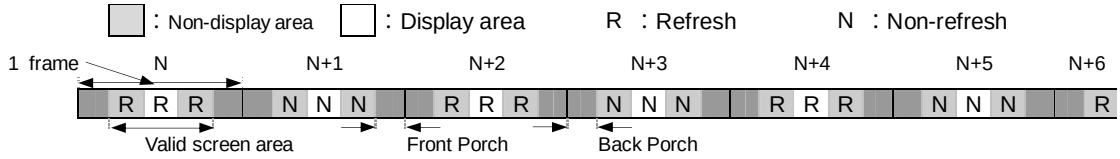
PTLNDR [3:0]: Partial non-Display area refreshes interval setting
This sets the cycle for the refresh frame in the display area not per VSYNC (per display color).

PTLNDR3	PTLNDR2	PTLNDR1	PTLNDR0	Refresh cycle
0	0	0	0	Refresh per frame
0	0	0	1	1/2 frame refresh
0	0	1	0	1/3 frame refresh
:	:	:	:	:
1	1	0	1	1/14 frame refresh
1	1	1	0	1/15 frame refresh
1	1	1	1	1/16 frame refresh

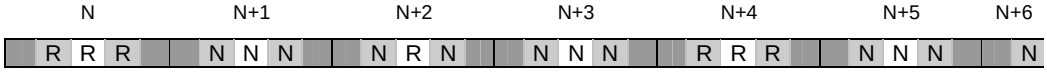
PTLDR [2:0]: Partial Display area refreshes interval setting

PTLDR2	PTLDR1	PTLDR0	Refresh cycle
0	0	0	Refresh per frame
0	0	1	Refresh every 2 frame
0	1	0	Refresh every 3 frame
:	:	:	:
1	0	1	Refresh every 6 frame
1	1	0	Refresh every 7 frame
1	1	1	Refresh every 8 frame

Example of ►PTLNDR[3:0]='0000B' @PTLDR[2:0]='001B'



Example of ►PTLNDR[3:0]='0001B' @PTLDR[2:0]='001B'



Example of ►PTLNDR[3:0]='0010B @PTLDR[2:0]='000B'

TBIAS1 Selected by MODE (D5) register of DSPCTL1 (ADR=30H)

65H	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	-	-	-	OBIAS3	OBIAS2	OBIAS1	OBIAS0
Default	0	0	0	0	0	0	1	0

TBIAS2

75H	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	-	-	-	OBIASL 3	OBIASL 2	OBIASL 1	OBIASL 0
Default	0	0	0	0	0	0	1	0

OBIAS [2:0]: This register sets the source output AMP and the bias current of gamma AMP.

OBIAS3	OBIAS2	OBIAS1	OBIAS0	AMP bias current
0	0	0	0	Minimum
0	0	0	1	:
0	0	1	0	: (default)
0	0	1	1	:
:	:	:	:	:
1	1	0	1	:
1	1	1	0	:
1	1	1	1	Maximum

VGMH1 Selected by MODE(D5) register of DSPCTL1 (ADR=30H)

66H	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	-	-	-	-	VGMH2	VGMH1	VGMH0
Default	0	0	0	0	0	0	0	0

VGMH2

76H	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	-	-	-	-	VGMHL2	VGMHL1	VGMHL0
Default	0	0	0	0	0	0	0	0

VGMH [2:0]: This sets the Gamma high voltage.

VGAMH2	VGAMH1	VGAMH0	Gamma AMP output voltage
0	0	0	4.6 V
0	0	1	4.7 V
0	1	0	4.8 V
0	1	1	4.9 V
1	0	0	5.0 V
1	0	1	5.1 V
1	1	0	5.2 V
1	1	1	5.3 V

VCOMH1

68H	D7	D6	D5	D4	D3	D2	D1	D0
Name	VCOMH7	VCOMH6	VCOMH5	VCOMH4	VCOMH3	VCOMH2	VCOMH1	VCOMH0
Default	0	0	0	0	0	1	1	1

VCOMH [7:0]: This sets VCOMH output voltage. This voltage will be used as the power supply to drive VCOM. Default value of this register is 07H. However the default value from built-in EEPROM is applied to the VCOMH circuit when in power sequence. But the register value is not changed.

Please set the 'EPDUSE' register to'0' using this register when adjusting VCOMH.

Setting range of this register is

07H≦VCOMH[7:0]≦B8H

And following conditions are set when setting other than above range.

VCOMH [7:0] =07H when VCOMH [7:0] < 07H

VCOMH [7:0] =B8H when VCOMH [7:0] > B8H

Output voltage of VCOMH is calculated by the following formula based on VGM as the standard voltage.

VCOMH output voltage=VGM*[0.500+0.004*(VCH-7))]

Refer to [12. VCOM output circuit] for more detail of output spec.

VCOML1

69H	D7	D6	D5	D4	D3	D2	D1	D0
Name	VCOML7	VCOML6	VCOML5	VCOML4	VCOML3	VCOML2	VCOML1	VCOML0
Default	0	0	0	0	0	1	1	1

VCOML [7:0]: This sets VCOML output voltage. This voltage will be used as the power supply to drive VCOM. Default value of this register is 07H. However the default value from built-in EEPROM is applied to the VCOML circuit when in power sequence. But the register value is not changed.

Please set the 'EPDUSE' register to'0' using this register when adjusting VCOML.

Setting range of this register is

07H≦VCOML[7:0]≦B8H

And following conditions are set when setting other than above range.

VCOML [7:0] =07H when VCOML [7:0] < 07H

VCOML [7:0] =B8H when VCOML [7:0] > B8H

Output voltage of VCOML is calculated by the following formula based on VGM as the standard voltage.

VCOML output voltage=VGM*[0.036+0.004*(VCL-7)]

Refer to [12. VCOM output circuit] for more detail of output spec.

COM_MODE

6AH	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	-	-	-	-	-	COM_MODE1	COM_MODE0
Default	-	-	-	-	-	-	0	0

This sets the output mode of VCOM.
Refer to [12. VCOM output circuit] for more detail of each mode.

COM_MODE1	COM_MODE0	VCOM output mode
0	0	Output mode 1-1
0	1	Output mode 1-2
1	0	Output mode 2
1	1	Output mode 3

CB

6BH	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	-	-	-	-	-	CB1	CB0
Default	-	-	-	-	-	-	1	0

This register is prepared for internal purpose.
DO NOT change the value.

POWCTL

80H	D7	D6	D5	D4	D3	D2	D1	D0
Name	V18M	ANAGOFF	VSR	VGMR	VCOMR	DCDC2	DCDC1	APWRS
Default	1	0	0	0	0	0	0	1

Other internal power supply circuits except the internal power supply regulator for 1.8V can be started up respectively regardless of Auto sequence. [When setting Do (APWRS) ='0']

V18M: This controls the internal power supply regulator for 1.8V.
"0"= Regulator OFF
"1"= Regulator ON
V18M is not controlled by Auto sequence.
Be sure to turn on it before Auto sequence is executed.
Note 1) When this register is turned OFF, it becomes the stand-by mode. Therefore set this bit to "1". All register accesses, except the stand-by release, are forbidden. The operation is not guaranteed if other bits are accessed during the stand-by mode.
Note 2) It takes 100 usec to stabilize the power supply until other registers can be accessed when releasing the stand-by mode by setting this bit.
Note 3) When recover from standby (V18 is OFF), previously it must be needed to reset.

ANAGOFF: This controls analog circuit.
"0"= analog circuit is ON
"1"= analog circuit is OFF

VSR: This controls Source power supply regulator (spare).
"0"= Source power supply regulator OFF
"1"= Source power supply regulator ON
This regulator is implemented as a spare circuit. It doesn't work. Please don't turn ON.

VGMR: This controls VGM Regulator control for Gamma
"0" = Regulator for Gamma is OFF.
"1" = Regulator for Gamma is ON.

VCOMR: This controls the regulators related to VCOM (VCOMH and VCOML).
"0"= VCOMH and VCOML Regulator OFF
"1"= VCOMH and VCOML Regulator ON

DCDC2: This controls DCDC2 (DC/DC converters for the power supply of Source and Gamma circuits).
"0"= Step-up circuit DCDC2 OFF
"1"= Step-up circuit DCDC2 ON

DCDC1: This controls DCDC1 (DCDC converters for the regulator power supply of VCOMH and VCOML)
"0"= Step-up circuit DCDC1 OFF
"1"= Step-up circuit DCDC1 ON

APWRS: This brings the power supply mode following AUTO POWER sequence under enable control.
"0"= this brings the power supply mode following AUTO sequence under Disable.
Setting of registers, VSR, VGMR, VCOMR, DCDC2 and DCDC1 become valid.
It is possible to control each power supply respectively.
"1"= this brings the power supply mode following AUTO sequence under Enable.
This register is controlled by the AUTO sequence control when setting '1'. Setting here does not influence the operation. Settings of Registers, VSR, VGMR, VCOMR, DCDC2 and DCDC1 become invalid.
※ Regulators for 1.8V are not controlled by Auto sequence. D7is not influenced by this D0.

DCCKS

81H	D7	D6	D5	D4	D3	D2	D1	D0
Name	—	DC2CK2	DC2CK1	DC2CK0	-	DC1CK2	DC1CK1	DC1CK0
Default	0	1	0	0	0	1	0	0

This sets the timing of making clocks for two Step-up circuits. Basically it operates using HSYNC as synchronous and generates Step-up clock using Starting-up of ASW and numbers of clocks.

DC2CK[2:0]：This sets the clock input of Step-up circuit DCDC2.
This operates Step-up based on HSYNC or ASW signal.

DC2CK2	DC2CK1	DC2CK0	Step-up clock frequency dividing rate
0	0	0	Starting-up@(per HSYNC and every 2 ASW)
0	0	1	Starting-up@(per HSYNC and every 3 ASW)
0	1	0	Starting-up@(per HSYNC and every 10-clock)
0	1	1	Starting-up@(per HSYNC and every 20-clock)
1	0	0	Starting-up@(per HSYNC)
1	0	1	Starting-up@(per 2HSYNC)
1	1	0	Starting-up@(per 3HSYNC)
1	1	1	Starting-up@(per 4HSYNC)

DC1CK[2:0]： This sets the clock input of Step-up circuit DCDC1.
This operates Step-up based on HSYNC or ASW signal.

DC1CK2	DC1CK1	DC1CK0	Step-up clock frequency dividing rate
0	0	0	Starting-up@(per HSYNC and every 2 ASW)
0	0	1	Starting-up@(per HSYNC and every 3 ASW)
0	1	0	Starting-up@(per HSYNC and every 10-clock)
0	1	1	Starting-up@(per HSYNC and every 20-clock)
1	0	0	Starting-up@(per HSYNC)
1	0	1	Starting-up@(per 2HSYNC)
1	1	0	Starting-up@(per 3HSYNC)
1	1	1	Starting-up@(per 4HSYNC)

PNLCKCTL

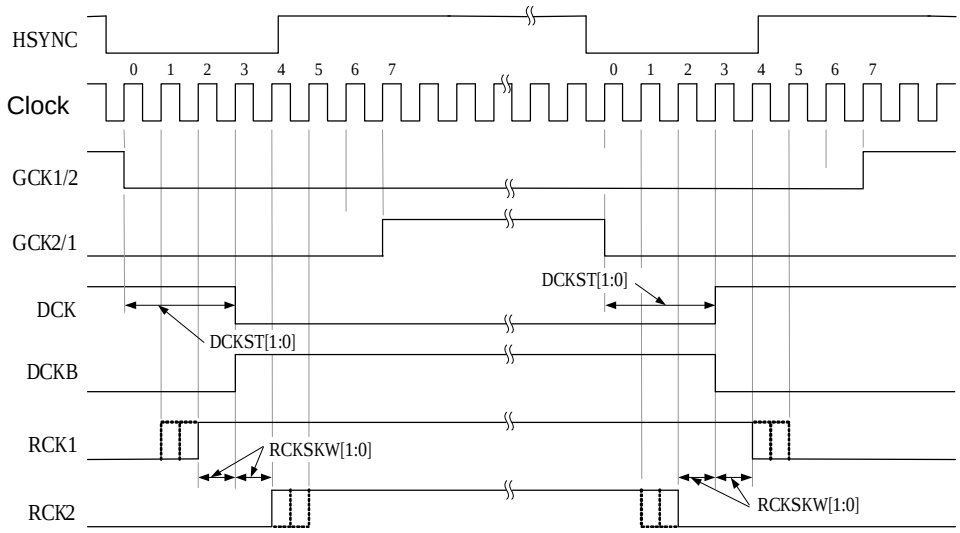
82H	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	-	DCKST1	DCKST0	RCKSKW1	RCKSKW0	DCKDIV1	DCKDIV0
Default	0	0	0	1	0	1	0	1

DCKST[1:0]：This sets the skew value of clock signals, DCK and DCKB, for panel.
The skew values set here are based on the HSYNC.

DCKST1	DCKST0	Skew value
0	0	2-clock
0	1	3-clock (Defaults)
1	0	4-clock
1	1	5-clock

RCKSKW[1:0]：This sets the skew value of clock signals, RCK1 and RCK2, for panel.
The skew values set here are based on the DCK (DCKB) and set RCK1 and RCK2.

RCKSKW1	RCKSKW0	Skew value
0	0	1.0-clock
0	1	1.5-clock
1	0	2.0-clock
1	1	prohibit

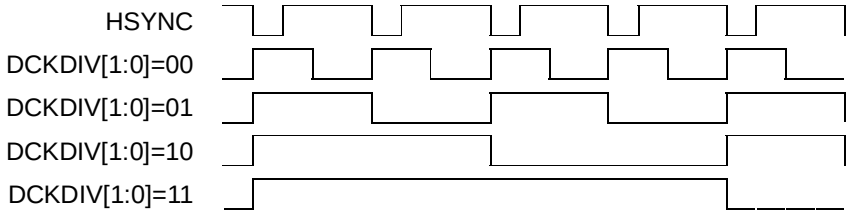


DCKDIV[1:0]：This sets DCK/DCKB frequency（based on internal HSYNC）.

DCKDIV1	DCKDIV0	DCK/DCKB frequency
0	0	1/2H width
0	1	1H width(defaults)
1	0	2H width
1	1	4H width

※If the clock during the term of HSYNC width is odd when DCKDIV[1:0] is‘00’, do division and round down to the nearest 1. HSYNC part operates synchronizing HSYNC.

1 cycle of DCK output（from starting-up to starting-up）is the width of 1HSYNC.
Refer to the figure in next page for setting and waveforms.



DC1CNT

83H	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	DC1MD1	DC1MD0	DC1DRV1	DC1DRV0	DC1OUT2	DC1OUT1	DC1OUT0
Default	0	0	1	1	1	1	0	0

DC1MD[1:0] : DCDC1 output ability setting

DC1MD1	DC1MD0	DCDC1 operation mode
0	0	X2 times step-up Single mode
0	1	X2 times step-up Dual mode
1	X	X3 times step-up

DC1DRV[1:0] : DCDC1 output ability setting

DC1DRV1	DC1DRV0	DCDC1 output ability
0	0	X1
0	1	X3
1	0	X2
1	1	X4

DC1OUT[2:0] : DCDC1 output voltage setting

DC1OUT2	DC1OUT1	DC1OUT0	DCDC1 output voltage
0	0	0	4.7V
0	0	1	4.8V
0	1	0	4.9V
0	1	1	5.0V
1	0	0	5.1V
1	0	1	5.2V
1	1	0	5.3V
1	1	1	5.4V

DC1SET

84H	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	-	-	RD1ON	DC1SET3	DC1SET2	DC1SET1	DC1SET0
Default	0	0	0	1	0	1	1	1

This register is for adjustment. Write in the designated value.
DC1SET[3:0] : DCDC1 clock timing setting
RD1ON：RDON timing setting

DC2CNT

85H	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	DC2MD1	DC2MD0	DC2DRV1	DC2DRV1	DC2OUT2	DC2OUT1	DC2OUT0
Default	0	0	1	0	0	0	0	0

DC2MD[1:0] : DCDC2 output ability setting

DC2MD1	DC2MD0	DCDC2 operation mode
0	0	X2 times step-up Single mode
0	1	X2 times step-up Dual mode
1	X	X3 times step-up

DC2DRV[1:0] : DCDC2 output ability setting

DC2DRV1	DC2DRV0	DCDC2 output ability
0	0	X1
0	1	X3
1	0	X2
1	1	X4

DC2OUT[2:0] : DCDC2 output voltage setting

DC2OUT2	DC2OUT1	DC2OUT0	DCDC2 output voltage
0	0	0	4.7V
0	0	1	4.8V
0	1	0	4.9V
0	1	1	5.0V
1	0	0	5.1V
1	0	1	5.2V
1	1	0	5.3V
1	1	1	5.4V

DC2SET

86H	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	-	-	RD2ON	DC2SET3	DC2SET2	DC2SET1	DC2SET0
Default	0	0	0	1	0	1	1	1

This register is for adjustment. Write in the designated value.

DC2SET[3:0] : DCDC2 clock timing setting

RD2ON : RDON timing setting

VPON1

90H	D7	D6	D5	D4	D3	D2	D1	D0
Name	PSTVR1	PSTVR0	PDC2ON1	PDC2ON0	PDC1ON1	PDC1ON0	PDCUP1	PDCUP0
Default	0	0	0	1	0	1	0	1

Parameter for Power ON sequence timing setting
Refer to “Power ON/OFF sequence” in next page for the timing set by each register.

PSTVR[1:0] : VR OUT Start-up waiting time setting

PSTVR1	PSTVR0	VR OUT Start-up waiting time
0	0	0.25 x Vsync(default)
0	1	0.5 x Vsync
1	0	0.75 x Vsync
1	1	1 x Vsync

PDC2ON[1:0] : Panel DCDC2 Start-up time setting

PDC2ON1	PDC2ON0	DCDC2 Start-up time
0	0	1 x Vsync
0	1	1.25 x Vsync(default)
1	0	1.5 x Vsync
1	1	1.75 x Vsync

PDC1ON[1:0] : Panel DCDC1 Start-up time setting

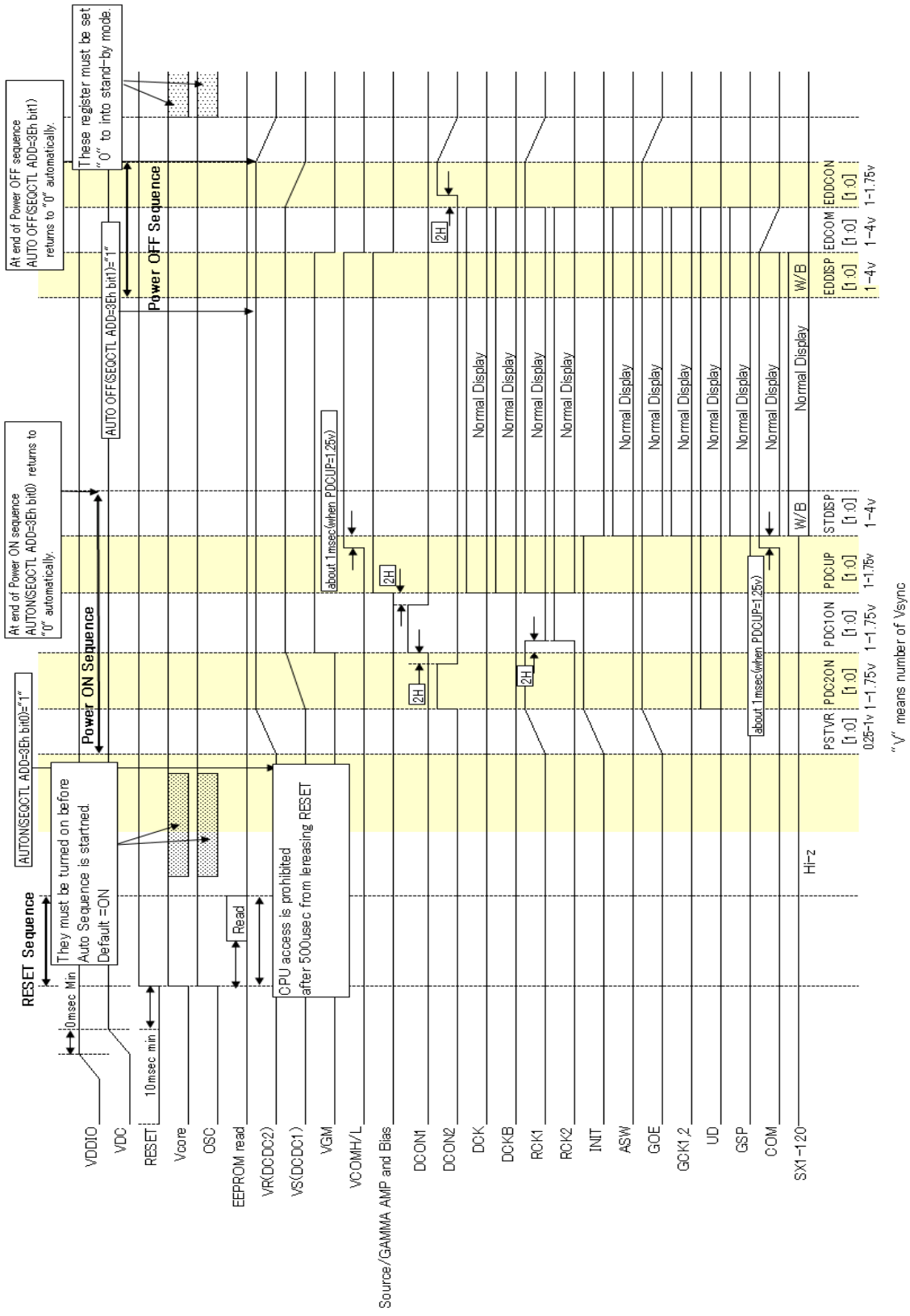
PDC1ON1	PDC1ON0	DCDC1 Start-up time
0	0	1 x Vsync
0	1	1.25 x Vsync(default)
1	0	1.5 x Vsync
1	1	1.75 x Vsync

PDCUP[1:0] : PANEL DCDC Start-up time

ST_DC1	ST_DC0	PANEL DCDC Start-up time
0	0	1 x Vsync
0	1	1.25 x Vsync(default)
1	0	1.5 x Vsync
1	1	1.75 x Vsync

By this register setting, a Start-up timing of VCOM is fixed.
In the Setting of 1.25v, a timing before 1ms is a start timing of VCOM.

Power ON/OFF sequence



VPON2

91H	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	-	-	-	-	SXDISP	STDISP1	STDISP0
Default	0	0	0	0	0	0	0	1

SXDISP : ON/OFF sequence Display data

SXDISP	NWB	
	0(Normal Black)	1(Normal White)
0	Black output	White output
1	White output	Black output

STDISP[1:0] : Display starting time

STDISP1	STDISP0	Display starting time
0	0	1 x Vsync
0	1	2 x Vsync
1	0	3 x Vsync
1	1	4 x Vsync

VPOFF1

92H	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	-	EDDCON 1	EDDCON 0	EDCOM1	EDCOM0	STDISP1	STDISP0
Default	0	0	0	1	0	1	0	1

Parameter for Power OFF sequence timing setting
Refer to "Power ON/OFF sequence" in previous page for the timing set by each register.

EDDCON[1:0] : Display down time

EDDCON1	EDDCON0	Display stop time
0	0	1 x Vsync
0	1	1.25 x Vsync
1	0	1.5 x Vsync
1	1	1.75 x Vsync

EDCOM[1:0] : COM down time

EDCOM1	EDCOM0	COM stop time
0	0	1 x Vsync
0	1	2 x Vsync
1	0	3 x Vsync
1	1	4 x Vsync

EDDISP[1:0] : Display stop time

EDDISP1	EDDISP0	Display stop time
0	0	1 x Vsync
0	1	2 x Vsync
1	0	3 x Vsync
1	1	4 x Vsync

ET1CTL

C0H	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	-	-	-	-	-	EPDUSE	ET1WR
Default	0	0	0	0	0	0	1	0

EPDUSE : Select data for VCOMH/L

"0" = Register data are used for VCOMH/L output voltage
"1"= EEPROM data are used for VCOMH/L output voltage

ET1WR : Write the built-in EEPROM for VCOM adjustment
"0" = Normal mode
"1"= Write EEPROM data
Writing the data is executed controlling the external PIN and following the Write sequence of EEPROM.

EPCOMH

D0H	D7	D6	D5	D4	D3	D2	D1	D0
Name	EPCOMH 7	EPCOMH 6	EPCOMH 5	EPCOMH 4	EPCOMH 3	EPCOMH 2	EPCOMH 1	EPCOMH 0
Default	-	-	-	-	-	-	-	-

EPCOMH[7:0] : VCOMH EEPROM data
EEPROM data for VCOMH can be read through this register.

EPCOML ADD=D1H

D1H	D7	D6	D5	D4	D3	D2	D1	D0
Name	EPCOML 7	EPCOML 6	EPCOML 5	EPCOML 4	EPCOML 3	EPCOML 2	EPCOML 1	EPCOML 0
Default	-	-	-	-	-	-	-	-

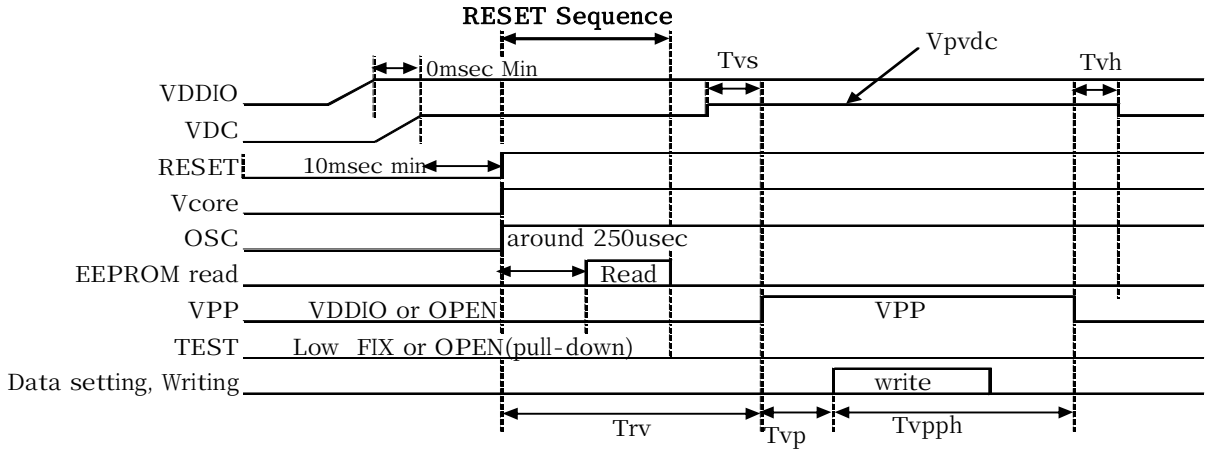
EPCOML[7:0] : VCOML EEPROM data
EEPROM data for VCOML can be read through this register.

※ACCESS Prohibition Register (MagnaChip Only)

ADR	D7	D6	D5	D4	D3	D2	D1	D0
C1H	-	-	-	-	E2PVCOMH3	E2PVCOMH2	E2PVCOMH1	E2PVCOMH0
C2H	-	-	-	-	E2PVCOML3	E2PVCOML2	E2PVCOML1	E2PVCOML0
C4H	-	-	-	-	-	-	MCREAD	MCERITE
C5H	-	-	-	-	-	UNDEFINE2	UNDEFINF1	UNDEFINE0
C6H	-	-	-	-	VREF3	VREF2	VREF1	VREF0
C7H	-	-	-	OSCCTRL4	OSCCTRL3	OSCCTRL2	OSCCTRL1	OSCCTRL0
C8H	-	-	-	-	-	-	-	REPAIRBA48
C9H	REPAIRBA47	REPAIRBA46	REPAIRBA45	REPAIRBA44	REPAIRBA43	REPAIRBA42	REPAIRBA41	REPAIRBA40
CAH	-	-	-	-	-	-	-	REPAIRBA38
CBH	REPAIRBA37	REPAIRBA36	REPAIRBA35	REPAIRBA34	REPAIRBA33	REPAIRBA32	REPAIRBA31	REPAIRBA30
CCH	-	-	-	-	-	-	-	REPAIRBA28
CDH	REPAIRBA27	REPAIRBA26	REPAIRBA25	REPAIRBA24	REPAIRBA23	REPAIRBA22	REPAIRBA21	REPAIRBA20
CEH	-	-	-	-	-	-	-	REPAIRBA18
CFH	REPAIRBA17	REPAIRBA16	REPAIRBA15	REPAIRBA14	REPAIRBA13	REPAIRBA12	REPAIRBA11	REPAIRBA10
D2H	-	-	-	-	-	E2PUNDEFINE2	E2PUNDEFINE1	E2PUNDEFINE0
D3H	-	-	-	-	E2PVREF3	E2PVREF2	E2PVREF1	E2PVREF0
D4H	-	-	-	E2POSCCTRL4	E2POSCCTRL3	E2POSCCTRL2	E2POSCCTRL1	E2POSCCTRL0
D5H	-	-	-	-	-	-	-	E2PREPAIRBA48
D6H	E2PREPAIRBA47	E2PREPAIRBA46	E2PREPAIRBA45	E2PREPAIRBA44	E2PREPAIRBA43	E2PREPAIRBA42	E2PREPAIRBA41	E2PREPAIRBA40
D7H	-	-	-	-	-	-	-	E2PREPAIRBA38
D8H	E2PREPAIRBA37	E2PREPAIRBA36	E2PREPAIRBA35	E2PREPAIRBA34	E2PREPAIRBA33	E2PREPAIRBA32	E2PREPAIRBA31	E2PREPAIRBA30
D9H	-	-	-	-	-	-	-	E2PREPAIRBA28
DAH	E2PREPAIRBA27	E2PREPAIRBA26	E2PREPAIRBA25	E2PREPAIRBA24	E2PREPAIRBA23	E2PREPAIRBA22	E2PREPAIRBA21	E2PREPAIRBA20
DBH	-	-	-	-	-	-	-	E2PREPAIRBA18
DCH	E2PREPAIRBA17	E2PREPAIRBA16	E2PREPAIRBA15	E2PREPAIRBA14	E2PREPAIRBA13	E2PREPAIRBA12	E2PREPAIRBA11	E2PREPAIRBA10
E1H	-	-	-	-	EADJH3	EADJH2	EADJH1	EADJH0
E2H	-	-	-	-	EADJL3	EADJL2	EADJL1	EADJL30

14. EEPROM Write Sequence

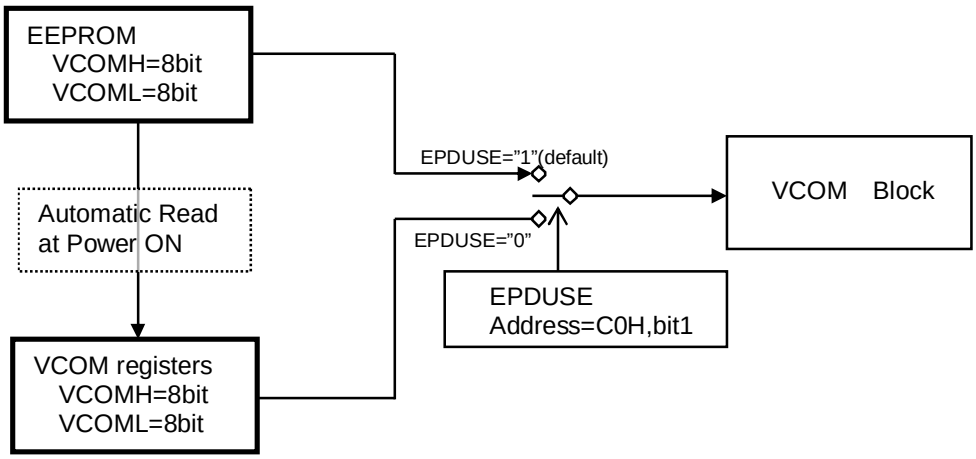
EEPROM Write Sequence for VCOM is as following.



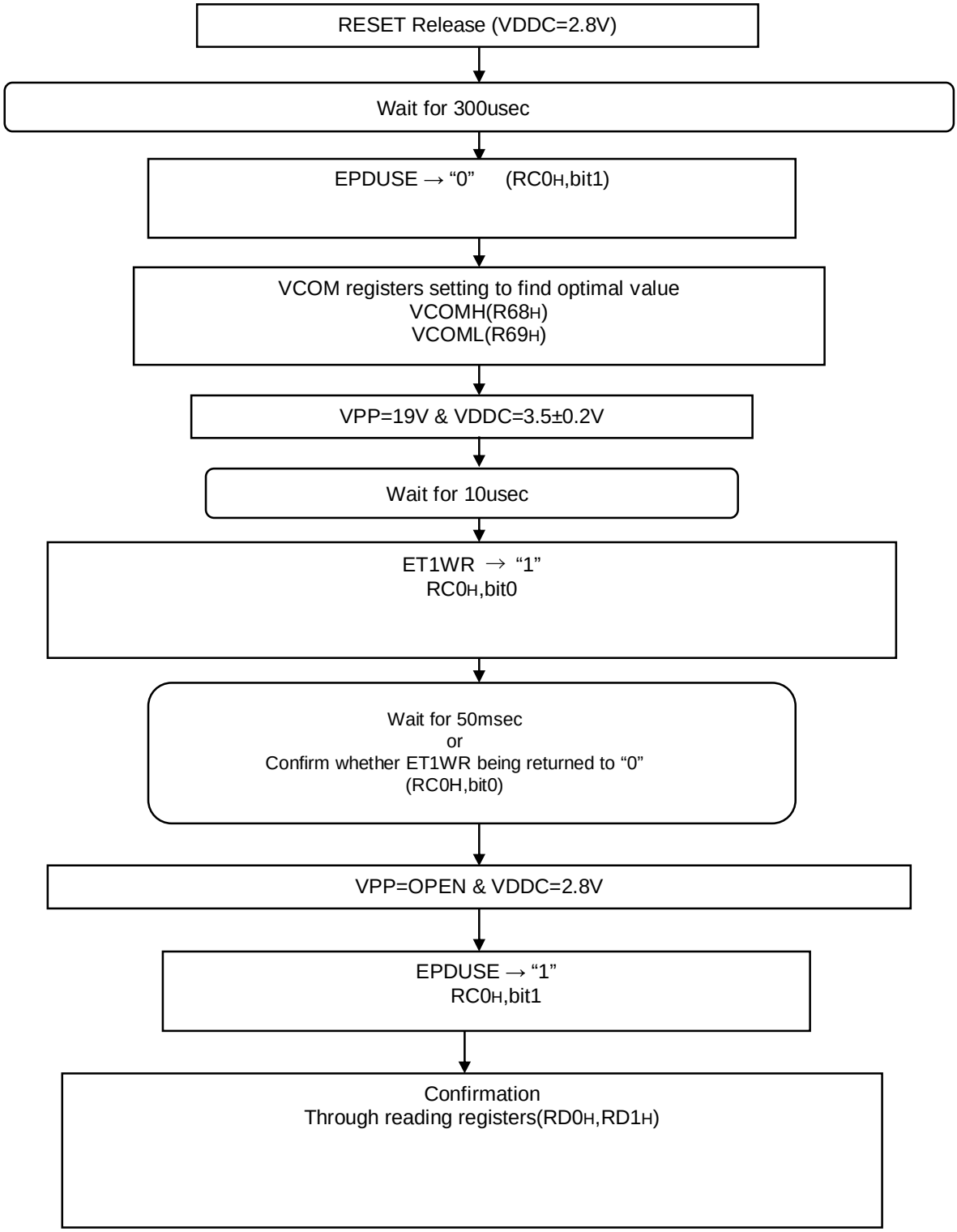
Item	Symbol	MIN	TYP	MAX	Unit
Vpp	Vvpp	19.6	19.7	19.8	V
Wait Time for VPP after Reset Release	Trv	300	-	-	Usec
Wait Time for Start Writing after VPP	Tvpw	10	-	-	Usec
Wait Time for Writing Completion (maintain Vpp)	Tvpph	40	50	60	msec
Vpp Voltage(Absolute Max)	Vvppm	-	-	20.0	V
VDC vs. VPP SetupTime(note)	Tvs	-10	-	10	Usec
VDC vs. VPP HoldTime(note)	Tvh	-10	-	10	Usec
VDC when Writing	Vpvdc	3.3	3.5	3.7	V
Guaranteed Writing times	Twite	10	-	-	times

(Note) It is needed to set VDC as 3.5V(±0.2V) simultaneously with VPP forcing.
Although ±10μsec is written in the table, recommendation is the same time.
For your information, there are other settings than VCOM, but those are only for usage of MagnaChip.

EEPROM Block diagram



EEPROM Write Flow Chart



15.ELECTRICAL CHARACTRISTICS

15.1. Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Power Supply Voltage	VDDC	-0.5～+6.0	V
Input Voltage 1 (except VPP,VDDCORE)	VIN	-0.5～VDDIO+0.5	V
Input Voltage 2 (apply to VPP)	VIN	-0.5～20.0	V
Input Voltage 3 (apply to VDDCORE)	VIN	-0.5～2.2	V
Input current	IIN	±10	mA
Output current	IOUT	±10	mA
Operation Ambient temperature	Ta	-30 ～85	℃
Storage Temperature	Tstg	-50 ～125	℃

GNDD=GNDA=GNDDC＝０Ｖ，ＶＤＤＣ≧ＶＤＤＩＯ

Caution: Product quality may be suffered if the absolute maximum rating exceeds the specified value even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

15.2. Recommended Operating Conditions (GNDD=GNDA=GNDDC=0V)

Parameter		Symbol	Terminals	MIN	TYP	MAX	Unit	Note
Power Supply	Logic(I/O)	Vddio	VDDIO	1.6	1.8	3.4	V	
	Logic(core)	Vddcore	VDDCORE	1.7	1.8	1.9	V	
	Analog	Vdc	VDDC	2.7	3.0	3.4	V	
Operating ambient temperature		Ta		-30		+85	℃	

15.3. DC Electrical Characteristics Conditions

15.3.1. Input/Output pin Characteristic

(VDDIO = 1.6 ～ 3.4V、VDDC = 2.7～ 3.4V、Ta = -30～ 85℃)

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit	Note
High Level Input voltage	VIH	VDDIO	0.8*VDDI			V	
Low Level Input voltage	VIL	VDDIO			0.8*VDDIO	V	
Output H voltage 1	VOH1	VDDIO output	0.8*VDDDI	-	-	V	1
Output L voltage 1	VOL1	VDDIO output	-	-	0.2*VDDDIO	V	1
Output H voltage 2	VOH2	Panel Control signals	0.8*VS	-	-	V	2
Output L voltage 2	VOL2		-	-	0.2*VS	V	2
Input Pin Leakage Current	IIL	VDDIO	-1		1	uA	
VCOM Output Voltage 1	Vcom 1	IOH=-3mA,VCOM=4.8V	4.7	4.8	4.85V	V	
VCOM Output Voltage 2	Vcom2	IOL= 3mA,VCOM=0.3V	0.25	0.3	0.4V	V	

Note 1） VDDIO output DB17-DB0,VSYNCO,ECK,ECS,EDO
Note 2） Panel Control signals
GSP,GCK1,GCK2,GOE,INIT,ASW1～6,FR,RCK1,RCK2,DCON1,DCON2

15.3.2. Source Drive Output

(VCC = 1.6 ～ 3.4V、VDC = 2.7～ 3.4V、Ta = -30～ 85℃)

Parameter	Symbol	Conditions		MIN	TYP	MAX	Unit	Note
Output Voltage Range	VSX	VGM=4.6～5.3V		0.2		VS-0.2	V	1
Voltage Variation (absolute value)	VDEF(1)	0～64 gray output VDEF(1)=Pos - target VDEF(1)=Neg - target	Gray1～43	-15		15	mV	1
			Gray44～54	-20		20		
			Gray55～64	-25		25		
Voltage Variation (amplitude)	VDEF(2)	0～64 gray output amplitude =Pos-Neg VDEF(2)= amplitude - average of all pins	Gray1～43	-8		8	mV	1
			Gray44～54	-10		10		
			Gray55～64	-13		13		
pin-to-pin variation	VDEF(3)	0～64 gray output amplitude=Pos-Neg VDEF3=difference amplitude between next pins	Gray1～43	-15		15	mV	1
			Gray44～54	-20		20		
			Gray55～64	-30		30		

Note1：SX1～SX120、source output Load R=5kΩ / C=30pF

15.3.3. Power circuits

（VDDIO = 1.6 ～ 3.4V、VDDC = 2.7～ 3.4V、Ta = -30～ 85℃）

Parameters	Symbol	Pins	MIN	TYP	MAX	Unit	Note
VS Output Voltage	VS	Io=-2mA VDDC=2.7～3.3V VS target=5.1V	5.0	5.1	5.2	V	1
VR Output Voltage	VR	Io=-2mA VDD=2.7～3.3V VR target=5.1V	5.0	5.1	5.2	V	1
VGM output Range	VGM(1)	VS=4.7～5.4V			VS-0.2	V	2
VGM output Voltage	VGM(2)	Io= 0.1mA VGM target=4.8V	4.75	4.8	4.85	V	2
VCOMH output range	VCOMH(1)	VR=4.7～5.4V VGM=4.8V	2.5	-	VR-0.2	V	2
VCOMH voltage	VCOMH(2)	Io= 0.1mA VCOMH target 4.8V	4.75	4.8	4.85	V	2
VCOML Output range	VCOML(1)	VR=4.7～5.4V	0.2	-	3.6	V	2
VCOML output voltage	VCOML(2)	Io= 0.1mA VCOML target=0.3V	0.25	0.3	0.35	V	2

注1：DC-DC Output voltage
注2：Voltage regulator output

15.3.4. Power Consumption

(VDDIO = 1.6 ~ 3.4V、VDDC = 2.7~ 3.4V、Ta = 25℃)

Parameters	Symbols	Pins	Conditions	MIN	TYP	MAX	Unit	Note
Operating current(1)	IDDop1io	VDDIO	VDDC=VDDIO=3V、Fosc=1.15Hz、60Hz Line Inversion Non-RAM access Check Pattern		1		uA	1
	IDDop1vdc	VDDC			5.5		uA	
Operating current(2)	IDDop2io	VDDIO	VDDC=VDDIO=3.0V、Fosc=1.15Hz、60Hz RAM Access 10MHz Check Pattern		350		uA	
	IDDop2vdc	VDDC			6		mA	
Stand-by current	IDDstio	VDDIO	DC/DC、OSC OFF 1.8V stand-by Regulator ON		1	10	uA	
	IDDstvdc	VDDC			10	25	uA	

Standby Out recommended sequence

Register	Data	Comment
80h	81h	Deep standby Out
wait 10us		
80h	01h	Deep standby In
wait 10us		
80h	81h	Deep standby Out
wait 10us		
80h	01h	Deep standby In
wait 10us		
Hardware RESET		Low pulse width = 10msec
wait 1msec		
Initial setting		write all register

15.3.5. Oscillator

(VDDIO = 1.6 ~ 3.4V、VDDC = 2.7~ 3.4V、Ta = -30~ 85℃)

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit	Note
Frequency	OSC	VDDIO=1.6~3.4V VDDC=2.7~3.4V	-8%	1.15	+8%	MHz	

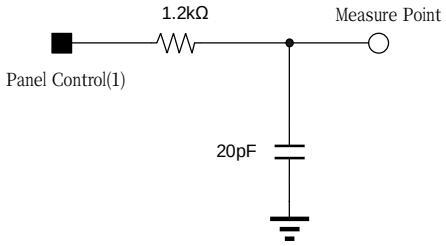
15.4. AC Electrical Characteristics Conditions

15.4.1. Level Shifter

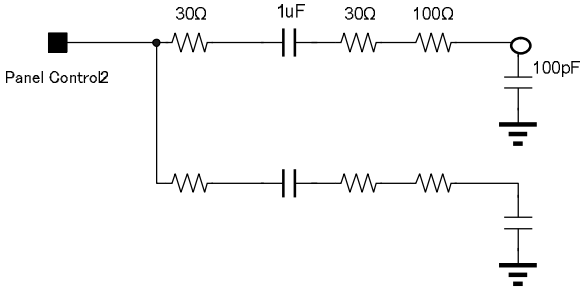
（VDDIO = 1.6 ～ 3.4V、VDDC = 2.7～ 3.4V、Ta = -30～ 85℃）

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit	Note
Panel Control(1)	tr,tf	10%～90%			100	ns	1
Panel Control(2)	tr,tf	10%～90%			100	ns	2

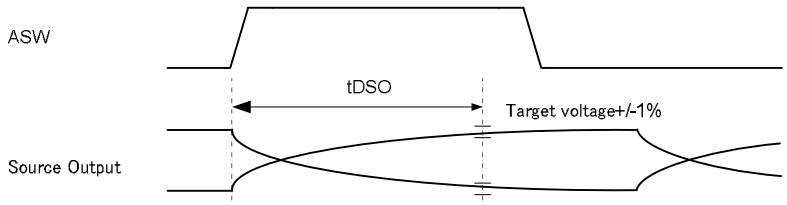
Note1 GSP、GCK1、GCK2、GOE、INIT、ASW1～6、FR、RCK1、RCK2、DCON1、DCON2



Note2 DCCK、DCCKB ports



15.4.2. Source Output

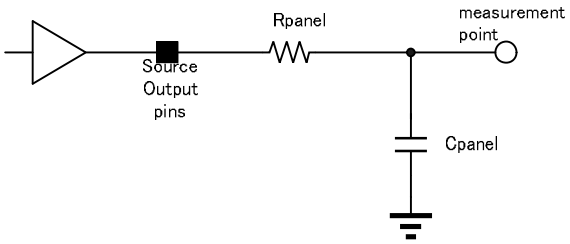


(VDDIO = 1.6 ～ 3.4V、VDDC = 2.7～ 3.4V、Ta = -30～ 85℃)

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit	Note
Settling time	tDSO	1%～99% Source output Max4.4V			2.5	us	1

Note.1 Each source output pins

Load model of source output



Source Load value

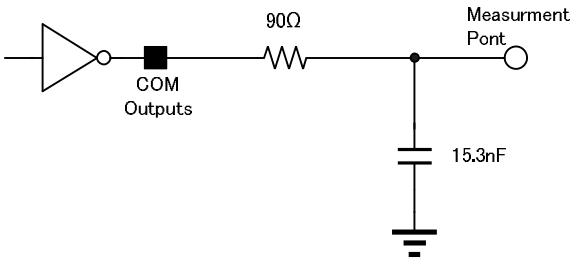
Source load	R-panel (kΩ)	C-panel (pF)
MAX	5.0	30.0
MIN	2	10
ASW OFF	0.3	3

15.4.3. COM Output

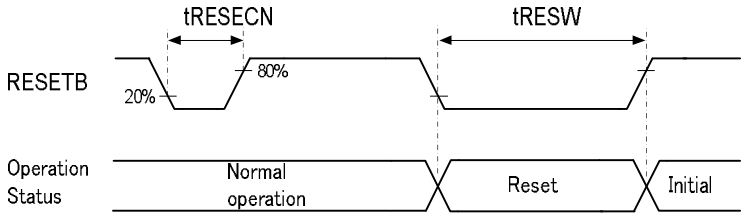
(VDDIO = 1.6 ～ 3.4V、VDDC = 2.7～ 3.4V、Ta = -30～ 85℃)

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit	Note
Settling time	tCOM	10%～90% COM voltage Max4.8V			6	us	1

COM output Load model



15.4.4. Reset enable

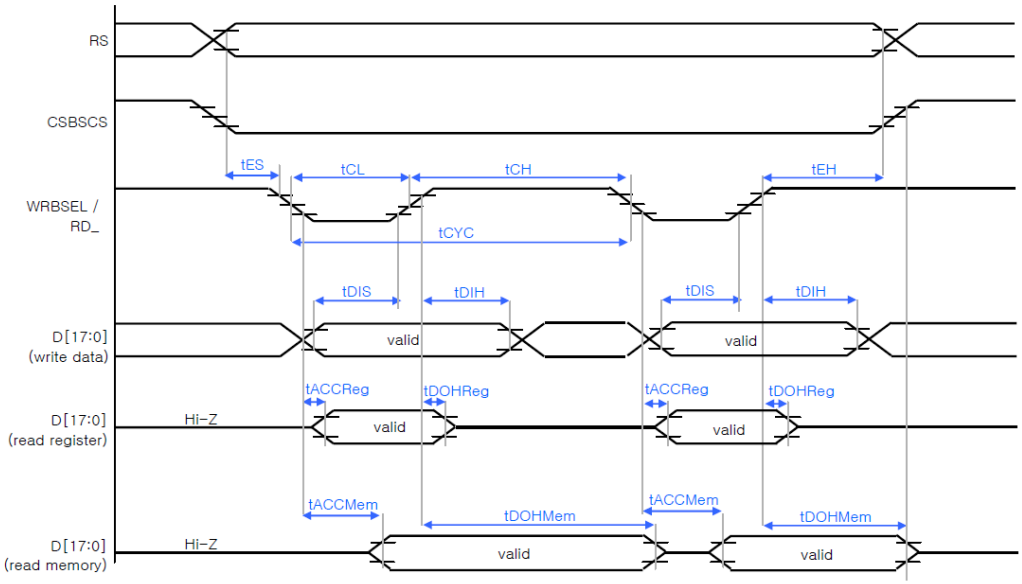


(VDDIO = 1.6 ～ 3.4V、VDDC = 2.7～ 3.4V、Ta = -30～ 85℃)

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit	Note
Minimum Pulse width	tRESW		10			us	
Rejected Pulse width	tRESCN				2	us	

15.4.5. CPU Interface

ACtiming(i80)



The read or write operation starts when both of the /CS and /WR(/RD) are low.
(TA=25℃, GND=0V, VDDC=VDDIO=Recommended Operating Conditions)

Parameter	Symbol	Condition		MIN	TYP	MAX	Unit
enable Setup Time	tES	CSBCS,RS		10			ns
enable Hold Time	tEH	CSBCS,RS		40			ns
Clock Cycle Period	tCYC	Write Register		80			ns
		Write Memory		110			ns
		Read Register CL=10pF	VDDIO>=2.2V	125			ns
			VDDIO<2.2V	160			ns
		Read Register CL=30pF	VDDIO>=2.2V	180			ns
			VDDIO<2.2V	240			ns
		Read Memory CL=10pF	VDDIO>=2.2V	225			ns
			VDDIO<2.2V	240			ns
		Read Memory CL=30pF	VDDIO>=2.2V	255			ns
			VDDIO<2.2V	300			ns
Clock Low Width	tCL	Write Register/Memory		40			ns
		Read Register CL=10pF	VDDIO>=2.2V	85			ns
			VDDIO<2.2V	120			ns
		Read Register CL=30pF	VDDIO>=2.2V	140			ns
			VDDIO<2.2V	200			ns
		Read Memory CL=10pF	VDDIO>=2.2V	155			ns
			VDDIO<2.2V	170			ns
		Read Memory CL=30pF	VDDIO>=2.2V	185			ns
			VDDIO<2.2V	230			ns
Clock High Width	tCH	Write/Read Register		40			ns
		Write/Read Memory		70			ns
Write Data Setup Time	tDIS	D0-D17		40			ns
Write Data Hold Time	tDIH	D0-D17		30			ns

Parameter	Symbol	Condition		MIN	TYP	MAX	Unit
Register Access Delay	tACCReg	D0-D17 CL=10pF	VDDIO>=2.2V			75	ns
			VDDIO<2.2V			100	ns
		D0-D17 CL=30pF	VDDIO>=2.2V			130	ns
			VDDIO<2.2V			190	ns
Memory Access Delay	tACCMem	D0-D17 CL=10pF	VDDIO>=2.2V			135	ns
			VDDIO<2.2V			150	ns
		D0-D17 CL=30pF	VDDIO>=2.2V			165	ns
			VDDIO<2.2V			210	ns
Read Data(Register) Hold Time	tDOHReg	D0-D17		30			ns
Read Data(Memory) Hold Time	tDOHMem	D0-D17		tCH+30			ns
Rising/Falling Time	tr,tf	All signals				15	ns

15.4.6 VSYNCO

Output terminal：The VSYNCO output has synchronized with
"Internal HSYNC and Internal VSYNC".
It shows internal display timing.