1/4” HD CMOS Image Sensor

GC1004

DataSheet

V1.1

2014-04-15

GalaxyCore Inc.

Content

1. Sensor Overview

1.1 General Description

The GC1004 features 1280V x 720H resolution with 1/4-inch optical format, and 4-transistor pixel structure for low light image quality and low noise variations.

The full scale integration of high-performance and low-power functions makes the GC1004 best fit the design, and reduce implementation process. The superior image quality in both low light and high dynamic range scene makes it the perfect choice for a wide range of applications, including surveillance, automobile and HD video.

It provides RAW10 and RAW8 data formats with MIPI interface. It has a commonly used two-wire serial interface for host to control the operation of the whole sensor.

1.2 Features

- Standard optical format of 1/4 inch
- Output formats: Raw Bayer 10bit/8bit
- Power supply requirement: AVDD: 3.0~3.6V
  DVDD: 1.7~1.9V
  IOVDD: 1.7~3.6V
- PLL support
- Full size @ 50fps
- Windowing support
- MIPI interface support
- Horizontal/Vertical mirror
- Image processing module
- High sensitivity for low-light operation

- Package: CSP

1.3 Application

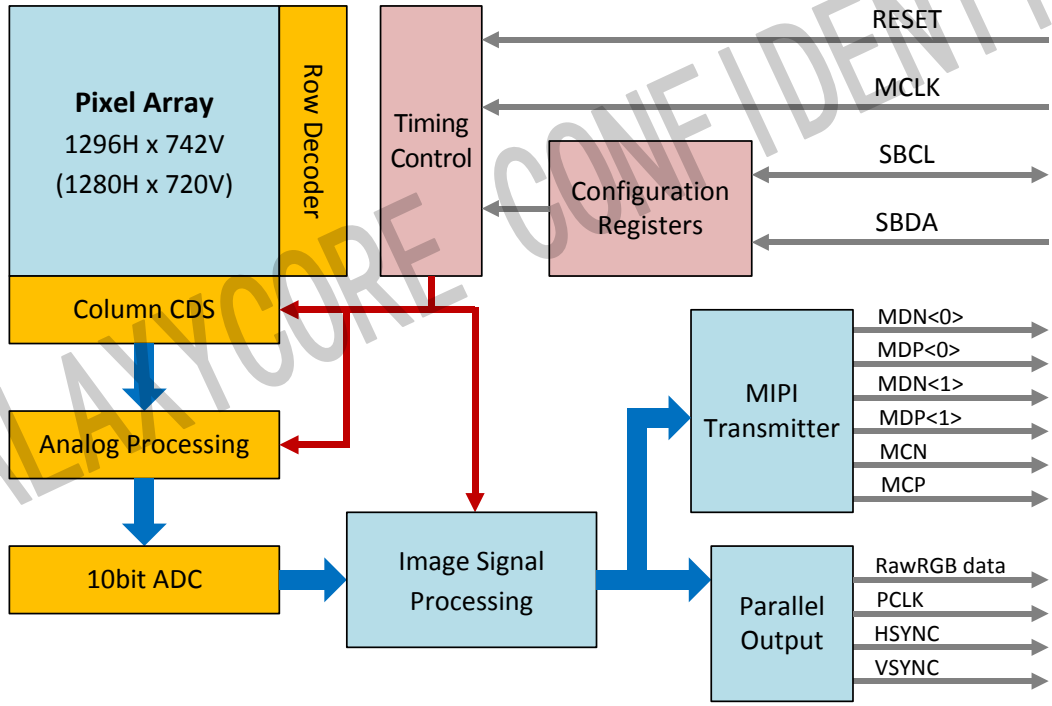
- Cellular Phone Cameras
- Notebook and desktop PC cameras
- PDAs
- Toys
- Digital still cameras and camcorders
- Video telephony and conferencing equipments
- Security systems
- Industrial and environmental systems
- Automobile video recorder

1.4 Technical Specifications

Parameter	Typical value
Optical Format	1/4 inch
Pixel Size	3.4um x 3.4um
Active pixel array	1296 x 742
ADC resolution	10 bit ADC
Max Frame rate	Full size@50fps
Power Supply	AVDD: 3.0~3.6V DVDD: 1.7~1.9V IOVDD: 1.7~3.6V
Power Consumption	180mW(Active) <100uA(Standby)
SNR	41db
Dark Current	15mV/s @ 60℃
Sensitivity	11000 e/(lux • s)
Operating temperature:	-30~70℃
Stable Image temperature	0~50℃
Optimal lens chief ray angle(CRA)	25° (non-linear)
Package type	CSP

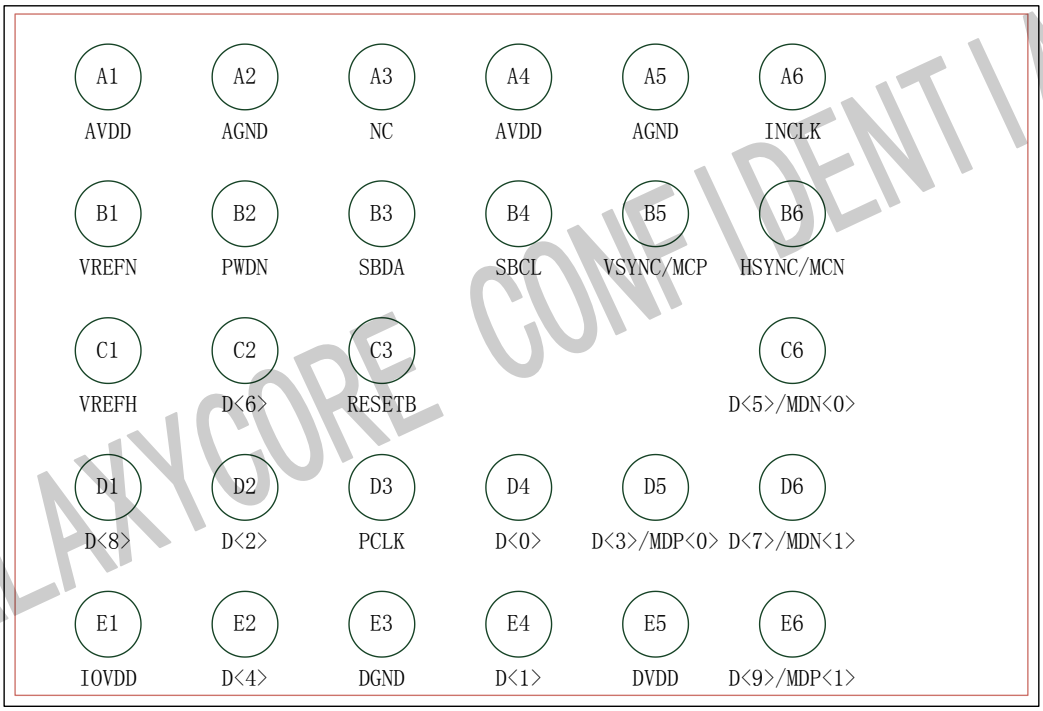
2. Block Diagram

2.1 Block Diagram



GC1004 has an active image array of 1296x742 pixels. The active pixels are read out progressively through column/row driver circuits. In order to reduce fixed pattern noise, CDS circuits are adopted. The analog signal is transferred to digital signal by 10 bit A/D converter. The digital signals are processed in the ISP Block. Users can easily control these functions via two-wire serial interface bus.

2.2 Pin Diagram



Top View

2.3 Signal Descriptions

Pin	Name	Pin Type	Description
A1	**AVDD**	Power	Analog power: 3.0~3.6V, please connect 0.1μF or 1μF capacity to ground.
A2	**AGND**	Ground	AGND
A3	**NC**	/	NC
A4	**AVDD**	Power	Analog power: 3.0~3.6V, please connect 0.1μF or 1μF capacity to ground.
A5	**AGND**	Ground	AGND
A6	**INCLK**	Input	Input clock
B1	**VREFN**	Reference	Reference voltage, please connect 0.1μF or 1μF capacity to ground.
B2	**PWDN**	Input	Sensor power down control: 0: normal work 1: standby
B3	**SBDA**	I/O	Two-wire serial bus, data
B4	**SBCL**	Input	Two-wire serial bus, clock
B5	**VSYNC**	Output	VSYNC output
	MCP	Output	MIPI clock (+)
B6	**HSYNC**	Output	HSYNC output
	MCN	Output	MIPI clock (-)

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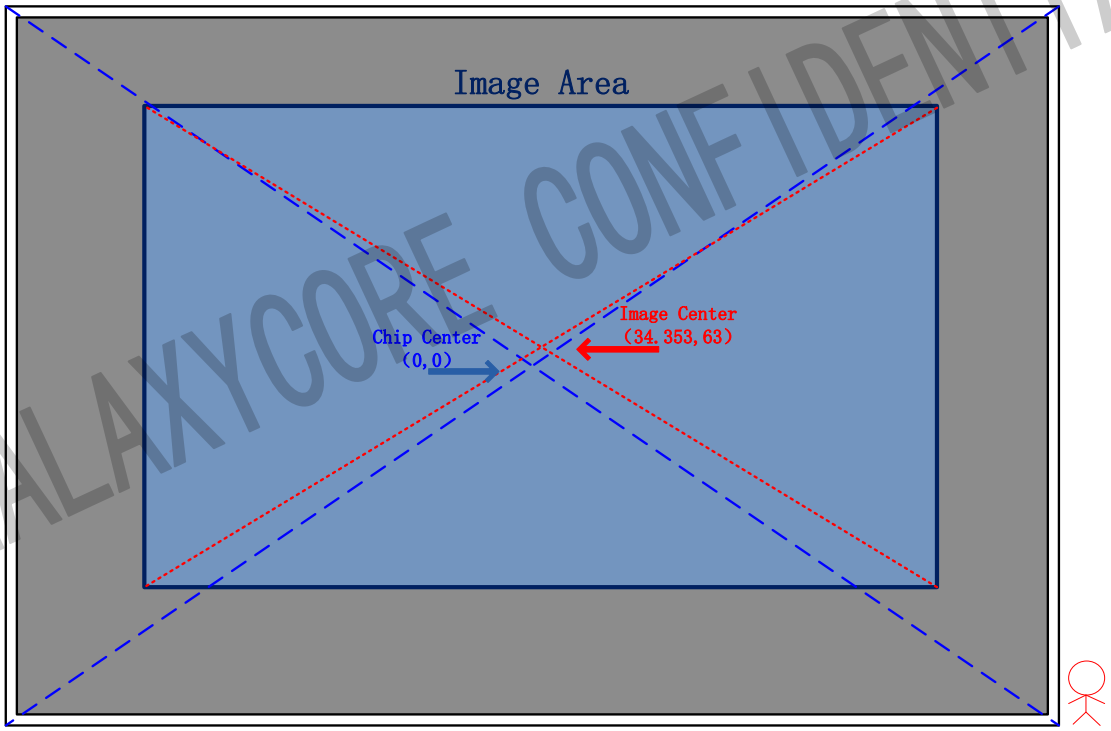
C1	**VREFH**	Reference	Reference voltage, please connect 0.1μF or 1μF capacity to ground.
C2	**D<6>**	Output	Raw RGB data output bit[6]
C3	**RESETB**	Input	Chip reset control: 0: chip reset 1: normal work
C6	**D<5>**	Output	Raw RGB data output bit[5]
	MDN<0>	Output	MIPI data<0> (-)
D1	**D<8>**	Output	Raw RGB data output bit[8]
D2	**D<2>**	Output	Raw RGB data output bit[2]
D3	**PCLK**	Output	Pixel clock output
D4	**D<0>**	Output	Raw RGB data output bit[0]
D5	**D<3>**	Output	Raw RGB data output bit[3]
	MDP<0>	Output	MIPI data<0> (+)
D6	**D<7>**	Output	Raw RGB data output bit[7]
	MDN<1>	Output	MIPI data<1> (-)
E1	**IOVDD**	Power	Power supply for I/O circuits: 1.7~3.6V, please connect 0.1μF or 1μF capacity to ground.
E2	**D<4>**	Output	Raw RGB data output bit[4]
E3	**DGND**	Ground	DGND
E4	**D<1>**	Output	Raw RGB data output bit[1]
E5	**DVDD**	Power	Power for digital core: 1.7~1.9V, please connect 0.1μF or 1μF capacity to ground.
E6	**D<9>**	Output	Raw RGB data output bit[9]
	MDP<1>	Output	MIPI data<1> (+)

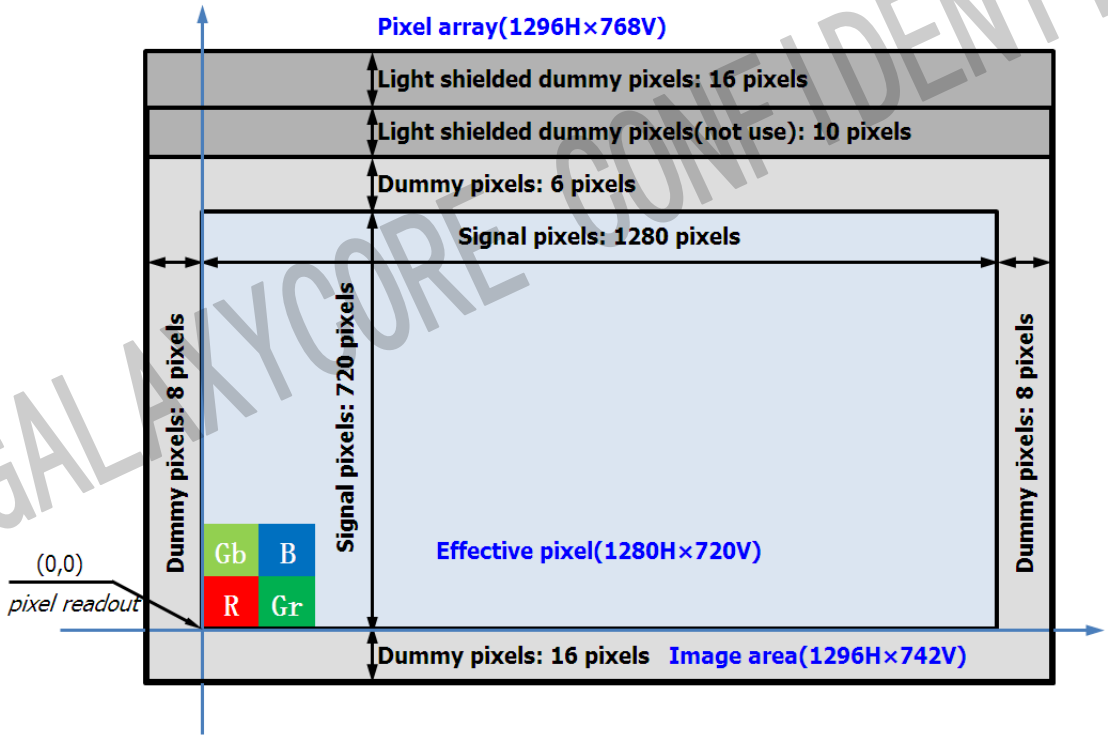
- **10-bit output (RAW): D<9>~D<0>.**
- **8-bit output (RAW): D<9>~D<2>.**

3. Optical Specifications

3.1 Sensor Array Center



3.2 Pixel Array

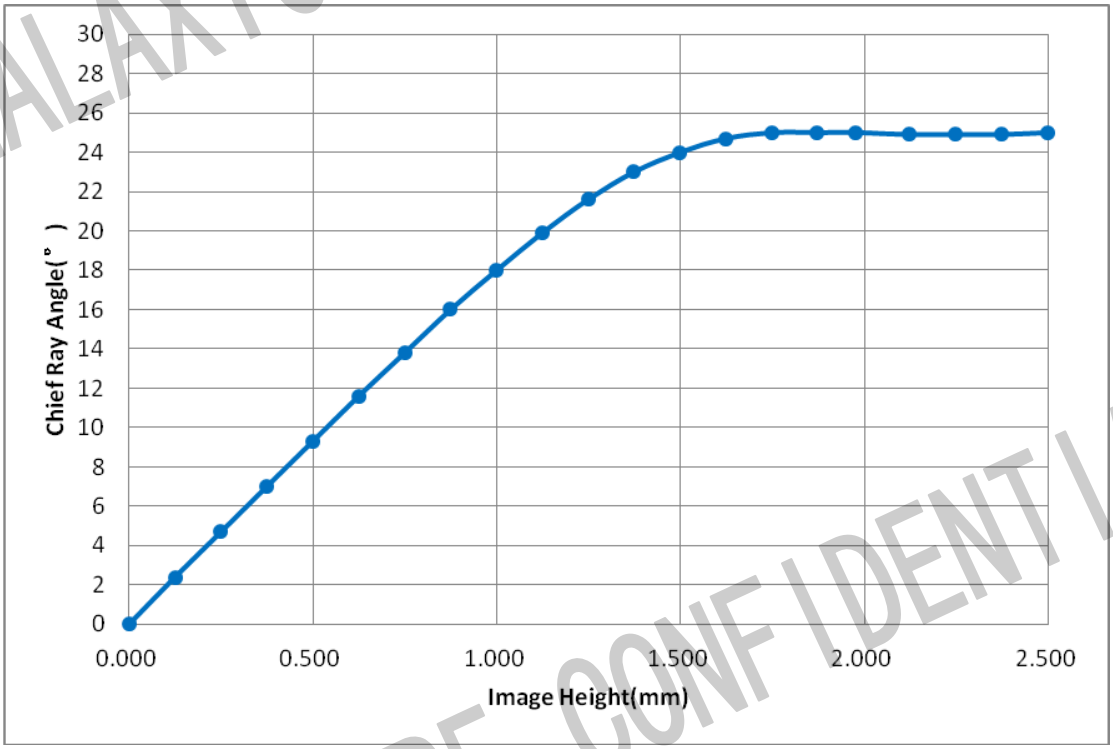


Pixel array is covered by Bayer pattern color filters. The primary color BG/GR array is arranged in line-alternating way.

If no flip in column, column is read out from 0 to 1295. If flip in column, column is read out from 1295 to 0.

If no flip in row, row is read out from 0 to 741.If flip in row, row is read out from 741 to 0.

3.3 Lens Chief Ray Angle (CRA)

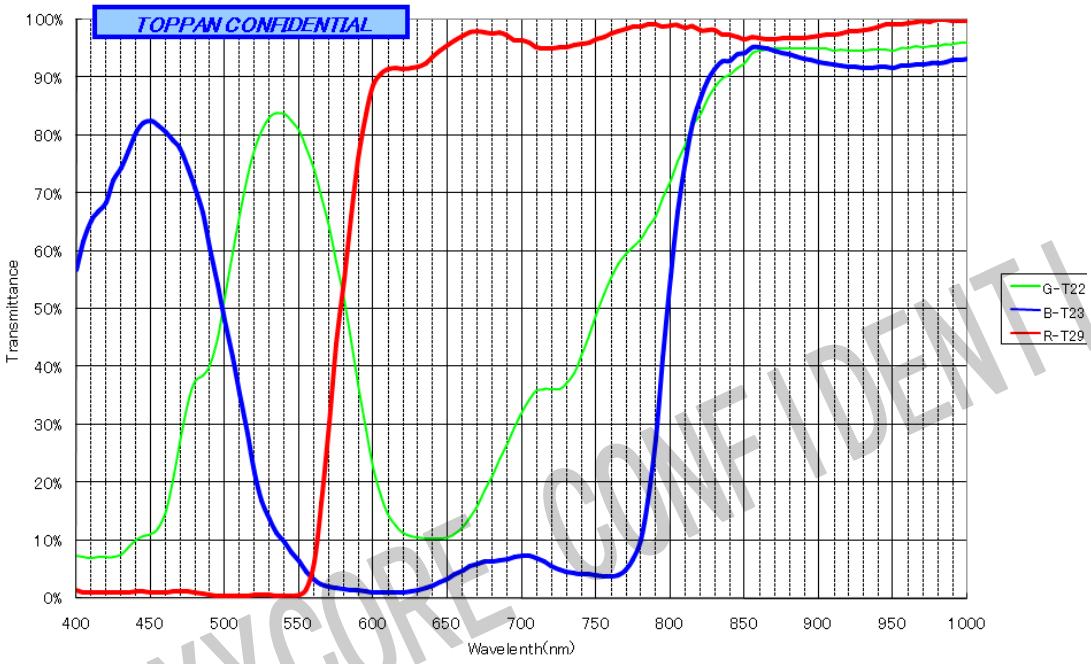


Field(%)	Image Height(mm)	CRA(degrees)
0	0.000	0.0
5	0.125	2.4
10	0.250	4.7
15	0.374	7.0
20	0.499	9.3
25	0.624	11.6
30	0.749	13.8
35	0.874	16.0
40	0.999	18.0
45	1.123	19.9

50	1.248	21.6
55	1.373	22.0
60	1.498	24.0
65	1.623	24.7
70	1.748	25.0
75	1.872	25.0
80	1.997	25.0
85	2.122	24.9
90	2.247	24.9
95	2.372	24.9
100	2.497	25.0

3.4 Color Filter Spectral Characteristics

The optical spectrum of color filters is shown below



4. Two-wire Serial Bus Communication

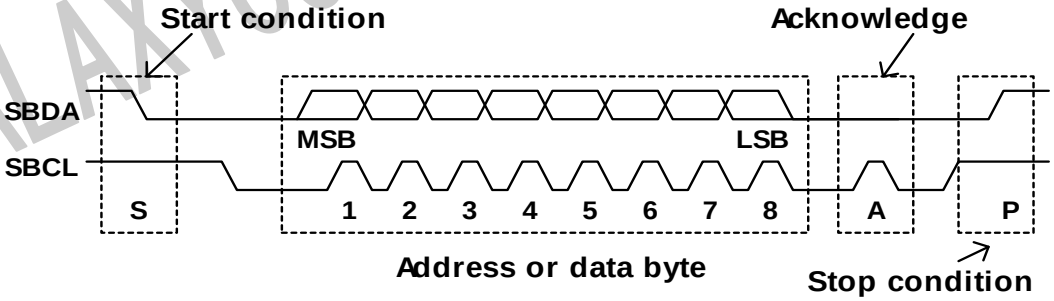
GC1004 Device Address:

serial bus write address = 0x78, serial bus read address = 0x79

4.1 Protocol

The host must perform the role of a communications master and GC1004 acts as either a slave receiver or transmitter. The master must do

- Generate the **Start(S)/Stop(P)** condition
- Provide the serial clock on **SBCL**.



Single Register Writing:

S	78H	A	Register Address	A	Data	A	P

Incremental Register Writing:

S	78H	A	Register Address	A	Data(1)	A	.....	Data(N)	A	P

Single Register Reading:

S	79H	A	Register Address	A	S	79H	A	Data	NA	P

Notes:

From master to slave From slave to master

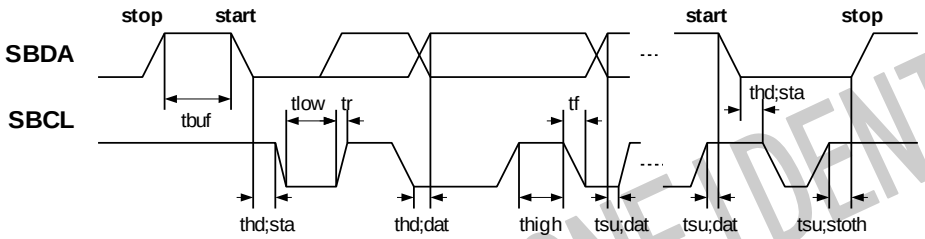
S: Start condition **P:** Stop condition

A: Acknowledge bit **NA:** No acknowledge

Register Address: Sensor register address

Data: Sensor register value

4.2 Serial Bus Timing

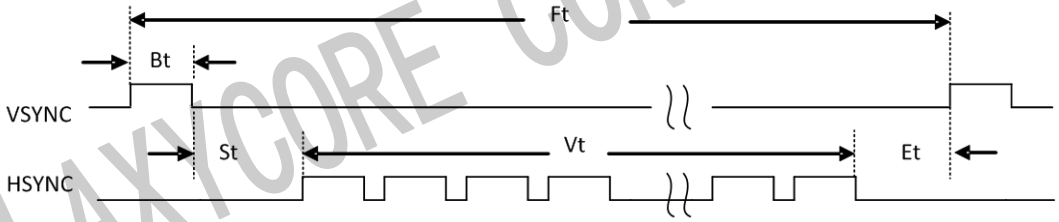


Parameter	Symbol	Min.	Max.	Unit
SBCL clock frequency	fscl	0	400	KHz
Bus free time between a stop and a start	tbuf	1.2	*	μs
Hold time for a repeated start	thd;sta	1.0	*	μs
LOW period of SBCL	tlow	1.2	*	μs
HIGH period of SBCL	thigh	1.0	*	μs
Set-up time for a repeated start	tsu;sta	1.2	*	ns
Data hold time	thd;dat	1.3	*	ns
Data Set-up time	tsu;dat	250	*	ns
Rise time of SBCL, SBDA	tr	*	250	ns
Fall time of SBCL, SBDA	tf	*	300	ns
Set-up time for a stop	tsu;sto	1.2	*	μs
Capacitive load of bus line (SBCL, SBDA)	Cb	*	*	pf

5. Applications

5.1 DVP Timing

Suppose Vsync is low active and Hsync is high active, and output format is RAW Bayer 10bit/8bit, then the timing of Vsync and Hsync is bellowing (take capture mode for example, preview mode is the same):



Ft =VB+ Vt +16(darkrow_line)(unit is row_time)

VB +16 = Bt + St + Et, Vblank/Dummy line, setting by register P0:0x07 and P0:0x08.

Ft -> Frame time, one frame time.

Bt -> Blank time, Vsync no active time.

St -> Start time, setting by register P0:0x13.

Et –> End time, setting by register P0:0x14.

Vt -> valid line time.Vt = win_height, win_height is setting by register P0:0x0d and P0:0x0e.

When exp_time ≤ win_height+VB+16, Bt = VB+16 – St - Et. Frame rate is controlled by window_height + VB+16.

When exp_time > win_height + VB, Bt = exp_time - win_height – St - Et. Frame rate is controlled by exp_time.

The following is row_time calculate:

row_time = (Hb + Sh_delay + win_width /2+ 4)/HPCLK.

Hb –> HBlank or dummy pixel，Setting by register P0:0x05 and P0:0x06.

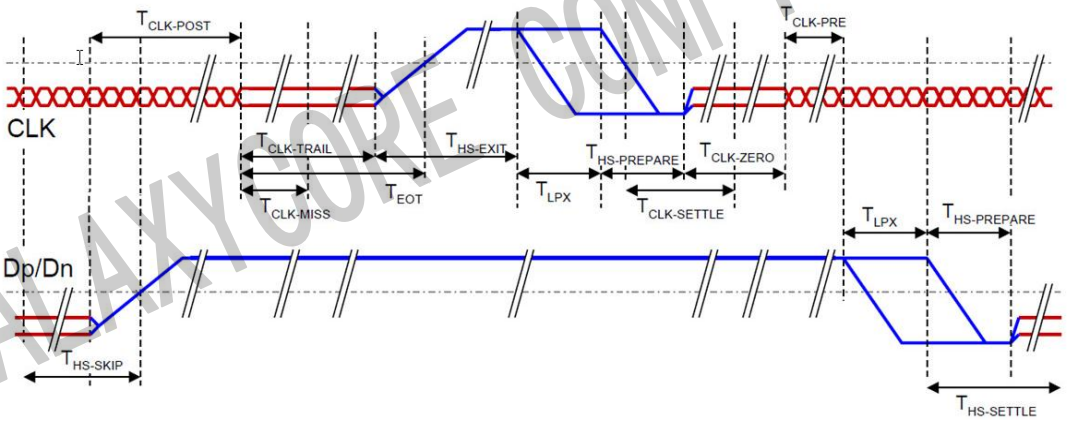
Sh_delay -> Setting by register P0:0x11, P0:0x12.

win_width -> Setting by register P0:0x0f and P0:0x10, win_width = final_output_width + 16. So for HD, we should set win_width as 1296.

HPCLK -> half PCLK.

5.2 MIPI

5.2.1 Clock lane low-power



Notice:

- Clock must be reliable during high speed transmission and mode-switching.
- Clock can go to LP only if data lanes are in LP (and nothing relies on it).
- In Low-Power data lanes are conceptually asynchronous (independent of the high speed clock).

  T_{CLK_PRE}: setting by Register P3: 0x24

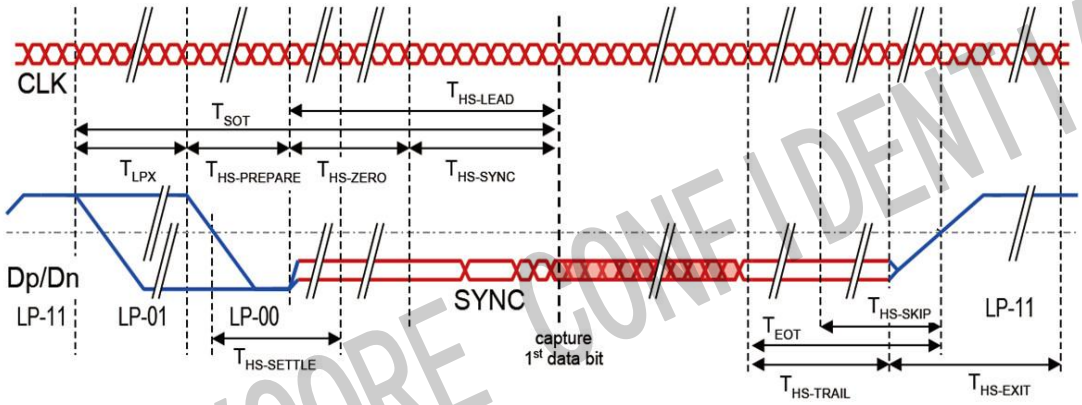
  $T_{CLK\_HS\_PRE}$: setting by Register P3: 0x22

  T_{CLK_POST} : setting by Register P3: 0x25

  T_{CLK_ZERO}: setting by Register P3: 0x23

  T_{CLK_TRAIL}: setting by Register P3: 0x26

5.2.2 Data Burst



Notice:

- Clock keeps running and samples data lanes (except for lanes in LPS).
- Unambiguous leader and trailer sequences required to distill real bits.
- Trailer is removed inside PHY (a few bytes).
- Time-out to ignore line values during line state transition.

  T_{LPX}: setting by Register P3:0x21

  $T_{HS\_PREPARE}$: setting by Register P3: 0x29

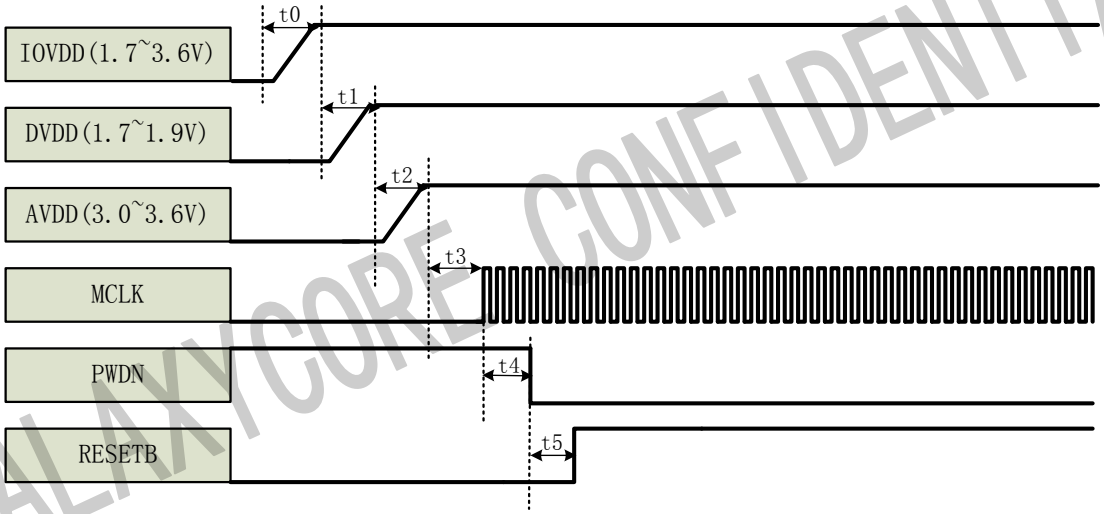
  T_{HS_ZERO}: setting by Register P3: 0x2a

  T_{HS_TRAIL}: setting by Register P3: 0x2b

  T_{HS_EXIT}: setting by Register P3: 0x27

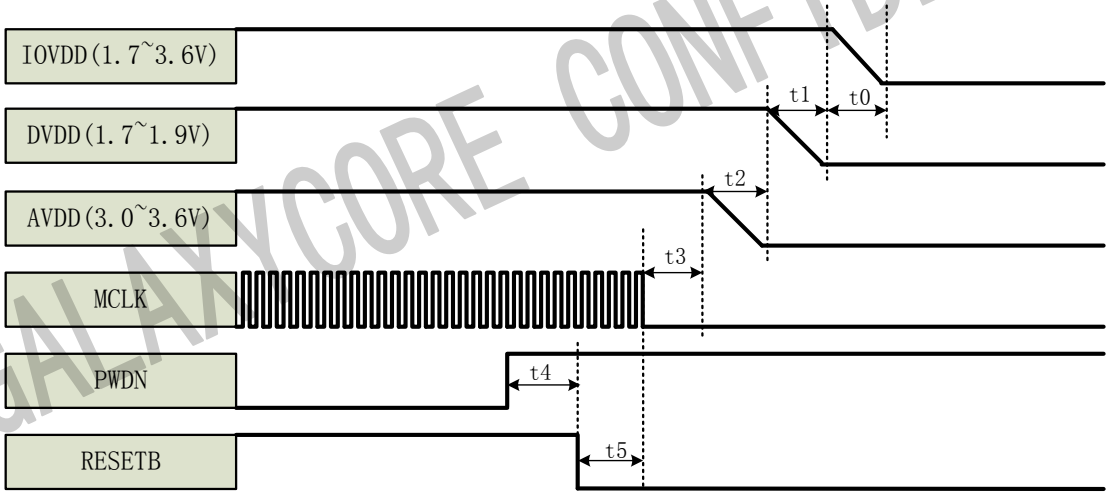
5.3 Power On/Off Sequence

5.3.1 Power On Sequence



Parameter	Description	Min.	Max.	Unit
t0	IOVDD rising time	100		us
t1	From IOVDD to DVDD	50		us
t2	From DVDD to AVDD	50		us
t3	From AVDD to MCLK applied	>0		us
t4	From MCLK applied to Sensor enable	>0		us
t5	From PWDN pull low to RESET pull high	>0		us

5.3.2 Power Off Sequence



Parameter	Description	Min.	Max.	Unit
t0	From DVDD to IOVDD falling time	>0		us

t1	From AVDD to DVDD falling time	>0		us
t2	AVDD falling time	>0		us
t3	From MCLK disable to sensor AVDD power down	>0		us
t4	From sensor disable sensor RESET pull low	>0		us
t5	From sensor RESET pull low to MCLK disable	>0		us

- **Recommended power on/off sequence is above.**
- **If you have special requirements in application, please contact with us to confirm.**

5.4 DC Parameters

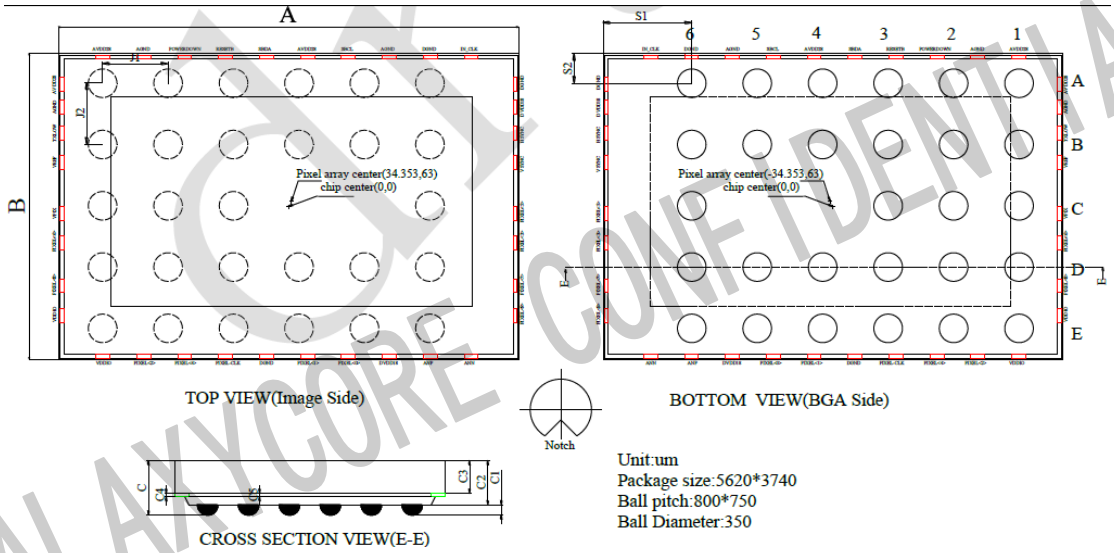
Supply					
Symbol	**Parameter**	**Min**	**Typ**	**Max**	**Unit**
V_{AVDD}	Power supply	3.0	3.3	3.6	V
V_{DVDD}	Supply voltage(digital core)	1.7	1.8	1.9	V
V_{IOVDD}	Supply voltage(digital I/O)	1.7	-	3.6	V

DVP	Symbol		Parameter	Min	Typ	Max	Unit
	I_{AVDD}		Active(operating) current	-	26	32	mA
	I_{DVDD18}			-	15	16	mA
	I_{IOVDD}	1.8V		-	8	10	mA
		3.3V		-	19	24	mA
	I_{DDS_PWD}		Standby Current	-	30	100	uA

MIPI	Symbol		Parameter	Min	Typ	Max	Unit
	I_{AVDD}		Active(operating) current	-	26	32	mA
	I_{DVDD18}			-	30	31	mA
	I_{IOVDD}	1.8V		-	0.1	0.1	mA
		3.3V		-	0.2	0.2	mA
	I_{DDS_PWD}		Standby Current	-	30	100	uA

Digital Input(Typical conditions: AVDD=3.3V，DVDD=1.8V，IOVDD=3.3V)					
V_{IH}	Input voltage HIGH	2.4			V
V_{IL}	Input voltage LOW			0.6	V
Digital Output(AVDD=3.3V，standard Loading 25PF，IOVDD=3.3V)					
V_{OH}	Output voltage HIGH	3.0			V
V_{OL}	Output voltage LOW			0.2	V

6. Package Specification



Parameter	Symbol	Nominal	Min.	Max.
		μm		
Package Body Dimension X	A	5620	5595	5645
Package Body Dimension Y	B	3740	3715	3765
Package Height	C	735	680	790
Ball Height	C1	175	145	205
Package Body Thickness	C2	560	525	595
Glass Thickness	C3	400	390	410
Cavity Height (glass to pixel distance)	C4	30	26	34
Cavity Wall + Epoxy Thickness (glass to the wafer bonding top point)	C5	32.5	27.5	37.5
Ball Diameter	D	350	320	380
Total Pin Count	N	28		
Pins Count X axis	N1	6		
Pins Count Y axis	N2	5		
Pins Pitch X axis	J1	800		
Pins Pitch Y axis	J2	750		
Edge to Pin Center Distance along X	S1	1083.645	1083.615	1083.675
Edge to Pin Center Distance along Y	S2	360	359.97	360.03

7. Register List

System Register

Address	Name	Width	Default Value	R/W	Description
0xf0	**Sensor_ID_high**	**8**	**0x10**	**RO**	**Sensor_ID**
0xf1	**Sensor_ID_low**	**8**	**0x04**	**RO**	**Sensor_ID**
0xf2	pad_vb_hiz_mode data_pad_io sync_pad_io	5	0x00	RW	[7:5] NA [4] pad_vb_hiz_mode [3] data_pad_io [2:0] sync_pad_io 0: input 1: output
0xf3	I2C_open_en	1	0x00	RW	[7:1] NA [0] I2C_open_en
0xf6	Up_down Pwd_dn	6	0x00	RW	[7:6] NA [5:4] up_dn 00: not pull 01: pull down 10: pull up 11: illegal [3:1] NA [0] PWD dn 0: pull down 1: not pull
0xf7	PLL_mode1	8	0x10	RW	[7]dvp mode [6:4]serial clk div [3]clk_double [2] 3/2 div [1] div2en [0] pll_en
0xf8	PLL_mode2	8	0x00	RW	[7] div2 enable [6] div2_frame [5:0] divx4
0xf9	Cm_mode	8	0x00	RW	[7] regf clk enable [6] use internal clk [5:4] NA [3] isp all clock enable [2] bypass auto switch clk [1] re_lock_pll

					[0] not_use_pll
0xfa	clk_div_mode	8	0x00	RW	[7:4] +1 represent the frequency division number [3:0] represent the high level in one pulse after frequency division MCLK by Div duty 0x11 2 1:1 0x21 3 1:2 0x22 3 2:1 0x31 4 1:3 0x32 4 2:2 0x33 4 3:1 …
0xfb	i2c_device_id	8	0x6c	RW	[7:1] I2C device ID, can write once [0] NA
0xfc	analog_pwc	8	0x01	RW	[7:6] post_eq_width [5:4] vpll_r [3] vpll_en [2] vpix_en [1] NA [0] apwd
0xfd	clk_div2_mode	8	0x11	RW	[7:4] divide_by [3:0] clock duty
0xfe	Reset related	8	0x00	RW	[7] soft_reset [6] cm_reset [5] mipi_reset [4] CISCTL_restart_n [3] spi_reset [2:0] page_select

Analog & CISCTL

Address	Name	Width	Default Value	R/W	Description
P0:0x03	Exposure[12:8]	5	0x00	RW	[7:5] NA [4:0] exposure[12:8], use line processing time as the unit.
P0:0x04	Exposure[7:0]	8	0x10	RW	Exposure[7:0]
P0:0x05	HB[11:8]	4	0x00	RW	H Blanking
P0:0x06	HB[7:0]	8	0xa4	RW	
P0:0x07	VB[12:8]	5	0x00	RW	Vertical blanking, if current exposure < (Vb + window Height) , frame rate will
P0:0x08	VB[7:0]	8	0x10	RW	

					be (Vb + window Height); otherwise frame rate will be determined by exposure
P0:0x09	Row_start[9:8]	2	0x00	RW	Row Start
P0:0x0a	Row_start[7:0]	8	0x00	RW	
P0:0x0b	Col_start[10:8]	3	0x00	RW	Col start
P0:0x0c	Col_start[7:1]	8	0x00	RW	
P0:0x0d	win_height[9:8]	2	0x02	RW	[7:2] NA [1:0] Window height[9:8]
P0:0x0e	win_height[7:0]	8	0xe0	RW	Window height[7:0]
P0:0x0f	win_width[10:8]	3	0x02	RW	[7:3] NA [2:0] Window width[10:8]
P0:0x10	win_width[7:0]	8	0x88	RW	window width[7:0]
P0:0x11	Sh_delay[9:8]	2	0x00	RW	Sh_delay[9:8]
P0:0x12	Sh_delay[7:0]	8	0x18	RW	Sh_delay[7:0]
P0:0x13	Vs_st	8	0x11	RW	Vs_st
P0:0x14	Vs_et	8	0x01	RW	Vs_et
P0:0x15	Reserved	8	0x00	RW	Reserved
P0:0x16	Reserved	8	0xc1	RW	Reserved
P0:0x17	Mirror & Flip	8	0X00	RW	[7:2] Reserved [1] Flip [0] mirror
P0:0x18	Reserved	8	0x0a	RW	Reserved
P0:0x19	Reserved	8	0x05	RW	Reserved
P0:0x1a	Reserved	8	0x18	RW	Reserved
P0:0x1b	Reserved	8	0x44	RW	Reserved
P0:0x1c	Reserved	8	0x10	RW	Reserved
P0:0x1d	Reserved	8	0x20	RW	Reserved
P0:0x1e	Reserved	8	0x90	RW	Reserved
P0:0x1f	Reserved	8	0x08	RW	Reserved
P0:0x20	Reserved	8	0x00	RW	Reserved
P0:0x21	Reserved	8	0x40	RW	Reserved
P0:0x22	Reserved	8	0xb2	RW	Reserved
P0:0x23	Reserved	8	0x01	RW	Reserved
P0:0x24	ANALOG_PAD_drv	8	0x55	RW	[7:6] data_low_drv [5:4] sync_drv

					[3:2] data_high_drv [1:0] pclk_drv
P0:0x25	Reserved	8	0x00	RW	Reserved
P0:0x27	Reserved	8	0x08	RW	Reserved
P0:0x2a	Reserved	4	0x01	RW	Reserved
P0:0x2b	Reserved	8	0x00	RW	Reserved
P0:0x2c	Reserved	8	0x58	RW	Reserved
P0:0x2d	Reserved	8	0x12	RW	Reserved
P0:0x2e	Reserved	8	0x43	RW	Reserved
P0:0x2f	Reserved	8	0x11	RW	Reserved
P0:0x30	Reserved	5	0x00	RW	Reserved
P0:0x31	Reserved	5	0x01	RW	Reserved
P0:0x32	Reserved	5	0x02	RW	Reserved
P0:0x33	Reserved	5	0x03	RW	Reserved
P0:0x34	Reserved	5	0x04	RW	Reserved
P0:0x35	Reserved	5	0x05	RW	Reserved
P0:0x36	Reserved	5	0x06	RW	Reserved
P0:0x37	Reserved	5	0x7	RW	Reserved
P0:0x38	Reserved	5	0x0f	RW	Reserved
P0:0x39	Reserved	5	0x17	RW	Reserved
P0:0x3a	Reserved	5	0x1f	RW	Reserved

CSI/PHY1.0

Address	Name	Width	Default Value	R/W	Description
P3:0x01	DPHY_analog_mode1	8	0x00	RW	[6] CTD_lane1 [5] CTD_lane0 [4] CTD_clk [2] PHY_lane1_en [1] PHY_lane0_en [0] PHY_clk_en
P3:0x02	DPHY_analog_mode2	8	0x00	RW	[6:4] lane0_diff [2:0] clk_diff
P3:0x03	DPHY_analog_mode3	8	0x00	RW	[7] LP low voltage enable [6] lane1_delay [5] lane0_delay [4] clk_delay [3] NA [2:0] lane1_diff
P3:0x04	FIFO_prog_full	8	0x01	RW	FIFO_prog_full_level[7:0]

	_level[7:0]				
P3:0x05	FIFO_prog_full_level[11:8]	4	0x00	RW	[7:4] NA [3:0] FIFO_prog_full_level[11:8]
P3:0x06	FIFO_mode	8	0x04	RW	[7] MIPI_clk_Module [6] manual CSI2_up_mode [5] no flop mode [4] fifo_rst_mode [3] FIFO write read gate mode [2] odd lwc [1] NA [0] mipi_write_gate mode
P3:0x10	buf_CSI2_mode	8	0x00	RW	[7] lane_ena [6] NA [5] ULP_mode [4] MIPI_ena [3] bit10_swicth [2] RAW8 [1] line_sync_mode [0] double_lane
P3:0x11	LDI_set	8	0x2b	RW	RAW10
P3:0x12	LWC_set[7:0]	8	0x40	RW	1280x5/4 RAW10
P3:0x13	LWC_set[15:8]	8	0x06	RW	1280x5/4 RAW10
P3:0x14	SYNC_set	8	0xb8	RW	SYNC_set
P3:0x15	DPHY_mode	8	0x00	RW	[7] DATA gate mode [6] quiet or lien rise [5] delay cnt [4] 1 adv trigger 0 prog [3] lane0_switch_msb [2] clk_switch_msb [1:0] clklane_mode 1X: frames keep 01: clock lane sync with data lane 00: every frame stop clk lane mode
P3:0x16	LP_set	8	0x09	RW	[7:6] hi-z [3:2] 1 [1:0] 0
P3:0x20	T_init_set	8	0x80	RW	Timing of initial setting, more than 100 us
P3:0x21	T_LPX_set	8	0x10	RW	Timing of LP setting, more than 50ns
P3:0x22	T_CLK_HS_PREPARE_set	8	0x05	RW	Timing of COCLK HS PREPARE setting, 38ns ~95ns LP00
P3:0x23	T_CLK_zero_s	8	0x30	RW	Timing of COCLK HS zero setting, more

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	et				than 300ns
P3:0x24	T_CLK_PRE_set	8	0x02	RW	Timing of COCLK HS PRE of Data setting, more than 8UI
P3:0x25	T_CLK_POST_set	8	0x10	RW	Timing of COCLK HS Post of Data setting, 60ns +52UI
P3:0x26	T_CLK_TRAIL_set	8	0x08	RW	Timing of COCLK tail setting, 60ns
P3:0x27	T_HS_exit_set	8	0x10	RW	Timing of HS exit setting, more than 100ns
P3:0x28	T_wakeup_set	8	0xa0	RW	Timing of wakeup setting, 1ms
P3:0x29	T_HS_PREPARE_set	8	0x06	RW	Timing of data HS PREPARE setting, 45+4UI~85+5UI
P3:0x2a	T_HS_Zero_set	8	0x0a	RW	Timing of data HS zero setting, 140ns
P3:0x2b	T_HS_TRAIL_set	8	0x08	RW	Timing of data HS trail setting, 60ns
P3:0x30	MIPI_test	2	0x00	RW	[7:2] NA [1:0] MIPI_test
P3:0x31	MIPI_test_data0	8	0x96	RW	MIPI_test_data0
P3:0x32	MIPI_test_data1	8	0x3a	RW	MIPI_test_data1
P3:0x33	MIPI_test_data2	8	0x87	RW	MIPI_test_data2
P3:0x34	MIPI_test_data3	8	0xb5	RW	MIPI_test_data3
P3:0x35	hsync_in_start_4_5_cnt_num[7:0]	8	0x08	RW	hsync_in_start_4_5_cnt_num[7:0]
P3:0x36	hsync_in_start_4_5_cnt_num[9:8]	2	0x00	RW	[7:2] NA [1:0] hsync_in_start_4_5_cnt_num[9:8]
P3:0x3f	fifo_error log	2		RO	fifo_error log

ISP Related

Address	Name	Width	Default Value	R/W	Description
P0:0x7b	pad_test_valid[11:8] pad_test_data[	8	0x00	RW	pad_test_valid[11:8], pad_test_data[11:8]

	11:8]				
P0:0x7c	pad_test_valid [7:0]	8	0x00	RW	pad_test_valid[7:0]
P0:0x7d	pad_test_data[7:0]	8	0x00	RW	pad_test_data[7:0]
P0:0x87	debug_mode4	8	0x00	RW	[7] clear frame_start_num =0 [6] AEC_delay_mode [5:4] fix_odd_even [3] OUT for SOC mode [2] protect_exp_mode [1:0] CISCTL_exp2_ratio
P0:0x88	start_num	8	0x53	RW	[7:4] BLK start cnt th [3:0] start cnt th
P0:0x89	bypass_mode	8	0x03	RW	[7] output 8bit [6] output 8bit round [5] dndd bypass [4] pregain bypass [3] is_8bit_bypass [2] output_dark_sun [1:0] bypass which 8bits from 11bit, in is_8bit_bypass mode
P0:0x8a	clock_gating_e n	8	0xbf	RW	[7] ISP_quiet_mode, in SH time, clock ISP's AAA clock [6] close AAA clk [5:4] pipe gate_first [3:2] pipe gate_second [1] AAA hsync gate [0] DIV_gatedclk_en
P0:0x8b	debug_mode1	8	0xa2	RW	[7] dd_en [6] dd_auto_gating_mode [5] switch not smooth 2 frame [4] test image in output [3] not_split_sram [2] OUT_gate_mode [1:0] BFF_gate_mode
P0:0x8c	debug_mode2	8	0x07	RW	[7] data_delay_half_2pclk [6] hsync_delay_half_2pclk [5] test_image when in VGA or UXGA [4] input_test_image [3] cur_exp change = total gain switch [2] pclk_out_polarity [1] hsync_polarity

					[0] vsync_polarity
P0:0x8d	debug_mode3	8	0x03	RW	[7:4] test image fix value [3] test image fix value mode [2] dark_sun_det_gate_mode [1] AAA_hpclk_save_mode [0] update_gain_mode
P0:0x8e	ACC_mode1	3	0x00	RW	[2] buf cal mode [1] skip_mode 1 is 1/16 [0] use buf parameter cal exp_gain
P0:0x8f	ACC_mode2	6	0x12	RW	[5:4] FIR 00: no filter for Y 01: 2 FIR 10: 4 FIR [3:0] luma select
P0:0x90	Crop_win_mode	1	0x00	RW	[7:1] NA [0] Crop out win mode
P0:0x91	out_win_y1[9:8]	2	0x00	RW	[7:2] NA [1:0] Crop _win_y1[9:8]
P0:0x92	out_win_y1[7:0]	8	0x00	RW	Crop _win_y1[7:0]
P0:0x93	out_win_x1[10:8]	3	0x00	RW	[7:3] NA [2:0] Crop _win_x1[10:8]
P0:0x94	out_win_x1[7:0]	8	0x00	RW	Crop _win_x1[7:0]
P0:0x95	out_win_height[9:8]	2	0x02	RW	[7:2] NA [1:0] Out window height[9:8]
P0:0x96	out_win_height[7:0]	8	0xd0	RW	Out window height[7:0]
P0:0x97	out_win_width[10:8]	3	0x05	RW	[7:3] NA [2:0] Out window width[10:8]
P0:0x98	out_win_width[7:0]	8	0x00	RW	Out window width[7:0]
P0:0x99	CTL_data_is_real_start	7	0x00	RW	CTL_data_is_real_start
P0:0x9a	CTL_data_is_real_width[10:8]	3	0x05	RW	CTL_data_is_real_width
P0:0x9b	CTL_data_is_real_width[7:0]	8	0x10	RW	CTL_data_is_real_width
P0:0xee	Y_avg_filter	8		RO	Y_avg_filter
P0:0xef	luma_value[15:8]	8		RO	[7:0]luma_value[15:8]

P0:0xe0	out_bt656_mode	8	0x00	RW	out_bt656_mode
P0:0xe1	BT656_FS_ODD	8	0xab	RW	BT656_FS_ODD
P0:0xe2	BT656_FE_ODD	8	0xb6	RW	BT656_FE_ODD
P0:0xe3	BT656_HS_ODD	8	0x80	RW	BT656_HS_ODD
P0:0xe4	BT656_HE_ODD	8	0x9d	RW	BT656_HE_ODD
P0:0xe5	BT656_FS_EVEN	8	0xec	RW	BT656_FS_EVEN
P0:0xe6	BT656_FE_EVEN	8	0xf1	RW	BT656_FE_EVEN
P0:0xe7	BT656_HS_EVEN	8	0xc7	RW	BT656_HS_EVEN
P0:0xe8	BT656_HE_EVEN	8	0xda	RW	BT656_HE_EVEN

BLK

Address	Name	Width	Default Value	R/W	Description
P0:0x40	Blk_mode1	8	0xab	RW	[7] not smooth [6:4] BLK_smooth_speed [3] BLK after gain [2] NA [1] dark_current_en [0] offset_en
P0:0x41	BLK_mode2	7	0x85	RW	[7] NA [6] various th mode [5:3] blooming mode [2:1] current limit ratio [0] dark dd disable
P0:0x42	BLK_limit_value	8	0xff	RW	low align 11bits
P0:0x44-0x4b	Current_offset[7:0]	8		RO	current _offset[7:0]
P0:0x4d	dark_current_exp_rated_flop	8		RO	dark_current_exp_rated_flop
P0:0x4e	BLK_select_row_bits[15:8]	8	0x00	RW	BLK_select_row_bits[15:8]

P0:0x4f	BLK_select_row_bits[7:0]	8	0x3c	RW	BLK_select_row_bits[7:0]
P0:0x54-0x5b	current_dark_current[7:0]	8		RO	currentt_dark_current[7:0]
P0:0x5c	exp_rate_darkc[7:0]	8	0x04	RO	low8 of 0.12
P0:0x5e	offset_ratio	6	0x18	RW	offset_ratio
P0:0x66	dark_current_ratio	6	0x20	RW	dark_current_ratio
P0:0x6a	manual_G1_odd_offset	6	0x00	RW	manual_G1_odd_offset S5, low align to 11
P0:0x6b	manual_G1_even_offset	6	0x00	RW	manual_G1_even_offset S5, low align to 11
P0:0x6c	manual_R1_odd_offset	6	0x00	RW	manual_R1_odd_offset S5, low align to 11
P0:0x6d	manual_R1_even_offset	6	0x00	RW	manual_R1_even_offset S5, low align to 11
P0:0x6e	manual_B2_odd_offset	6	0x00	RW	manual_B2_odd_offset S5, low align to 11
P0:0x6f	manual_B2_even_offset	6	0x00	RW	manual_B2_even_offset S5, low align to 11
P0:0x70	manual_G2_odd_offset	6	0x00	RW	manual_G2_odd_offset S5, low align to 11
P0:0x71	manual_G2_even_offset	6	0x00	RW	manual_G2_even_offset S5, low align to 11
P0:0x72	Reserved	8	0xf2	RW	Reserved
P0:0x73	Reserved	8	0x10	RW	Reserved
P0:0x74	Reserved	8	0x10	RW	Reserved
P0:0x75	Reserved	8	0x00	RW	Reserved
P0:0x76	Reserved	4	0x00	RW	Reserved
P0:0xc4-0xcb	current_offset[10:8]	3		RO	current_offset[10:8]
P0:0xd4-0xdb	current_dark_current[10:8]	3		RO	current_dark_current[10:8]

GLOBAL/PRE/POSTGAIN

Address	Name	Width	Default Value	R/W	Description
P0:0xa3	channel_gain_G1_odd	8	0x80	RW	G1 odd Channel gain
P0:0xa4	channel_gain_	8	0x80	RW	G1 even Channel gain

	G1_even				
P0:0xa5	channel_gain_R1_odd	8	0x80	RW	R1 odd Channel gain
P0:0xa6	channel_gain_R1_even	8	0x80	RW	R1 even Channel gain
P0:0xa7	channel_gain_B2_odd	8	0x80	RW	B2 odd channel gain
P0:0xa8	channel_gain_B2_even	8	0x80	RW	B2 even channel gain
P0:0xa9	channel_gain_G2_odd	8	0x80	RW	G2 odd channel gain
P0:0xaa	channel_gain_G2_even	8	0x80	RW	G2 even channel gain
P0:0xb0	global_gain	8	0x40	RW	Global gain
P0:0xb1	bauto_pregain[9:6]	4	0x01	RW	[7:4] NA [3:0] Auto_pregain[9:6]
P0:0xb2	auto_pregain[5:0]	8	0x00	RW	[7:2] Auto_pregain[5:0] [1:0] NA
P0:0xb3	AWB_R_gain	8	0x40	RW	AWB_R_gain
P0:0xb4	AWB_G_gain	8	0x40	RW	AWB_G_gain
P0:0xb5	AWB_B_gain	8	0x40	RW	AWB_B_gain
P0:0xb6	Analog_gain	4	0x00	RW	[7:4] NA [3:0] Analog_gain
P0:0xb7	buf_freq_div2	1	0x00	RW	[7:1] NA [0] freq_div2

DARK SUN CORRECTION

Address	Name	Width	Default Value	R/W	Description
P2:0x40	dark_sun_en	8	0xb7	RW	[7] darksun enable [6:0] NA
P2:0x41	Reserved	8	0xf0	RW	Reserved
P2:0x42	Reserved	6	0x35	RW	Reserved
P2:0x43	Reserved	8	0x99	RW	Reserved
P2:0x44	Reserved	8	0xb0	RW	Reserved
P2:0x45	Reserved	8	0x14	RW	Reserved
P2:0x46	Reserved	8	0x0f	RW	Reserved
P2:0x47	Reserved	8	0xff	RW	Reserved
P2:0x48	Reserved	4	Ox00	RW	Reserved
P2:0x49	Reserved	6	0x03	RW	Reserved

DD

Address	Name	Width	Default Value	R/W	Description
P2:0x80	DD_mode_en	8	0x02	RW	DD_mode_en
P2:0x81	DD_dark_bright_TH	8	0x05	RW	DD_dark_bright_TH
P2:0x82	DD_flat_TH	8	0x86	RW	dd th subtract
P2:0x83	DD_limit DD_max_V_mode DD_ratio	8	0xf2	RW	[7:4] DD limit [3:2] DD_max_V_mode [1:0] DD_ratio
P2:0x84	DD_is_bright_dark_th	8	0x33	RW	[7:0] DD_is_bright_dark_th
P2:0x85	DD_on_edge_th	8	0x33	RW	DD_on_edge_th
P2:0x86	Reserved	8	0xaa	RW	Reserved
P2:0x87	Reserved	8	0x8a	RW	Reserved
P2:0x88	DD_luma_value_dd_th2	8	0x40	RW	[7:0] DD_luma_value_dd_th2
P2:0x89	DD_luma_value_dd_th3	8	0x30	RW	[7:0] DD_luma_value_dd_th3
P2:0x8a	DD_luma_value_dd_th4	8	0x20	RW	[7:0] DD_luma_value_dd_th4
P2:0x8b	auto_dd_en	1	0x00	RW	[0] auto_dd_en

ASDE

Address	Name	Width	Default Value	R/W	Description
P2:0xa0	ASDE_low_luma_value_DD_th	8	0x20	RW	ASDE_low_luma_value_DD_th
P2:0xa1	ASDE_low_luma_value_OT_th	8	0x20	RW	ASDE_low_luma_value_OT_th
P2:0xa2	ASDE_DD_bright_th_slope ASDE_DD_limit_slope	8	0x5f	RW	[7:4] ASDE_DD_bright_th_slope [3:0] ASDE_DD_limit_slope

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P2:0xa4	ASDE_dark_offset_slope	4	0x08	RW	[3:0] ASDE_dark_offset_slope

Revision History

Version V1.0 2014.02.14

- Document Release