

# 实验1 学习使用gem5模拟器

## 1 编译gem5模拟器

运行下列指令，配置环境后对gem5模拟器进行编译：

```
sudo apt install build-essential git m4 scons zlib1g zlib1g-dev libprotobuf-dev
protobuf-compiler libprotoc-dev libgoogle-perftools-dev python-dev python
sudo apt install libhdf5-dev
sudo apt install libpng-dev
scons build/X86/gem5.opt -j7
CPU_MODELS=AtomicSimpleCPU,TimingSimpleCPU,O3CPU,MinorCPU
```

编译后terminal显示结果如下，编译后得到的可执行文件可以在 build 文件夹下找到：

```
mingkai@mingkai-HP-ZHAN-66-Pro-14-G2-~/Course/architecture/calab-gem5/gem5-stable
(base) → gem5-stable git:(master) X scons build/X86/gem5.opt -j7 CPU_MODELS=AtomicSimpleCPU,TimingSimpleCPU,O3CPU,MinorCPU
scons: Reading SConscript files ...
Checking for linker -Wl,--as-needed support... yes
Checking for compiler -Wno-free-nonheap-object support... yes
Checking for compiler -Oz support... yes
Checking for linker -Oz support... yes
Info: Using Python config: python3-config
Checking for C header file Python.h... yes
Checking Python version... 3.8.10
Checking for accept(0,0,0) in C++ library None... yes
Checking for zlibVersion() in C++ library z... yes
Checking for C library tcalloc... yes
Checking for shm_open("/test", 0, 0) in C library None... no
Checking for shm_open("/test", 0, 0) in C library rt... yes
Checking for char temp; backtrace_symbols_fd((void *)&temp, 0, 0) in C library None... yes
Checking for C header file linux/kvm.h... yes
Checking for timer_create(CLOCK_MONOTONIC, NULL, NULL) in C library None... yes
Checking size of struct kvm_xsave ... yes
Checking for member exclude_host in struct perf_event_attr...yes
Checking for pkg-config package protobuf... yes
Checking for GOOGLE_PROTOBUF_VERIFY_VERSION in C++ library protobuf... yes
Checking for C header file linux/if_tun.h... yes
Checking for C header file fenv.h... yes
Checking for C header file png.h... yes
Checking for clock_nanosleep(0,0,NULL,NULL) in C library None... yes
Checking for C header file valgrind/valgrind.h... no
Warning: Deprecated namespaces are not supported by this compiler.
Please make sure to check the mailing list for deprecation announcements.
Checking for pkg-config package hdf5-serial... yes
Checking for H5Fcreate("", 0, 0, 0) in C library hdf5... yes
Checking for H5:HSFfile("", 0) in C++ library hdf5_cpp... yes
Checking whether __l306__ is declared... no
Checking whether __x86_64__ is declared... yes
Building in /home/mingkai/Course/architecture/calab-gem5/gem5-stable/build/X86
Variables file /home/mingkai/Course/architecture/calab-gem5/gem5-stable/build/variables/X86 not found,
using defaults in /home/mingkai/Course/architecture/calab-gem5/gem5-stable/build_opts/X86
Checking for compiler -Wno-self-assign-overloaded support... yes
scons: done reading SConscript files.
scons: Building targets ...
[ CXX ] X86/python/gem5py.cc -> .pyo
[ SLIC ] src/mem/ruby/protocol/MESI_Two_Level.slice -> X86/mem/ruby/protocol/AccessPermission.cc, X86/mem/ruby/protocol/AccessPermission.hh, X86/mem/ruby/protocol/AccessType.cc, X86/mem/ruby/protocol/AccessType.hh, X86/mem/ruby/protocol/CacheRequestType.cc, X86/mem/ruby/protocol/CacheRequestType.hh, X86/mem/ruby/protocol/CacheResourceType.cc, X86/mem/ruby/protocol/CacheResourceType.hh, X86/mem/ruby/protocol/CoherenceRequestType.cc, X86/mem/ruby/protocol/CoherenceRequestType.hh, X86/mem/ruby/protocol/CoherenceResponseType.cc, X86/mem/ruby/protocol/CoherenceResponseType.hh, X86/mem/ruby/protocol/DMASequencerRequestType.cc, X86/mem/ruby/protocol/DMASequencerRequestType.hh, X86/mem/ruby/protocol/DMA_Controller.cc, X86/mem/ruby/protocol/DMA_Controller.hh, X86/mem/ruby/protocol/DMA_Controller.py, X86/mem/ruby/protocol/DMA_Controller.pyi
```

```
mingkai@mingkai-HP-ZHAN-66-Pro-14-G2-~/Course/architecture/calab-gem5/gem5-stable
[ SHCC ] softfloat/s_shortShiftRightJan64Extra.c -> .os
[ SHCC ] softfloat/s_shortShiftRightM.c -> .os
[ SHCC ] softfloat/s_sub128.c -> .os
[ SHCC ] softfloat/s_sub1XM.c -> .os
[ SHCC ] softfloat/s_sub256M.c -> .os
[ SHCC ] softfloat/s_subMagsF128.c -> .os
[ SHCC ] softfloat/s_subMagsF16.c -> .os
[ SHCC ] softfloat/s_subMagsF32.c -> .os
[ SHCC ] softfloat/s_subMagsF64.c -> .os
[ SHCC ] softfloat/s_subM.c -> .os
[ SHCC ] softfloat/ui32_to_f128.c -> .os
[ SHCC ] softfloat/ui32_to_f16.c -> .os
[ SHCC ] softfloat/ui32_to_f32.c -> .os
[ SHCC ] softfloat/ui32_to_f64.c -> .os
[ SHCC ] softfloat/ui64_to_f128.c -> .os
[ SHCC ] softfloat/ui64_to_f16.c -> .os
[ SHCC ] softfloat/ui64_to_f32.c -> .os
[ SHCC ] softfloat/ui64_to_f64.c -> .os
[ SHCXX ] drampower/src/CommandAnalysis.cc -> .os
[ SHCXX ] drampower/src/MemArchitectureSpec.cc -> .os
[ SHCXX ] drampower/src/MemCommand.cc -> .os
[ AR ] -> softfloat/libsoftfloat.a
[ SHCXX ] drampower/src/MemPowerSpec.cc -> .os
[ RANLIB ] -> softfloat/libsoftfloat.a
[ SHCXX ] drampower/src/MemTimingSpec.cc -> .os
[ SHCXX ] drampower/src/MemoryPowerModel.cc -> .os
[ SHCXX ] drampower/src/MemorySpecification.cc -> .os
[ SHCXX ] drampower/src/Parameter.cc -> .os
[ SHCXX ] drampower/src/Parametrizable.cc -> .os
[ SHCXX ] drampower/src/libdrampower/LibDRAMPower.cc -> .os
[ SHCXX ] drampower/src/CAHelpers.cc -> .os
[ SHCXX ] drampower/src/CndHandlers.cc -> .os
[ SHCXX ] drampower/src/MemBankWiseParams.cc -> .os
[ SHCXX ] tostream3/zfstream.cc -> .os
[ AR ] -> drampower/libdrampower.a
[ RANLIB ] -> drampower/libdrampower.a
[ AR ] -> tostream3/libtoastream3.a
[ RANLIB ] -> tostream3/libtoastream3.a
[ CXX ] X86/base/date.cc -> .o
[ LINK ] -> X86/gem5.opt
scons: done building targets.
*** Summary of Warnings ***
Warning: Deprecated namespaces are not supported by this compiler.
Please make sure to check the mailing list for deprecation announcements.
(base) → gem5-stable git:(master) X
```

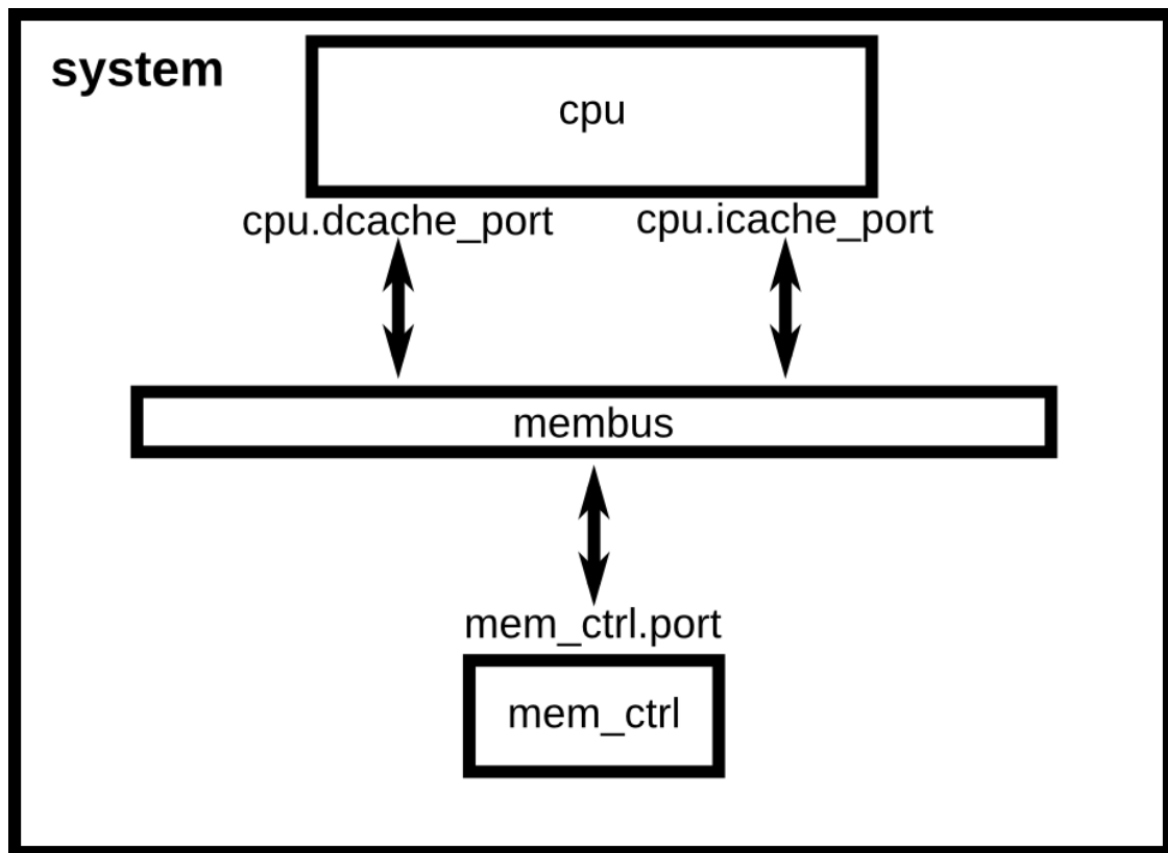
## 2 运行 simple.py

```
(base) → gem5-stable git:(master) X build/X86/gem5.opt configs/tutorial/part1/simple.py
gem5 Simulator System.  http://gem5.org
gem5 is copyrighted software; use the --copyright option for details.

gem5 version 21.2.1.0
gem5 compiled Mar 16 2022 21:30:22
gem5 started Mar 17 2022 20:44:55
gem5 executing on mingkai-HP-ZHAN-66-Pro-14-G2, pid 5815
command line: build/X86/gem5.opt configs/tutorial/part1/simple.py

Global frequency set at 1000000000000 ticks per second
warn: No dot file generated. Please install pydot to generate the dot file and pdf.
build/X86/mem/mem_interface.cc:791: warn: DRAM device capacity (8192 Mbytes) does not match the address range assigned (512 Mbytes)
0: system.remote_gdb: listening for remote gdb on port 7000
Beginning simulation!
build/X86/sim/simulate.cc:194: info: Entering event queue @ 0. Starting simulation...
Hello world!
Exiting @ tick 508536000 because exiting with last active thread context
(base) → gem5-stable git:(master) X
```

simple.py 描述了如下的体系结构：



由于所有的class都是系统预设的，所以可以直接将这些预设class实例化。需要注意的是，在port之间的连接时，需要遵循request port到response port的连接准则。具体来说，request port作为=的左值，response port作为=的右值，如此进行port之间的连接。另外一点需要注意的是，在设置path时（包括binary的path和调用包的path），需要根据当前python程序的实际位置进行相对位置的设置。

## 3 运行 two\_level.py

```

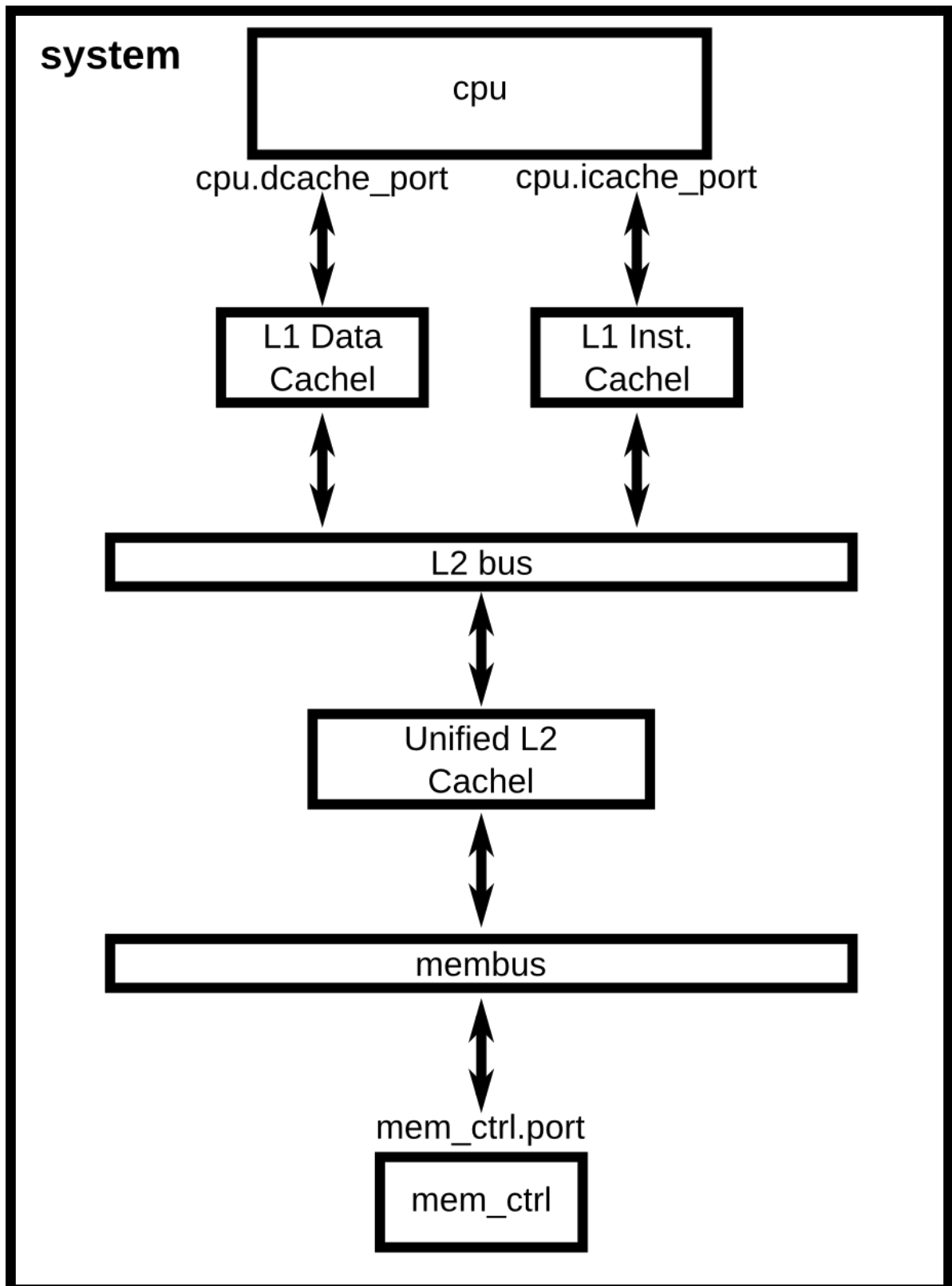
(base) → gem5-stable git:(master) X build/X86/gem5.opt configs/tutorial/part1/two_level.py --l2_size='1MB' --l1d_size='128kB'
gem5 Simulator System. http://gem5.org
gem5 is copyrighted software; use the --copyright option for details.

gem5 version 21.2.1.0
gem5 compiled Mar 16 2022 21:30:22
gem5 started Mar 17 2022 20:47:48
gem5 executing on mingkai-HP-ZHAN-66-Pro-14-G2, pid 6105
command line: build/X86/gem5.opt configs/tutorial/part1/two_level.py --l2_size=1MB --l1d_size=128kB

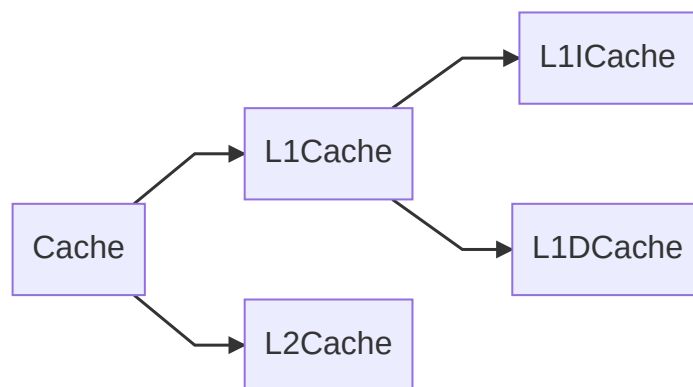
Global frequency set at 100000000000 ticks per second
warn: No dot file generated. Please install pydot to generate the dot file and pdf.
build/X86/mem/mem_interface.cc:791: warn: DRAM device capacity (8192 Mbytes) does not match the address range assigned (512 Mbytes)
0: system.remote_gdb: listening for remote gdb on port 7000
Beginning simulation!
build/X86/sim/simulate.cc:194: info: Entering event queue @ 0. Starting simulation...
Hello world!
Exiting @ tick 58125000 because exiting with last active thread context
(base) → gem5-stable git:(master) X

```

two\_level.py 描述了如下的体系结构：



由于L1的Data Cache、Instruction Cache和L2 Cache都是自定义的，这些class需要在 `cache.py` 中进行定义。它们之间的继承关系如下所示：



在对这些class进行妥善定义后，对各个部件进行实例化。和 `simple.py` 类似，按照request port到response port的连接方式即可在 `two_level.py` 中对该体系结构进行描述。需要注意的是，任意两个部件之间需要有bus的参与，它们往往在系统中以预设的class存在。