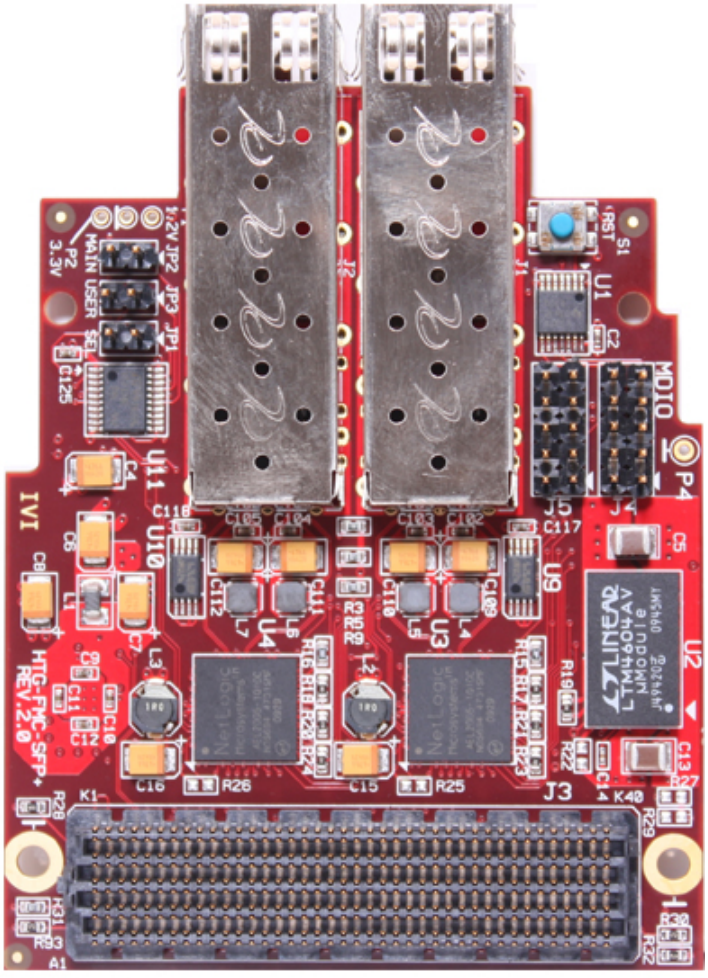
Vita57 SFP+ FMC Module User Manual

HTG-FMC-SFP-PLUS

Version 3.0 January 2011



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Revision History

Date	Version	Notes
02/21/2010	1.0	Preliminary
11/01/2010	2.0	
1/12/2011	3.0	Adding additional FMC/FPGA control lines

Table of Contents:

1) Introduction:

Vita 57 provides a mechanical standard for I/O mezzanine modules. This standard introduces a methodology that shall allow the front panel IO of IEEE 1101 form factor cards to be configured via mezzanine boards. Vita 57 modules have fixed locations for serial/parallel IOs, clocks, Jtag signals, VCC, and GND. HiTech Global's Vita 57 modules can be plugged into any Vita 57 based boards.

The FMC standard specifies Samtec's SEARAY™ connector set. The VITA 57 SEAM/SEAF Series system provides 400 I/Os in a 40 x 10 configuration or 160 I/Os in a selectively loaded 40 x 10 configuration, in 8.5mm and 10mm stack heights.

The SFP+ FMC Module (HTG-FMC-SFP-PLUS) is a FPGA Mezzanine Connector (FMC) daughter card with two SFP+ ports interfacing to total of 8 serial transceivers (XAUI)

2) Main Features:

- Two SFP+ Connectors
- 156.25MHz for 10Gig operation
- 125.00MHz for 1Gig operation
- Additional clock controlled by FPGA
- Three EEPROMs
- FMC Connector
- MDIO Headers
- Parallel Port Header

3) Block Diagram

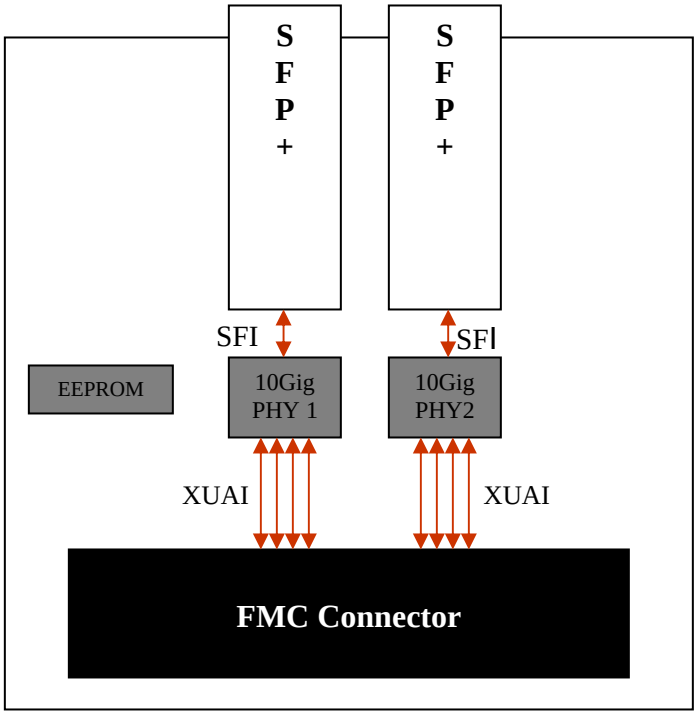


Figure (1): Primary Side

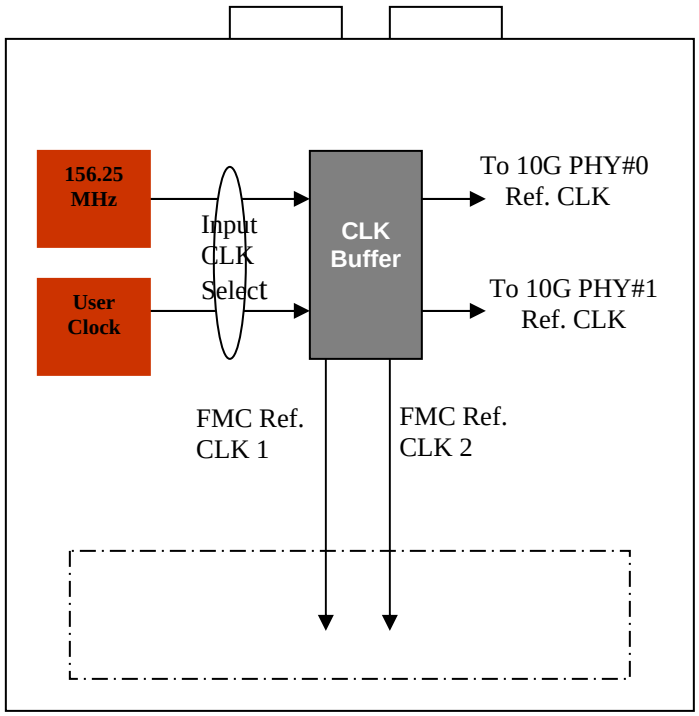


Figure (2): Secondary Side

4) SFP + Interface

To create a 10G SFP+ interface, four FPGA serial transceivers (each @ 3.125Gbps) are connected to the Netlogic ALE2005 PHY using XAUI protocol. Figure (3) illustrates the SFP+ implementation.

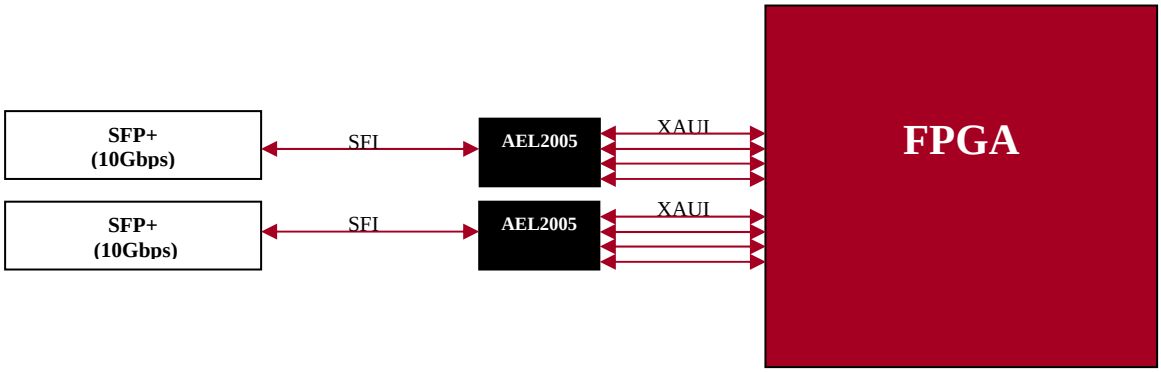


Figure (3): SFP+ Interface

The AEL2005 is a bidirectional single-channel 10 Gigabit Ethernet/10 Fibre Channel transceiver contacting integrated electronic desperation compensation (EDC) circuits targeted for 10GBASE-LRM optical modules and 10Gbps SFP+ applications. The consolidation of the receiver and transmitter physical layer (PHY) functions on a single ship is combined with the integration of an EDC block, integrated clock drivers, multiple loopback and PRBS for both the line side and the system side.

The AEL2005 device is compliant with the following specifications:

- IEEE 802.3ae 10 Gigabit Ethernet
- IEEE 802.3aq 10 GBASE-LRM
- INCITS TII 10 Gigabit Fibre Channel
- XENPAK MS Rev. 3.0
- X2 MSA, Rev. 1.0b
- XPAK MSA, Rev. 2.3
- SFP+ MSA, Rev. 3.0

4.1) Clock Generation for FPGA Serial Transceivers & 10GE PHY

The 10GE PHY (Netlogic AEL2005) device incorporates a flexible clocking methodology wherein 10.3125 Gbps LAN and 10.51875 Gbps SAN data rates may all be generated within the device using a flexible clock synthesizer. This capability allows the use a crystal oscillator at the 10Gigabit Ethernet frequency of 156.25 MHz . If the AEL2005 is used only in SAN mode, the clock input to a crystal oscillator at the 10 Gigabit Fibre Channel frequency of 159.375 MHz. An overview of clocking configurations is provided in the AEL2005 device datasheet.

Serial Transmit Clock frequencies are shown by table (1).

Mode	Reference	Input Frequency	Output Frequency (HSTXCLK)	Output Frequency (HSTXCLK) Divide by 64 Mode
10 Gigabit Ethernet	CMU_REF Clock Synthesizer	156.25 MHz	10.3125 GHz	161.13 MHz
10 Gigabit Fibre Channel	CMU_REF Clock Synthesizer	159.375 MHz	10.5175 GHz	164.36 MHz

Table (1) Serial Transmit Clock Frequencies

Clock generation and distribution for the HTG-FMC-SFP-PLUS module is illustrated by figure (4).

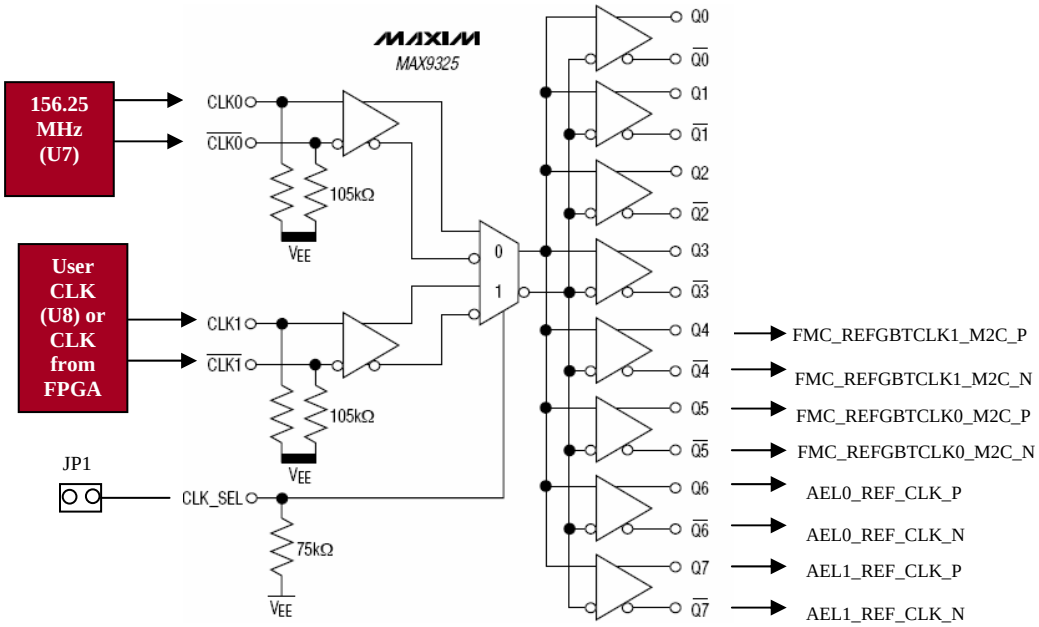


Figure (4): Clock Generation & Distribution

"U8" can be populated by a 125.00MHz clock for 1.0Gig Ethernet or 159.375 for 10Gig Fibre channel applications. C113 and C114 capacitors should be installed (0.1uF) when these clocks are used. Differential clock from FPGA can also be used instead of using clock installed on the "U8". This differential clock is provided through 'K4" and "K5"pins of the FMC connector. This clock can also be enabled/disabled through FPGA. The "JP1" header should be used for clock selection.

4.2) AEL2005 Initialization for SFP+ Compliant

Table (2) lists necessary and optional register writes for bringing up the AEL2005 in the SFP+ compliant configuration. Since the RX_LOS input of the AEL2005 is active high by default, it needs to be changed to active low to comply to the SFP+ MSA. When following the Aeluros layout recommendation for the HSRXDATA differential trace, the polarity of this input

needs to be flipped in the software configuration. One additional feature that the AEL2005 offers, is the RX and TX activity LEDs. When activated by one register write, the CMU_LOL and the CDR_LOL output pins get reconfigured as LED output drivers. The LEDs will toggle whenever valid 10GE packets are received or transmitted.

Register bits	Content	Optional	Function
1.C017.5	1		Flip polarity of RX_LOS input to be active low.
1.C01F.5	1		Flip polarity of HSRXDATA input to facilitate layout of the differential trace from the SFP+ receiver output pins to the AEL2005 receiver input pins.
1.C214.3:0 1.C217.15:0	9 0xFF00	X	Enable RX activity LED indicator when receiving valid 10Gb Ethernet packages.
1.C214.7:4 1.C216.15:0	0 0xCCCC	X	Enable TX activity LED indicator when transmitting valid 10Gb Ethernet packages.

Table (2): Initialization Register Writes for the AEL2005

After the mandatory power on reset, the AEL2005 reads in the contents of an EEPROM at address 0xA0 in RevB and 0xA8 in RevC on the I2C bus for internal initialization. The necessary register writes can be accomplished by this patching sequence. Since the patch space accessible by the EEPROM is limited from 1.C000 to 1.C01F the optional writes need to be accomplished by an external u-controller. Table (3) lists the registers that need to be written to the EEPROM for patching upon reset:

EEPROM Register	Data	Function
A0.C0	0x17	Set register 1.C017[7:0] to 0xB0 (Flip polarity of RX_LOS input)
A0.C1	0xB0	
A0.C2	0x1F	Set register 1.C01F[7:0] to 0x28 (Flip polarity of HSRXDATA input)
A0.C3	0x28	

Table (3): EEPROM Register Contents for Patching of the AEL2005 upon Reset

4.3) LEDs

D7: SFP1 _RX_LOS
D8: ALE1_RX_ACTIVITIY (U3)
D9: ALE1_TX_ACTIVITIY (U3)
D11: SFP0 _RX_LOS
D12: ALE0_RX_ACTIVITIY (U4)
D13: ALE0_TX_ACTIVITIY (U4)
D4: 3.3V Power
D5: 1.2V Power

5) FMC Interface

The SFP+ Module is populated with a 400-pin Samtec connector for implementation of Vita 57 FPGA Mezzanine Card (FMC) interface. The Vita57 calls for fixed location of IOs, Power, Clocks, and JTAG signals so any compliant module can easily be pluggable into any compliant carrier card.

The FMC connector provides access to 8 Serial Transceivers (on the FPGA side) JTAG signals, 12V/3.3V/Adjustable supplies, I2C signals, and multiple differential clocks.

Table (4) and (5) illustrate pin assignment for the FMC connector interface.

	K	J	H	G	F	E	D	C	B	A
1	VREF_B_M2C	GND	VREF_A_M2C	GND	PG_M2C	GND	PG_C2M	GND	CLK_DIR	GND
2	GND	CLK3_BIDIR_P	PRSNT_M2C_L	CLK1_M2C_P	GND	HA01_P_CC	GND	DP0_C2M_P	GND	DP1_M2C_P
3	GND	CLK3_BIDIR_N	GND	CLK1_M2C_N	GND	HA01_N_CC	GND	DP0_C2M_N	GND	DP1_M2C_N
4	CLK2_BIDIR_P	GND	CLK0_M2C_P	GND	HA00_P_CC	GND	GBTCLK0_M2C_P	GND	DP9_M2C_P	GND
5	CLK2_BIDIR_N	GND	CLK0_M2C_N	GND	HA00_N_CC	GND	GBTCLK0_M2C_N	GND	DP9_M2C_N	GND
6	GND	HA03_P	GND	LA00_P_CC	GND	HA05_P	GND	DP0_M2C_P	GND	DP2_M2C_P
7	HA02_P	HA03_N	LA02_P	LA00_N_CC	HA04_P	HA05_N	GND	DP0_M2C_N	GND	DP2_M2C_N
8	HA02_N	GND	LA02_N	GND	HA04_N	GND	LA01_P_CC	GND	DP8_M2C_P	GND
9	GND	HA07_P	GND	LA03_P	GND	HA09_P	LA01_N_CC	GND	DP8_M2C_N	GND
10	HA06_P	HA07_N	LA04_P	LA03_N	HA08_P	HA09_N	GND	LA05_P	GND	DP3_M2C_P
11	HA06_N	GND	LA04_N	GND	HA08_N	GND	LA05_P	LA05_N	GND	DP3_M2C_N
12	GND	HA11_P	GND	LA08_P	GND	HA13_P	LA05_N	GND	DP7_M2C_P	GND
13	HA10_P	HA11_N	LA07_P	LA08_N	HA12_P	HA13_N	GND	GND	DP7_M2C_N	GND
14	HA10_N	GND	LA07_N	GND	HA12_N	GND	LA09_P	LA10_P	GND	DP4_M2C_P
15	GND	HA14_P	GND	LA12_P	GND	HA16_P	LA09_N	LA10_N	GND	DP4_M2C_N
16	HA17_P_CC	HA14_N	LA11_P	LA12_N	HA15_P	HA16_N	GND	GND	DP5_M2C_P	GND
17	HA17_N_CC	GND	LA11_N	GND	HA15_N	GND	LA13_P	GND	DP5_M2C_N	GND
18	GND	HA18_P	GND	LA16_P	GND	HA20_P	LA13_N	LA14_P	GND	DP5_M2C_P
19	HA21_P	HA18_N	LA15_P	LA16_N	HA19_P	HA20_N	GND	LA14_N	GND	DP5_M2C_N
20	HA21_N	GND	LA15_N	GND	HA19_N	GND	LA17_P_CC	GND	GBTCLK1_M2C_P	GND
21	GND	HA22_P	GND	LA20_P	GND	HB03_P	LA17_N_CC	GND	GBTCLK1_M2C_N	GND
22	HA23_P	HA22_N	LA19_P	LA20_N	HB02_P	HB03_N	GND	LA18_P_CC	GND	DP1_C2M_P
23	HA23_N	GND	LA19_N	GND	HB02_N	GND	LA23_P	LA18_N_CC	GND	DP1_C2M_N
24	GND	HB01_P	GND	LA22_P	GND	HB05_P	LA23_N	GND	DP9_C2M_P	GND
25	HB00_P_CC	HB01_N	LA21_P	LA22_N	HB04_P	HB05_N	GND	GND	DP9_C2M_N	GND
26	HB00_N_CC	GND	LA21_N	GND	HB04_N	GND	LA26_P	LA27_P	GND	DP2_C2M_P
27	GND	HB07_P	GND	LA25_P	GND	HB09_P	LA26_N	LA27_N	GND	DP2_C2M_N
28	HB06_P_CC	HB07_N	LA24_P	LA25_N	HB08_P	HB09_N	GND	GND	DP8_C2M_P	GND
29	HB06_N_CC	GND	LA24_N	GND	HB08_N	GND	TCK	GND	DP8_C2M_N	GND
30	GND	HB11_P	GND	LA29_P	GND	HB13_P	TDI	SCL	GND	DP3_C2M_P
31	HB10_P	HB11_N	LA28_P	LA29_N	HB12_P	HB13_N	TDO	SDA	GND	DP3_C2M_N
32	HB10_N	GND	LA28_N	GND	HB12_N	GND	3P3VAUX	GND	DP7_C2M_P	GND
33	GND	HB15_P	GND	LA31_P	GND	HB19_P	TMS	GND	DP7_C2M_N	GND
34	HB14_P	HB15_N	LA30_P	LA31_N	HB16_P	HB19_N	TRST_L	GA0	GND	DP4_C2M_P
35	HB14_N	GND	LA30_N	GND	HB16_N	GND	GA1	12P0V	GND	DP4_C2M_N
36	GND	HB18_P	GND	LA33_P	GND	HB21_P	3P3V	GND	DP6_C2M_P	GND
37	HB17_P_CC	HB18_N	LA32_P	LA33_N	HB20_P	HB21_N	GND	12P0V	DP6_C2M_N	GND
38	HB17_N_CC	GND	LA32_N	GND	HB20_N	GND	3P3V	GND	GND	DP5_C2M_P
39	GND	VIO_B_M2C	GND	VADJ	GND	VADJ	GND	3P3V	GND	DP5_C2M_N
40	VIO_B_M2C	GND	VADJ	GND	VADJ	GND	3P3V	GND	RES0	GND
			LPC Connector	LPC Connector			LPC Connector	LPC Connector		

Table (4): FMC Pin Assignment

	Column "B"				Column "A"		
	FMC Pin Name	Pin Description	DEST.		FMC Pin Name	Pin Description	DEST.
1	CLK_DIR	Reserved	3..3V	1	GND	GND	
2	GND	GND		2	DP1_M2C_P	AEL0_DP[1]_M2C_P	U4-5
3	GND	GND		3	DP1_M2C_N	AEL0_DP[1]_M2C_N	U4-4
4	DP9_M2C_P	NC	NC	4	GND	GND	
5	DP9_M2C_N	NC	NC	5	GND	GND	
6	GND	GND		6	DP2_M2C_P	AEL0_DP[2]_M2C_P	U4-8
7	GND	GND		7	DP2_M2C_N	AEL0_DP[2]_M2C_N	U4-9
8	DP8_M2C_P	NC	NC	8	GND	GND	
9	DP8_M2C_N	NC	NC	9	GND	GND	
10	GND	GND		10	DP3_M2C_P	AEL0_DP[3]_M2C_P	U4-13
11	GND	GND		11	DP3_M2C_N	AEL0_DP[3]_M2C_N	U4-12
12	DP7_M2C_P	AEL1_DP[0]_M2C_P	U3-2	12	GND	GND	
13	DP7_M2C_N	AEL1_DP[0]_M2C_N	U3-1	13	GND	GND	
14	GND	GND		14	DP4_M2C_P	AEL1_DP[2]_M2C_P	U3-8
15	GND	GND		15	DP4_M2C_N	AEL1_DP[2]_M2C_N	U3-9
16	DP6_M2C_P	AEL1_DP[1]_M2C_P	U3-5	16	GND	GND	
17	DP6_M2C_N	AEL1_DP[1]_M2C_N	U3-4	17	GND	GND	
18	GND	GND		18	DP5_M2C_P	AEL1_DP[3]_M2C_P	U3-13
18	GND	GND		18	DP5_M2C_N	AEL1_DP[3]_M2C_N	U3-12
20	GBTCLK1_M2C_P	FMC_REF_CLK1_P	U6-23	20	GND	GND	
21	GBTCLK1_M2C_N	FMC_REF_CLK1_P	U6-22	21	GND	GND	
22	GND	GND		22	DP1_C2M_P	AEL0_DP[1]_C2M_P	U4-20
23	GND	GND		23	DP1_C2M_N	AEL0_DP[1]_C2M_N	U4-19
24	DP9_C2M_P	NC	NC	24	GND	GND	
25	DP9_C2M_N	NC	NC	25	GND	GND	
26	GND	GND		26	DP2_C2M_P	AEL0_DP[2]_C2M_P	U4-23
27	GND	GND		27	DP2_C2M_N	AEL0_DP[2]_C2M_N	U4-24
28	DP8_C2M_P	NC	NC	28	GND	GND	
29	DP8_C2M_N	NC	NC	29	GND	GND	
30	GND	GND		30	DP3_C2M_P	AEL0_DP[3]_C2M_P	U4-27
31	GND	GND		31	DP3_C2M_N	AEL0_DP[3]_C2M_N	U4-26
32	DP7_C2M_P	AEL1_DP[0]_C2M_P	U3-16	32	GND	GND	
33	DP7_C2M_N	AEL1_DP[0]_C2M_V	U3-17	33	GND	GND	
34	GND	GND		34	DP4_C2M_P	AEL1_DP[2]_C2M_P	U3-23
35	GND	GND		35	DP4_C2M_N	AEL1_DP[2]_C2M_N	U3-24
36	DP6_C2M_P	AEL1_DP[1]_C2M_P	U3-20	36	GND	GND	
37	DP6_C2M_N	AEL1_DP[1]_C2M_N	U3-19	37	GND	GND	
38	GND	GND		38	DP5_C2M_P	AEL1_DP[3]_C2M_P	U3-27
39	GND	GND		39	DP5_C2M_N	AEL1_DP[3]_C2M_N	U3-26
40	RES0	NC		40	GND	GND	

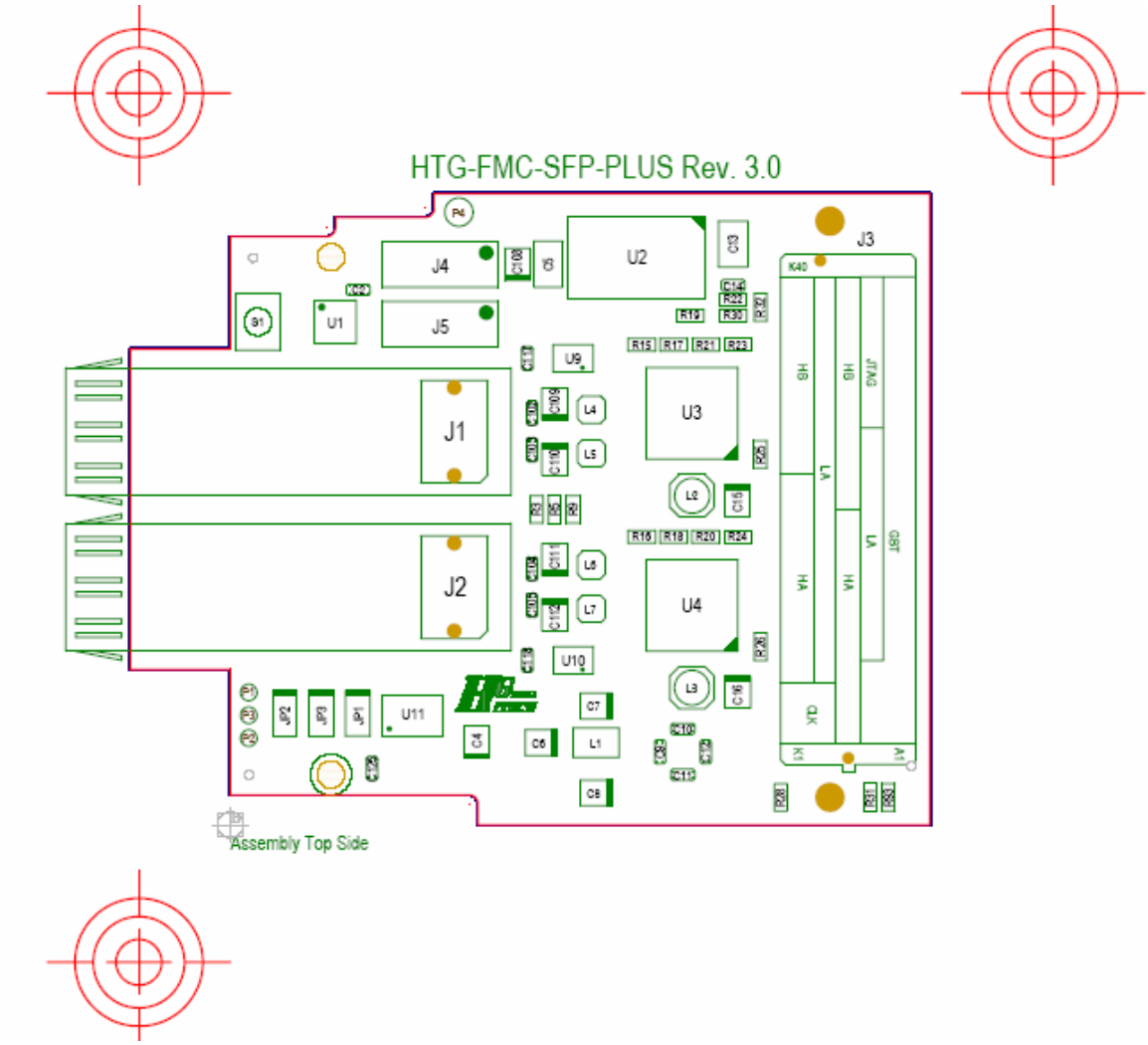
	Column "D"				Column " C"		
	FMC Pin Name	Pin Description	DEST.		FMC Pin Name	Pin Description	DEST.
1	PG_C2M	Power Good	D3	1	GND	NC	
2	GND	GND		2	DP0_C2M_P	AEL0_DP[0]_C2M_P	U4-16
3	GND	GND		3	DP0_C2M_N	AEL0_DP[0]_C2M_N	U4-17
4	GBTCLK0_M2C_P	FMC_REF_CLK0_P	U6-16	4	GND	GND	
5	GBTCLK0_M2C_N	FMC_REF_CLK0_P	U6-15	5	GND	GND	
6	GND	GND		6	DP0_M2C_P	AEL0_DP[0]_M2C_P	U4-2
7	GND	GND		7	DP0_M2C_N	AEL0_DP[0]_M2C_N	U4-1
8	LA01_P_CC	SFP0_SCL	U4-36	8	GND	GND	
9	LA01_N_CC	SFP0_SDA	U4-35	9	GND	GND	
10	GND	GND		10	LA06_P	NC	NC
11	LA05_P	User defined signal	NC	11	LA06_N	NC	NC
12	LA05_N	User defined signal	NC	12	GND	GND	
13	GND	GND		13	GND	GND	
14	LA09_P	User defined signal	NC	14	LA10_P	NC	NC
15	LA09_N	User defined signal	NC	15	LA10_N	NC	NC
16	GND	GND		16	GND	GND	
17	LA13_P	User defined signal	NC	17	GND	GND	
18	LA13_N	User defined signal	NC	18	LA14_P	NC	NC
18	GND	GND		18	LA14_N	NC	NC
20	LA17_P_CC	User defined signal	NC	20	GND	GND	
21	LA17_N_CC	User defined signal	NC	21	GND	GND	
22	GND	GND		22	LA18_P_CC	NC	NC
23	LA23_P	User defined signal	NC	23	LA18_N_CC	NC	NC
24	LA23_N	User defined signal	NC	24	GND	GND	
25	GND	GND		25	GND	GND	
26	LA26_P	User defined signal	NC	26	LA27_P	NC	NC
27	LA26_N	User defined signal	NC	27	LA27_N	NC	NC
28	GND	GND		28	GND	GND	
29	TCK	JTAG		29	GND	GND	
30	TDI	JTAG BYPASS		30	SCL	I2C serial clock.	U5 -6
31	TDO	JTAG		31	SDA	I2C serial data.	U5 -5
32	3P3VAUX	3.3V Aux. Supply	3.3V	32	GND	GND	-
33	TMS	JTAG		33	GND	GND	-
34	TRST_L	Asynch. Init.		34	GA0	Geographical address	U5-1
35	GA1	Geographical address	U5-2	35	12P0V	12V Supply	
36	3P3V	3.3V Supply	3.3V	36	GND	GND	
37	GND	GND	GND	37	12P0V	12V Supply	
38	3P3V	3.3V Supply	3.3V	38	GND	GND	
39	GND	GND	GND	39	3P3V	3.3V Supply	
40	3P3V	3.3V Supply	3.3V	40	GND	GND	

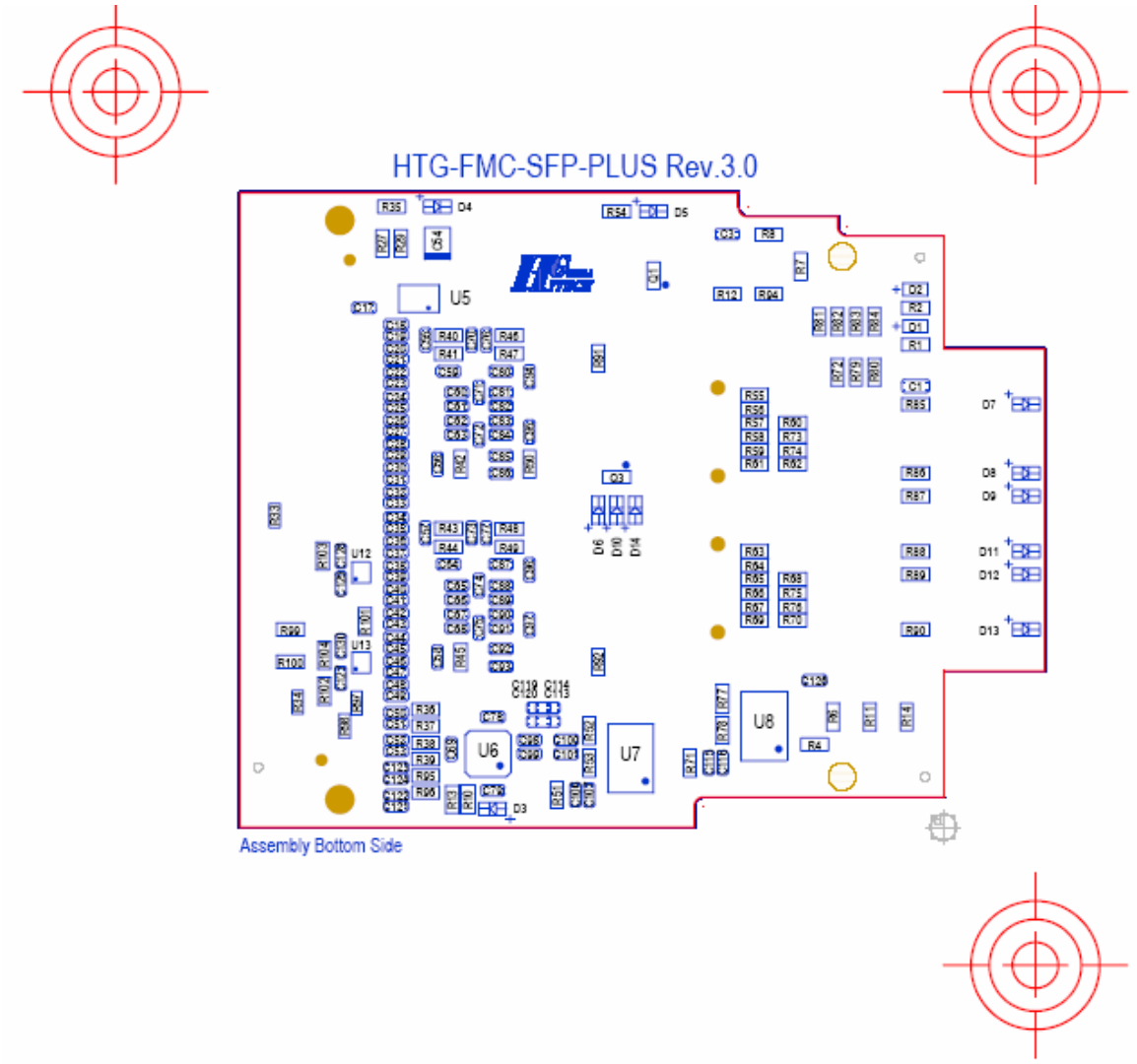
	Column "F"				Column "E"		
	FMC Pin Name	Pin Description	DEST.		FMC Pin Name	Pin Description	DEST.
1	PG_M2C	Power Good	3.3V	1	GND	GND	GND
2	GND	GND	GND	2	HA01_P_CC	User defined signal	NC
3	GND	GND	GND	3	HA01_N_CC	User defined signal	NC
4	HA00_P_CC	User defined signal	NC	4	GND	GND	GND
5	HA00_N_CC	User defined signal	NC	5	GND	GND	GND
6	GND	GND	GND	6	HA05_P	User defined signal	NC
7	HA04_P	User defined signal	NC	7	HA05_N	User defined signal	NC
8	HA04_N	User defined signal	NC	8	GND	GND	GND
9	GND	GND	GND	9	HA09_P	User defined signal	NC
10	HA08_P	User defined signal	NC	10	HA09_N	User defined signal	NC
11	HA08_N	User defined signal	NC	11	GND	GND	GND
12	GND	GND	GND	12	HA13_P	User defined signal	NC
13	HA12_P	User defined signal	NC	13	HA13_N	User defined signal	NC
14	HA12_N	User defined signal	NC	14	GND	GND	GND
15	GND	GND	GND	15	HA16_P	User defined signal	NC
16	HA15_P	User defined signal	NC	16	HA16_N	User defined signal	NC
17	HA15_N	User defined signal	NC	17	GND	GND	GND
18	GND	GND	GND	18	HA20_P	User defined signal	NC
18	HA19_P	User defined signal	NC	18	HA20_N	User defined signal	NC
20	HA19_N	User defined signal	NC	20	GND	GND	GND
21	GND	GND	GND	21	HB03_P	User defined signal	NC
22	HB02_P	User defined signal	NC	22	HB03_N	User defined signal	NC
23	HB02_N	User defined signal	NC	23	GND	GND	GND
24	GND	GND	GND	24	HB05_P	User defined signal	NC
25	HB04_P	User defined signal	NC	25	HB05_N	User defined signal	NC
26	HB04_N	User defined signal	NC	26	GND	GND	GND
27	GND	GND	GND	27	HB09_P	User defined signal	NC
28	HB08_P	User defined signal	NC	28	HB09_N	User defined signal	NC
29	HB08_N	User defined signal	NC	29	GND	GND	GND
30	GND	GND	GND	30	HB13_P	User defined signal	NC
31	HB12_P	User defined signal	NC	31	HB13_N	User defined signal	NC
32	HB12_N	User defined signal	NC	32	GND	GND	GND
33	GND	GND	GND	33	HB19_P	User defined signal	NC
34	HB16_P	User defined signal	NC	34	HB19_N	User defined signal	NC
35	HB16_N	User defined signal	NC	35	GND	GND	GND
36	GND	GND	GND	36	HB21_P	User defined signal	NC
37	HB20_P	User defined signal	NC	37	HB21_N	User defined signal	NC
38	HB20_N	User defined signal	NC	38	GND	GND	GND
39	GND	GND	GND	39	VADJ	Adjustable Voltage	
40	VADJ	Adjustable Voltage		40	GND	GND	GND

	Column "H"				Column "G"		
	FMC Pin Name	Pin Description	DEST.		FMC Pin Name	Pin Description	DEST.
1	VREF_A_M2C	Reference voltage		1	GND	GND	GND
2	PRSNT_M2C_L	Present Signal		2	CLK1_M2C_P	CLK1_M2C_P	NC
3	GND	GND	GND	3	CLK1_M2C_N	CLK1_M2C_N	NC
4	CLK0_M2C_P	CLK0_M2C_P	U6-19	4	GND	GND	GND
5	CLK0_M2C_N	CLK0_M2C_N	U6-17	5	GND	GND	GND
6	GND	GND	GND	6	LA00_P_CC	MDC_F	U11-18
7	LA02_P	SFP1_SCL	U3-36	7	LA00_N_CC	MDIO-F	U11-16
8	LA02_N	SFP1_SDA	U3-35	8	GND	GND	GND
9	GND	GND	GND	9	LA03_P	EN_CLK_USER_F	U11-4
10	LA04_P	CLK_SEL_F	U11-2	10	LA03_N	EN_CLK_156_F	U11-6
11	LA04_N	User defined signal	NC	11	GND	GND	GND
12	GND	GND	GND	12	LA08_P	User defined signal	NC
13	LA07_P	User defined signal	NC	13	LA08_N	User defined signal	NC
14	LA07_N	User defined signal	NC	14	GND	GND	GND
15	GND	GND	GND	15	LA12_P	User defined signal	NC
16	LA11_P	User defined signal	NC	16	LA12_N	User defined signal	NC
17	LA11_N	User defined signal	NC	17	GND	GND	GND
18	GND	GND	GND	18	LA16_P	User defined signal	NC
18	LA15_P	User defined signal	NC	18	LA16_N	User defined signal	NC
20	LA15_N	User defined signal	NC	20	GND	GND	GND
21	GND	GND	GND	21	LA20_P	User defined signal	NC
22	LA19_P	User defined signal	NC	22	LA20_N	User defined signal	NC
23	LA19_N	User defined signal	NC	23	GND	GND	GND
24	GND	GND	GND	24	LA22_P	User defined signal	NC
25	LA21_P	User defined signal	NC	25	LA22_N	User defined signal	NC
26	LA21_N	User defined signal	NC	26	GND	GND	GND
27	GND	GND	GND	27	LA25_P	User defined signal	NC
28	LA24_P	User defined signal	NC	28	LA25_N	User defined signal	NC
29	LA24_N	User defined signal	NC	29	GND	GND	GND
30	GND	GND	GND	30	LA29_P	User defined signal	NC
31	LA28_P	User defined signal	NC	31	LA29_N	User defined signal	NC
32	LA28_N	User defined signal	NC	32	GND	GND	GND
33	GND	GND	GND	33	LA31_P	User defined signal	NC
34	LA30_P	User defined signal	NC	34	LA31_N	User defined signal	NC
35	LA30_N	User defined signal	NC	35	GND	GND	GND
36	GND	GND	GND	36	LA33_P	User defined signal	NC
37	LA32_P	User defined signal	NC	37	LA33_N	User defined signal	NC
38	LA32_N	User defined signal	NC	38	GND	GND	GND
39	GND	GND	GND	39	VADJ	Adjustable Voltage	
40	VADJ	Adjustable Voltage		40	GND	GND	

	Column "K"				Column "J"		
	FMC Pin Name	Pin Description	DEST.		FMC Pin Name	Pin Description	DEST.
1	VREF_B_M2C	Reference voltage		1	GND	GND	GND
2	GND	GND	GND	2	CLK3_M2C_P	Differential Clock	NC
3	GND	GND	GND	3	CLK3_M2C_N	Differential Clock	NC
4	CLK2_C2M_P	CLK2_C2M_P	U6-7	4	GND	GND	GND
5	CLK2_C2M_N	CLK2_C2M_N	U6-8	5	GND	GND	GND
6	GND	GND	GND	6	HA03_P	User defined signal	NC
7	HA02_P	User defined signal	NC	7	HA03_N	User defined signal	NC
8	HA02_N	User defined signal	NC	8	GND	GND	GND
9	GND	GND	GND	9	HA07_P	User defined signal	NC
10	HA06_P	User defined signal	NC	10	HA07_N	User defined signal	NC
11	HA06_N	User defined signal	NC	11	GND	GND	GND
12	GND	GND	GND	12	HA11_P	User defined signal	NC
13	HA10_P	User defined signal	NC	13	HA11_N	User defined signal	NC
14	HA10_N	User defined signal	NC	14	GND	GND	GND
15	GND	GND	GND	15	HA14_P	User defined signal	NC
16	HA17_P_CC	User defined signal	NC	16	HA14_N	User defined signal	NC
17	HA17_N_CC	User defined signal	NC	17	GND	GND	GND
18	GND	GND	GND	18	HA18_P	User defined signal	NC
18	HA21_P	User defined signal	NC	18	HA18_N	User defined signal	NC
20	HA21_N	User defined signal	NC	20	GND	GND	GND
21	GND	GND	GND	21	HA22_P	User defined signal	NC
22	HA23_P	User defined signal	NC	22	HA22_N	User defined signal	NC
23	HA23_N	User defined signal	NC	23	GND	GND	GND
24	GND	GND	GND	24	HB01_P	User defined signal	NC
25	HB00_P_CC	User defined signal	NC	25	HB01_N	User defined signal	NC
26	HB00_N_CC	User defined signal	NC	26	GND	GND	GND
27	GND	GND	GND	27	HB07_P	User defined signal	NC
28	HB06_P_CC	User defined signal	NC	28	HB07_N	User defined signal	NC
29	HB06_N_CC	User defined signal	NC	29	GND	GND	GND
30	GND	GND	GND	30	HB11_P	User defined signal	NC
31	HB10_P	User defined signal	NC	31	HB11_N	User defined signal	NC
32	HB10_N	User defined signal	NC	32	GND	GND	GND
33	GND	GND	GND	33	HB15_P	User defined signal	NC
34	HB14_P	User defined signal	NC	34	HB15_N	User defined signal	NC
35	HB14_N	User defined signal	NC	35	GND	GND	GND
36	GND	GND	GND	36	HB18_P	User defined signal	NC
37	HB17_P_CC	User defined signal	NC	37	HB18_N	User defined signal	NC
38	HB17_N_CC	User defined signal	NC	38	GND	GND	GND
39	GND	GND	GND	39	VIO_B_M2C	IO Bank Voltage	
40	VIO_B_M2C	IO Bank Voltage		40	GND	GND	

Table (5): FMC Pin Assignment


HTG-FMC-SFP-PLUS Rev. 3.0
Assembly Top Side
J1
J2
J3
J4
J5
U1
U2
U3
U4
U9
U10
U11
S1
P4
JP1
JP2
JP3
K40
HB
HA
LA
JTAG
CLK
GBT


HTG-FMC-SFP-PLUS Rev.3.0
U5
U6
U7
U8
U12
U13
Assembly Bottom Side