How to Contribute to ICS

—

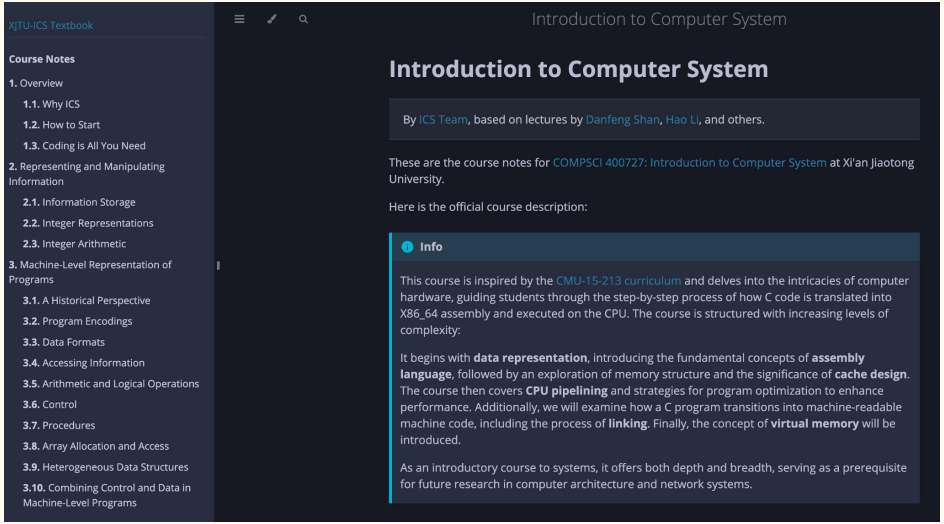
Boxuan Hu. Feb 23

如何为ICS开源社区做出贡献

❤️ is all u need

- Issue
- PR
- Contributor for ICS Textbook

XJTU-ICS Textbook



License

Acknowledgements

The design of this textbook is inspired by many outstanding courses. We would like to express our gratitude to the following courses that have provided us with valuable inspiration:

- CSAPP @CMU
- CS168 @UC Berkeley
- CS161 @UC Berkeley
- Operating System @PKU
- Operating System @IPADS-SJTU
- ICS @NJU

Core Developers

We would like to express our heartfelt thanks to all the contributors who have helped improve XJTU-ICS! Your efforts and collaboration make this project better every day 🌟.

Special thanks to **XJTU-ICS Team Members**. Big shout-out to them 🚀:

- Danfeng Shan (Professor)
- Hao Li (Professor)
- Yunguang Li (HEAD TA, Master)
- Orion (TA, Senior)
- Tang Tang (TA, Senior)
- Jinnuo Du (TA, Senior)
- Jiajun Luan (TA, Senior)
- Jinyu Fu (TA, Senior)
- Boxuan Hu (TA, Junior)
- Yike Liu (TA, Junior)
- Yuxuan Li (TA, Junior)

You can view the full list of contributors and their contributions here.

If you feel your contributions are not listed, please feel free to open a pull request to add yourself. Your work is greatly appreciated 🎉!

How to Contribute

We welcome contributions from everyone! If you're interested in contributing to XJTU-ICS, please follow these steps 👀:

1. Fork the repository to your own GitHub account.
2. Clone the forked repository to your local machine.
3. Create a new branch for your changes.
4. Make your changes and commit them with clear and concise commit messages.
5. Push your changes to your forked repository.
6. Open a pull request to the main repository.
    - Since *Rule Set* is in use, you must contribute with a PR!
7. Delete your branch after merging it. This keeps the repo clean and faster to sync.

It's always a good habit to check CONTRIBUTING.md before contributing ⚠️!

If you are curious about how to set up a textbook with mdBook, we have also provided a detailed tutorial for you to start.

你将收获什么？

Experience

Shanghai Jiao Tong University — Shanghai, China
Research Intern in SJTU EPCC Lab, advised by Prof. Quan Chen — Jun. 2024 - Present

Personal Project

Comet Compiler — *Course project of Advanced Compiler* — Feb. 2024
A compiler for Mx (a C-like educational programming language) to RISC-V backend.
- Implement most optimizations in LLVM.
- Also serves as the compiler of Gelato (below), compiling Mx with SIMT extension to RISC-V with custom ISA extension.
- Written in Java, then rewritten in Rust.

Gelato GPU — *Optional course project of Computer Architecture* — Dec. 2023
A RISC-V General Purpose GPU with SIMT programming model
- Design a set of ISA extension to support CUDA SIMT programming model.
- Capable of running machine learning tasks. (in simulation)
- Written in SystemVerilog.

Remire OS — *Optional course project of Operating System* — Jun. 2024
A microkernel operating system on RISC-V platform
- Implement a microkernel with shell and basic file system.
- All services are implemented as user-space processes except memory management.
- Written in Rust.

CachedLLM — *Best course project of Machine Learning* — Jun. 2024
An efficient LLM serving system for multi-tenant LoRA serving
- Implement a page cache system to manage adapters and persistent states of LLM.
- Built on top of vLLM.
- Written in Python.

Teaching Experience

Teaching Assistant Programming, Data Structure and PPCA — 2023-2025
- Worked as TA team leader in those courses.

Projects

Electromagnetic Induction tracking smart car | *Analog Circuit, Arduino uno, PCB, multisim* — **December 2023**
- Successfully runs an automatic track-control car with electromagnetic induction principle on a given sophisticated track.
- Used multisim to simulate the analog circuit and design the circuit parameters.
- Implemented the analog system on PCB board, with an amplifier, a rectifier, a filter for each induction and a differential amplifier to process the signal.
- Implemented the control unit on Arduino Uno platform with PID as central algorithm.

Notes and Thoughts in Design and Analysis of Algorithms | *latex* — **September-December, 2023**
- Open-sourced a 40-page notes based on course 'Design and Analysis of Algorithms', with insightful thoughts and reorganization of proofs

Optimization of multi-beam line layout based on terrain clustering model | *python, DBSCAN* — **September, 2023**
- Successfully optimized the layout of multi-beam line under different terrain conditions.
- Achieved remarkable results on benchmarks such as overlap rate, leaking rate and length of the whole line.
- Roughly cluster the depth map by designed feature (trend of the isobath) by DBSCAN. Then obtain different regions by SVM. Optimize the layout of the beam line in each region in the end.

Teaching Experience

Principle and Practice of Computer Algorithms
Teaching Assistant guided by Prof. Yong Yu — *June. 2022 - Aug. 2022*
Advised students to implement a RISC-V simulator.Helped students with ray tracing projects, designed some additional tracks, and handed on every student with the outline of the project and details.

Compiler design
Teaching Assistant guided by Prof. Yong Yu — *Sept. 2022 - Feb. 2023*
Help students design their compiler and teach them my own experience and knowledge in compiling.

Projects

Personal Project: RayTracer
About 8K LoC in RUST [repo] — *Jun. 2021 - Jul. 2021*
A system that can build its scene and track the refraction and reflection of light in it. Several compilation-related optimizations were undertaken to enhance the overall performance.

Course Project: Compiler for Mx* Language
About 8K LoC in JAVA [repo] — *Sept. 2021 - Feb. 2022*
Using the technology of ANTLR, semantic checking, code generation, and optimization to develop a compiler that compiles C-and-Java-like language (Mx*) to RV32I Assembly.

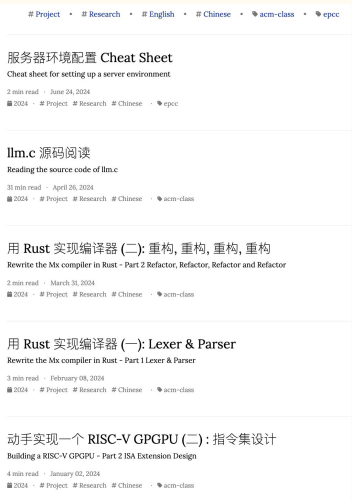
Course Project: RISC-V CPU Implemented in Verilog RTL
About 3K LoC in Verilog [repo] — *Sept. 2021 - Dec. 2021*
Designed a RISC-V CPU with Write Buffer, ICache, DCache, and Branch Prediction. Supports RV32I instruction set (2.1-2.6 in RISC-V User Manual). Used Vivado to generate bitstream and program the Basys3 FPGA board.

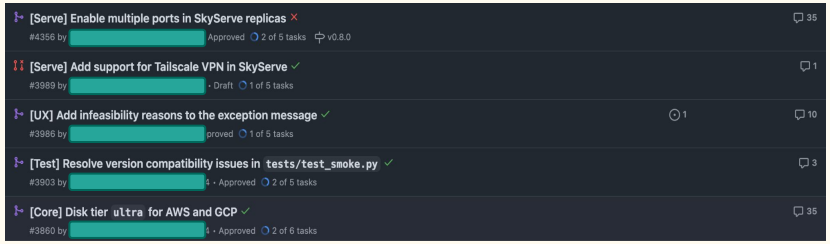
Course Project: Ticket System
About 4K LoC in C++[repo] — *Apr. 2021 - Jun. 2021*
Designed a train ticket system with multi-user support and privilege management. I implemented the backend and built a Bplustree storage. All used C++ STL data structures are from scratch (including map, and queue).

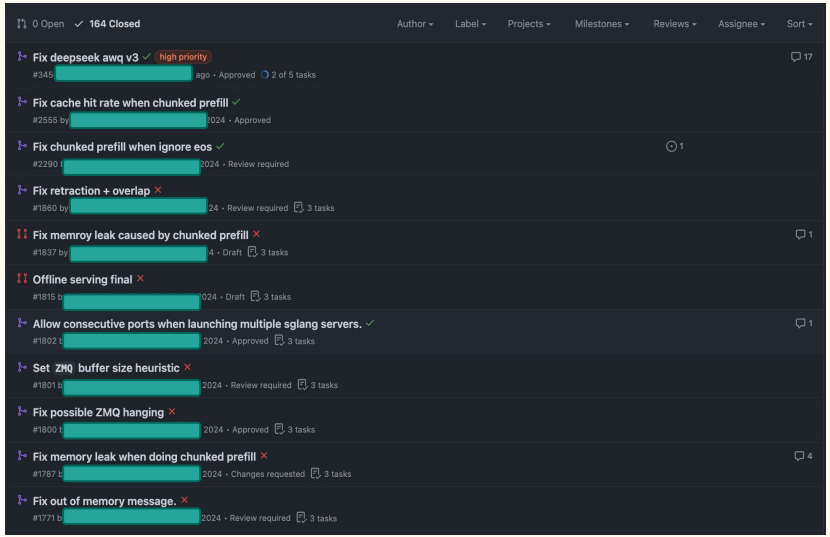
Currently, I am fortunate to work with Lianmin Zheng and Ying Sheng from LMSYS.ORG, working as a core developer of **SGLang**, and avised by Ion Stoica and Joseph E. Gonzalez in Sky Computing. We are committed to developing more efficient and powerful system for Artificial Intelligence. I am also an applicant for the 2025 Fall Ph.D. program in Computer Science.

Feel free to check out my CV and drop me an e-mail if you want to chat with me!

是真材实料吗？








Sufficient Algorithms

February 3, 2024

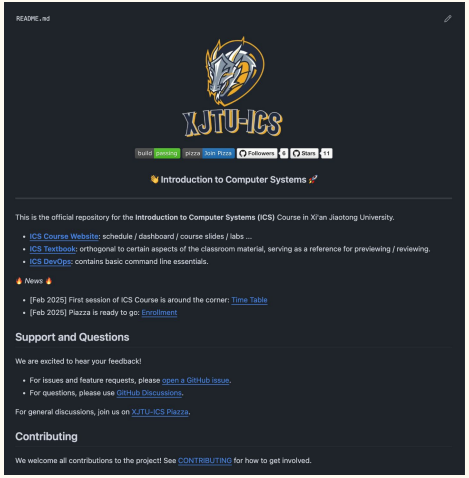
Contents

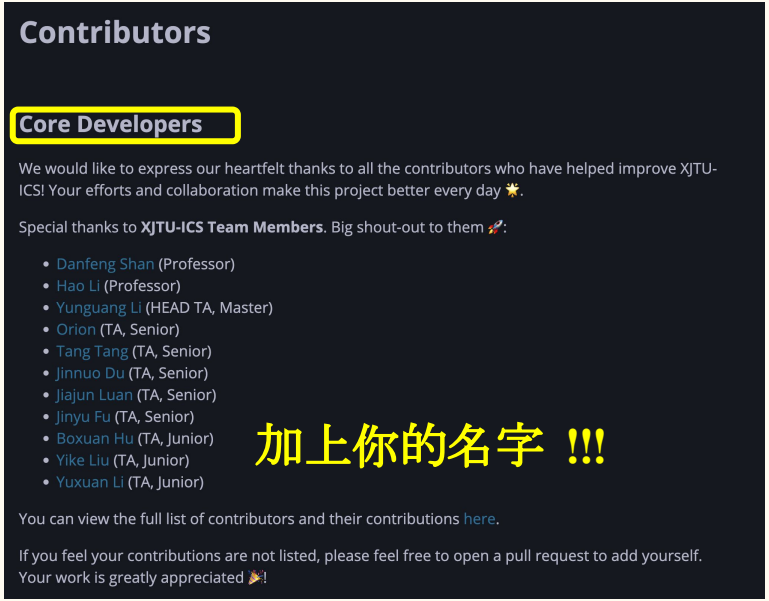
获得2024年国家奖学金是一份殊荣，更是一种责任。一方书香校园、两载求知历程，我愈发笃信，技术的光芒在于照亮多远的前路，更在于温暖多少人的现实。从在张峰教授指导下埋首系统架构的优化，到拥抱开源世界的协作，每一次探索都在印证一个真理——创新的浪潮从不因个人而起，却总为众人而澎湃。

这份技术服务于人的信念，在计算机协会的舞台上得到了最好的演绎。作为会长，我深知创新生态的构建既需要点亮个人的星火，更需要汇聚燎原之势。从函数式编程到Rust生态，一场场前沿技术分享不只是知识的传递，更是打造了开源精神和创新文化的基石。这种理念，在如是社区平台中得到升华、化为了触手可及的现实。看到几百名同学在平台的科研平台区上互助共进、探索科研，我更深切地感受到，技术的价值就在于为他人创造更多的可能性。而在柴云鹏教授和王晶教授的指导下，我和助教团队更是一起推动了 ICS 课程改革，见证了这门经典课程的华丽蝶变。从开创性地设计 LinkLab，到引入前沿 GPU 优化理念，每一步都在印证：成就他人的征途上，既需要耐心倾听的热忱，更需要推陈出新的勇气。

我们将提供什么？

1. 官方 XJTU-ICS 开源社区
2. 与助教团队定期互动交流
3. 在开源社区提出 “第一个PR”
4. 丰富个人简历, 迈向对计算机开源世界的第一步
5. 成为rising star, 有机会成为下一任 ICS TA





我们需要你：

1. 有一颗热爱计算机科学的 ❤️
2. 能够投入一定时间在Textbook项目 (每周约2h, 考试周不做要求)
3. 善于沟通与合作
4. 熟练掌握 Markdown 文法

如果你想加入, please feel free to contact us with your CV !

我们计划今年招募 **3-5 名常任 Contributors**, 其余同学也可以积极构建Textbook内容