

# CMPE 315: Principles of VLSI Design

## Lab Cover Page

Lab # : 1  
Lab Title : Project Submission 2

Name : Nem Negash and Sean Mullins  
Section : 1

Date Submitted : 12/10/2021

### TA / Grader Use Only:

Late Submission Deduction (20% per day late):

Other Deductions:

Final Lab Grade:

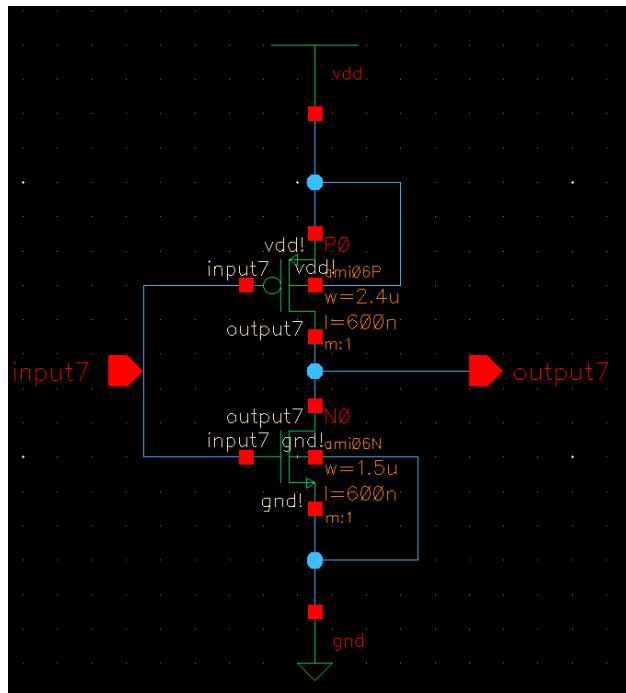
Comments to student:

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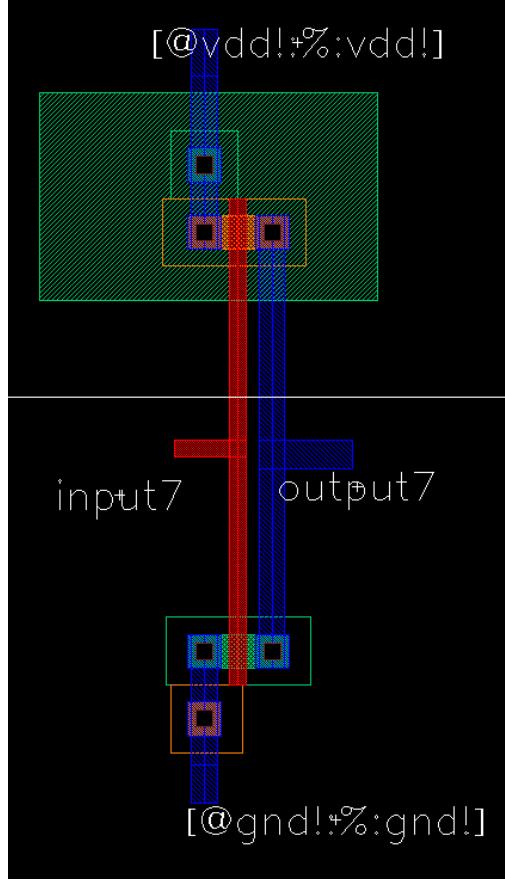
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## Schematic, Layout, and LVS

### Inverter



**Figure 1: Inverter Schematic**



**Figure 2: Inverter Layout**

```
The net-lists match.

          layout schematic
          instances
un-matched      0      0
rewired         0      0
size errors     0      0
pruned          0      0
active          2      2
total           2      2

          nets
un-matched      0      0
merged          0      0
pruned          0      0
active          4      4
total           4      4

          terminals
un-matched      0      0
matched but
different type   0      0
total           4      4

Probe files from /afs/umbc.edu/users/s/e/seanm5/home/home/LVS/schematic
devbad.out:
netbad.out:
mergenet.out:
termbad.out:
prunenet.out:
prunedev.out:
audit.out:

Probe files from /afs/umbc.edu/users/s/e/seanm5/home/home/LVS/layout
devbad.out:
netbad.out:
mergenet.out:
termbad.out:
prunenet.out:
prunedev.out:
audit.out:
```

Figure 3: Inverter LVS

## Nand2

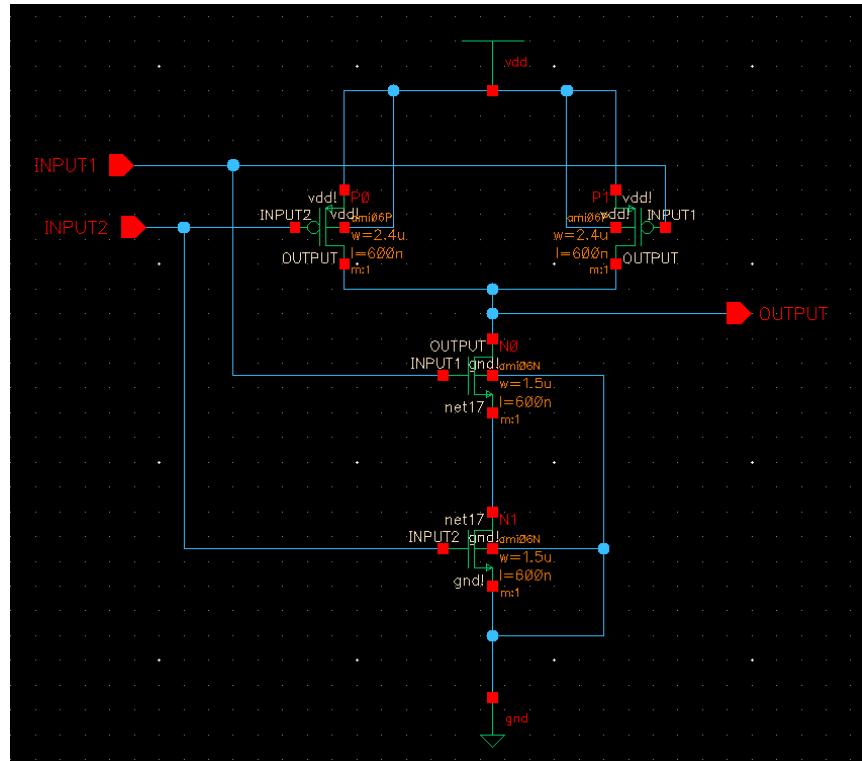


Figure 4: Nand2 Schematic

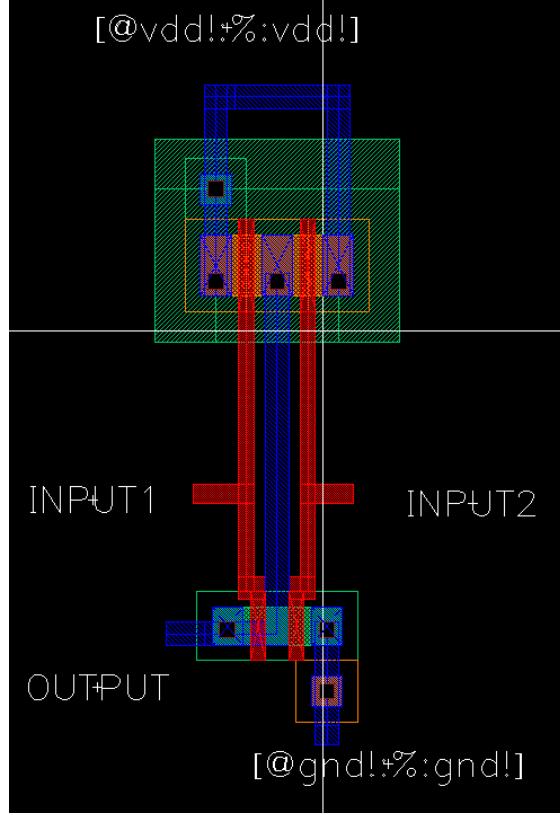


Figure 5: Nand2 Layout

```
The net-lists match.                                1

          layout schematic
          instances
un-matched      0      0
rewired         0      0
size errors     0      0
pruned          0      0
active          4      4
total           4      4

          nets
un-matched      0      0
merged          0      0
pruned          0      0
active          6      6
total           6      6

          terminals
un-matched      0      0
matched but
different type   0      0
total            5      5

Probe files from /afs/umbc.edu/users/s/e/seam5/home/home/LVS/schematic
devbad.out:
netbad.out:
mergenet.out:
termbad.out:
prunenet.out:
prunedev.out:
audit.out:

Probe files from /afs/umbc.edu/users/s/e/seam5/home/home/LVS/layout
devbad.out:
netbad.out:
mergenet.out:
termbad.out:
prunenet.out:
prunedev.out:
audit.out:
```

---

**Figure 6: Nand2 LVS**

And2

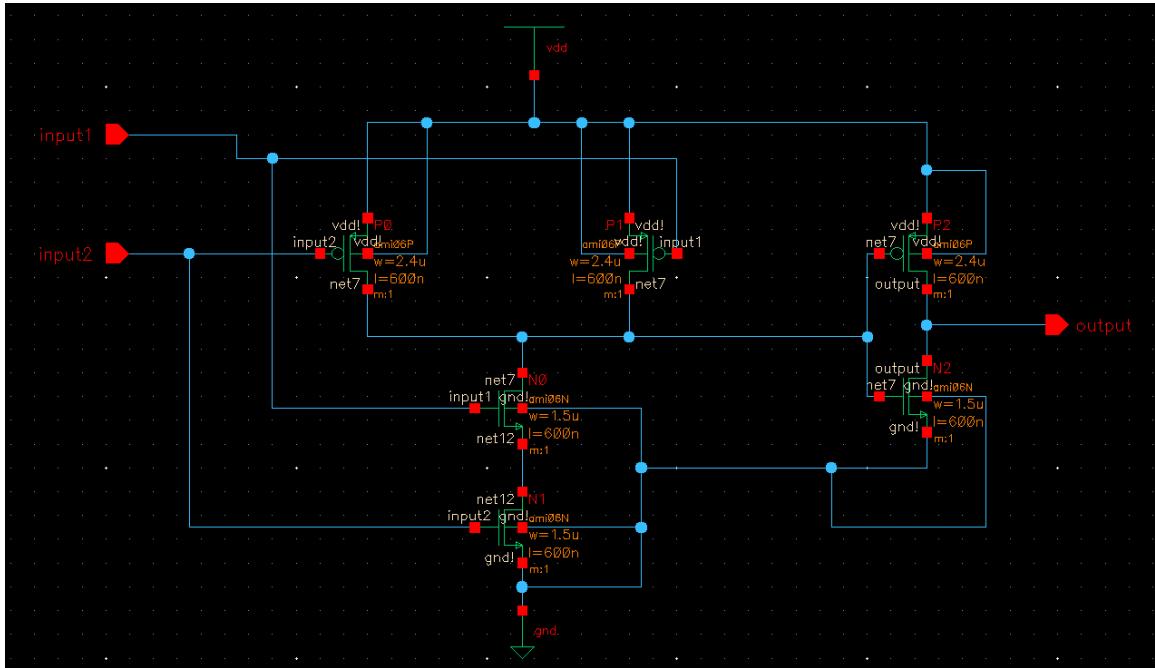


Figure 7: And2 Schematic

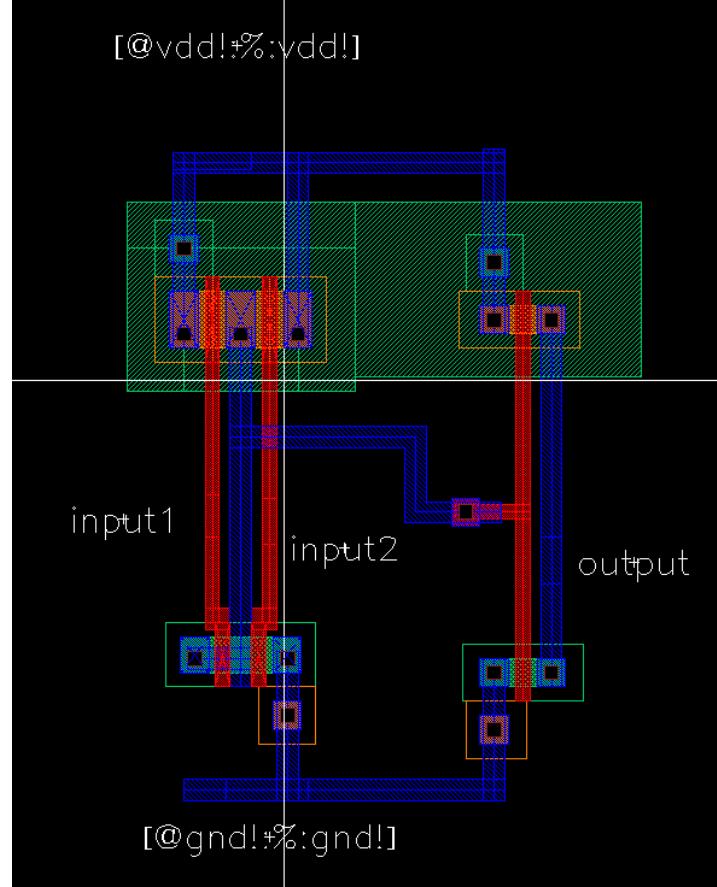


Figure 8: And2 Layout

The net-lists match.

	layout	schematic
	instances	
un-matched	0	0
rewired	0	0
size errors	0	0
pruned	0	0
active	6	6
total	6	6

	nets	
un-matched	0	0
merged	0	0
pruned	0	0
active	7	7
total	7	7

	terminals	
un-matched	0	0
matched but different type	0	0
total	5	5

Probe files from /afs/umbc.edu/users/s/e/seanm5/home/home/LVS/schematic

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:

Probe files from /afs/umbc.edu/users/s/e/seanm5/home/home/LVS/layout

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:

---

Figure 9: And2 LVS

Nor2

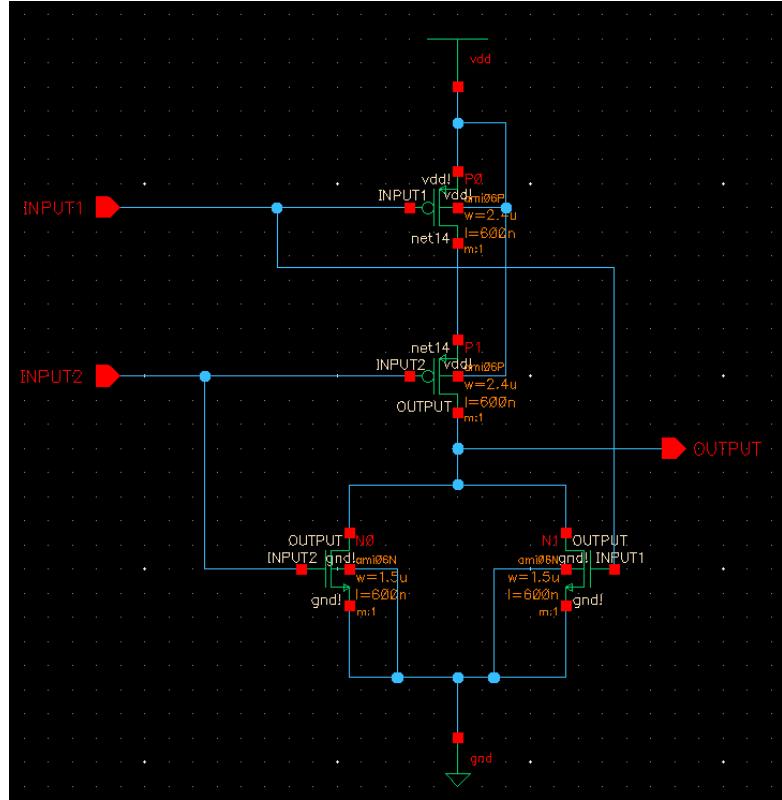


Figure 10: Nor2 Schematic

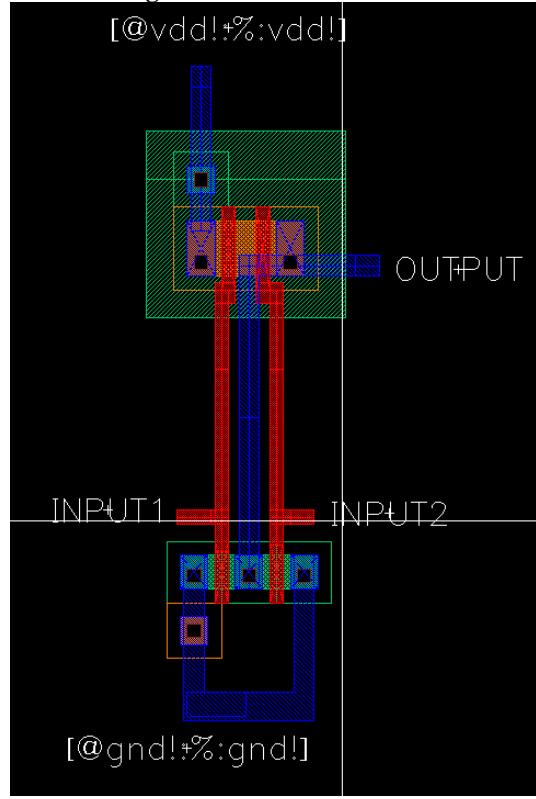


Figure 11: Nor2 Layout

The net-lists match.

	layout	schematic
	instances	
un-matched	0	0
rewired	0	0
size errors	0	0
pruned	0	0
active	4	4
total	4	4

	nets	
un-matched	0	0
merged	0	0
pruned	0	0
active	6	6
total	6	6

	terminals	
un-matched	0	0
matched but		
different type	0	0
total	5	5

Probe files from /afs/umbc.edu/users/s/e/seannm5/home/home/LVS/schematic

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:

Probe files from /afs/umbc.edu/users/s/e/seannm5/home/home/LVS/layout

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:

**Figure 12: Nor2 LVS**

Or2

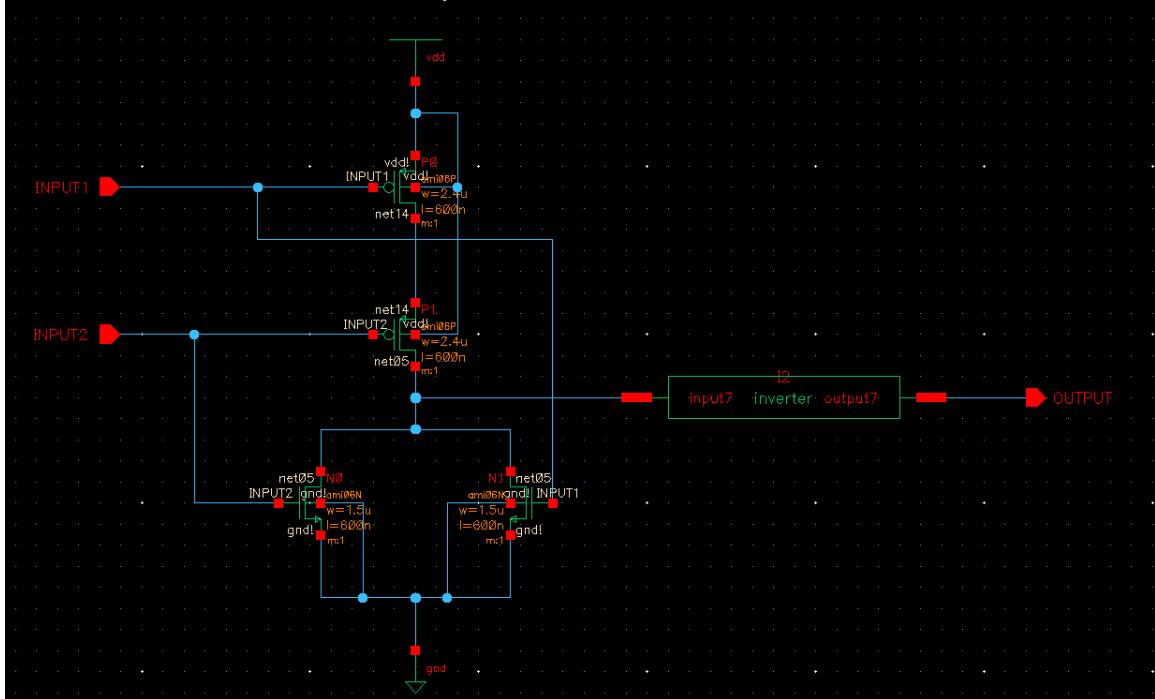


Figure 13: Or2 Schematic

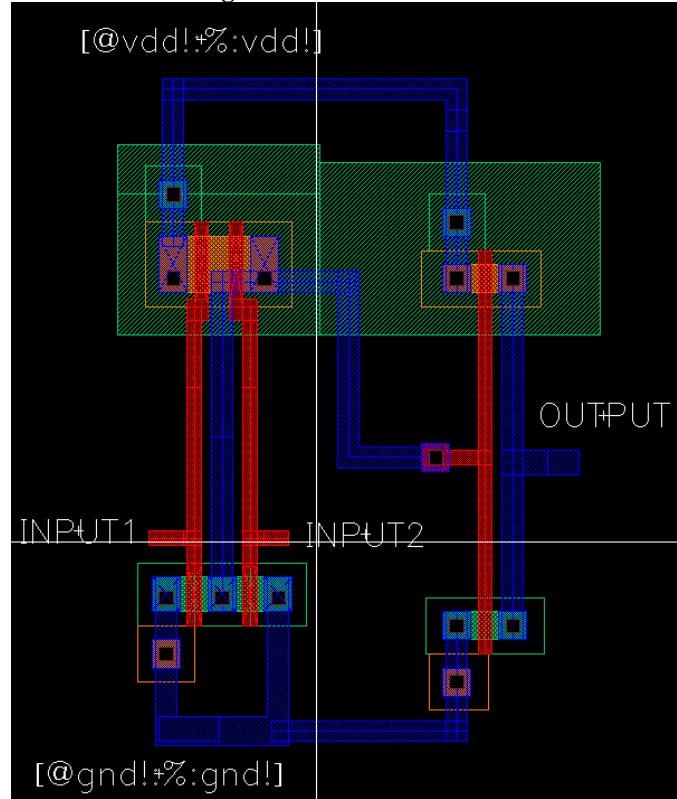


Figure 14: Or2 Layout

The net-lists match.

	layout	schematic
	instances	
un-matched	0	0
rewired	0	0
size errors	0	0
pruned	0	0
active	6	6
total	6	6

	nets	
un-matched	0	0
merged	0	0
pruned	0	0
active	7	7
total	7	7

	terminals	
un-matched	0	0
matched but different type	0	0
total	5	5

Probe files from /afs/umbc.edu/users/s/e/seannm5/home/home/LVS/schematic

```
devbad.out:  
netbad.out:  
mergenet.out:  
termbad.out:  
prunenet.out:  
prunedev.out:  
audit.out:
```

Probe files from /afs/umbc.edu/users/s/e/seannm5/home/home/LVS/layout

```
devbad.out:  
netbad.out:  
mergenet.out:  
termbad.out:  
prunenet.out:  
prunedev.out:  
audit.out:
```

**Figure 15: Or2 LVS**

Xor2

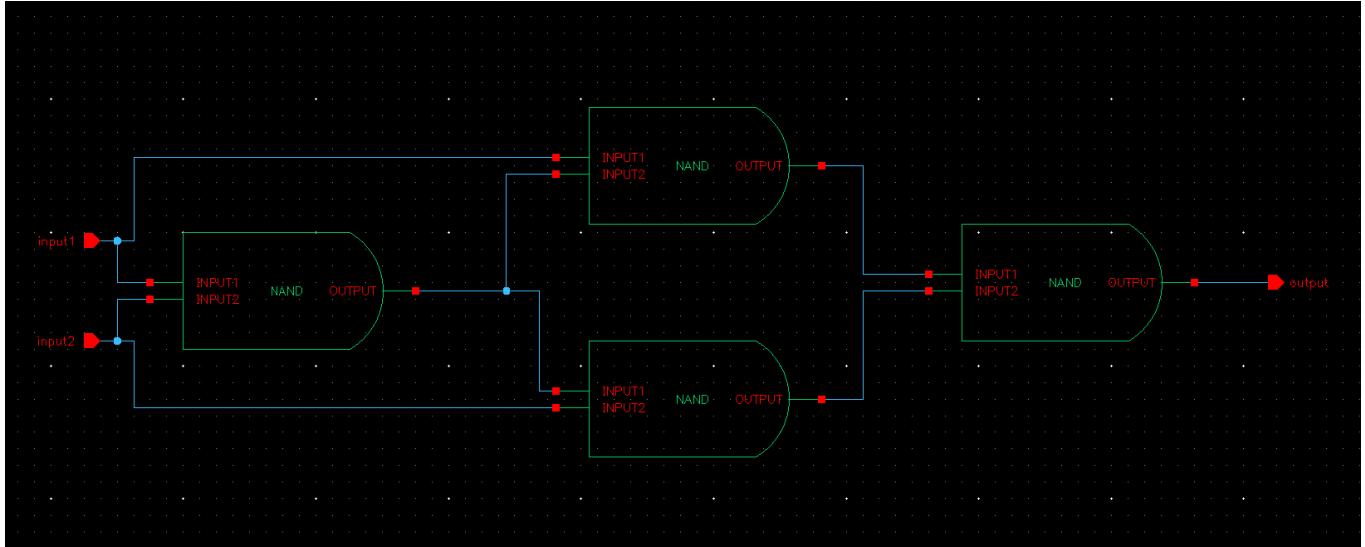


Figure 16: Xor2 Schematic

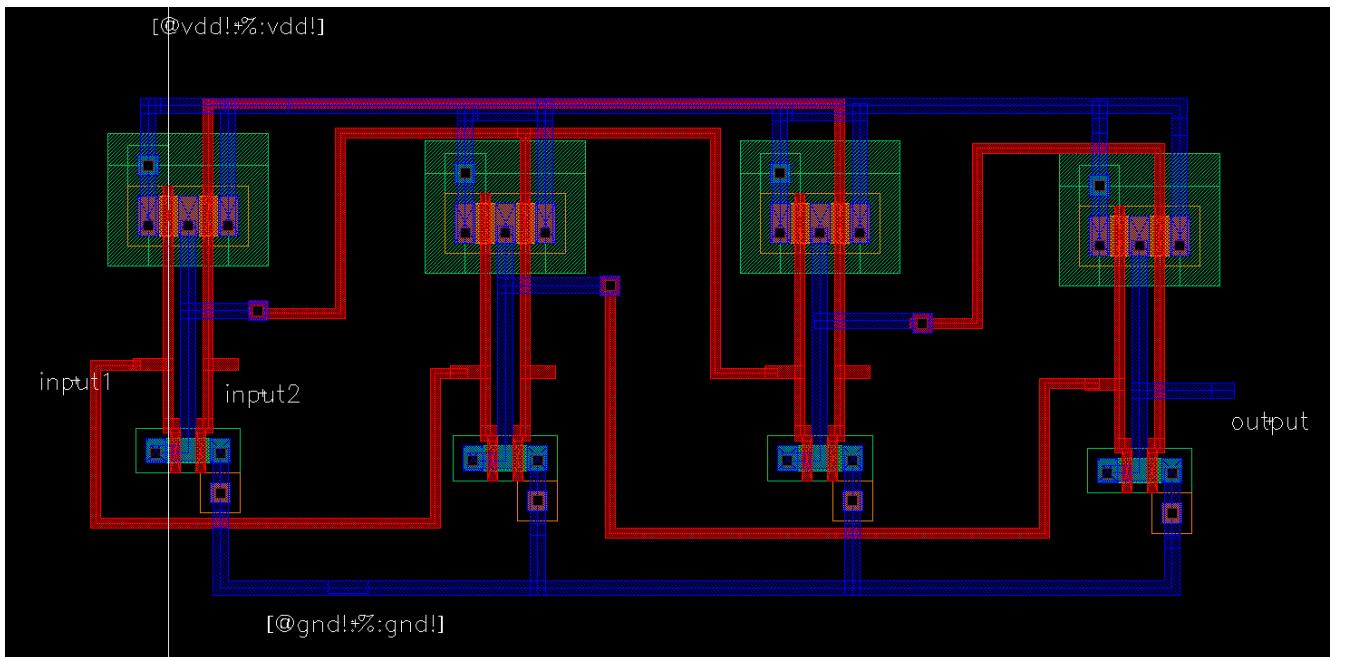


Figure 17: Xor2 Schematic

The net-lists match.

	layout	schematic
	instances	
un-matched	0	0
rewired	0	0
size errors	0	0
pruned	0	0
active	16	16
total	16	16

	nets	
un-matched	0	0
merged	0	0
pruned	0	0
active	12	12
total	12	12

	terminals	
un-matched	0	0
matched but different type	0	0
total	5	5

Probe files from /afs/umbc.edu/users/s/e/searnm5/home/home/LVS/schematic

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:

Probe files from /afs/umbc.edu/users/s/e/searnm5/home/home/LVS/layout

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:

---

Figure 18: Xor2 LVS

Tran\_Gate

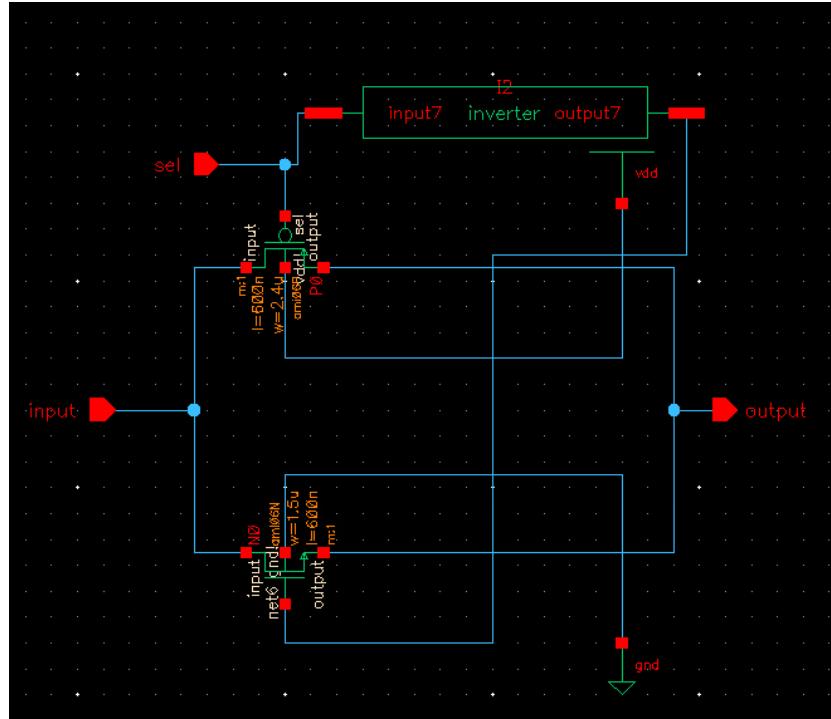


Figure 19: Tran\_Gate Schematic

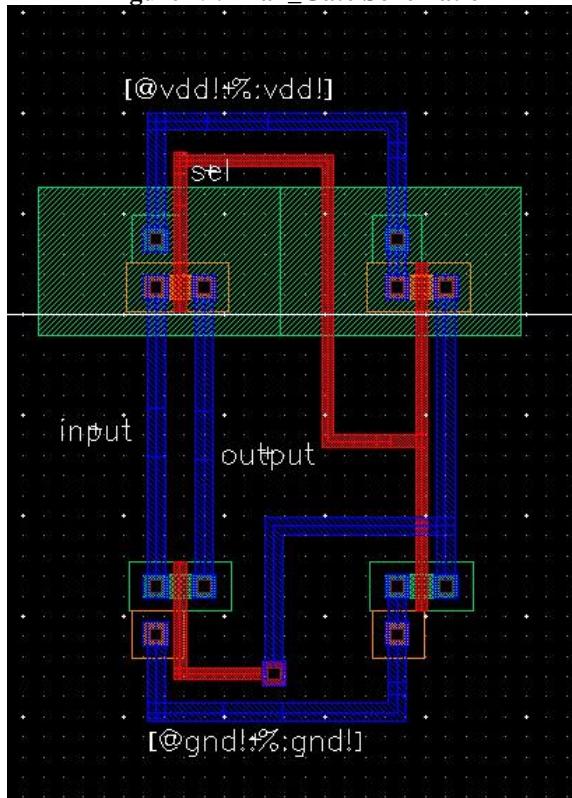


Figure 20: Tran\_Gate Layout

The net-lists match.

	layout	schematic
	instances	
un-matched	0	0
rewired	0	0
size errors	0	0
pruned	0	0
active	4	4
total	4	4
	nets	
un-matched	0	0
merged	0	0
pruned	0	0
active	6	6
total	6	6
	terminals	
un-matched	0	0
matched but different type	0	0
total	5	5

Probe files from /afs/umbc.edu/users/s/e/seanm5/home/home/LVS/schematic

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

---

Figure 21: Tran\_Gate LVS

## Dlatch

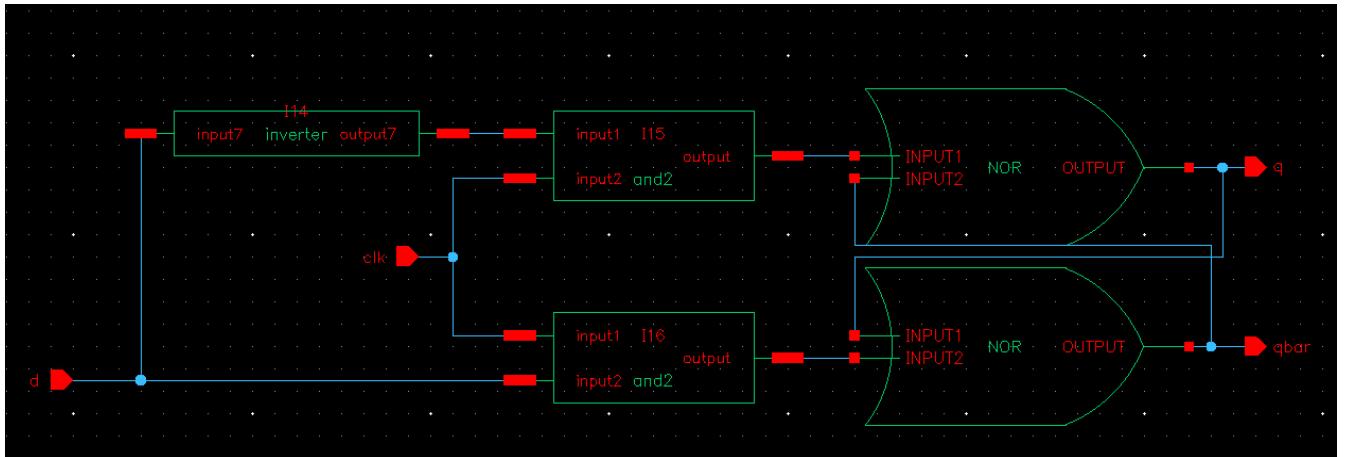


Figure 22: Dlatch Schematic

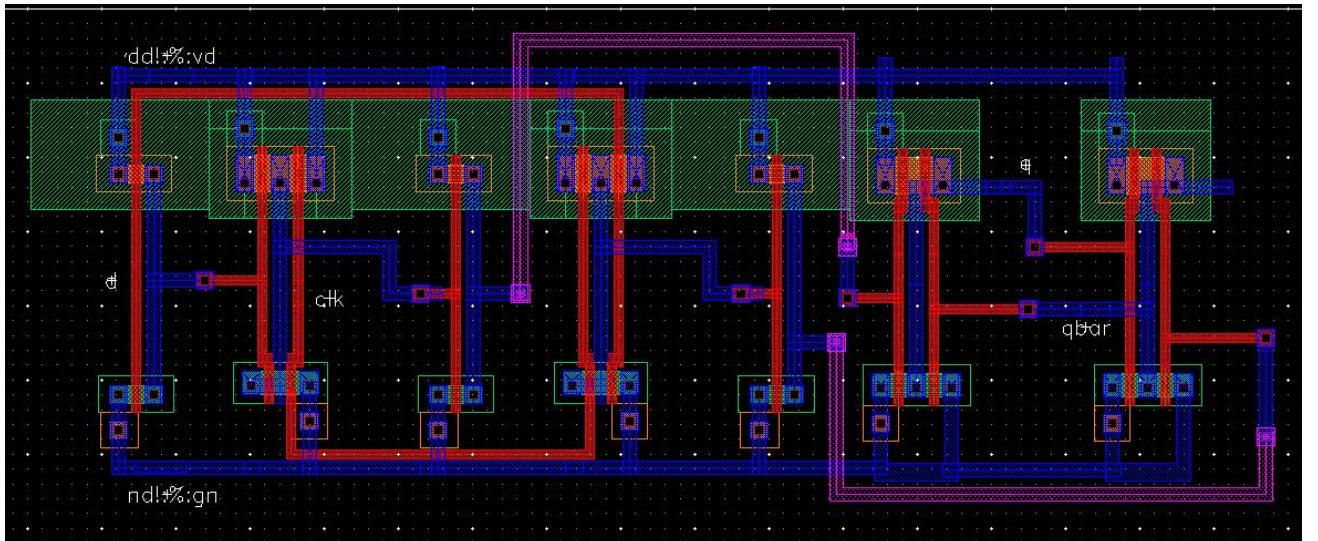


Figure 23: Dlatch Layout

The net-lists match.

	layout	schematic
	instances	
un-matched	0	0
rewired	0	0
size errors	0	0
pruned	0	0
active	22	22
total	22	22
	nets	
un-matched	0	0
merged	0	0
pruned	0	0
active	15	15
total	15	15
	terminals	
un-matched	0	0
matched but different type	0	0
total	6	6

Probe files from /afs/umbc.edu/users/s/e/seanm5/home/home/LVS/schematic

devbad.out:

netbad.out:

mergenet.out:

Figure 24: Dlatch LVS

Dlatch\_8bit

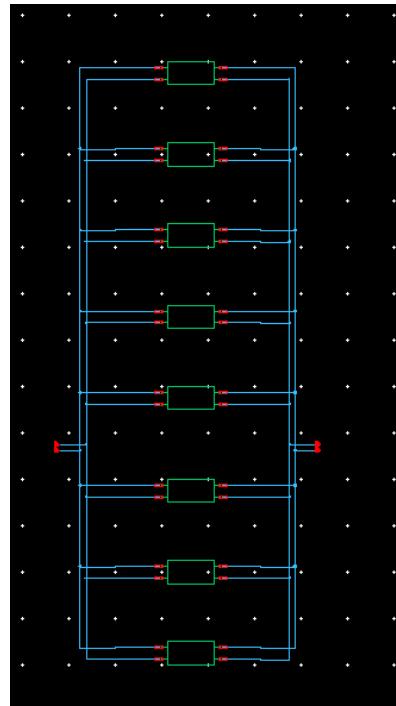


Figure 25: Dlatch\_8bit Schematic

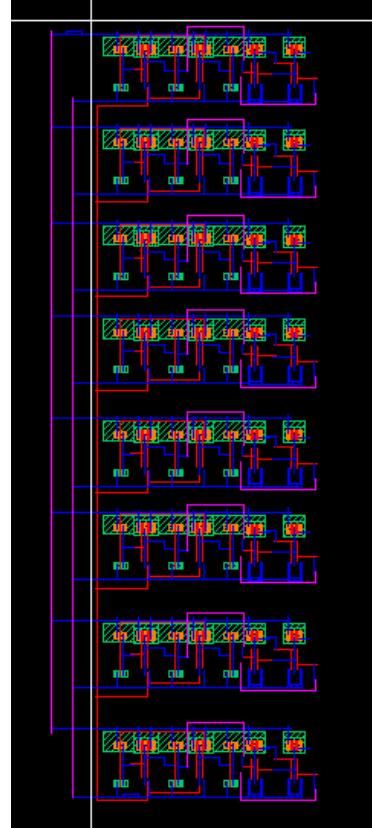


Figure 26: Dlatch\_8bit Layout

The net-lists match.

	layout	schematic
	instances	
un-matched	0	0
rewired	0	0
size errors	0	0
pruned	0	0
active	176	176
total	176	176

	nets	
un-matched	0	0
merged	0	0
pruned	0	0
active	99	99
total	99	99

	terminals	
un-matched	0	0
matched but different type	0	0
total	27	27

Probe files from /afs/umbc.edu/users/s/e/seanm5/home/home/LVS/schematic

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:

Figure 27: Dlatch\_8bit LVS

## Dff (D-flip-flop)

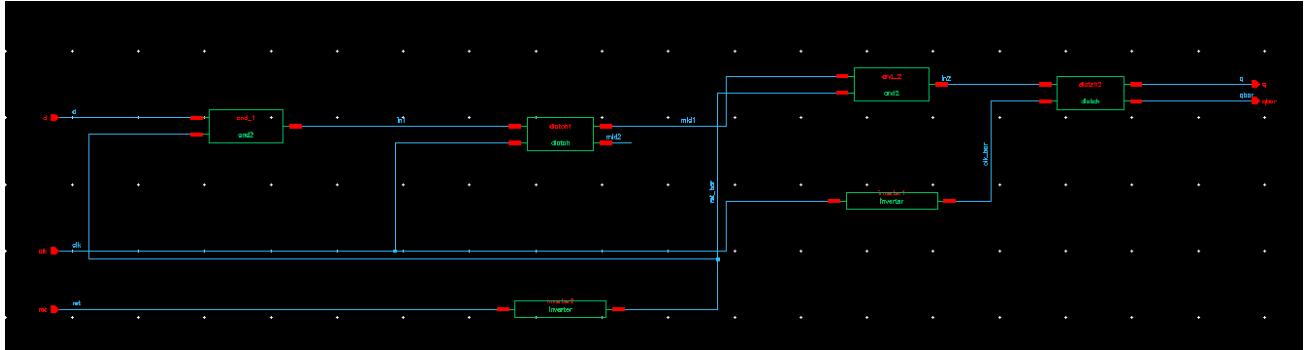


Figure 28: Dff (D-flip-flop) Schematic

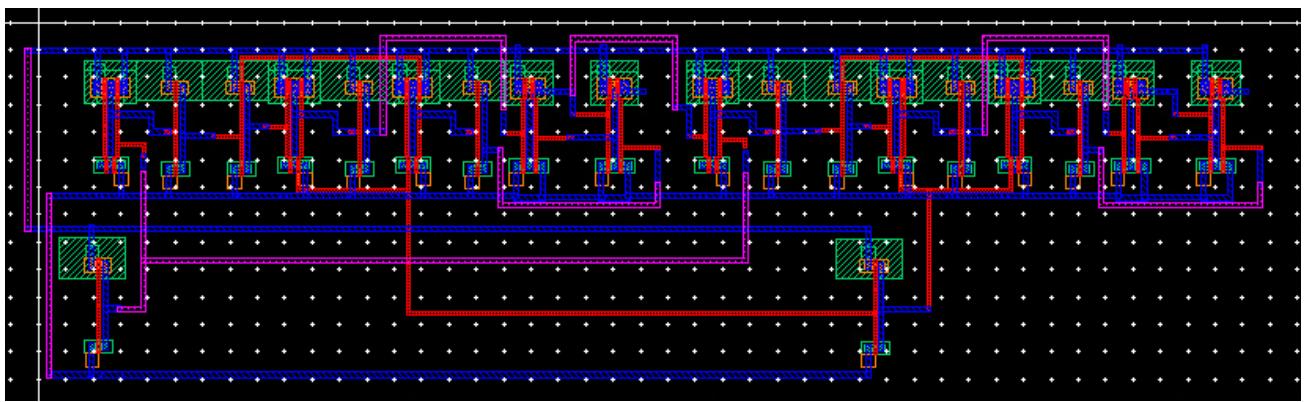


Figure 29: Dff (D-flip-flop) Layout

The net-lists match.

	layout	schematic
	instances	
un-matched	0	0
rewired	0	0
size errors	0	0
pruned	0	0
active	60	60
total	60	60
	nets	
un-matched	0	0
merged	0	0
pruned	0	0
active	35	35
total	35	35
	terminals	
un-matched	0	0
matched but different type	0	0
total	7	7

```
Probe files from /afs/umbc.edu/users/s/e/seanm5/home/home/LVS/schematic

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:
```

Figure 30: Dff (D-flip-flop) LVS

Mux\_2\_1

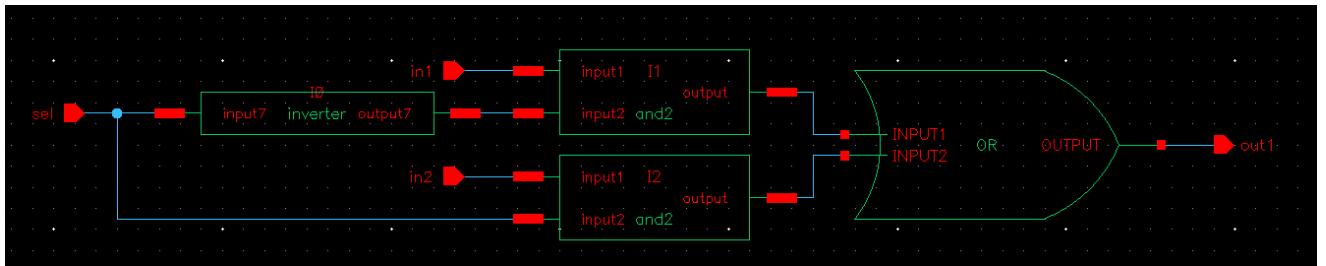


Figure 31: Mux\_2\_1 Schematic

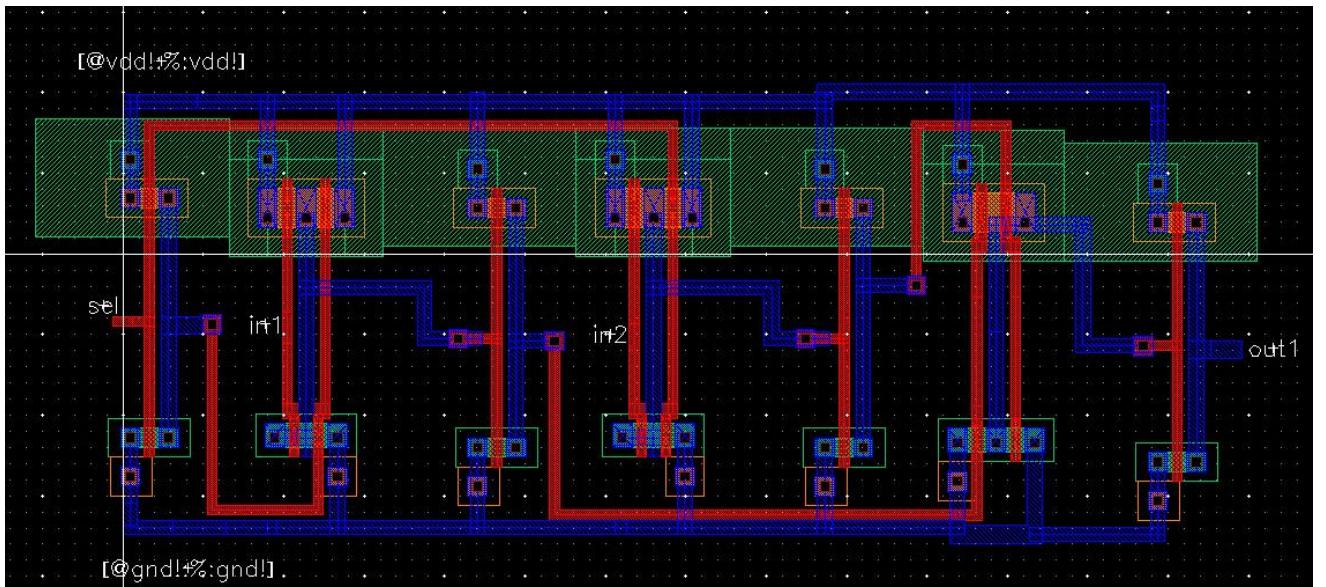


Figure 32: Mux\_2\_1 Layout

---

The net-lists match.

	layout	schematic
	instances	
un-matched	0	0
rewired	0	0
size errors	0	0
pruned	0	0
active	20	20
total	20	20

	nets	
un-matched	0	0
merged	0	0
pruned	0	0
active	15	15
total	15	15

	terminals	
un-matched	0	0
matched but		
different type	0	0
total	6	6

Probe files from /afs/umbc.edu/users/s/e/seanm5/home/home/LVS/schematic

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:

Probe files from /afs/umbc.edu/users/s/e/seanm5/home/home/LVS/layout

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:

---

Figure 33: Mux\_2\_1 LVS

Mux\_2\_1\_8\_bit

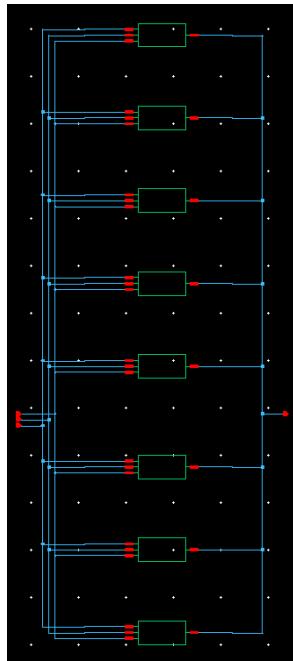


Figure 34: Mux\_2\_1\_8\_bit Schematic

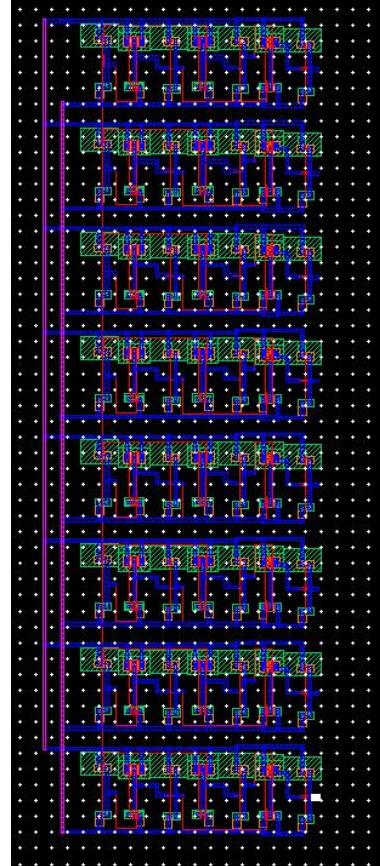


Figure 35: Mux\_2\_1\_8\_bit Layout

The net-lists match.

	layout	schematic
	instances	
un-matched	0	0
rewired	0	0
size errors	0	0
pruned	0	0
active	160	160
total	160	160

	nets	
un-matched	0	0
merged	0	0
pruned	0	0
active	99	99
total	99	99

	terminals	
un-matched	0	0
matched but different type	0	0
total	27	27

```
Probe files from /afs/umbc.edu/users/s/e/seanm5/home/home/LVS/schematic

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:
```

**Figure 36: Mux\_2\_1\_8\_bit LVS**

Mux\_4\_1

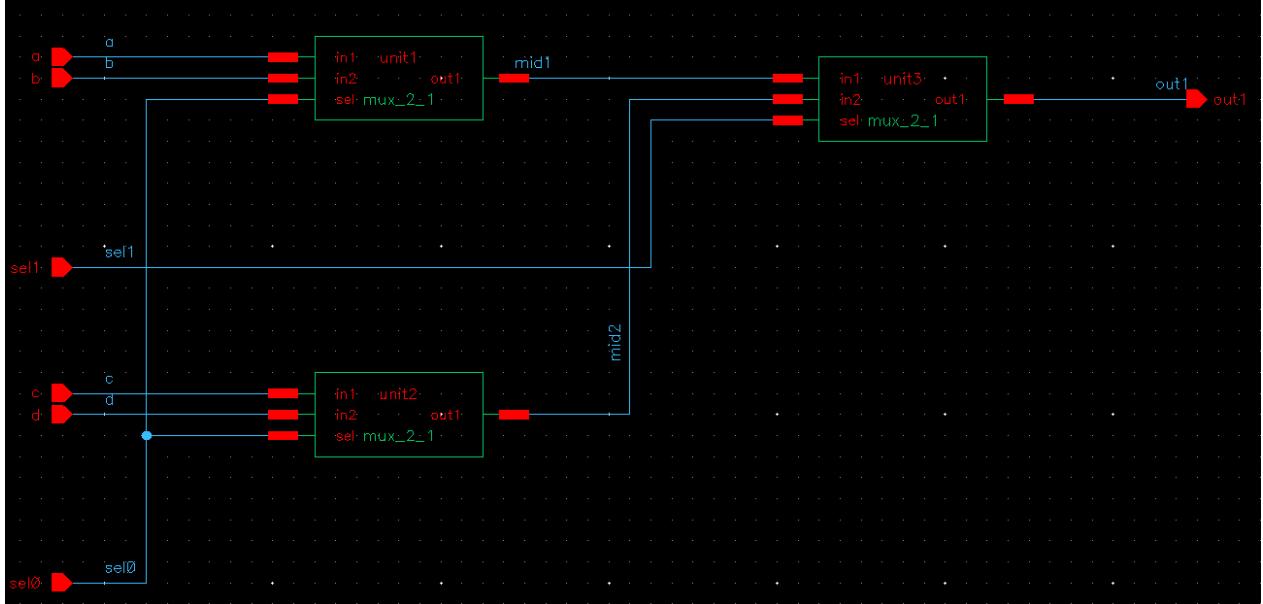


Figure 37: Mux\_4\_1 Schematic

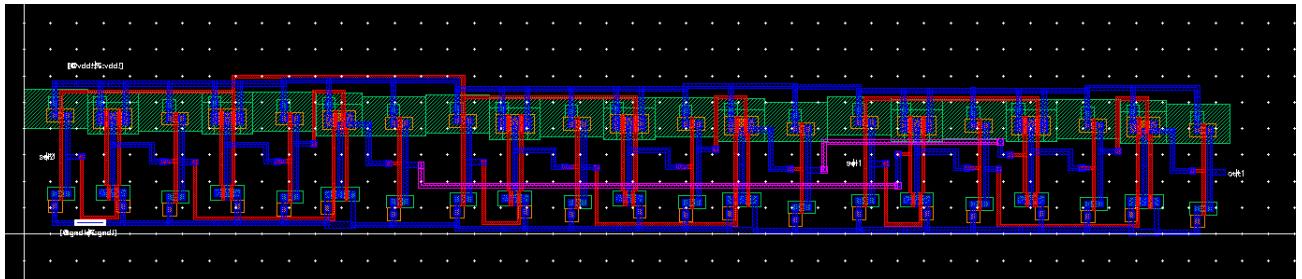


Figure 38: Mux\_4\_1 Layout

---

The net-lists match.

	layout	schematic
	instances	
un-matched	0	0
rewired	0	0
size errors	0	0
pruned	0	0
active	60	60
total	60	60

	nets	
un-matched	0	0
merged	0	0
pruned	0	0
active	38	38
total	38	38

	terminals	
un-matched	0	0
matched but		
different type	0	0
total	9	9

Probe files from /afs/umbc.edu/users/s/e/seanm5/home/home/LVS/schematic

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:

Probe files from /afs/umbc.edu/users/s/e/seanm5/home/home/LVS/layout

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:

Figure 39: Mux\_4\_1 LVS

## Mux\_3\_bit

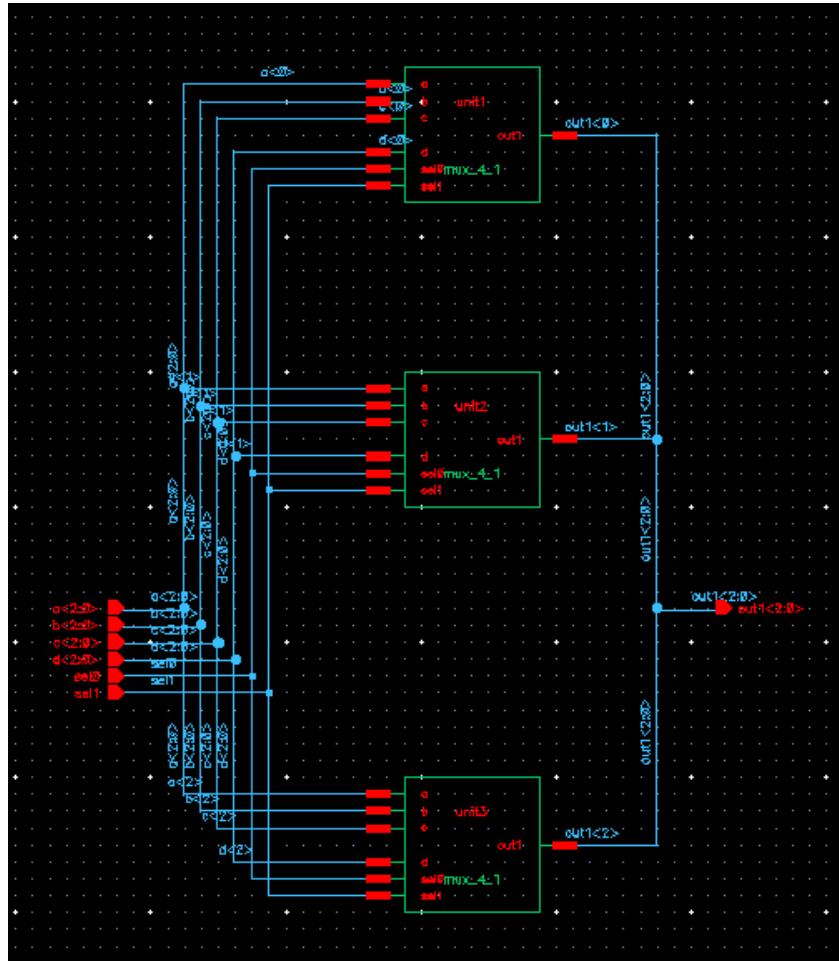


Figure 40: Mux\_3\_bit Schematic

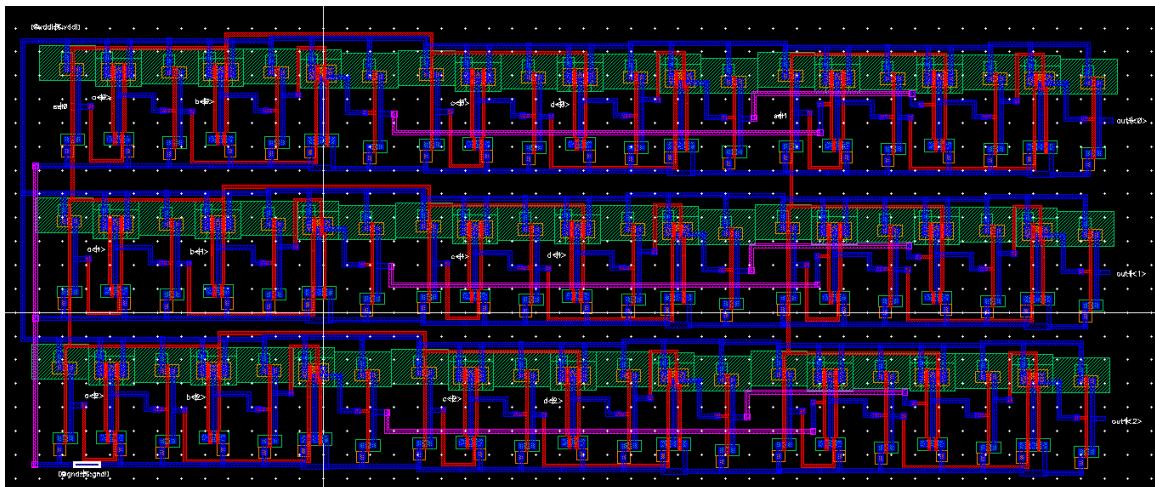


Figure 41: Mux\_3\_bit Schematic

---

The net-lists match.

	layout	schematic
	instances	
un-matched	0	0
rewired	0	0
size errors	0	0
pruned	0	0
active	180	180
total	180	180
	nets	
un-matched	0	0
merged	0	0
pruned	0	0
active	106	106
total	106	106
	terminals	
un-matched	0	0
matched but different type	0	0
total	19	19

Probe files from /afs/umbc.edu/users/s/e/seannm5/home/home/LVS/schematic

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:

Probe files from /afs/umbc.edu/users/s/e/seannm5/home/home/LVS/layout

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:

---

Figure 42: Mux\_3\_bit LVS

Mux\_8\_bit

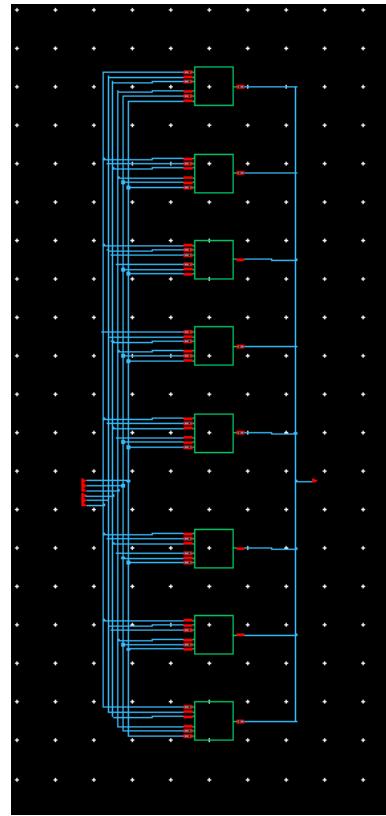


Figure 43: Mux\_8\_bit Schematic

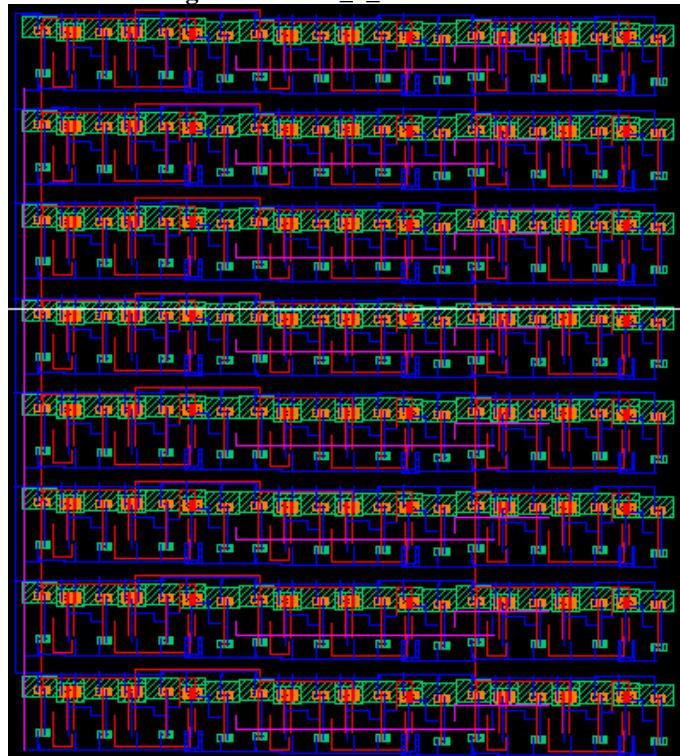


Figure 44: Mux\_8\_bit Layout

The net-lists match.

	layout	schematic
	instances	
un-matched	0	0
rewired	0	0
size errors	0	0
pruned	0	0
active	480	480
total	480	480
	nets	
un-matched	0	0
merged	0	0
pruned	0	0
active	276	276
total	276	276
	terminals	
un-matched	0	0
matched but different type	0	0
total	44	44

Probe files from /afs/umbc.edu/users/s/e/seanm5/home/home/LVS/schematic

```
devbad.out:  
netbad.out:  
mergenet.out:  
termbad.out:  
prunenet.out:  
prunedev.out:  
audit.out:
```

Probe files from /afs/umbc.edu/users/s/e/seanm5/home/home/LVS/layout

```
devbad.out:  
netbad.out:  
mergenet.out:  
termbad.out:  
prunenet.out:  
prunedev.out:  
audit.out:
```

Figure 45: Mux\_8\_bit LVS

Mux\_8\_1\_3\_bit

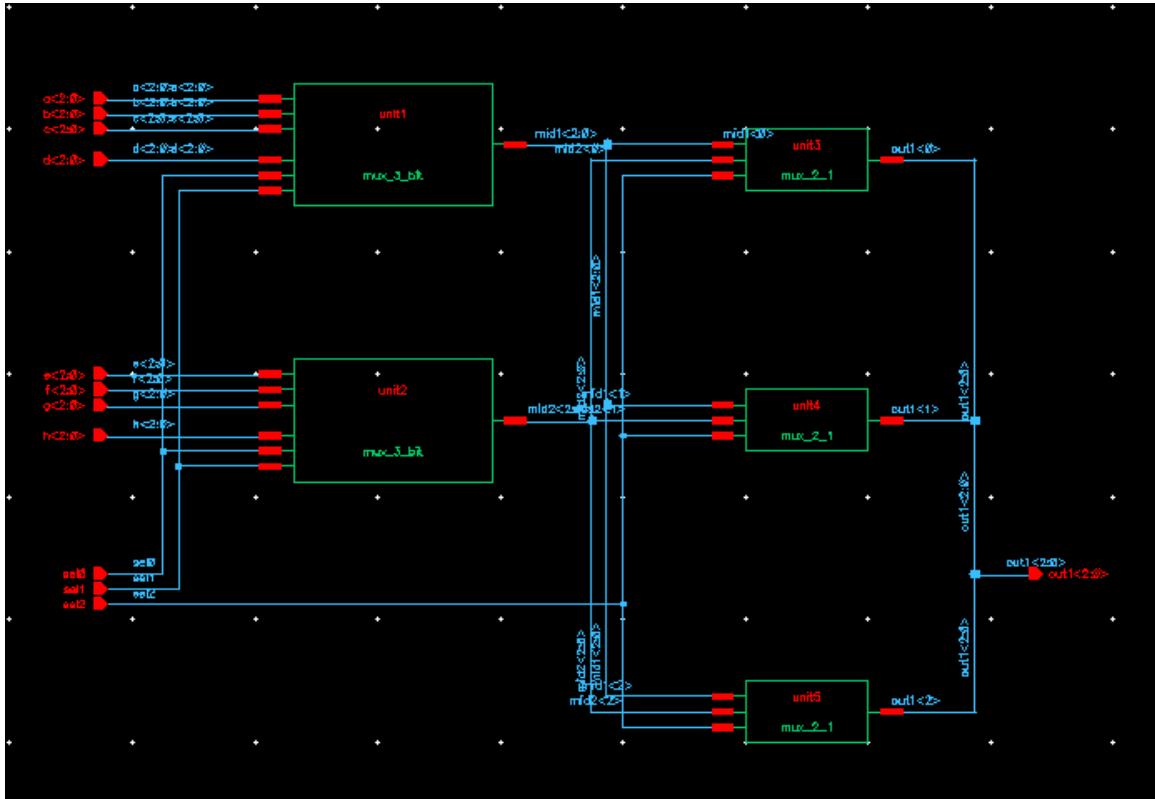


Figure 46: Mux\_8\_1\_3\_bit Schematic

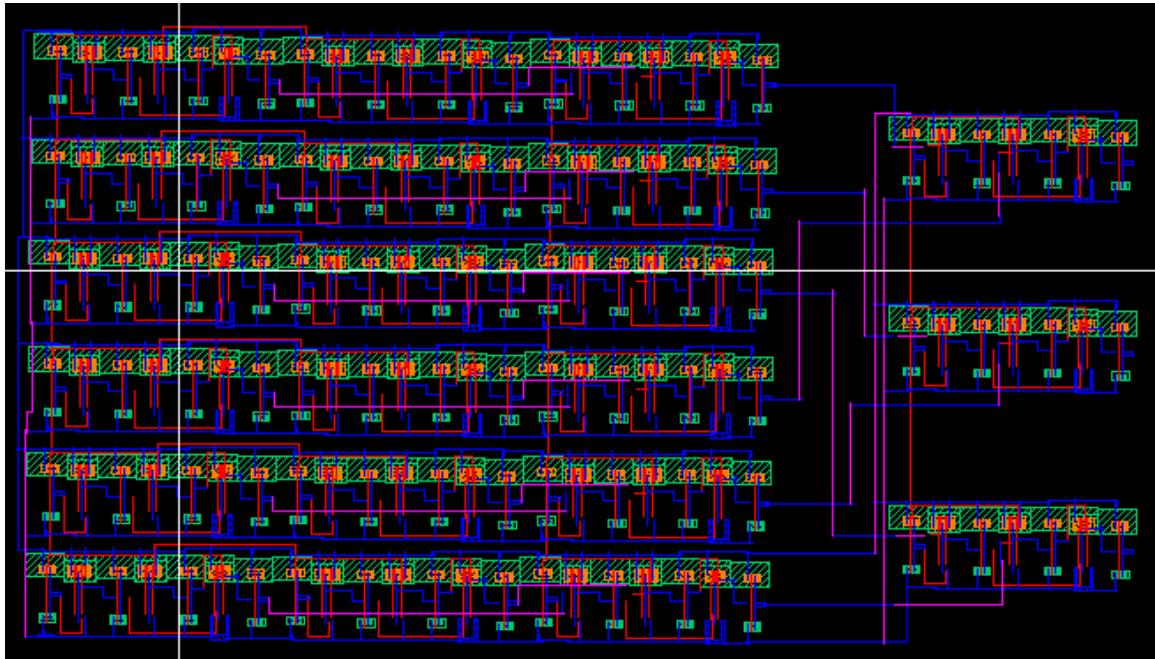


Figure 47: Mux\_8\_1\_3\_bit Layout

---

The net-lists match.

	layout	schematic
	instances	
un-matched	0	0
rewired	0	0
size errors	0	0
pruned	0	0
active	420	420
total	420	420

	nets	
un-matched	0	0
merged	0	0
pruned	0	0
active	239	239
total	239	239

	terminals	
un-matched	0	0
matched but different type	0	0
total	32	32

Probe files from /afs/umbc.edu/users/s/e/seanm5/home/home/LVS/schematic

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:

Probe files from /afs/umbc.edu/users/s/e/seanm5/home/home/LVS/layout

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:

Figure 48: Mux\_8\_1\_3\_bit LVS

Mux\_8\_1\_8\_bit

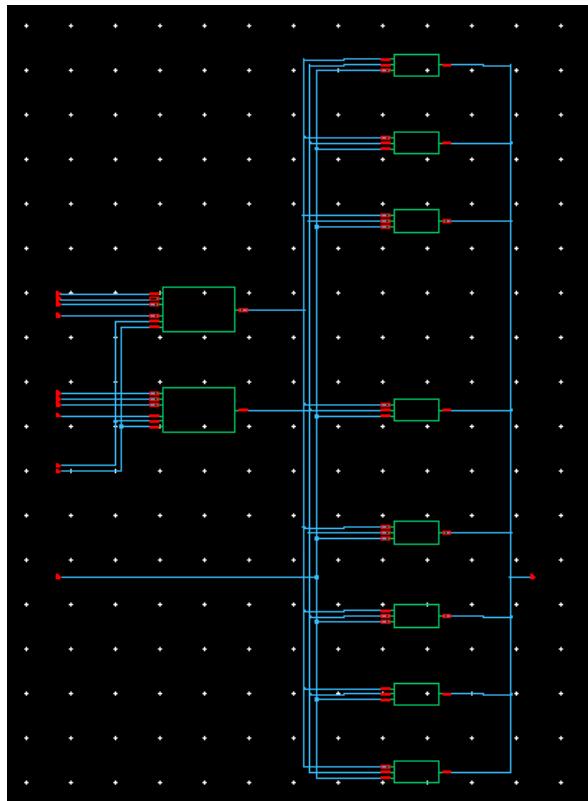


Figure 49: Mux\_8\_1\_8\_bit Schematic

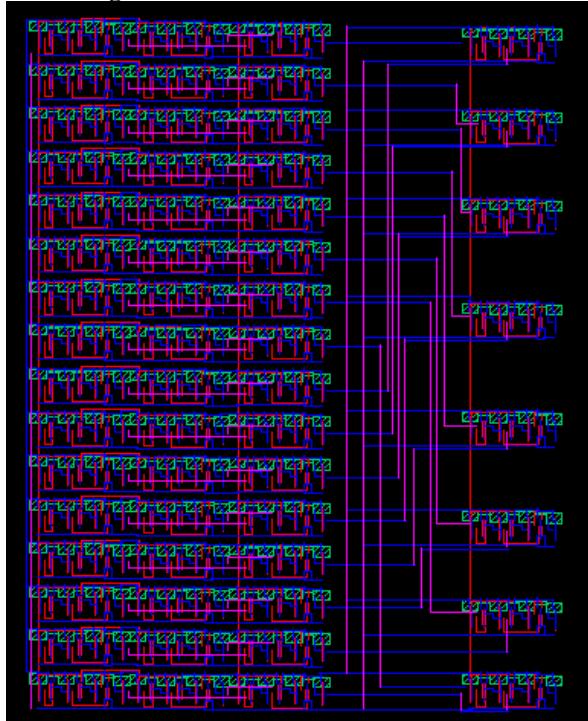


Figure 50: Mux\_8\_1\_8\_bit Layout

The net-lists match.

	layout	schematic
	instances	
un-matched	0	0
rewired	0	0
size errors	0	0
pruned	0	0
active	1120	1120
total	1120	1120

	nets	
un-matched	0	0
merged	0	0
pruned	0	0
active	629	629
total	629	629

	terminals	
un-matched	0	0
matched but different type	0	0
total	77	77

Probe files from /afs/umbc.edu/users/s/e/seanm5/home/home/LVS/schematic

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:

Probe files from /afs/umbc.edu/users/s/e/seanm5/home/home/LVS/layout

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:

---

Figure 51: Mux\_8\_1\_8\_bit LVS

Decoder2\_4

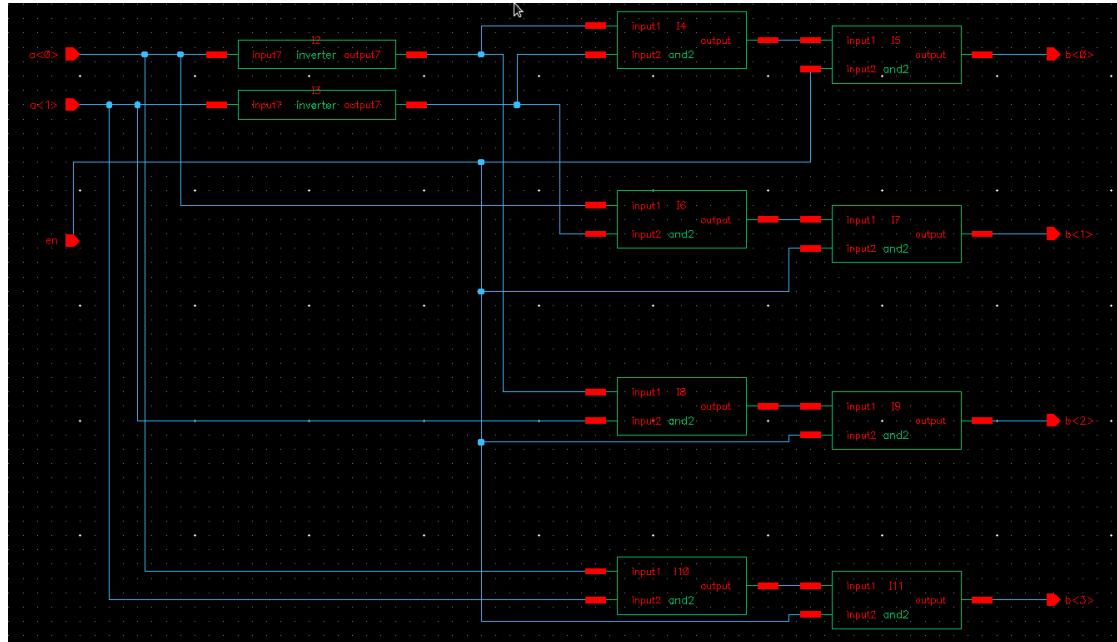


Figure 52: Decoder2\_4 Schematic

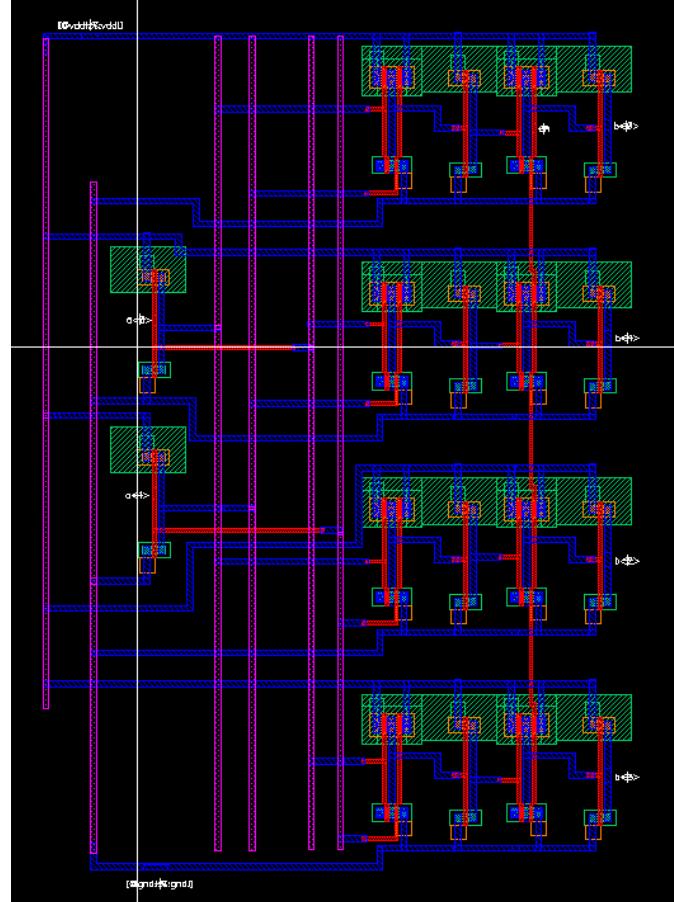


Figure 53: Decoder2\_4 Layout

The net-lists match.

	layout	schematic
	instances	
un-matched	0	0
rewired	0	0
size errors	0	0
pruned	0	0
active	52	52
total	52	52

	nets	
un-matched	0	0
merged	0	0
pruned	0	0
active	31	31
total	31	31

	terminals	
un-matched	0	0
matched but different type	0	0
total	9	9

Probe files from /afs/umbc.edu/users/s/e/seannm5/home/home/LVS/schematic

```
devbad.out:  
netbad.out:  
mergenet.out:  
termbad.out:  
prunenet.out:  
prunedev.out:  
audit.out:
```

Probe files from /afs/umbc.edu/users/s/e/seannm5/home/home/LVS/layout

```
devbad.out:  
netbad.out:  
mergenet.out:  
termbad.out:  
prunenet.out:  
prunedev.out:  
audit.out:
```

---

Figure 54: Decoder2\_4 LVS

Decoder3\_8

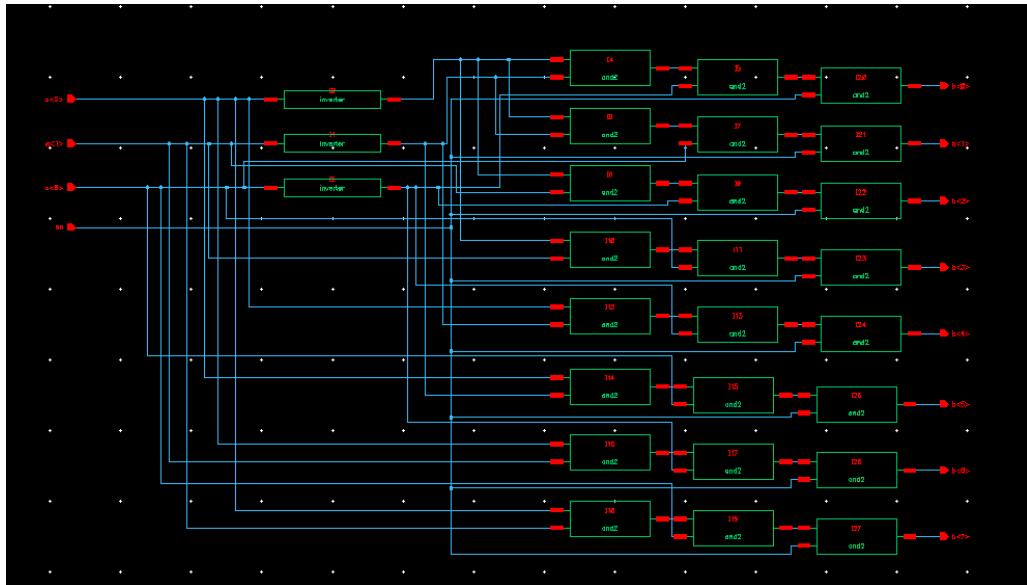


Figure 55: Decoder3\_8 Schematic

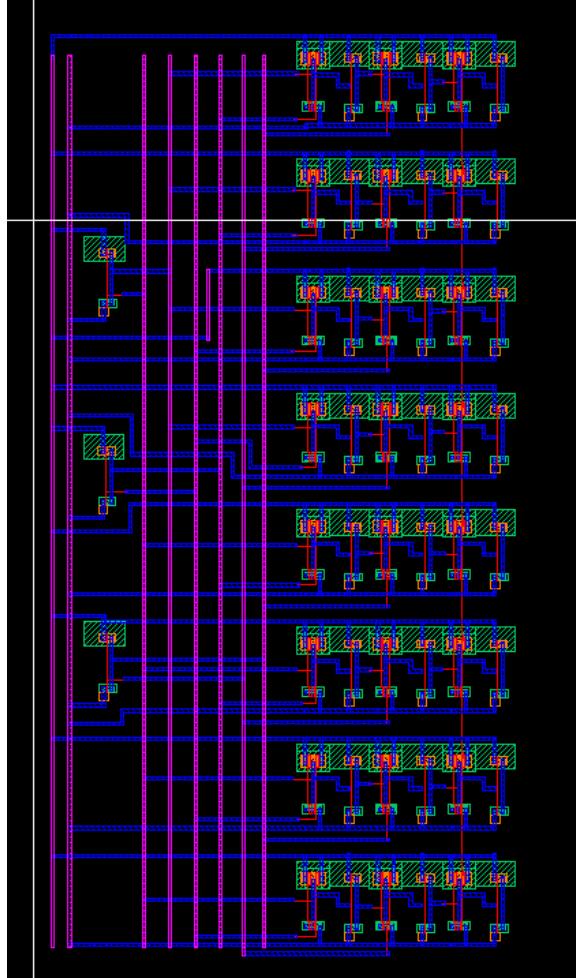


Figure 56: Decoder3\_8 Layout

The net-lists match.

	layout	schematic
	instances	
un-matched	0	0
rewired	0	0
size errors	0	0
pruned	0	0
active	150	150
total	150	150

	nets	
un-matched	0	0
merged	0	0
pruned	0	0
active	81	81
total	81	81

	terminals	
un-matched	0	0
matched but different type	0	0
total	14	14

Probe files from /afs/umbc.edu/users/s/e/seanm5/home/home/LVS/schematic

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:

Probe files from /afs/umbc.edu/users/s/e/seanm5/home/home/LVS/layout

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:

Figure 57: Decoder3\_8 LVS

Encoder4\_2

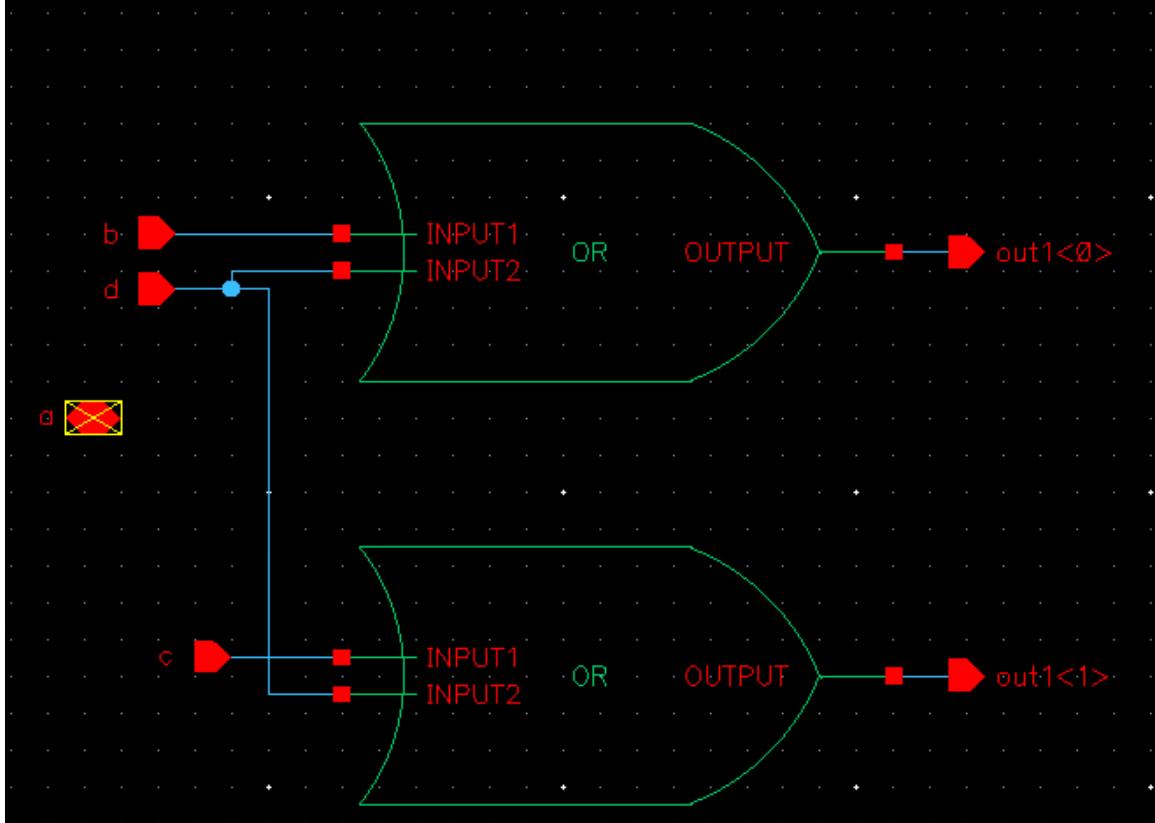


Figure 58: Encoder4\_2 Schematic

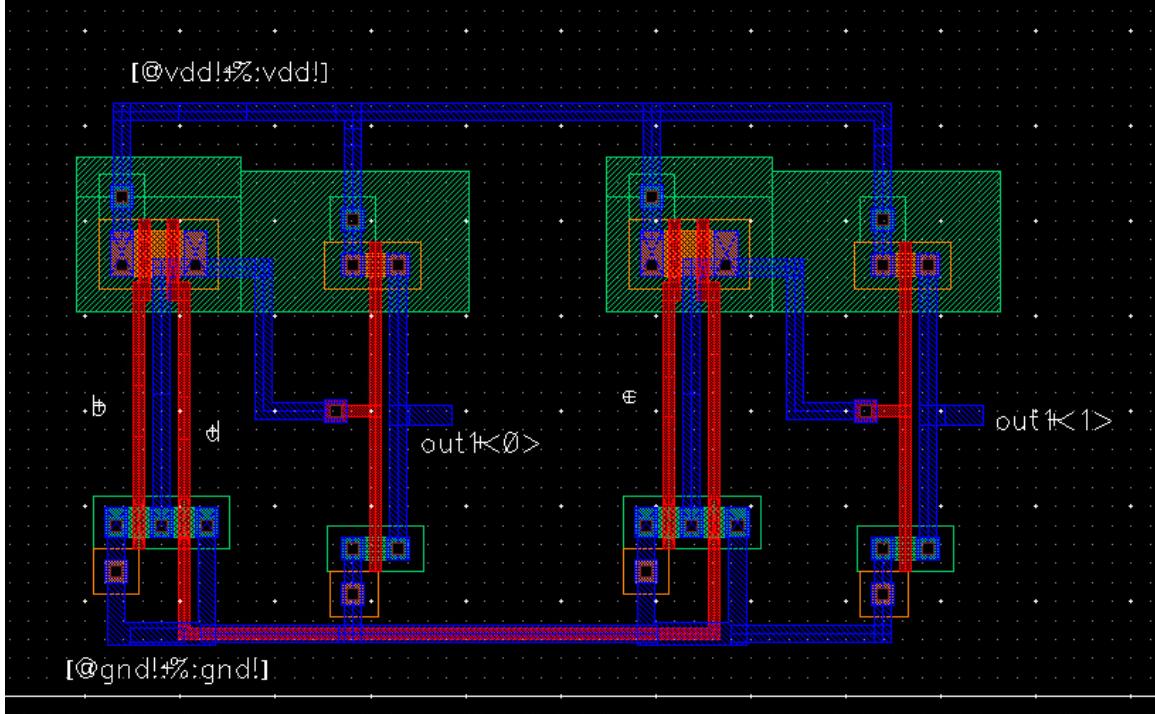


Figure 59: Encoder4\_2 Layout

The net-lists match.

	layout	schematic
	instances	
un-matched	0	0
rewired	0	0
size errors	0	0
pruned	0	0
active	12	12
total	12	12
	nets	
un-matched	0	0
merged	0	0
pruned	0	0
active	11	11
total	11	11
	terminals	
un-matched	0	0
matched but		
different type	0	0
total	7	8

Probe files from /afs/umbc.edu/users/s/e/seanm5/home/home/LVS/schematic  
devbad.out:  
netbad.out:  
mergenet.out:  
termbad.out:  
? Terminal a is floating in the schematic.

Figure 60: Encoder4\_2 LVS

## Hit\_or\_Miss

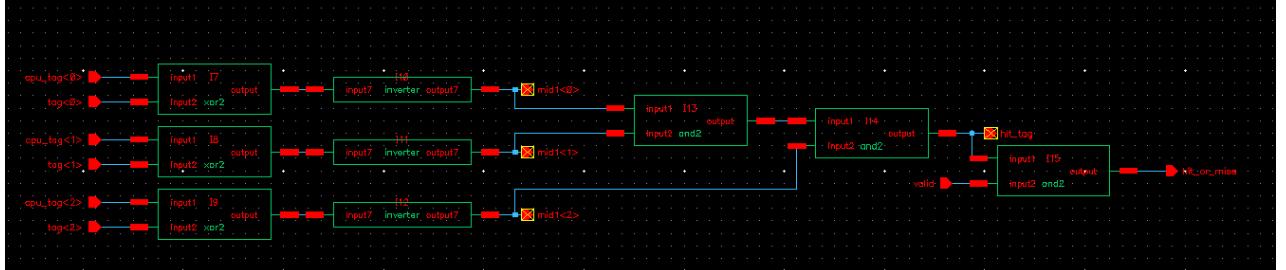


Figure 61: Hit\_or\_Miss Schematic

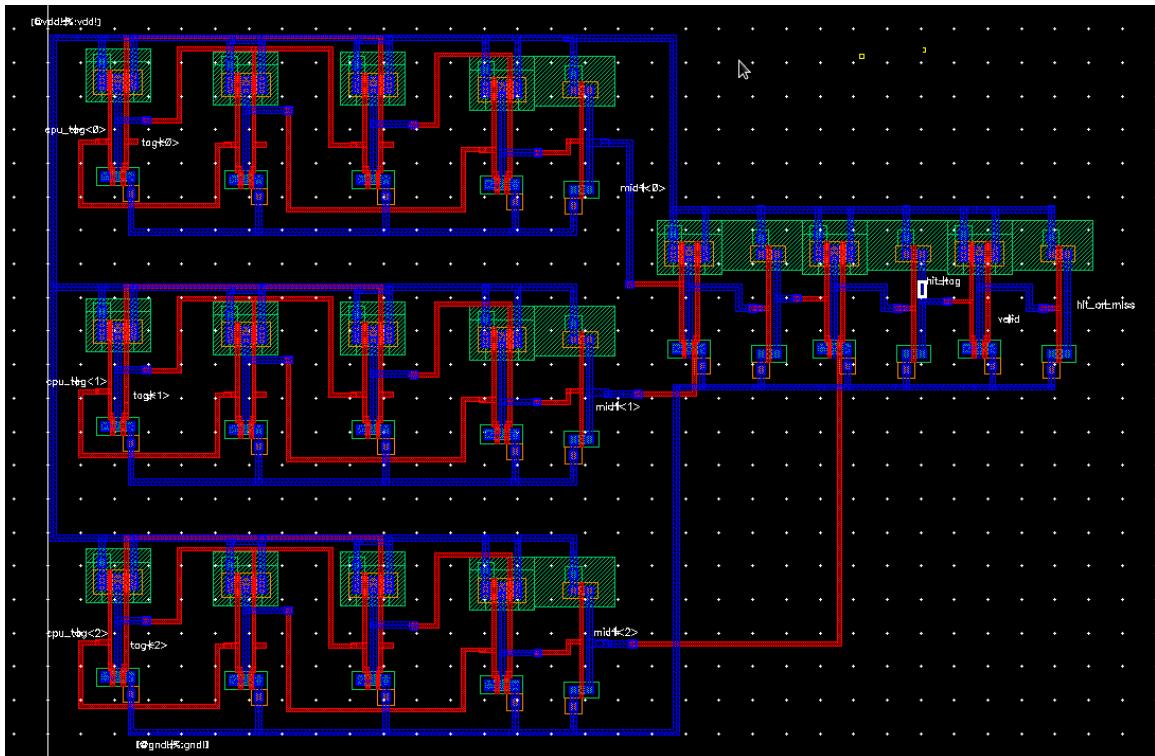


Figure 62: Hit\_or\_Miss Layout

The net-lists match.

	layout	schematic
	instances	
un-matched	0	0
rewired	0	0
size errors	0	0
pruned	0	0
active	72	72
total	72	72

	nets	
un-matched	0	0
merged	0	0
pruned	0	0
active	45	45
total	45	45

	terminals	
un-matched	0	0
matched but different type	0	0
total	14	14

Figure 63: Hit\_or\_Miss LVS

Cache\_1\_bit

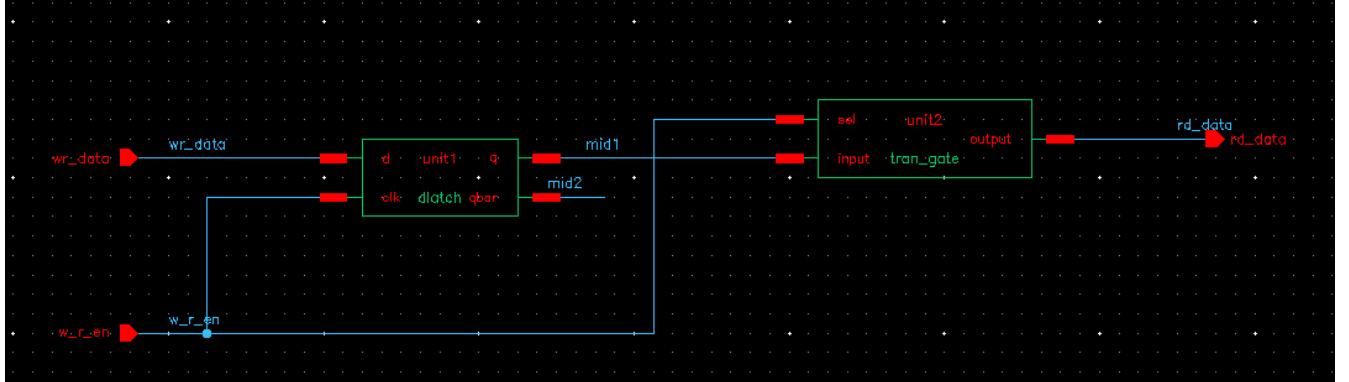


Figure 64: Cache\_1\_bit Schematic

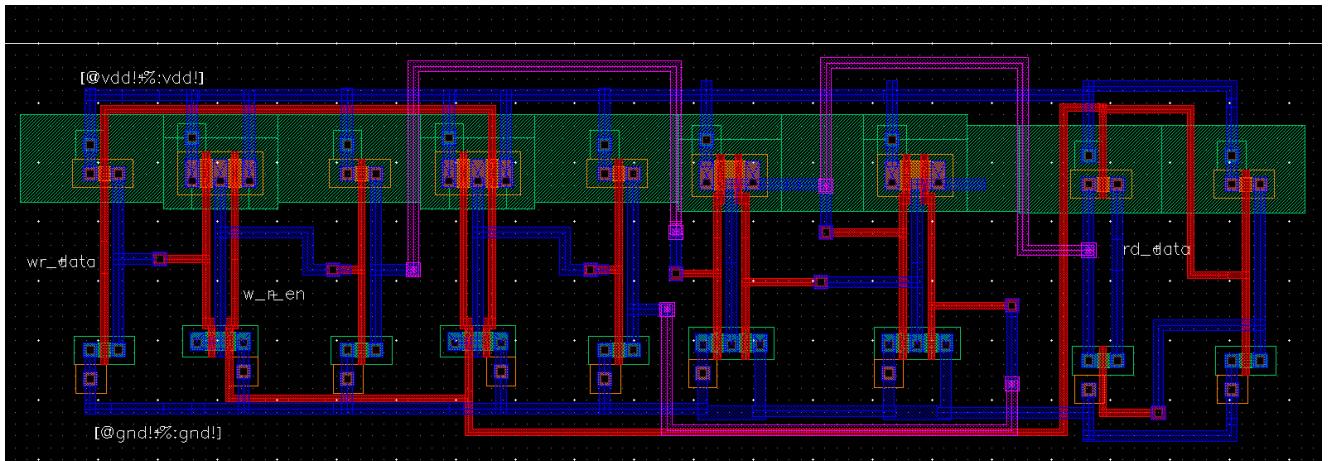


Figure 65: Cache\_1\_bit Layout

The net-lists match.

	layout	schematic
	instances	
un-matched	0	0
rewired	0	0
size errors	0	0
pruned	0	0
active	26	26
total	26	26

	nets	
un-matched	0	0
merged	0	0
pruned	0	0
active	17	17
total	17	17

	terminals	
un-matched	0	0
matched but		
different type	0	0
total	5	5

```
Probe files from /afs/umbc.edu/users/s/e/seanm5/home/home/LVS/schematic
devbad.out:
netbad.out:
mergenet.out:
termbad.out:
prunenet.out:
prunedev.out:
audit.out:
```

```
Probe files from /afs/umbc.edu/users/s/e/seanm5/home/home/LVS/layout
devbad.out:
netbad.out:
mergenet.out:
termbad.out:
prunenet.out:
```

---

Figure 66: Cache\_1\_bit LVS

Cache\_8\_bit

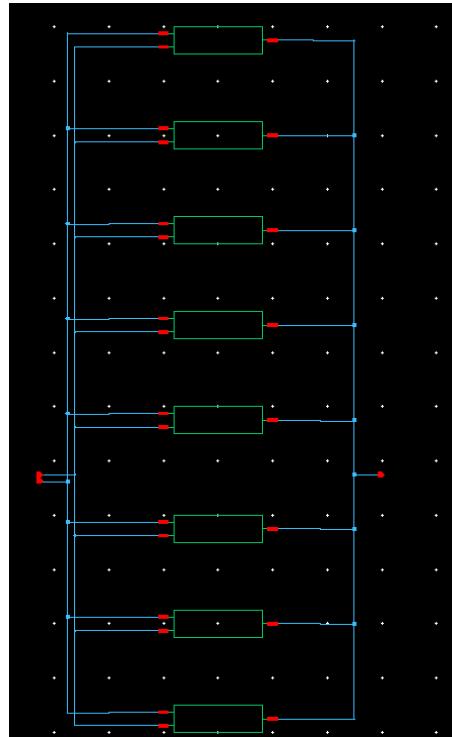


Figure 67: Cache\_8\_bit Schematic

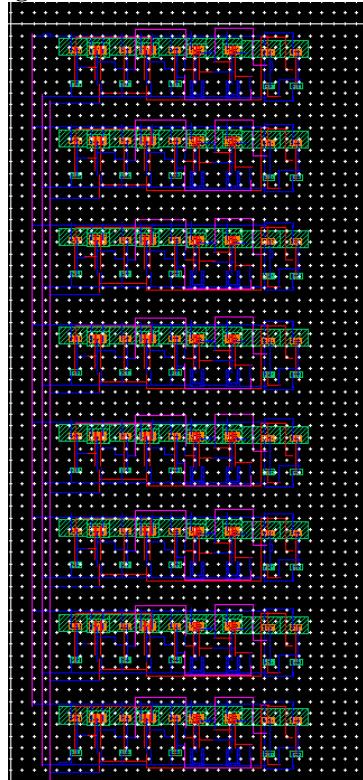


Figure 68: Cache\_8\_bit Layout

The net-lists match.

	layout	schematic
	instances	
un-matched	0	0
rewired	0	0
size errors	0	0
pruned	0	0
active	208	208
total	208	208

	nets	
un-matched	0	0
merged	0	0
pruned	0	0
active	115	115
total	115	115

	terminals	
un-matched	0	0
matched but different type	0	0
total	19	19

Probe files from /afs/umbc.edu/users/s/e/seanm5/home/home/LVS/schematic

**devbad.out:**

**netbad.out:**

**mergenet.out:**

**termbad.out:**

**prunenet.out:**

**prunedev.out:**

**audit.out:**

Probe files from /afs/umbc.edu/users/s/e/seanm5/home/home/LVS/layout

**devbad.out:**

**netbad.out:**

**mergenet.out:**

**termbad.out:**

**prunenet.out:**

**prunedev.out:**

**Figure 69: Cache\_8\_bit LVS**

## Cache\_block

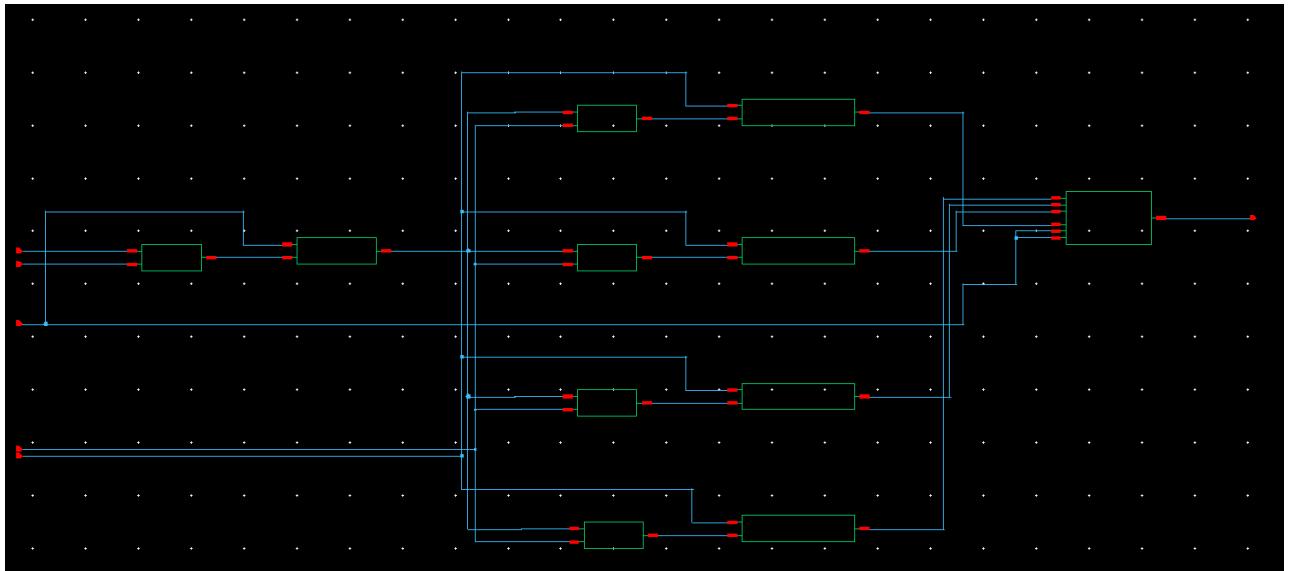


Figure 70: Cache\_block Schematic

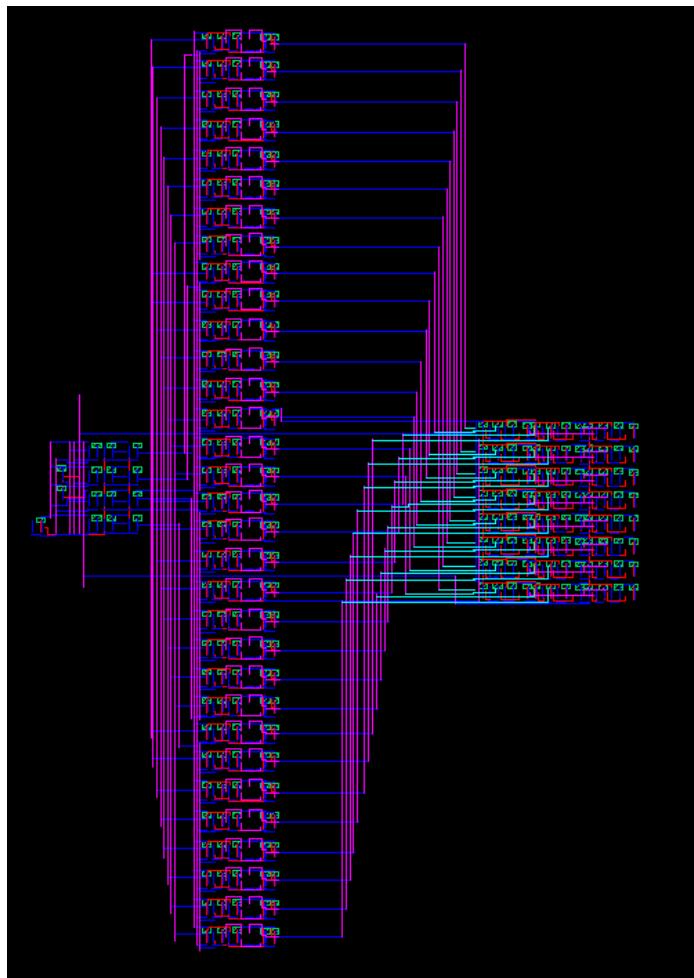


Figure 71: Cache\_block Layout

---

```
The net-lists match.

          layout schematic
          instances
un-matched      0      0
rewired         0      0
size errors     0      0
pruned          0      0
active          1394   1394
total           1394   1394

          nets
un-matched      0      0
merged          0      0
pruned          0      0
active          712    712
total           712    712

          terminals
un-matched      0      0
matched but
different type   0      0
total            23    23

Probe files from /afs/umbc.edu/users/s/e/seanm5/home/home/LVS/schematic

devbad.out:
netbad.out:
mergenet.out:
termbad.out:
prunenet.out:
prunedev.out:
audit.out:

Probe files from /afs/umbc.edu/users/s/e/seanm5/home/home/LVS/layout

devbad.out:
netbad.out:
mergenet.out:
termbad.out:
prunenet.out:
prunedev.out:
audit.out:
```

Figure 72: Cache\_block LVS

## Cache

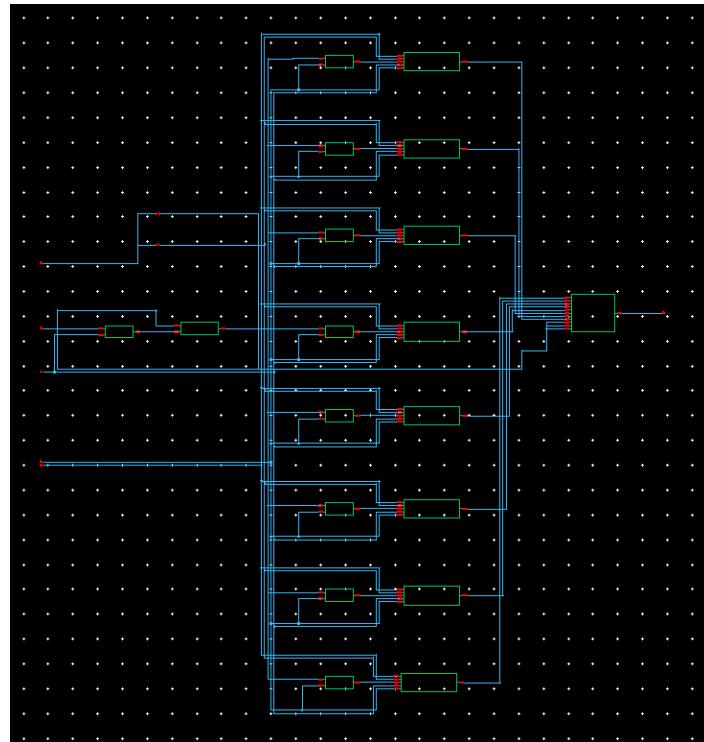


Figure 73: Cache Schematic

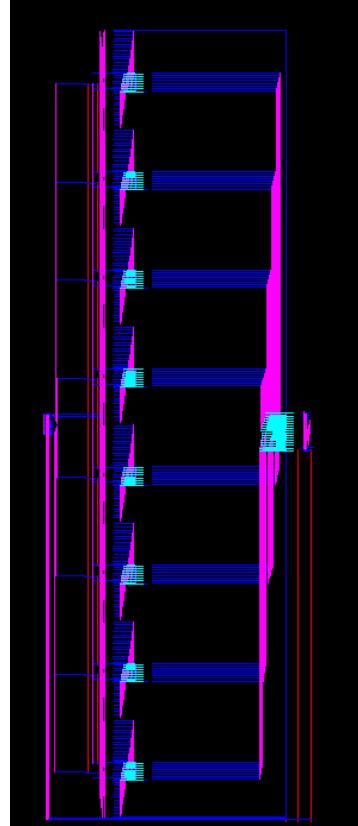


Figure 74: Cache Layout

The net-lists match.

	layout	schematic
	instances	
un-matched	0	0
rewired	0	0
size errors	0	0
pruned	0	0
active	12476	12476
total	12476	12476

	nets	
un-matched	0	0
merged	0	0
pruned	0	0
active	6256	6256
total	6256	6256

	terminals	
un-matched	0	0
matched but different type	0	0
total	26	29

Probe files from /afs/umbc.edu/users/s/e/seanm5/home/home/LVS/schematic

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

? Terminal cpu\_addr<5> is floating in the schematic.

? Terminal cpu\_addr<6> is floating in the schematic.

? Terminal cpu\_addr<7> is floating in the schematic.

prunenet.out:

prunedev.out:

audit.out:

Probe files from /afs/umbc.edu/users/s/e/seanm5/home/home/LVS/layout

devbad.out:

netbad.out:

~~mergenet.out~~:

Figure 75: Cache LVS

### Cache\_tag\_block

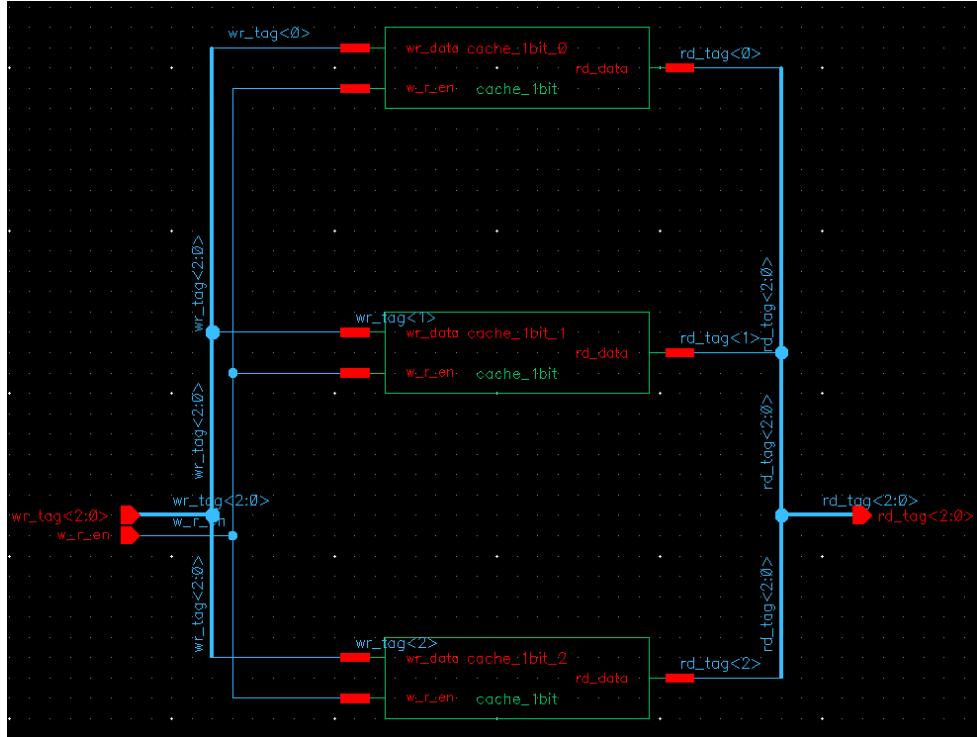


Figure 76: Cache\_tag\_block Schematic

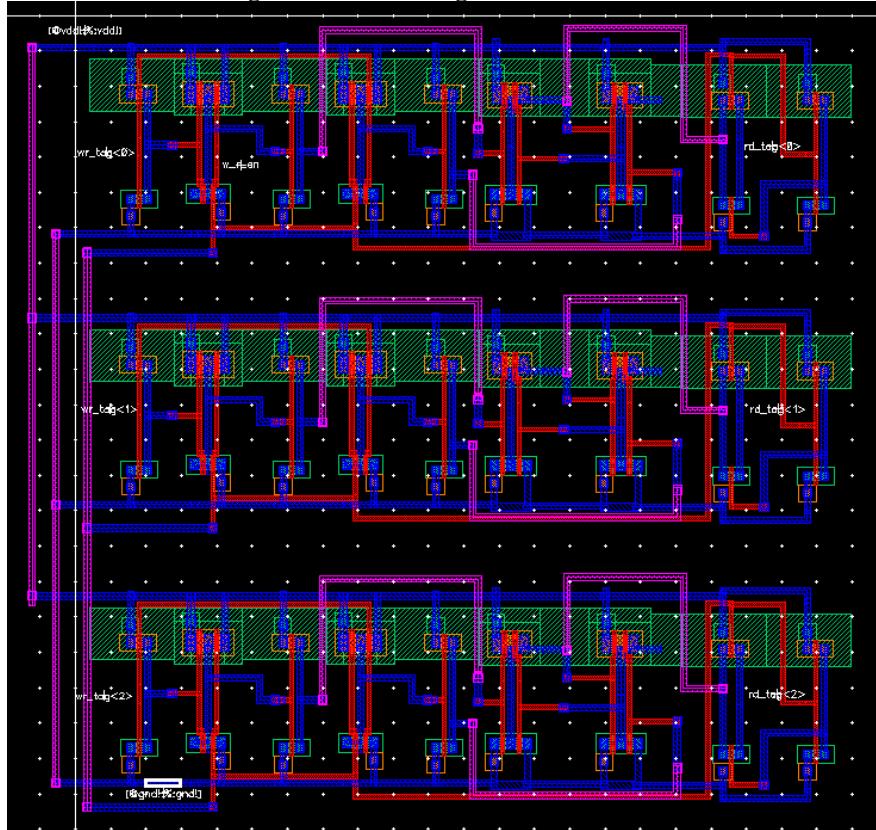


Figure 77: Cache\_tag\_block Layout

The net-lists match.

	layout	schematic
	instances	
un-matched	0	0
rewired	0	0
size errors	0	0
pruned	0	0
active	78	78
total	78	78

	nets	
un-matched	0	0
merged	0	0
pruned	0	0
active	45	45
total	45	45

	terminals	
un-matched	0	0
matched but different type	0	0
total	9	9

Probe files from /afs/umbc.edu/users/s/e/seanm5/home/home/LVS/schematic

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:

↳

Probe files from /afs/umbc.edu/users/s/e/seanm5/home/home/LVS/layout

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

---

Figure 78: Cache\_tag\_block LVS

Cache\_tag

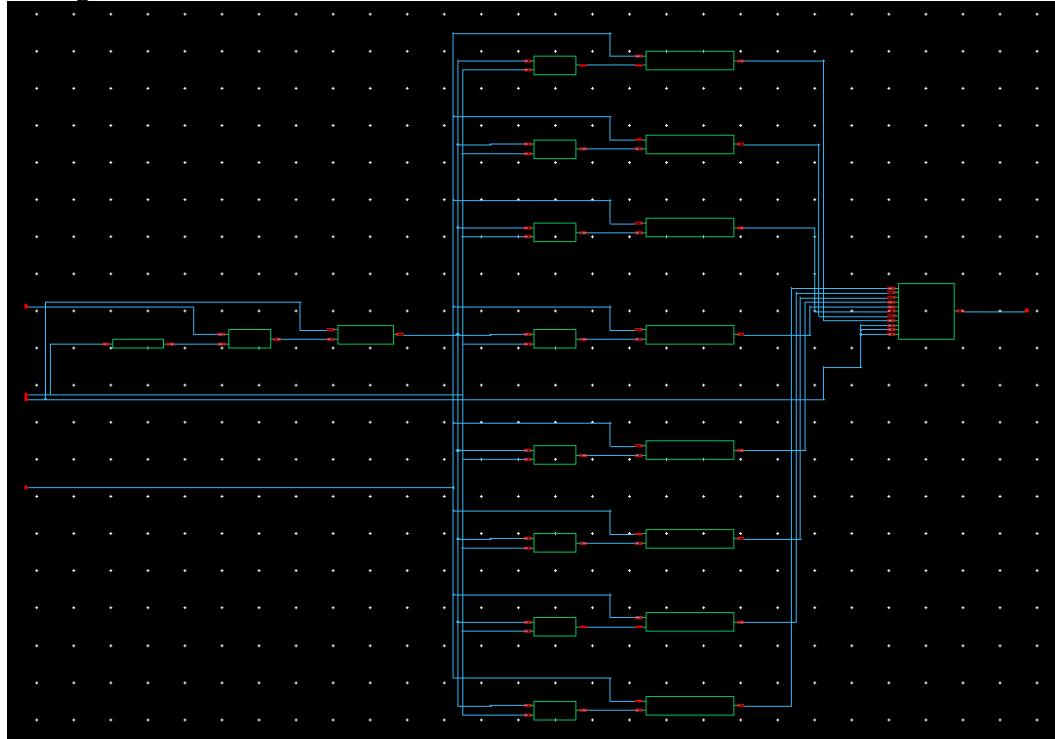


Figure 79: Cache\_tag Schematic

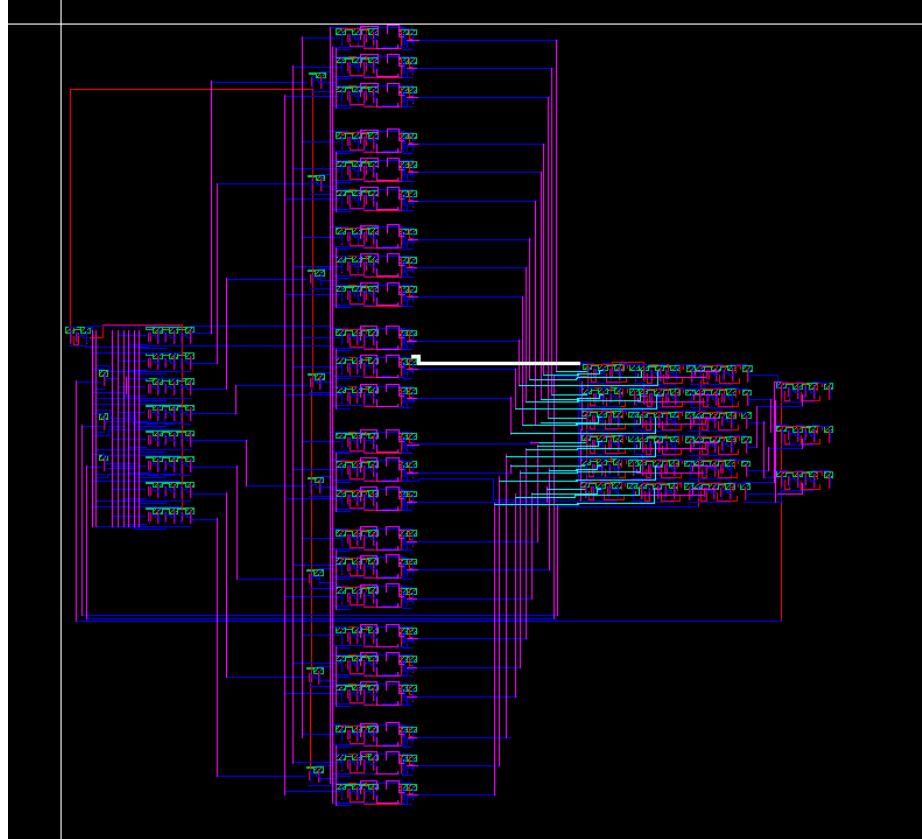


Figure 80: Cache\_tag Layout

The net-lists match.

	layout	schematic
	instances	
un-matched	0	0
rewired	0	0
size errors	0	0
pruned	0	0
active	1250	1250
total	1250	1250
	nets	
un-matched	0	0
merged	0	0
pruned	0	0
active	635	635
total	635	635
	terminals	
un-matched	0	0
matched but different type	0	0
total	13	13

Probe files from /afs/umbc.edu/users/s/e/seanm5/home/home/LVS/schematic

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:

Probe files from /afs/umbc.edu/users/s/e/seanm5/home/home/LVS/layout

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

Figure 81: Cache\_tag LVS

Cache\_valid

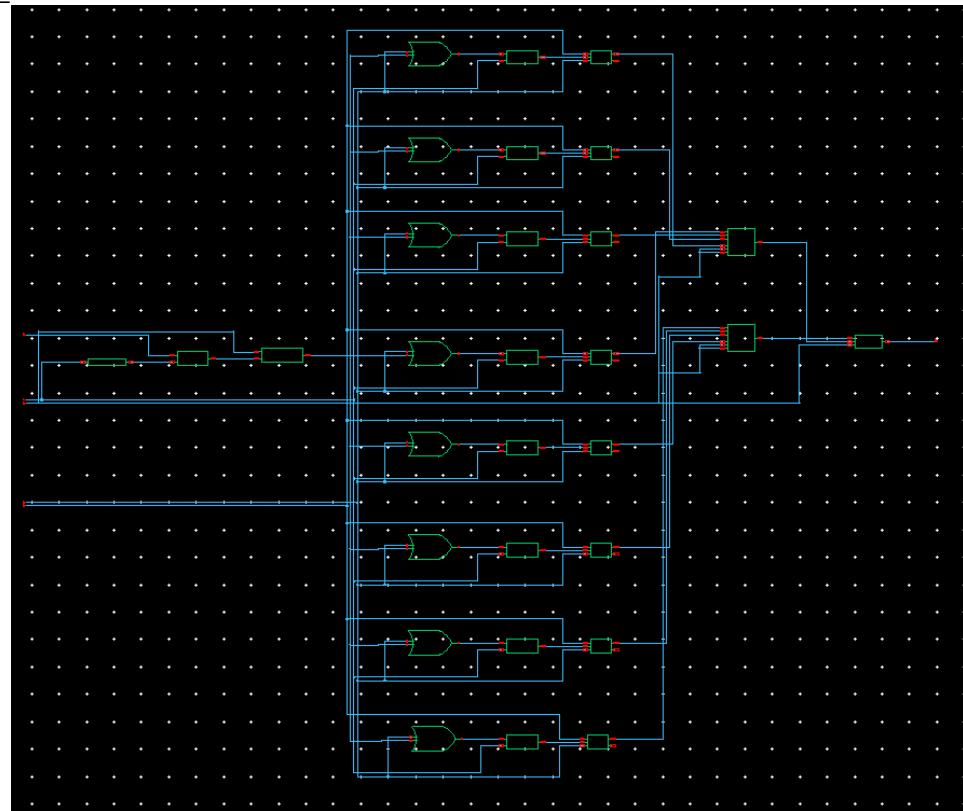


Figure 82: Cache\_valid Schematic

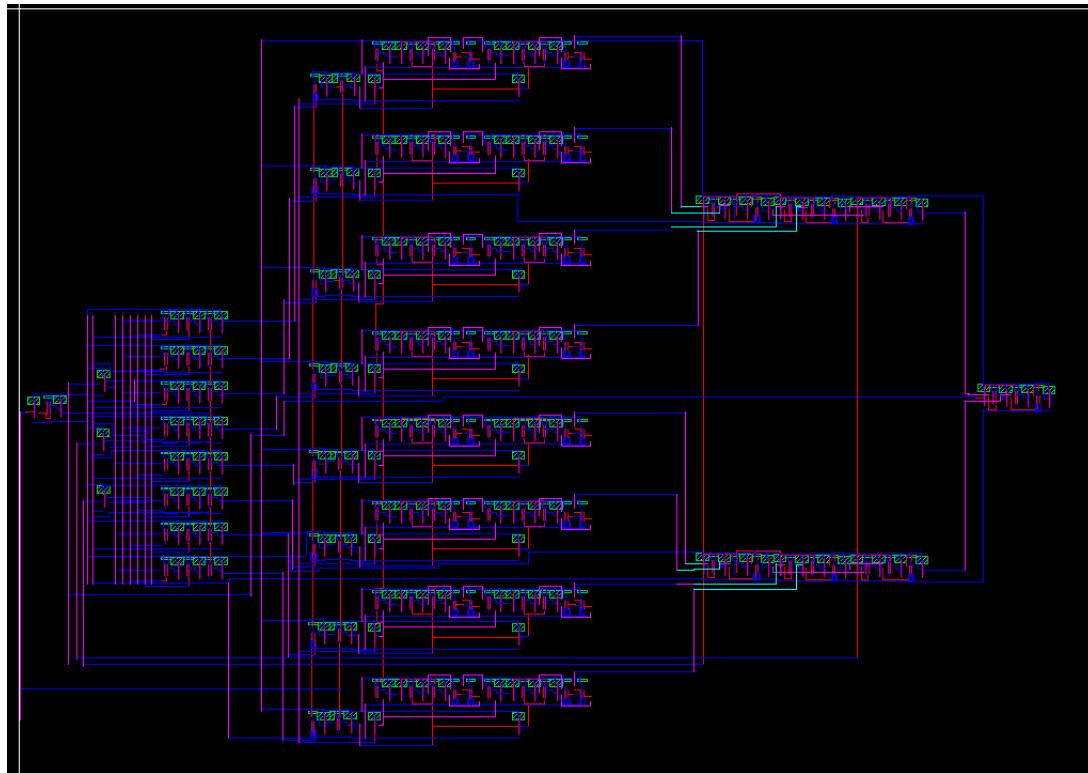


Figure 83: Cache\_valid Layout

The net-lists match.

	layout	schematic
	instances	
un-matched	0	0
rewired	0	0
size errors	0	0
pruned	0	0
active	874	874
total	874	874

	nets	
un-matched	0	0
merged	0	0
pruned	0	0
active	446	446
total	446	446

	terminals	
un-matched	0	0
matched but different type	0	0
total	8	10

Probe files from /afs/umbc.edu/users/s/e/seanm5/home/home/LVS/schematic

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:

Probe files from /afs/umbc.edu/users/s/e/seanm5/home/home/LVS/layout

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

Figure 84: Cache\_valid LVS

## Counter

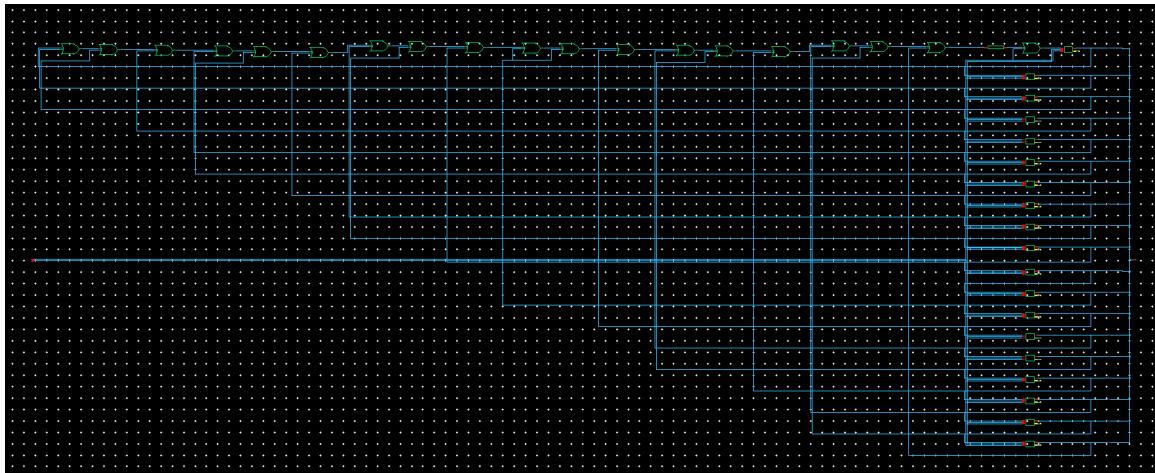


Figure 85: Counter Schematic



Figure 86: Counter Layout

The net-lists match.

	layout	schematic
	instances	
un-matched	0	0
rewired	0	0
size errors	0	0
pruned	0	0
active	1256	1256
total	1256	1256

	nets	
un-matched	0	0
merged	0	0
pruned	0	0
active	632	632
total	632	632

	terminals	
un-matched	0	0
matched but different type	0	0
total	23	23

Probe files from /afs/umbc.edu/users/s/e/seanm5/home/home/LVS/schematic

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:

Probe files from /afs/umbc.edu/users/s/e/seanm5/home/home/LVS/layout

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

Figure 87: Counter LVS

State\_Machine

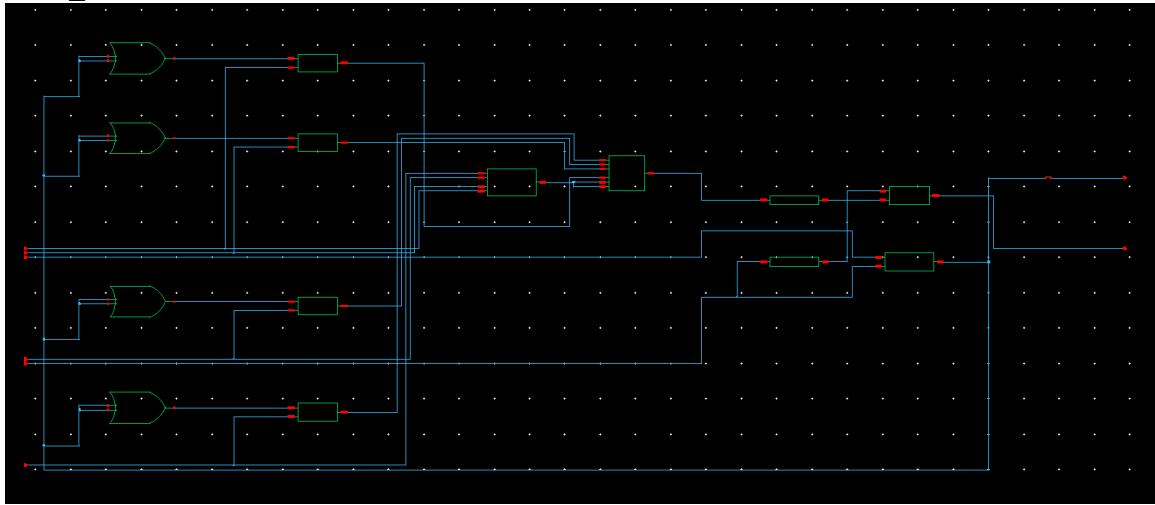


Figure 88: State\_Machine Schematic

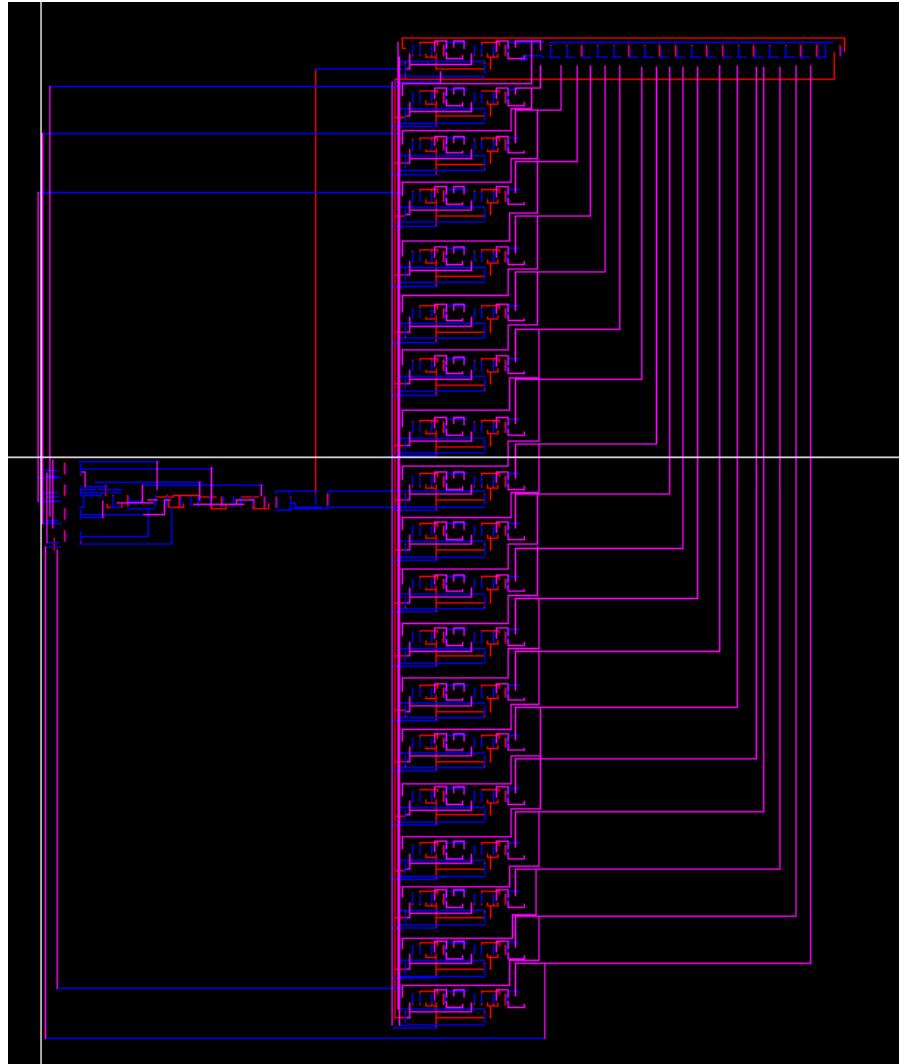


Figure 89: State\_Machine Layout

The net-lists match.

	layout	schematic
	instances	
un-matched	0	0
rewired	0	0
size errors	0	0
pruned	0	0
active	1386	1386
total	1386	1386

	nets	
un-matched	0	0
merged	0	0
pruned	0	0
active	701	701
total	701	701

	terminals	
un-matched	0	0
matched but		
different type	0	0
total	26	28

Probe files from /afs/umbc.edu/users/s/e/seanm5/home/home/LVS/schematic

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:

Probe files from /afs/umbc.edu/users/s/e/seanm5/home/home/LVS/layout

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

**Figure 90: State\_Machine LVS**

Chip

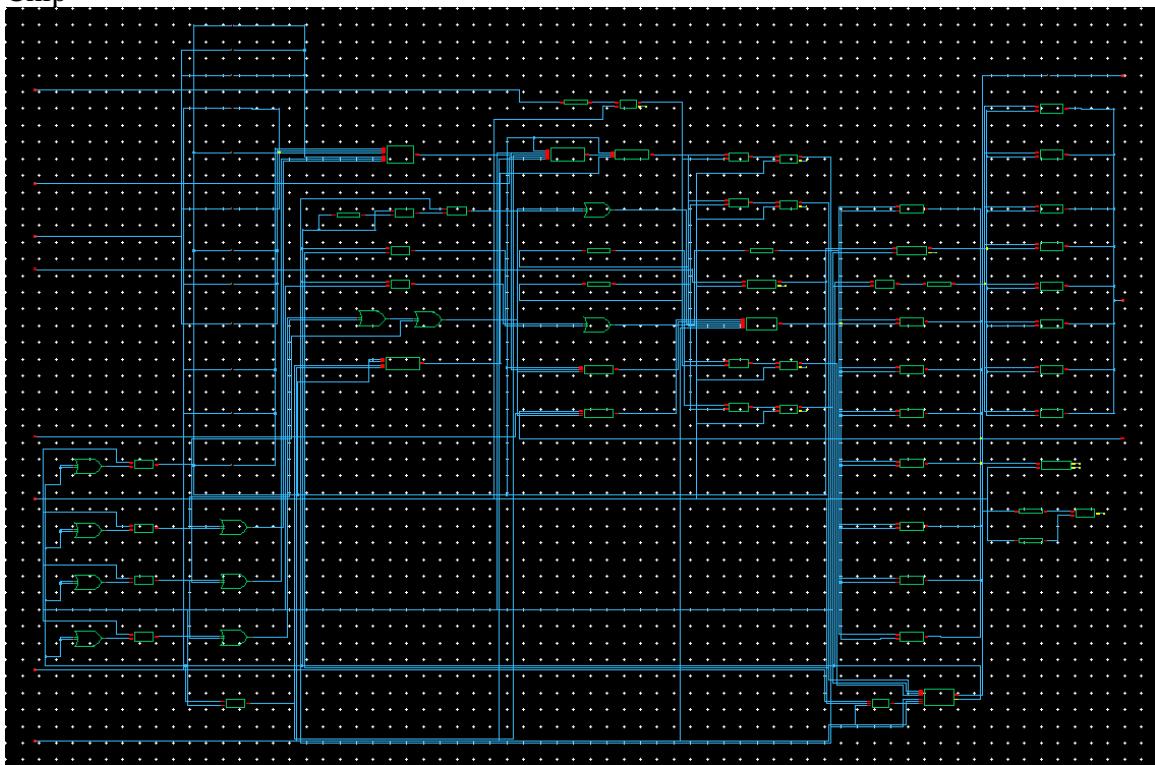


Figure 91: Chip Schematic

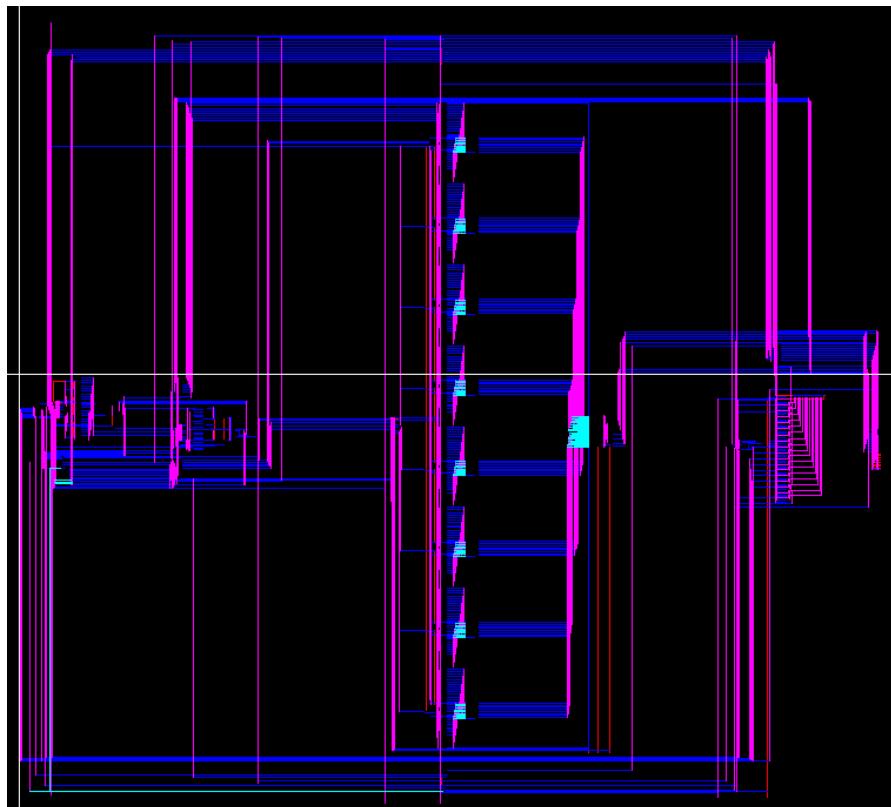


Figure 92: Chip Layout

The net-lists match.

	layout	schematic
	instances	
un-matched	0	0
rewired	0	0
size errors	0	0
pruned	0	0
active	17752	17752
total	17752	17752

	nets	
un-matched	0	0
merged	0	0
pruned	0	0
active	8900	8900
total	8900	8900

	terminals	
un-matched	0	0
matched but different type	0	0
total	41	41

Probe files from /afs/umbc.edu/users/s/e/seanm5/home/home/LVS/schematic

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:

Probe files from /afs/umbc.edu/users/s/e/seanm5/home/home/LVS/layout

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

-----

Figure 93: Chip LVS

**Project Status:** Our project is fully complete and functional.

### Layout Area Table

Layout	Length	Width	Area
Decoder2_4	135	95	12825
Decoder3_8	250	130	32500
Counter	810	1767	1432170
State Machine	1785	1445	2579325
Cache Block	1395	900	1255500
Cache	10700	3600	38520000
Chip	12700	14180	180086000

### Work Breakdown

Team Member	Work Completed
Nem Negash	<ul style="list-style-type: none"> <li>• State Machine</li> <li>• Chip</li> <li>• Counter</li> <li>• Encoder and Decoder</li> </ul>
Sean Mullins	<ul style="list-style-type: none"> <li>• All Cache Components</li> <li>• Hit or Miss</li> <li>• Muxes</li> </ul>