CMPE 315: Principles of VLSI Design

Lab Cover Page

Lab # : 2

Lab Title : Schematic Design and Spectre Simulations

Name : Nem Negash

Section : 1

Date Submitted : 09/29/2021

TA / Grader Use Only:

Late Submission Deduction (20% per day late):

Other Deductions:

Final Lab Grade:

Comments to student:

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Lab Procedure:

The lab had three parts to complete which was to create schematics, create symbols, creating configurations, running simulations, and plotting results. We used a cadence tool that allowed to do all these steps to complete the lab. Creating schematics was done by creating cell views and in those cell-views designing the specific gates like the inverter, NOR and NAND gates. From those cell-views, I created other cell-views to create symbols who the schematics. Form there I create other schematics in the library that incorporated the inverter, NOR, and NAND gates alongside other instances such as vdd and vpulse. These schematics were used to create simulation and for that I must set up configurations for each schematic. From there I select the libraries need and what simulator to use for the simulation. After selecting the input and output of the driver gate to be plotted I run the simulation and get the plot. This is done for a INVx1, INVx2, INVx4, NOR2x1, NAND2x1 gates where the INV gates each had 5 schematics where they are driving 1,2,4,8, and 16 copies of INVx1 gate. The NOR2x1 and NAND2x1 gates each had three schematics where they are driving 1,2,4 copies of the INVx1 gate. These three schematics were repeated by flipping the two inputs. These gives a total of 27 schematics and plots.

pMOS and nMOS sizes for gates:

Table 1: pMOS and nMOS width sizes for gates

Gate	pMOS width	nMOS width
INVx1	2.4u	1.5u
INVx2	4.8u	1.5u
INVx4	9.6u	1.5u
NOR2x1	2.4u	1.5u
NAND2x1	4.8u	3u

Schematics and Plots Discussion:

INVx1:

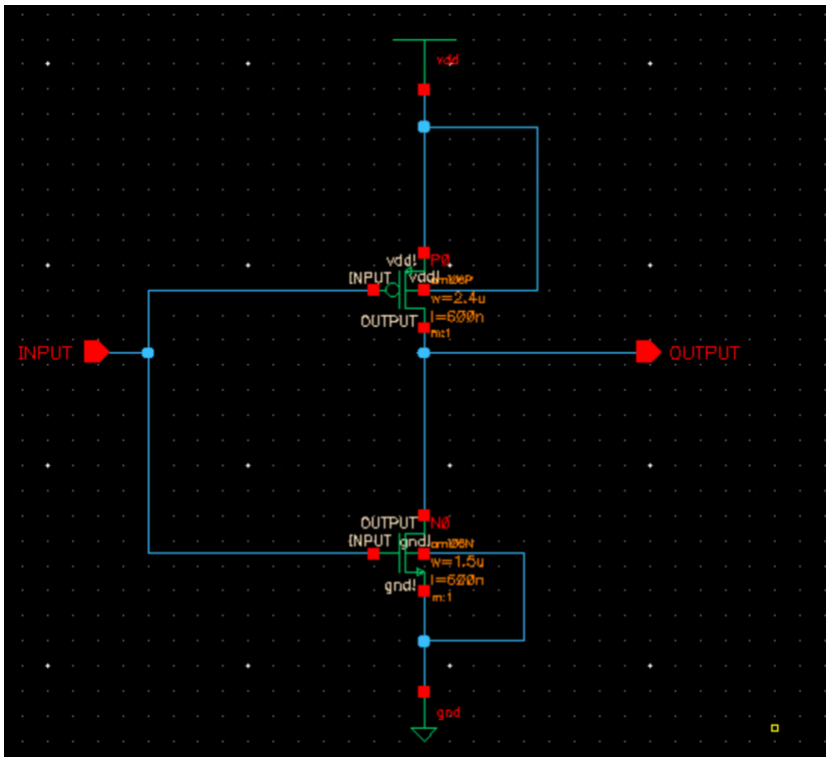

Figure 1: Schematic for INVx1

INVx1 driving 1 INVx1:

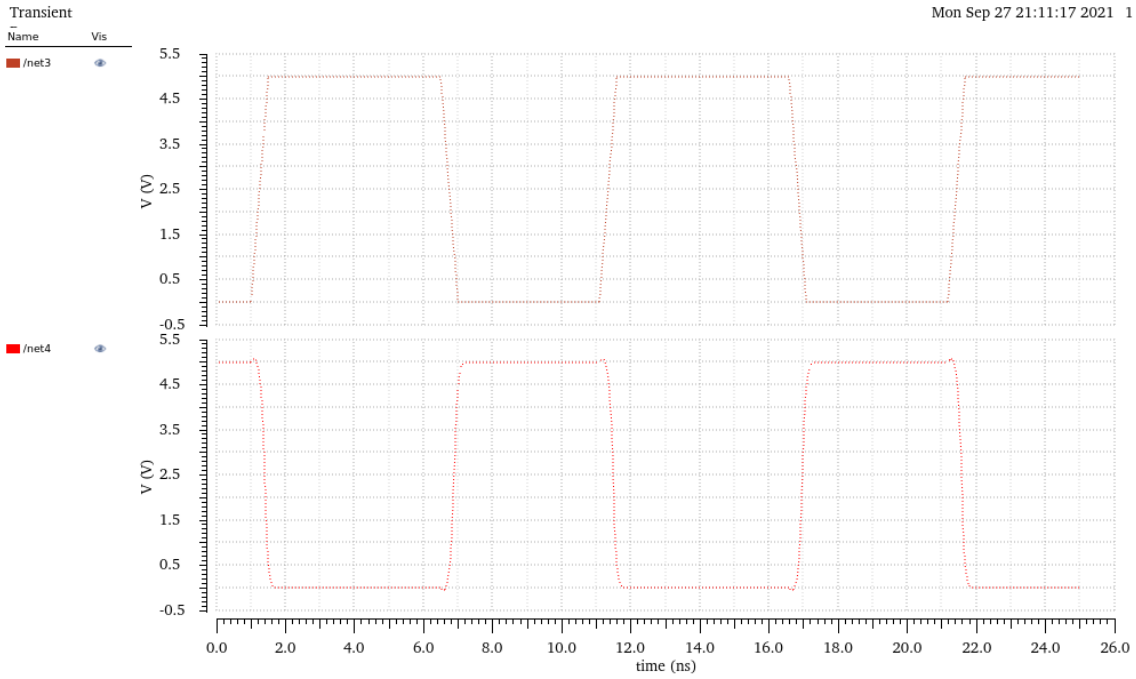

Figure 2: Simulation Plot for INVx1 driving 1 INVx1

INVx1 driving 2 INVx1:

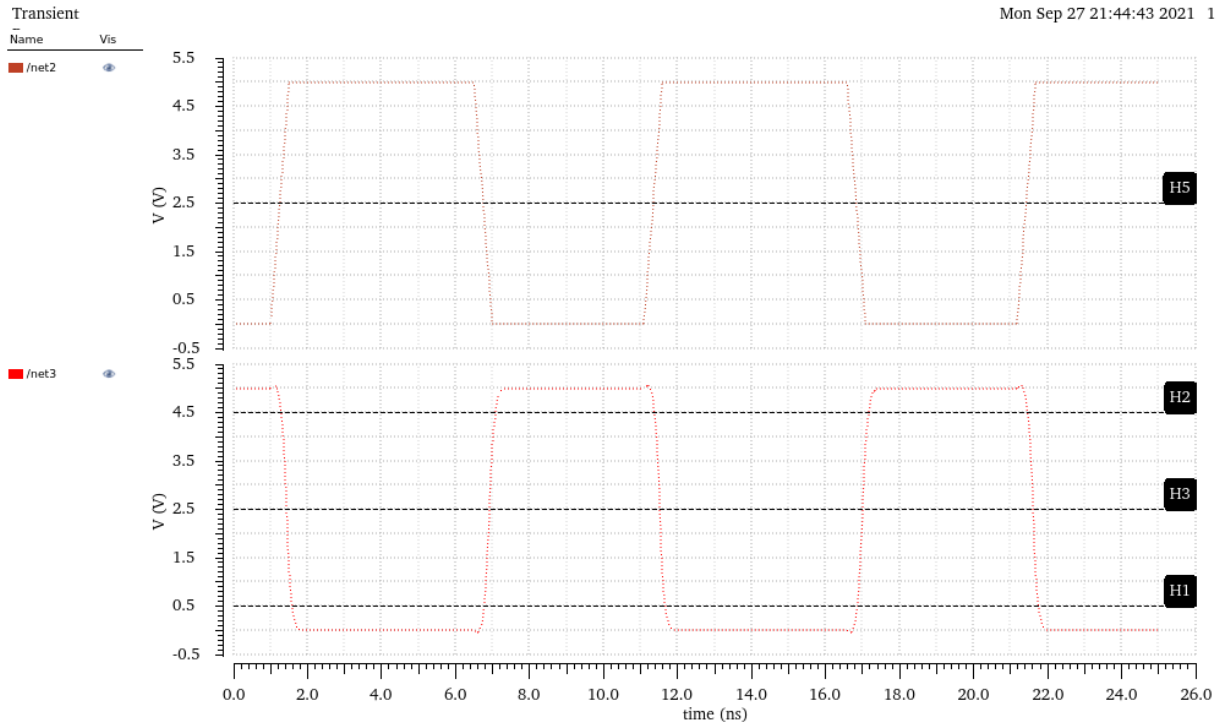

Figure 3: Simulation plot for INVx1 driving 2 INVx1

INVx1 driving 4 INVx1:

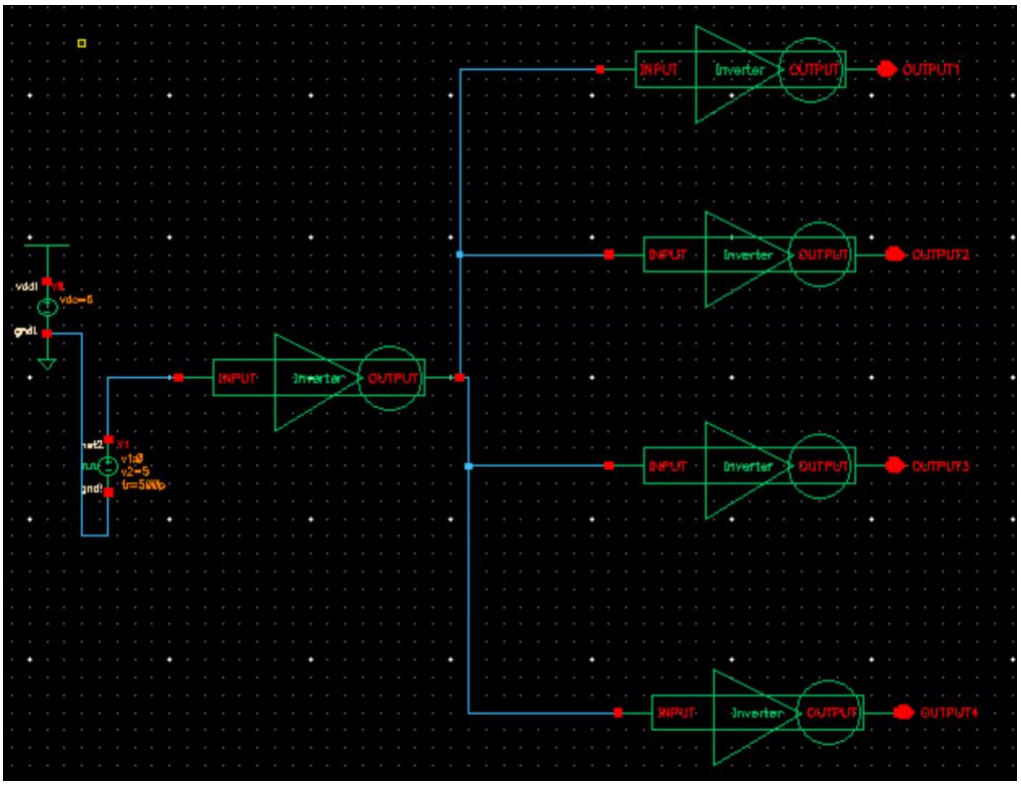

Figure 4: Schematic for INVx1 driving 4 INVx1

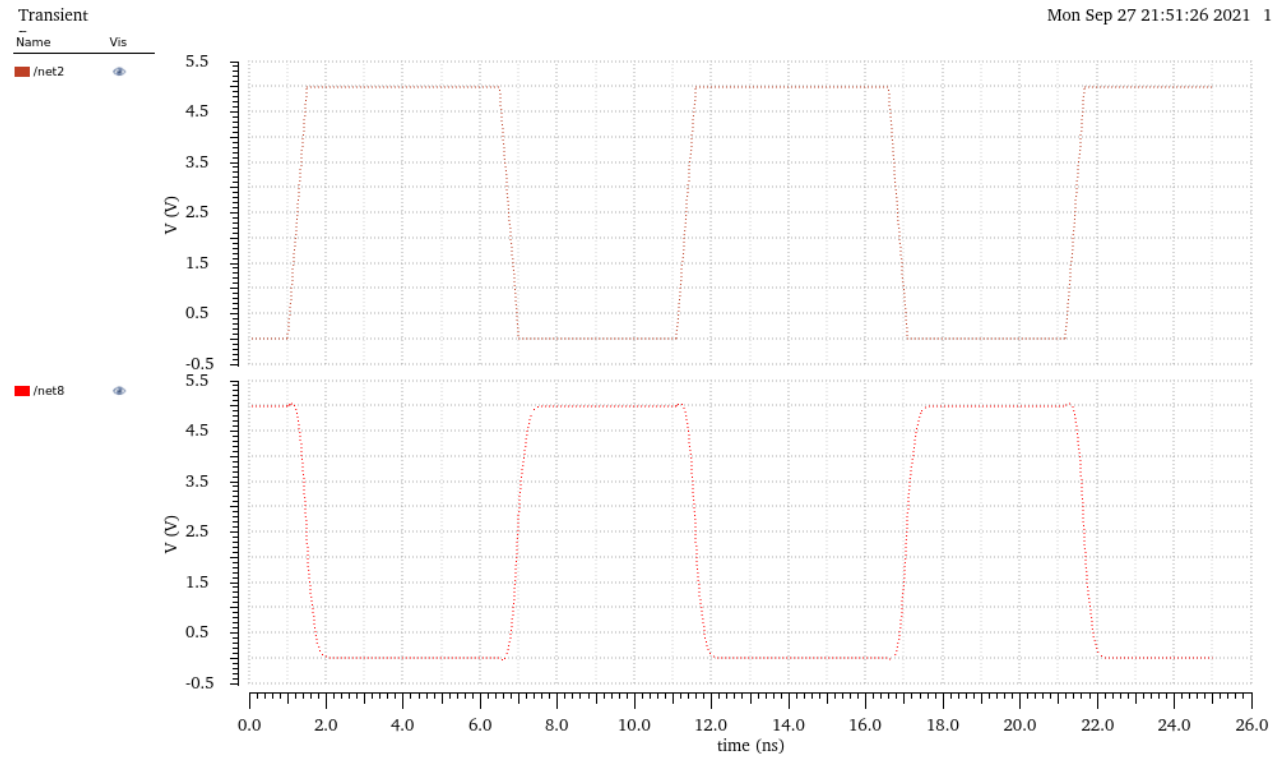

Figure 5: Simulation plot for INVx1 driving 4 INVx1

INVx1 driving 8 INVx1:

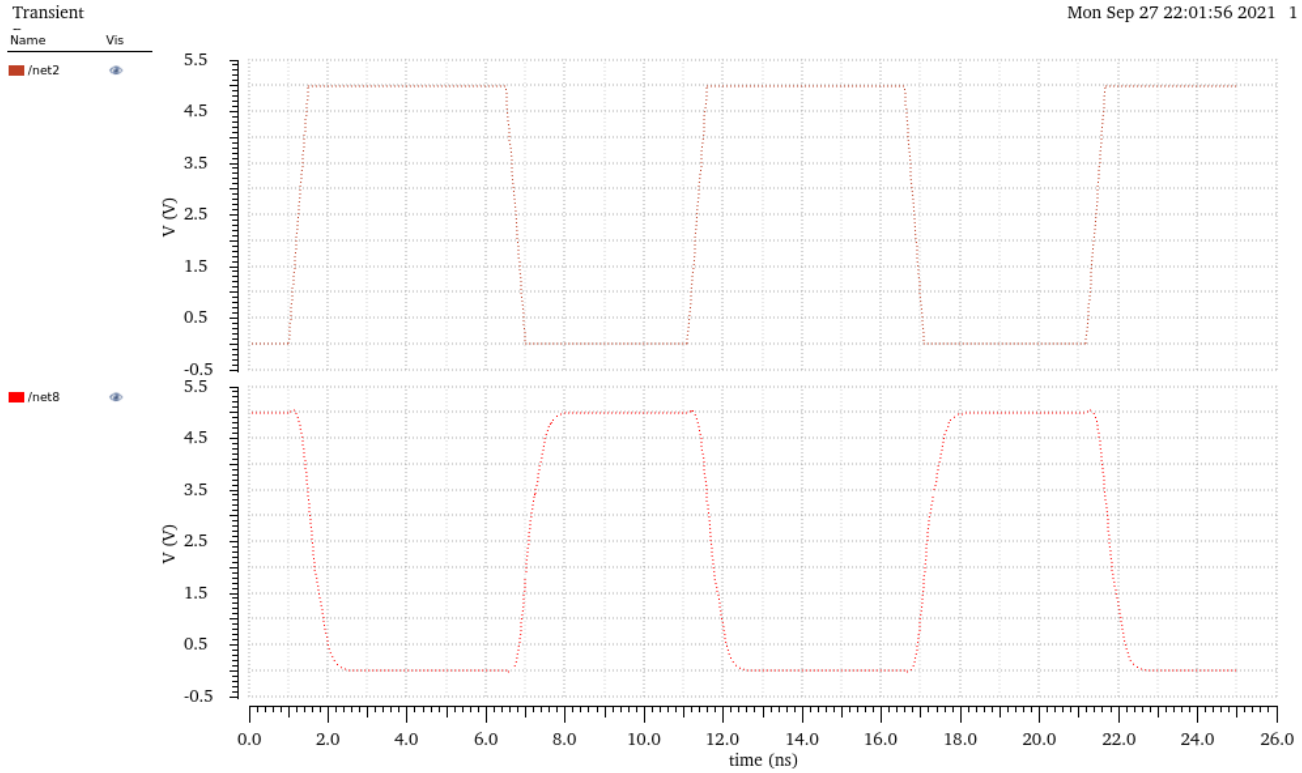

Figure 6: Simulation plot for INVx1 driving 8 INVx1

INVx1 driving 16 INVx1:

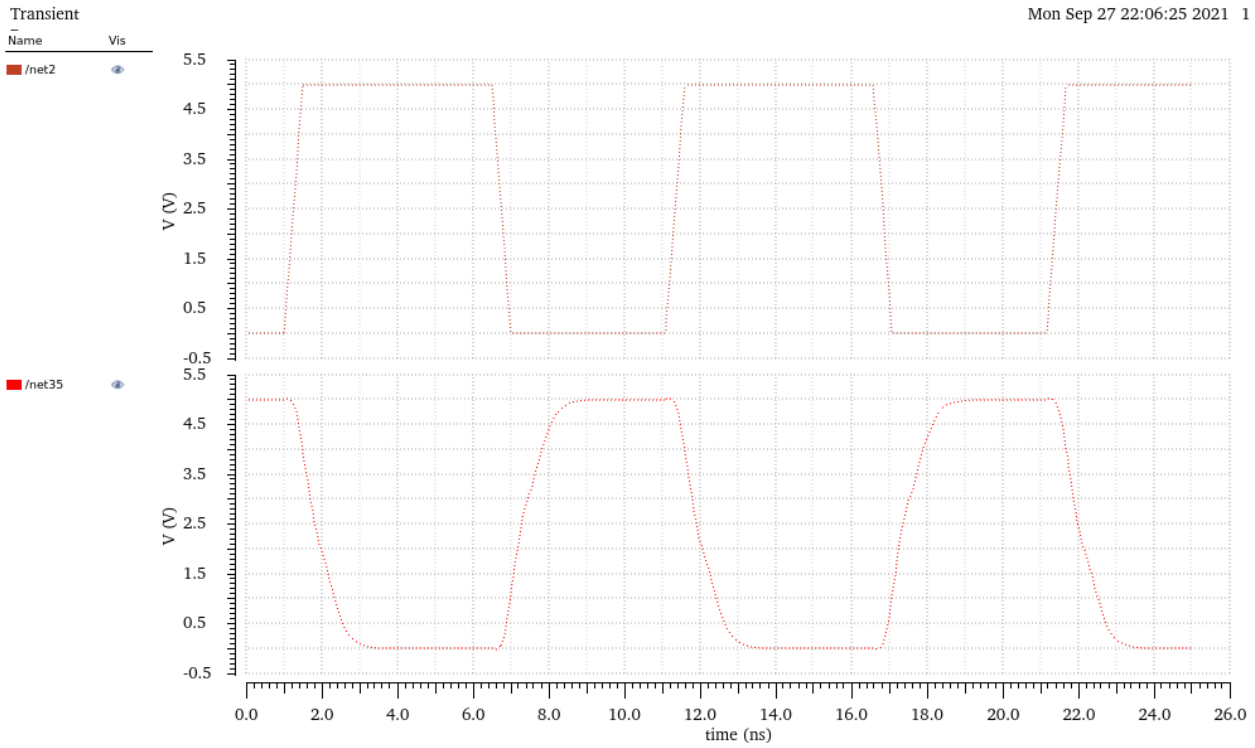

Figure 7: Simulation plot for INVx1 driving 16 INVx1

INVx2:

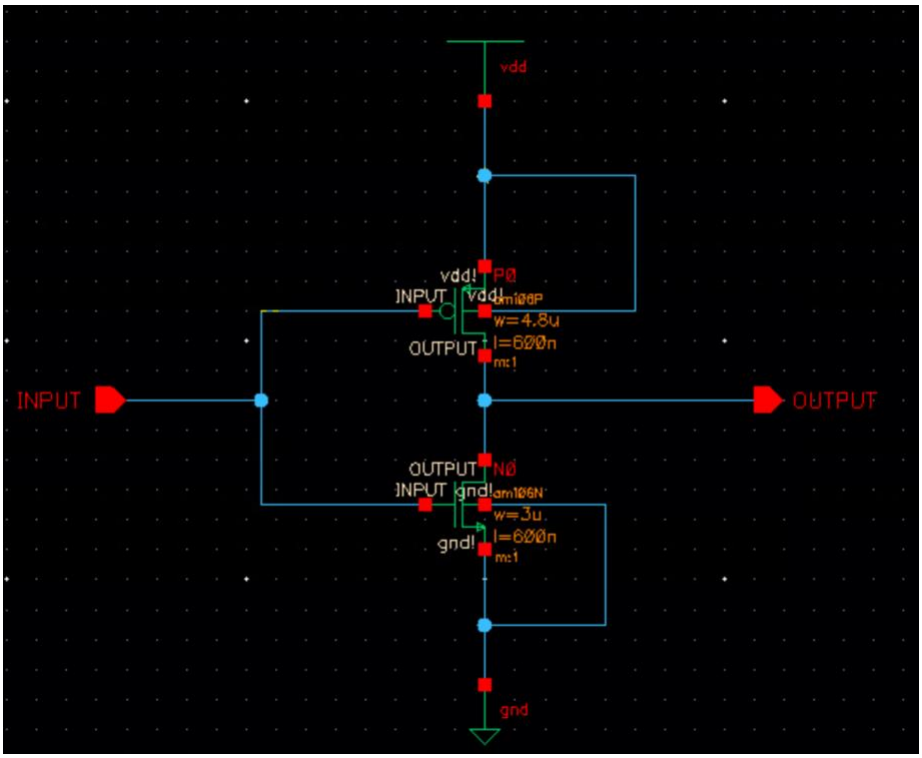

Figure 8: Schematic for INVx2

INVx2 driving 1 INVx1:

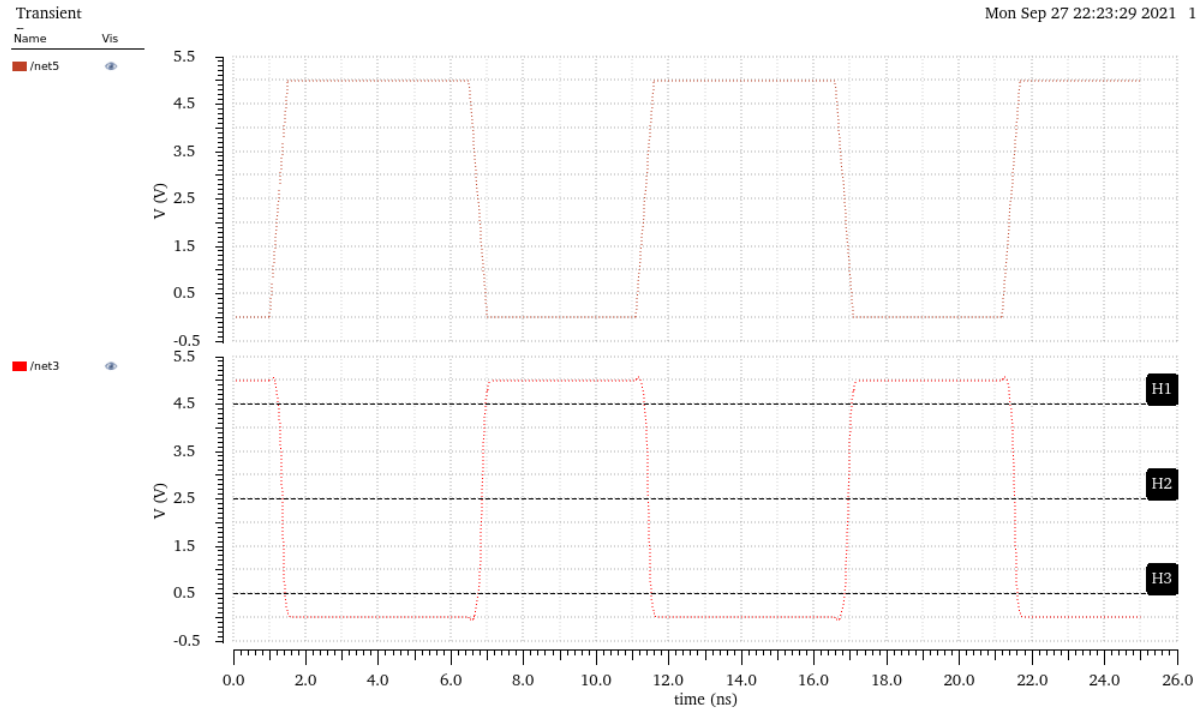

Figure 9: Simulation plot for INVx2 driving 1 INVx1

INVx2 driving 2 INVx1:

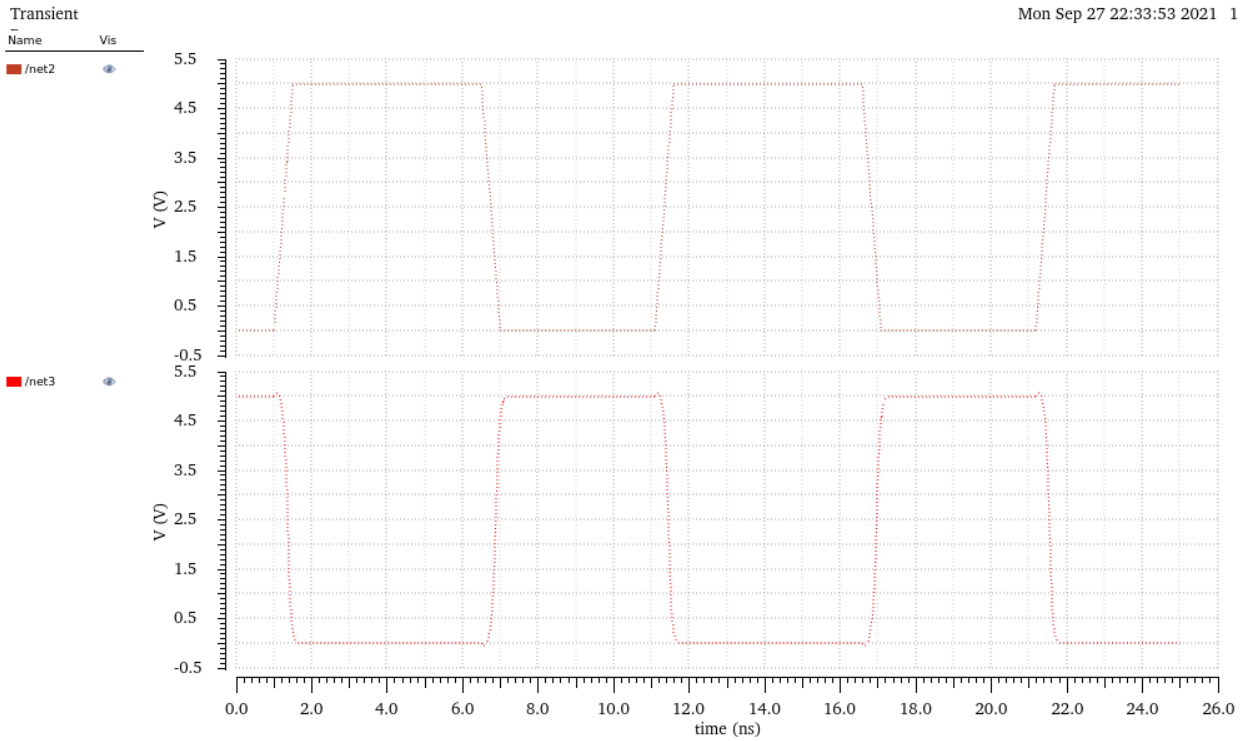

Figure 10: Simulation plot for INVx2 driving 2 INVx1

INVx2 driving 4 INVx1:

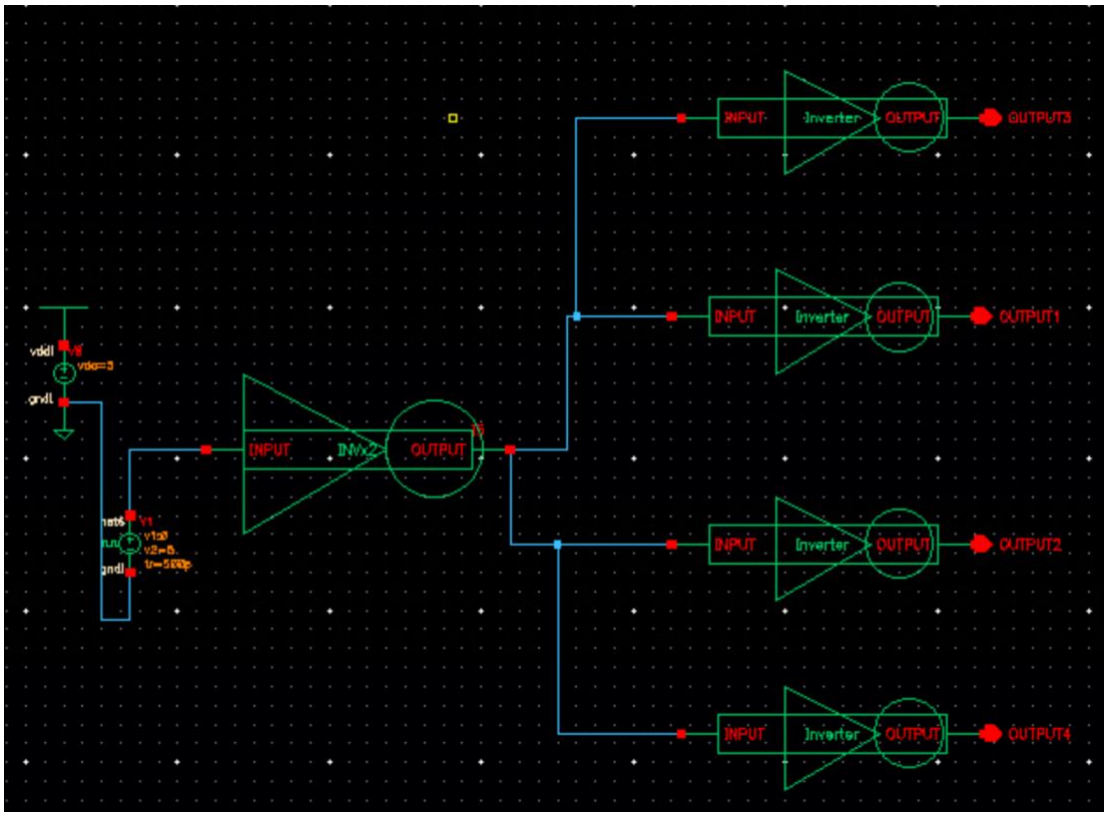

Figure 11: Schematic for INVx2 driving 4 INVx1

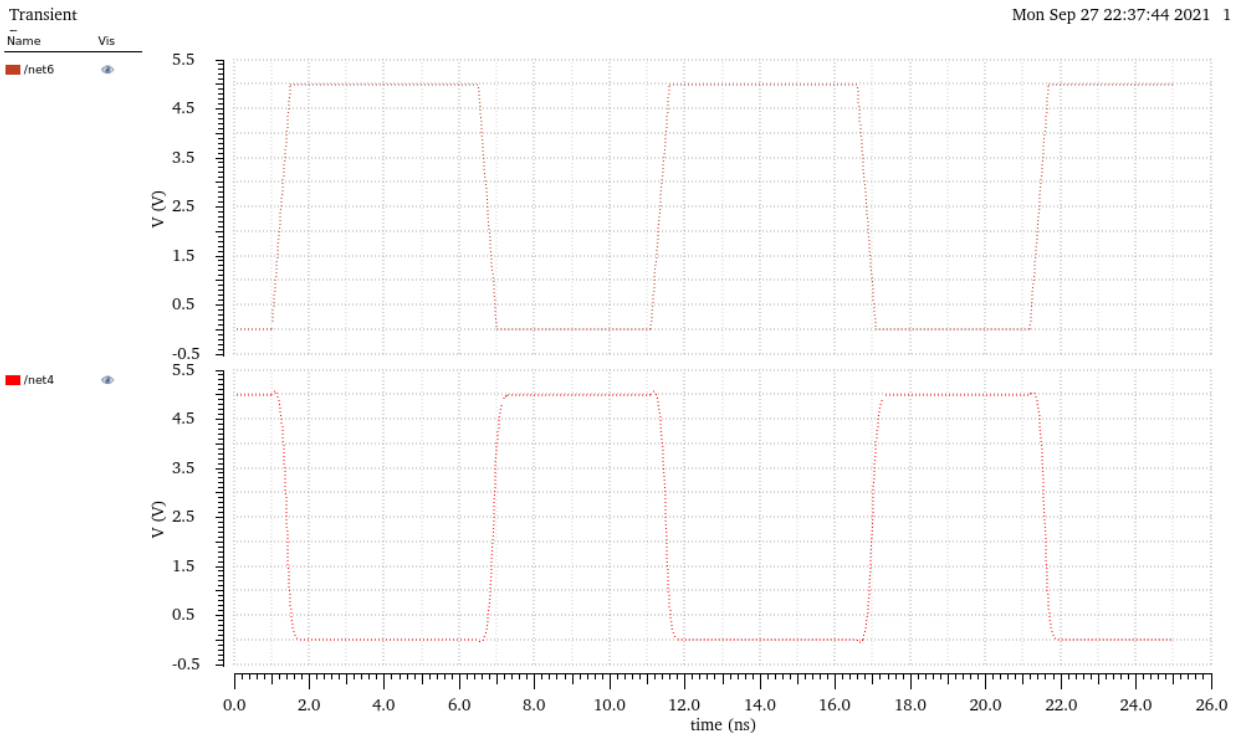

Figure 12: Simulation plot for INVx2 driving 4 INVx1

INVx2 driving 8 INVx1:

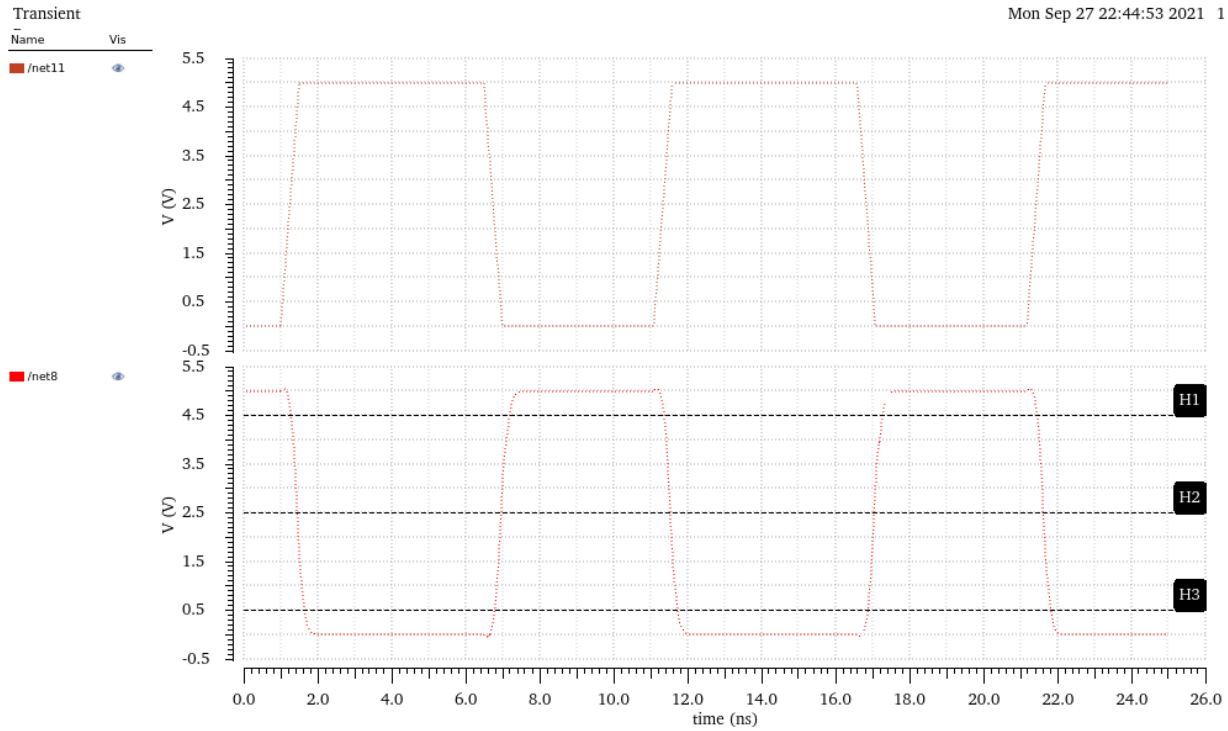

Figure 13: Simulation plot for INVx2 driving 8 INVx1

INVx2 driving 16 INVx1:

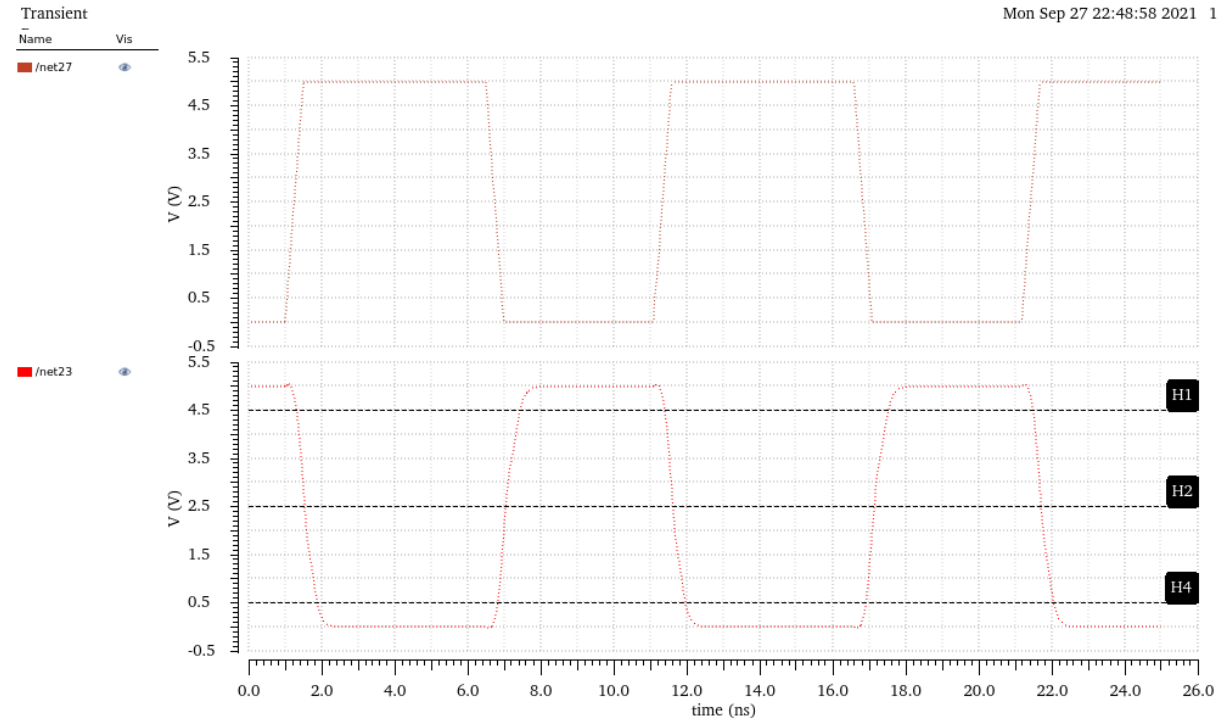

Figure 14: Simulation plot for INVx2 driving 16 INVx1

INVx4:

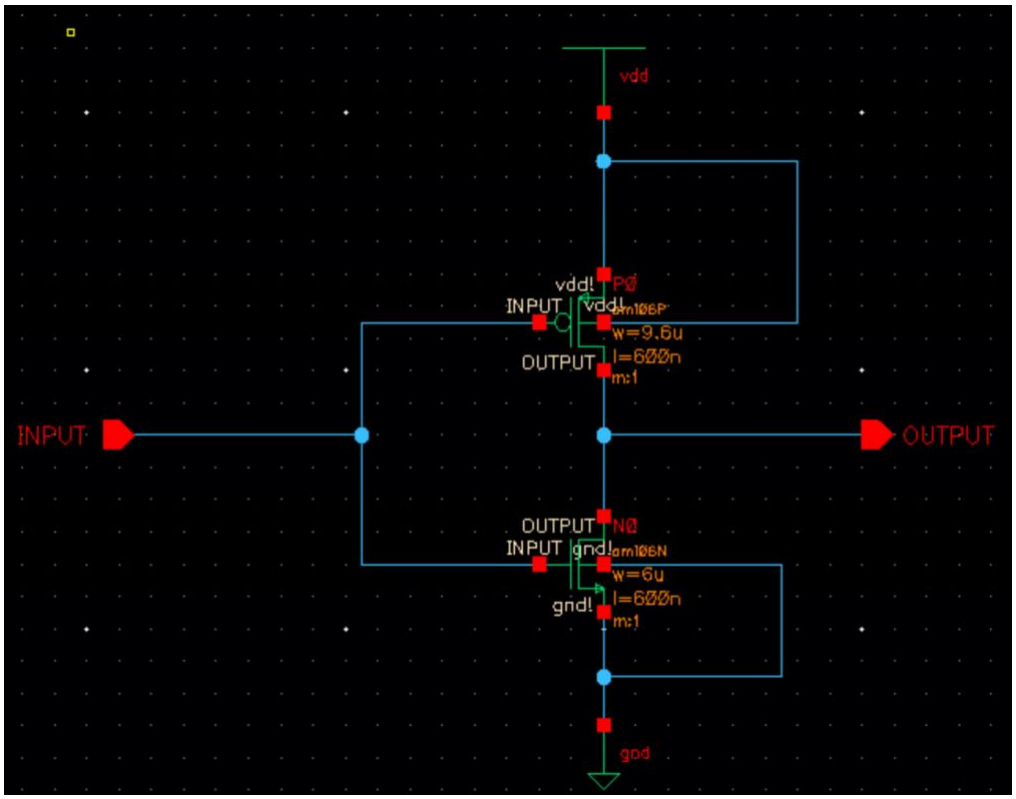

Figure 15: Schematic for INVx4

INVx4 driving 1 INVx1:

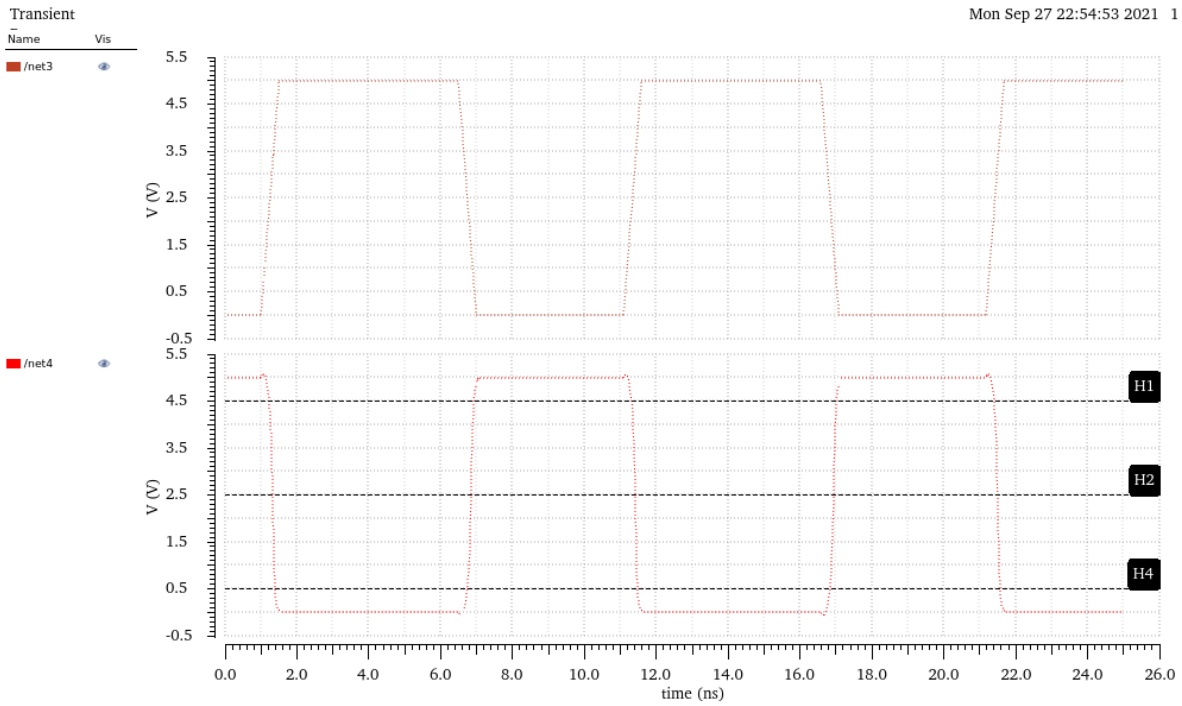

Figure 16: Simulation plot for INVx4 driving 1 INVx1

INVx4 driving 2 INVx1:

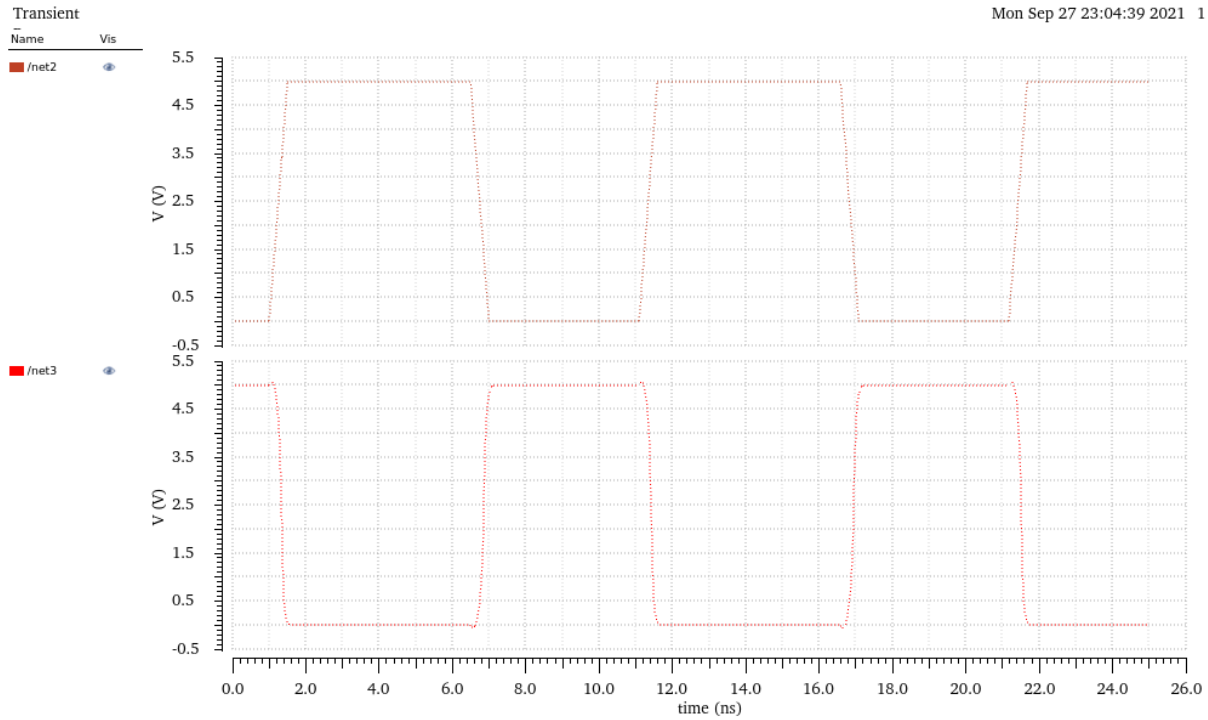

Figure 17: Simulation plot for INVx4 driving 2 INVx1

INVx4 driving 4 INVx1:

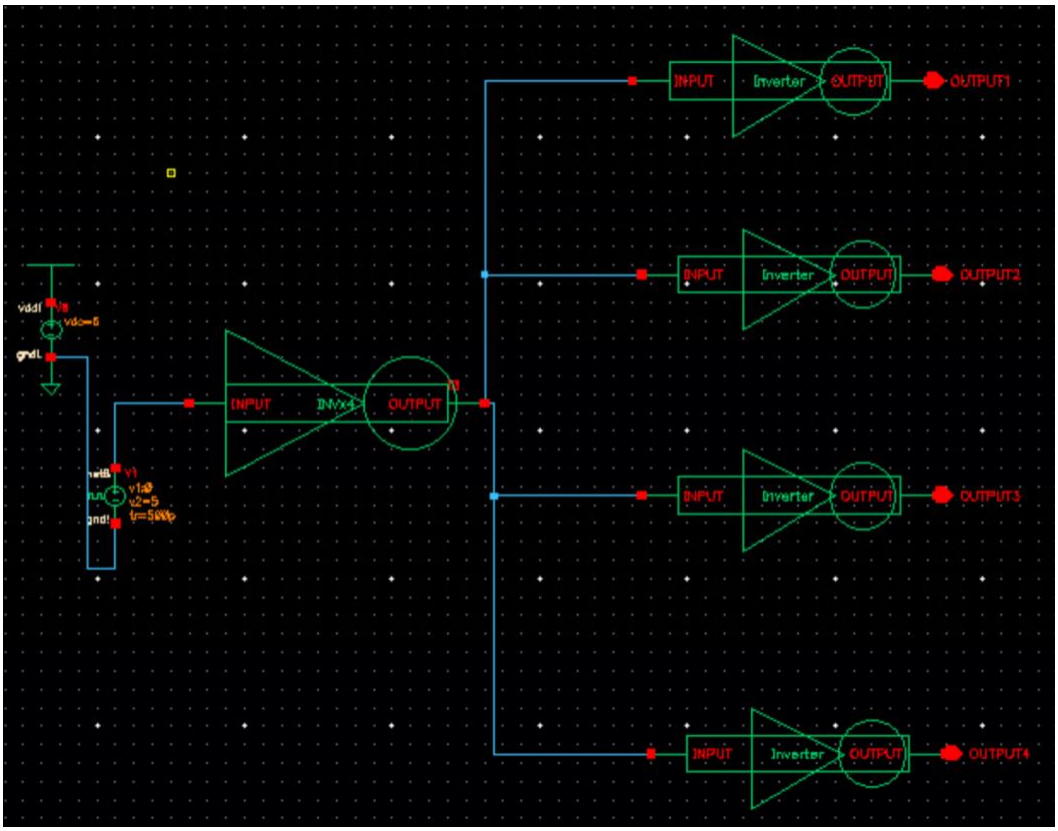

Figure 18: Schematic for INVx4 driving 4 INVx1

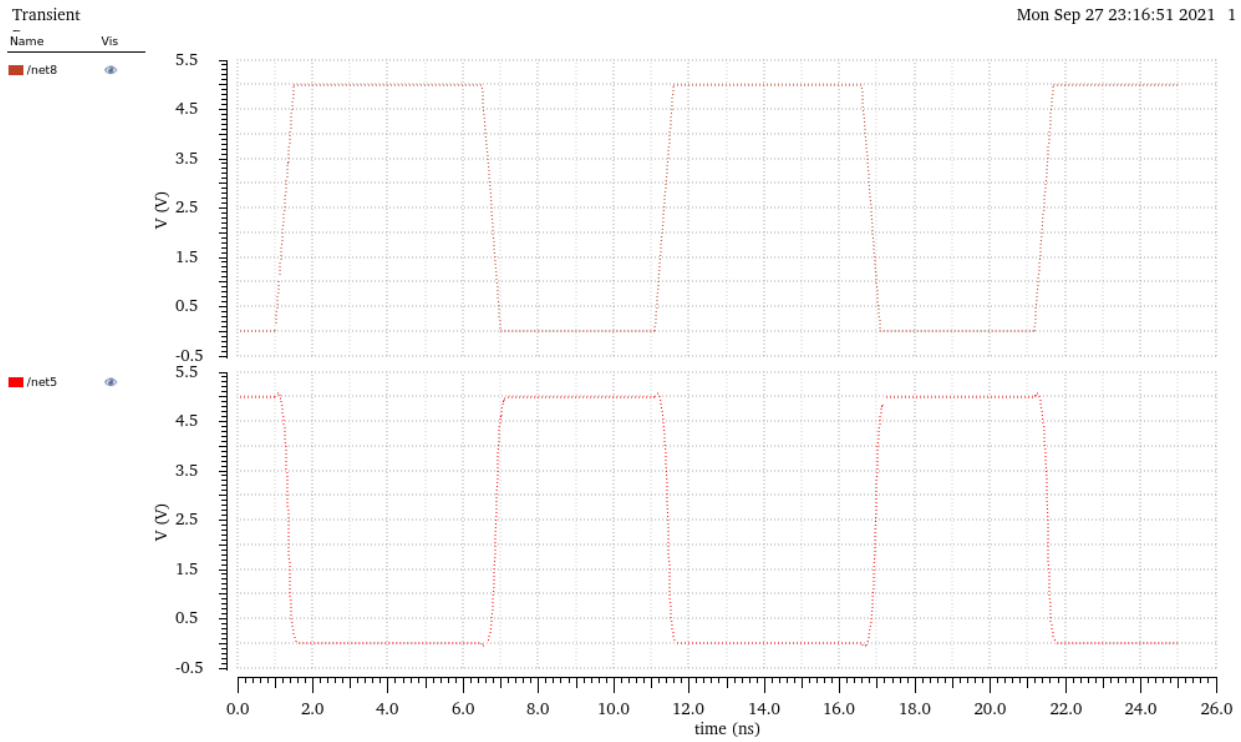

Figure 19: Simulation plot for INVx4 driving 4 INVx1

INVx4 driving 8 INVx1:

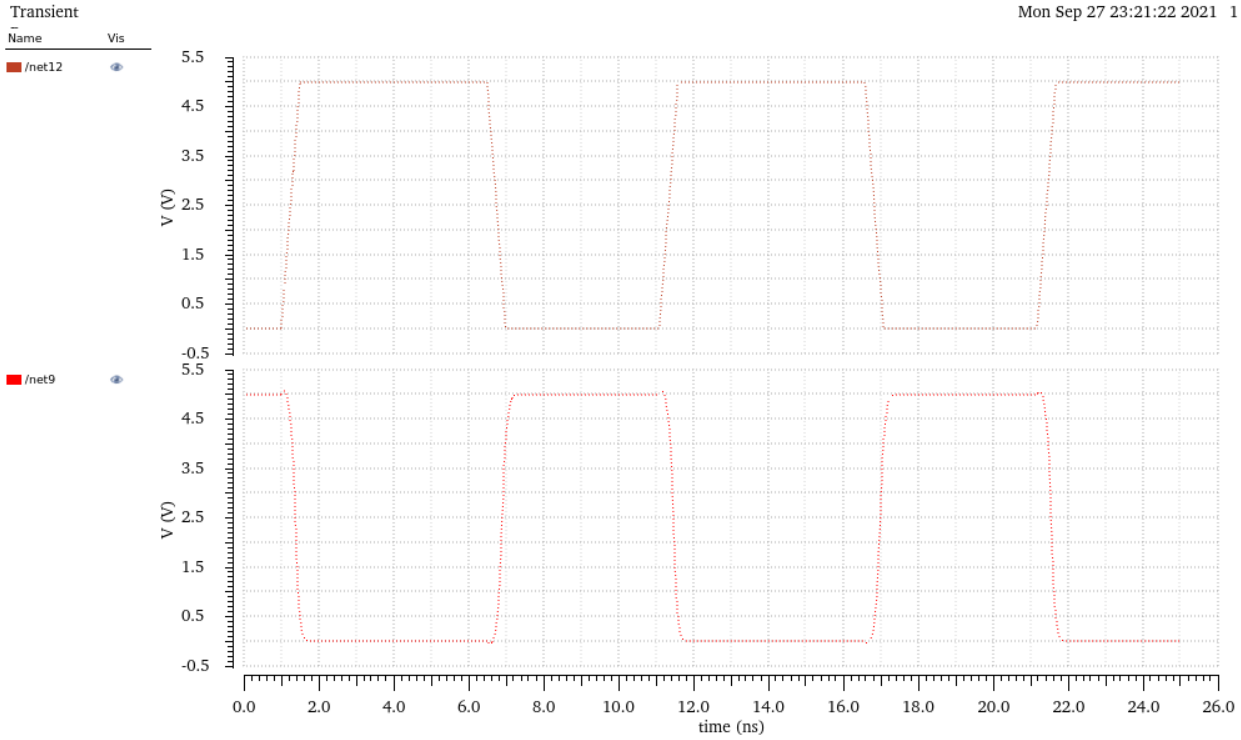

Figure 20: Simulation plot for INVx4 driving 8 INVx1

INVx4 driving 16 INVx1:

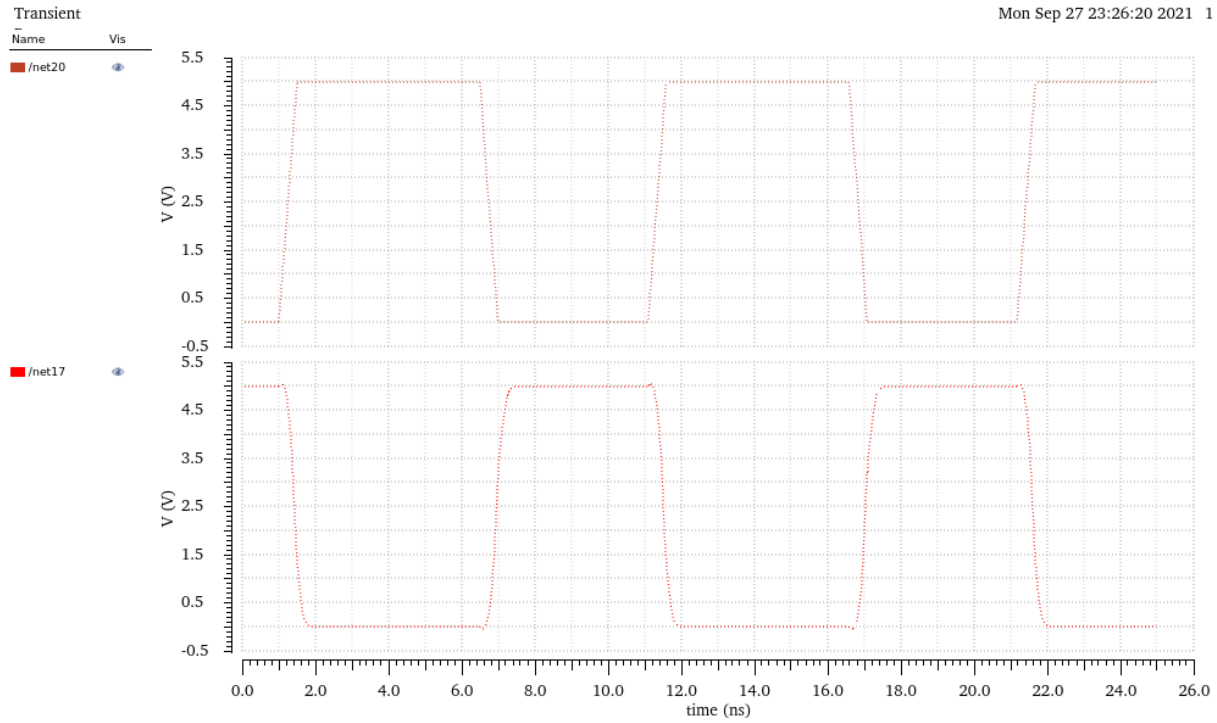

Figure 21: Simulation plot for INVx4 driving 16 INVx1

NOR2x1:

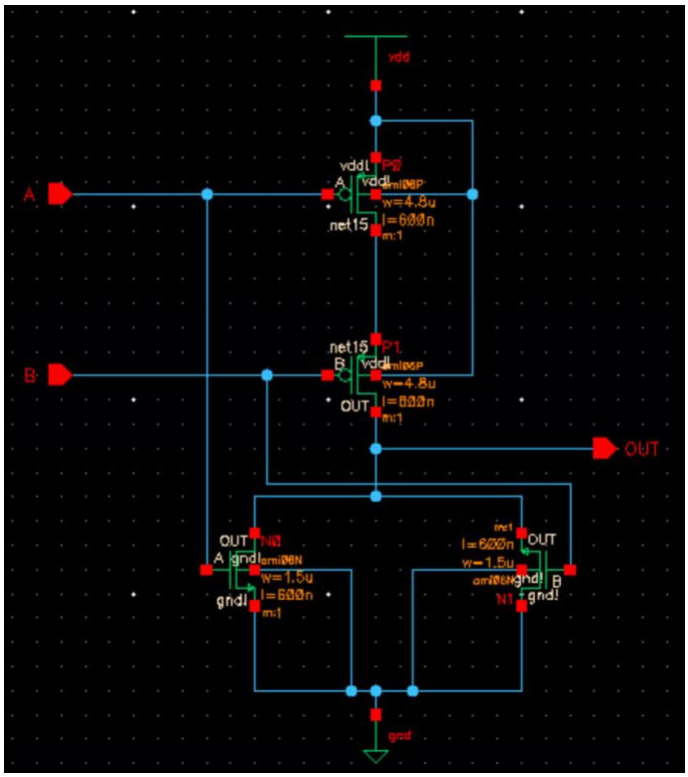

Figure 22: Schematic for NOR2x1

NOR2x1 driving 1 INVx1:

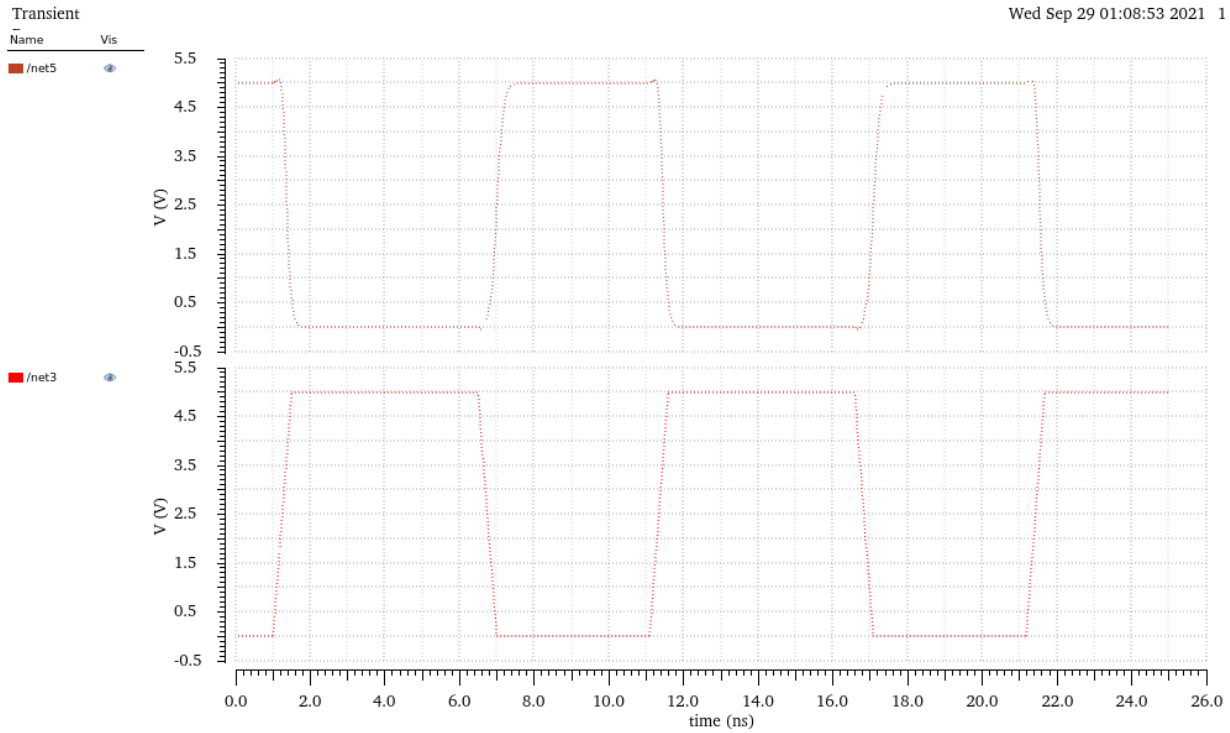

Figure 23: Simulation plot for NOR2x1 driving 1 INVx1

NOR2x1 driving 1 INVx1 flipped:

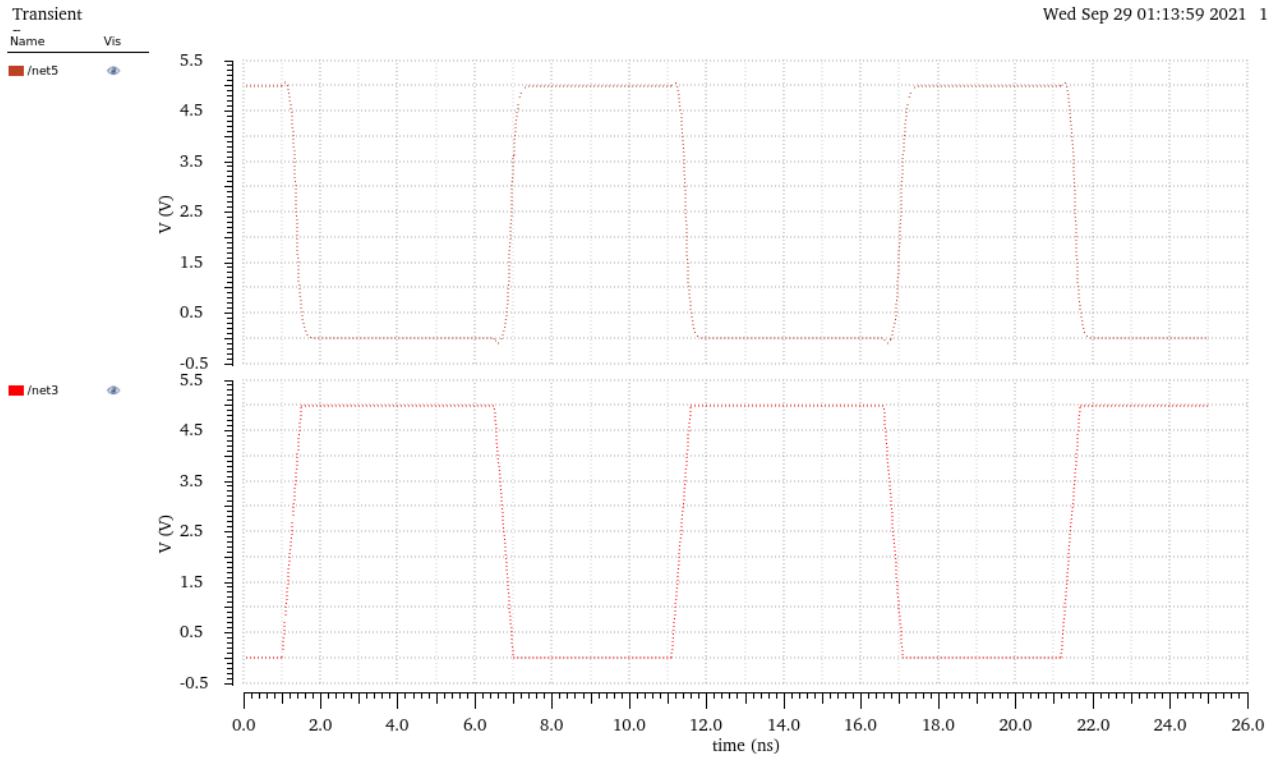

Figure 24: Simulation plot for NOR2x1 driving 1 INVx1 with flipped inputs

NOR2x1 driving 2 INVx1:

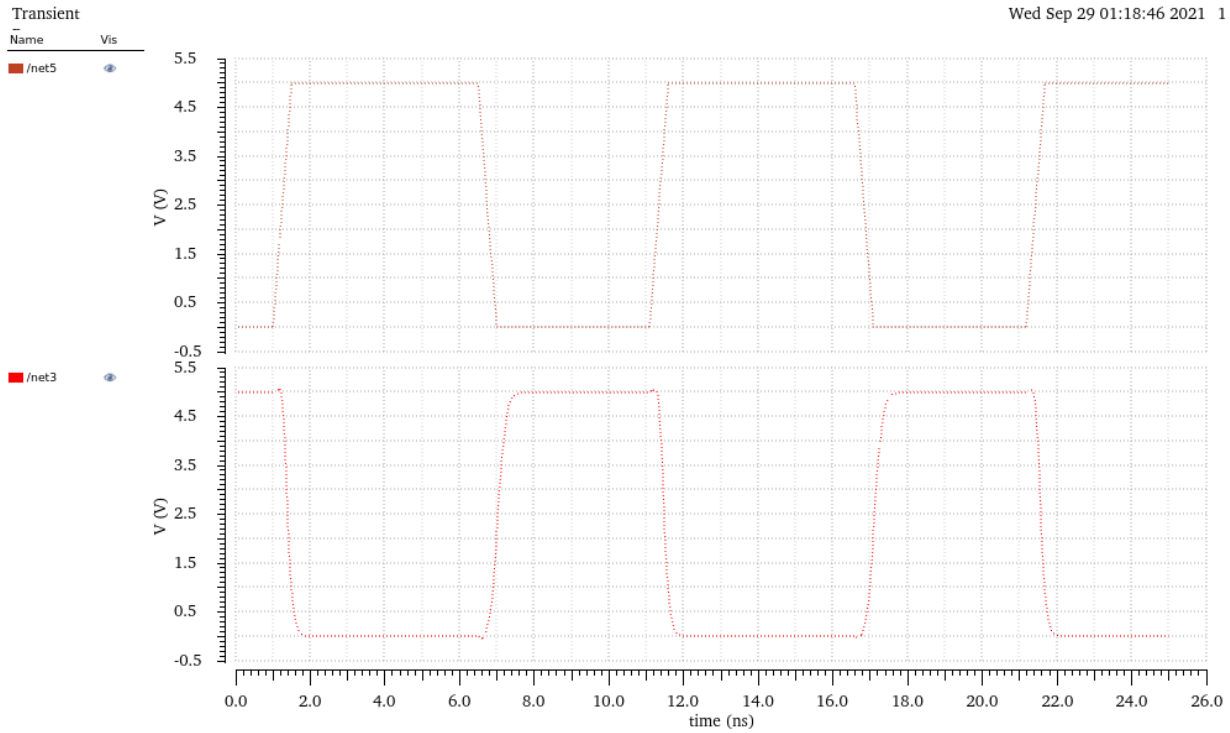

Figure 25: Simulation plot for NOR2x1 driving 2 INVx1

NOR2x1 driving 2 INVx1 flipped:

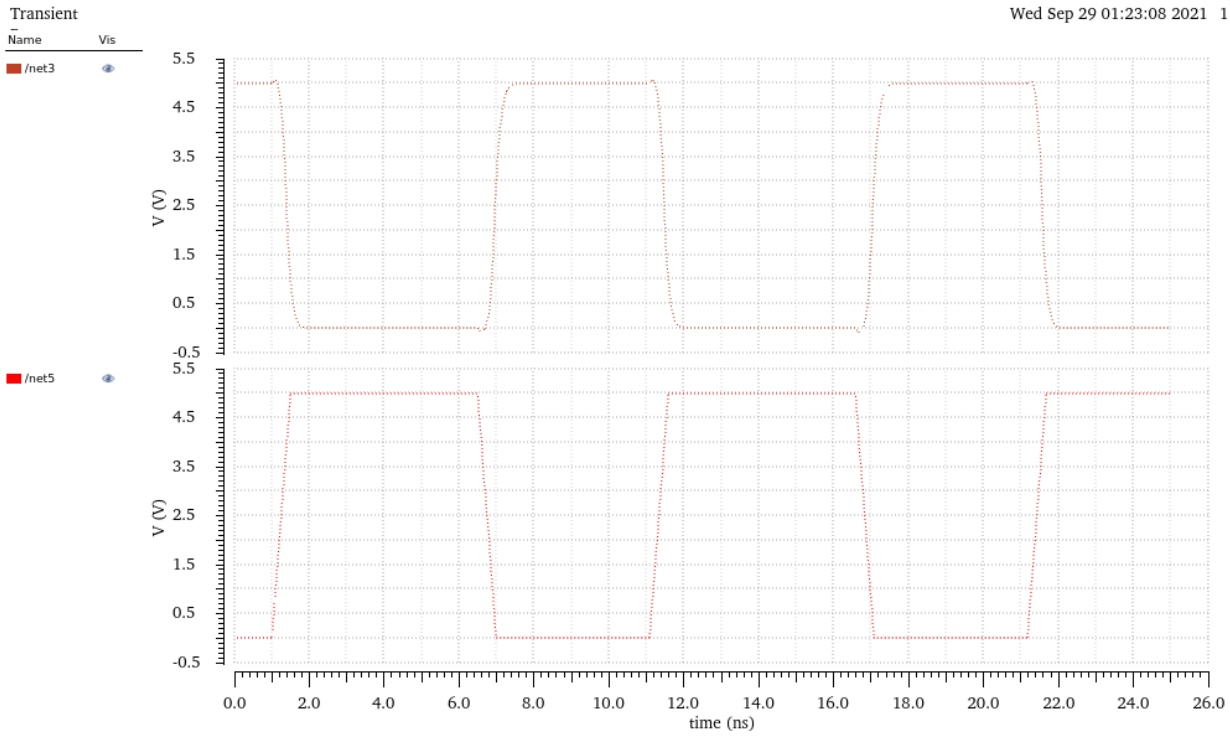

Figure 26: Simulation plot for NOR2x1 driving 2 INVx1 with flipped inputs

NOR2x1 driving 4 INVx1:

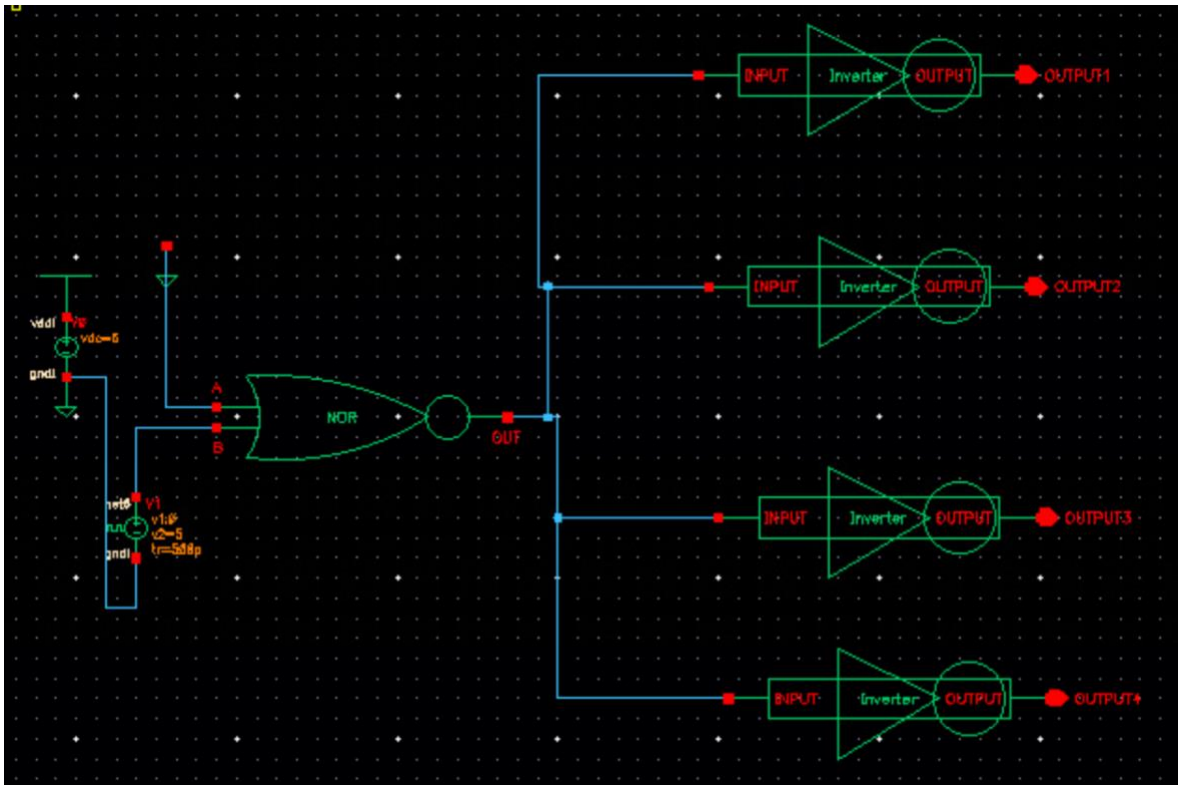

Figure 27: NOR2x1 driving 4 INVx1

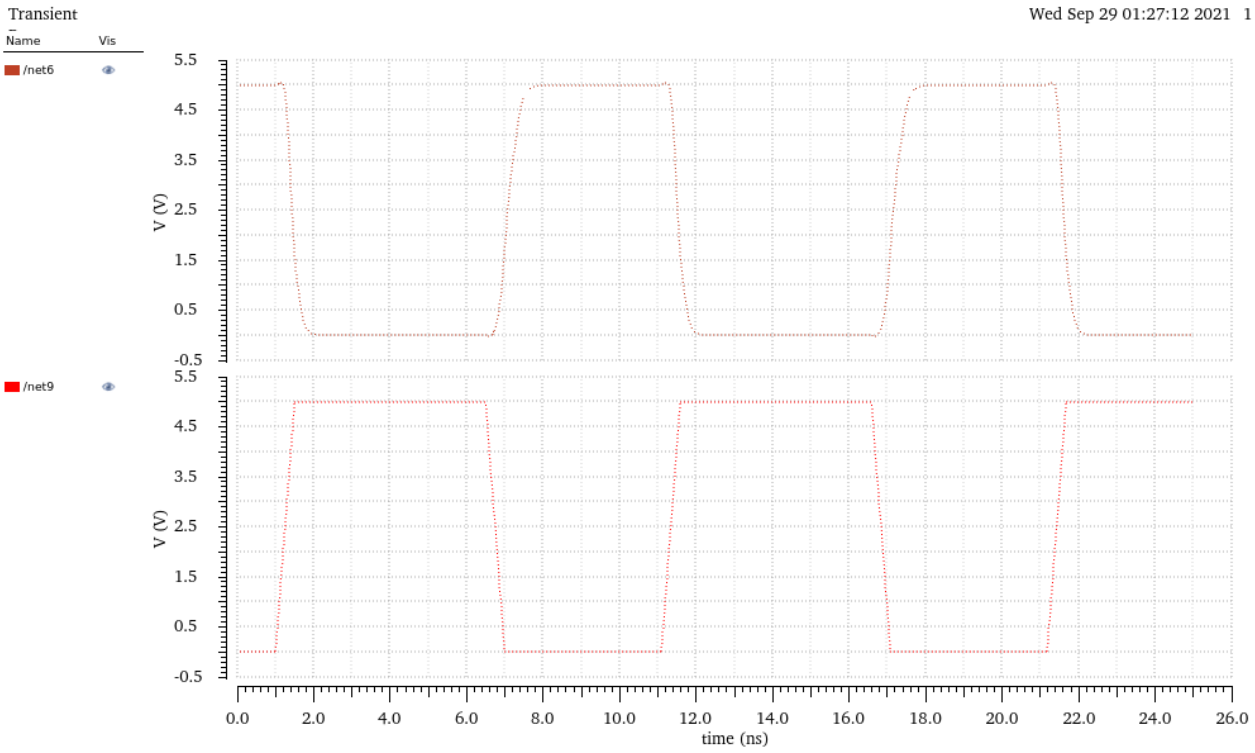

Figure 28: Simulation plot for NOR2x1 driving 4 INVx1

NOR2x1 driving 4 INVx1 flipped:

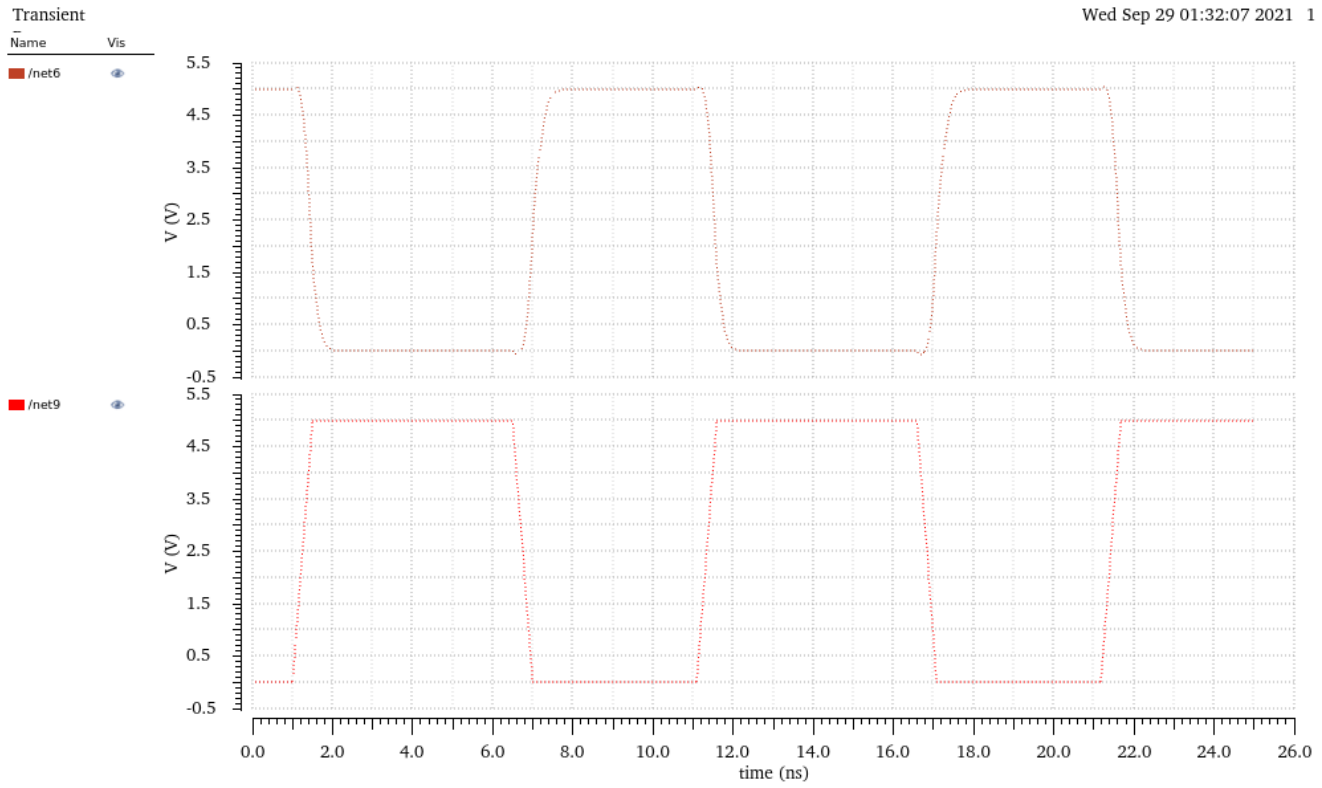

Figure 29: Simulation plot for NOR2x1 driving 4 INVx1 with flipped inputs

NAND2x1:

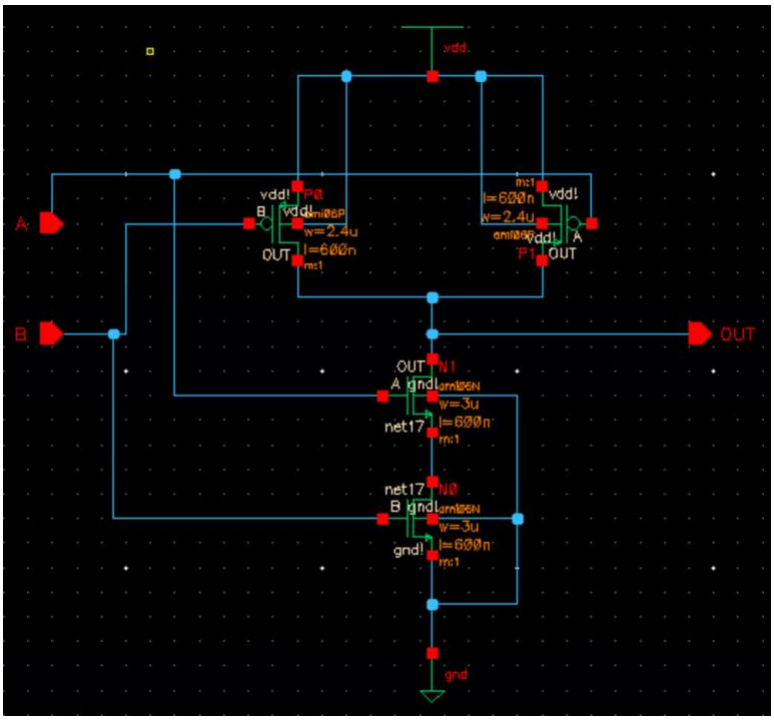

Figure 30: Schematic for NAND2x1

NAND2x1 driving 1 INVx1:

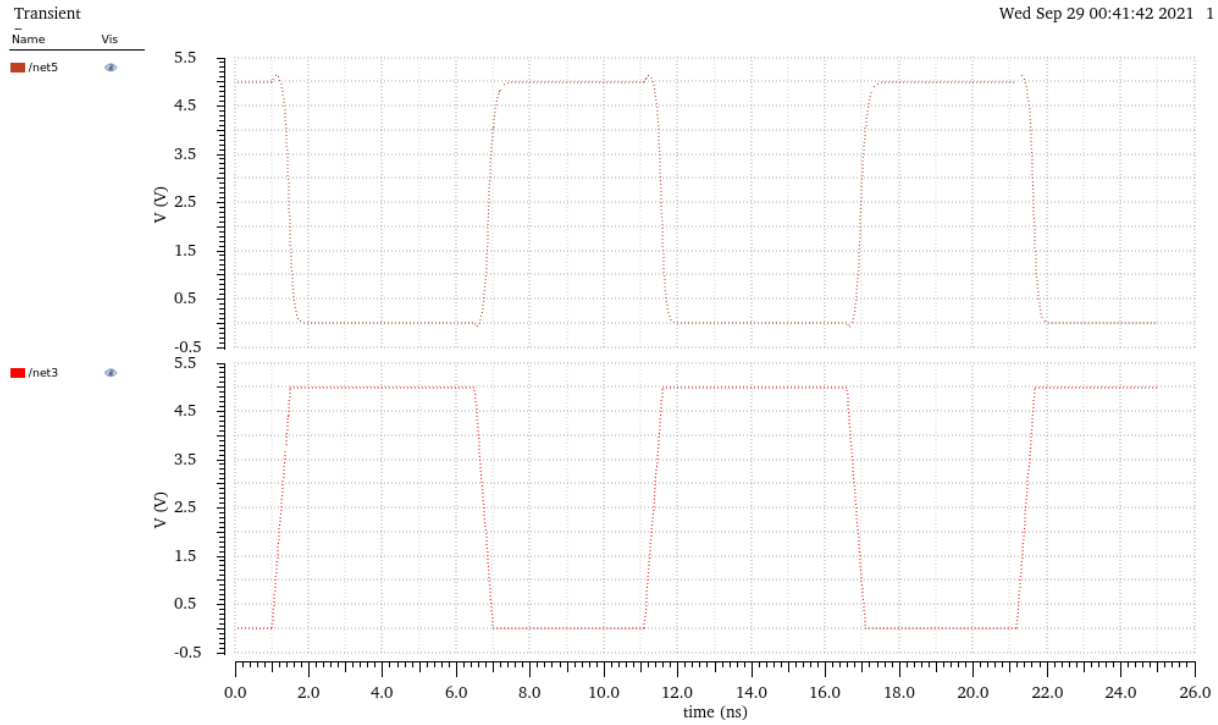

Figure 31: Simulation plot for NAND2x1 driving 1 INVx1

NAND2x1 driving 1 INVx1 flipped:

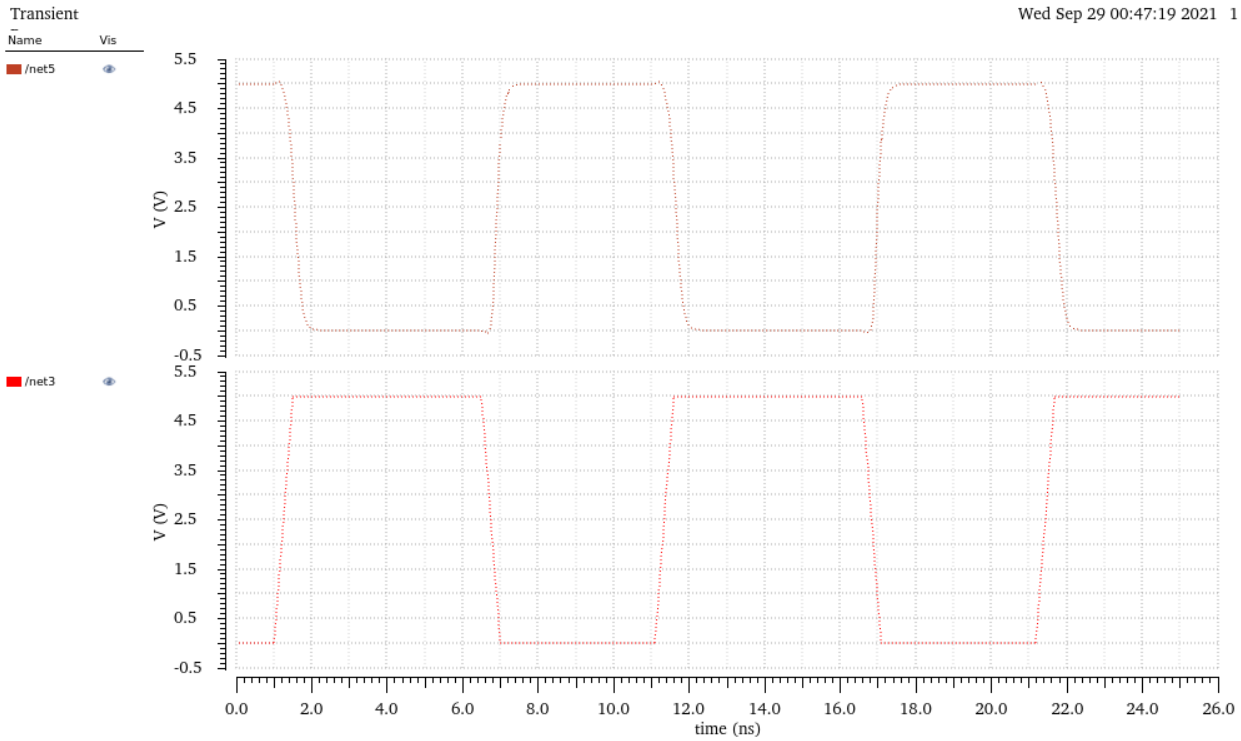

Figure 32: Simulation plot for NAND2x1 driving 1 INVx1 with flipped inputs

NAND2x1 driving 2 INVx1:

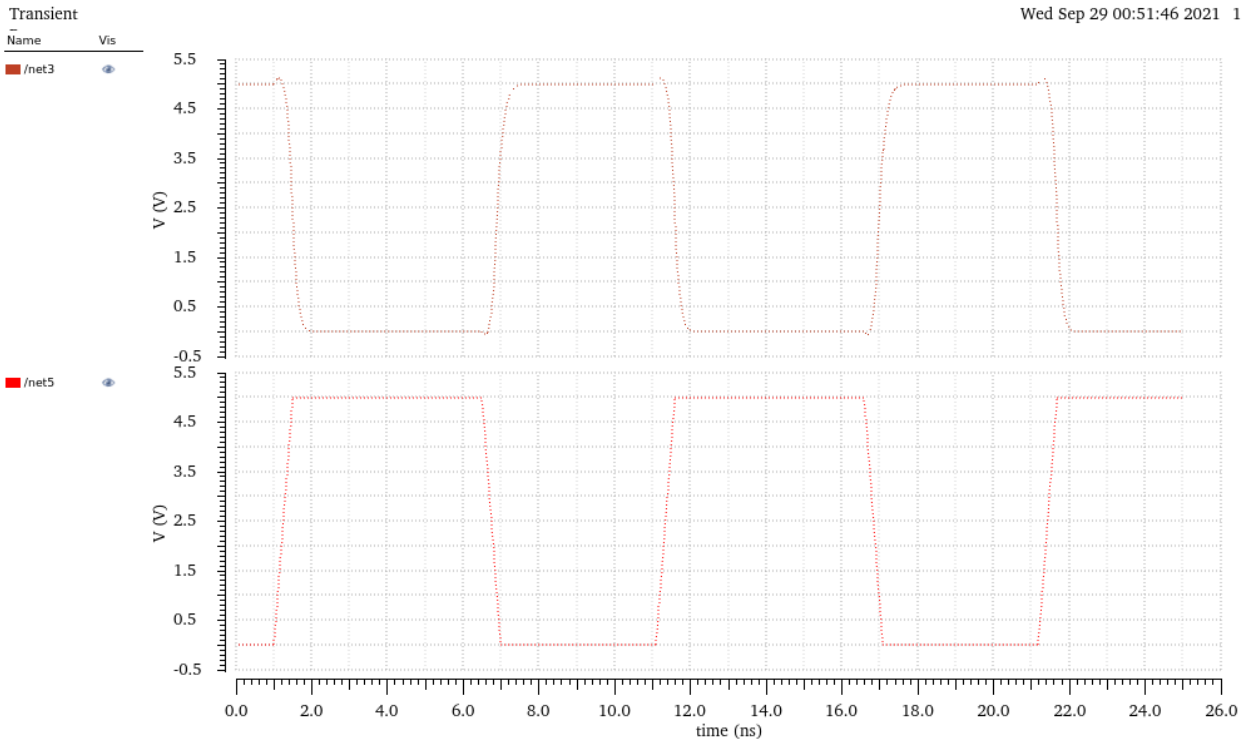

Figure 33: Simulation plot for NAND2x1 driving 2 INVx1

NAND2x1 driving 2 INVx1 flipped:

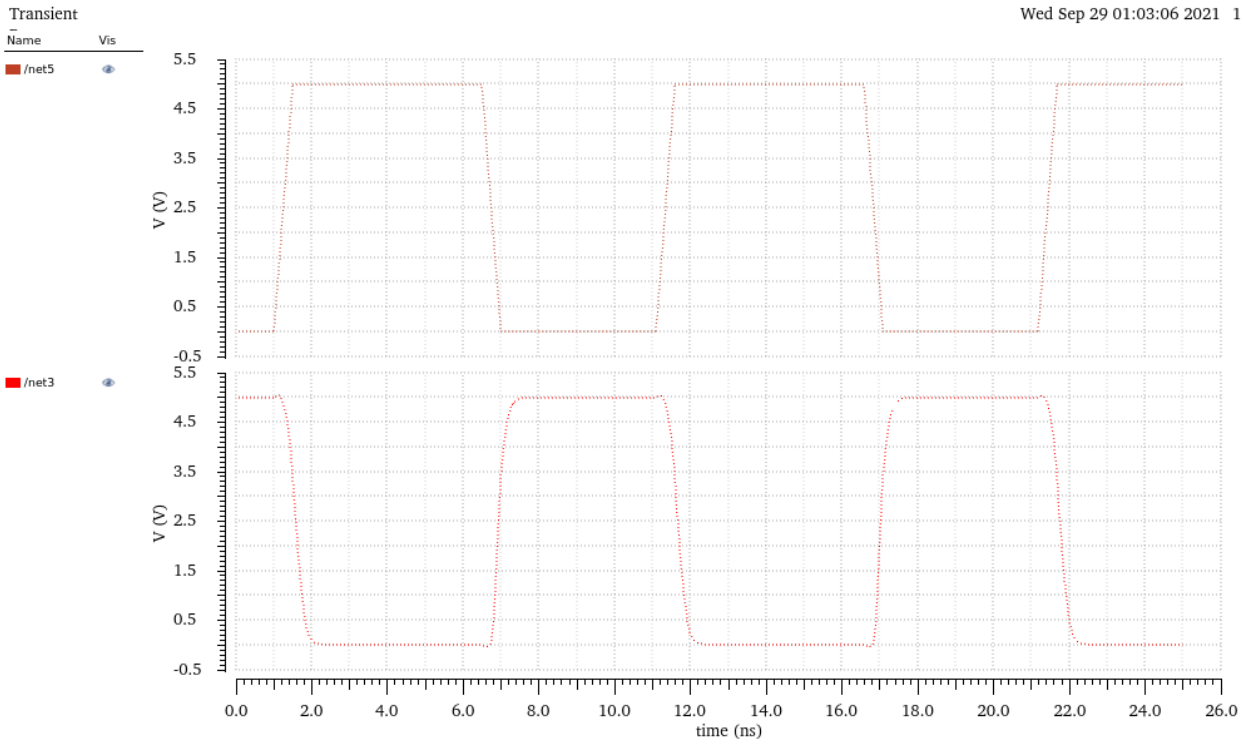

Figure 34: Simulation plot for NAND2x1 driving 2 INVx1 with flipped inputs

NAND2x1 driving 4 INVx1:

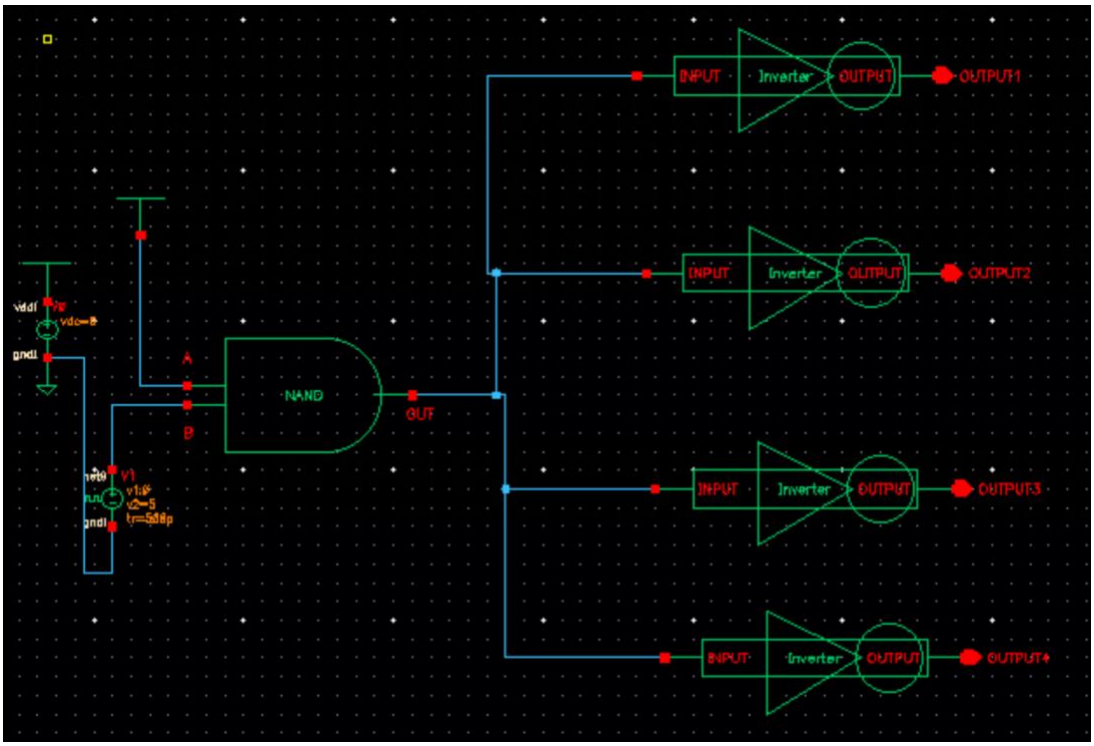

Figure 35: Schematic for NAND2x1 driving 4 INVx1

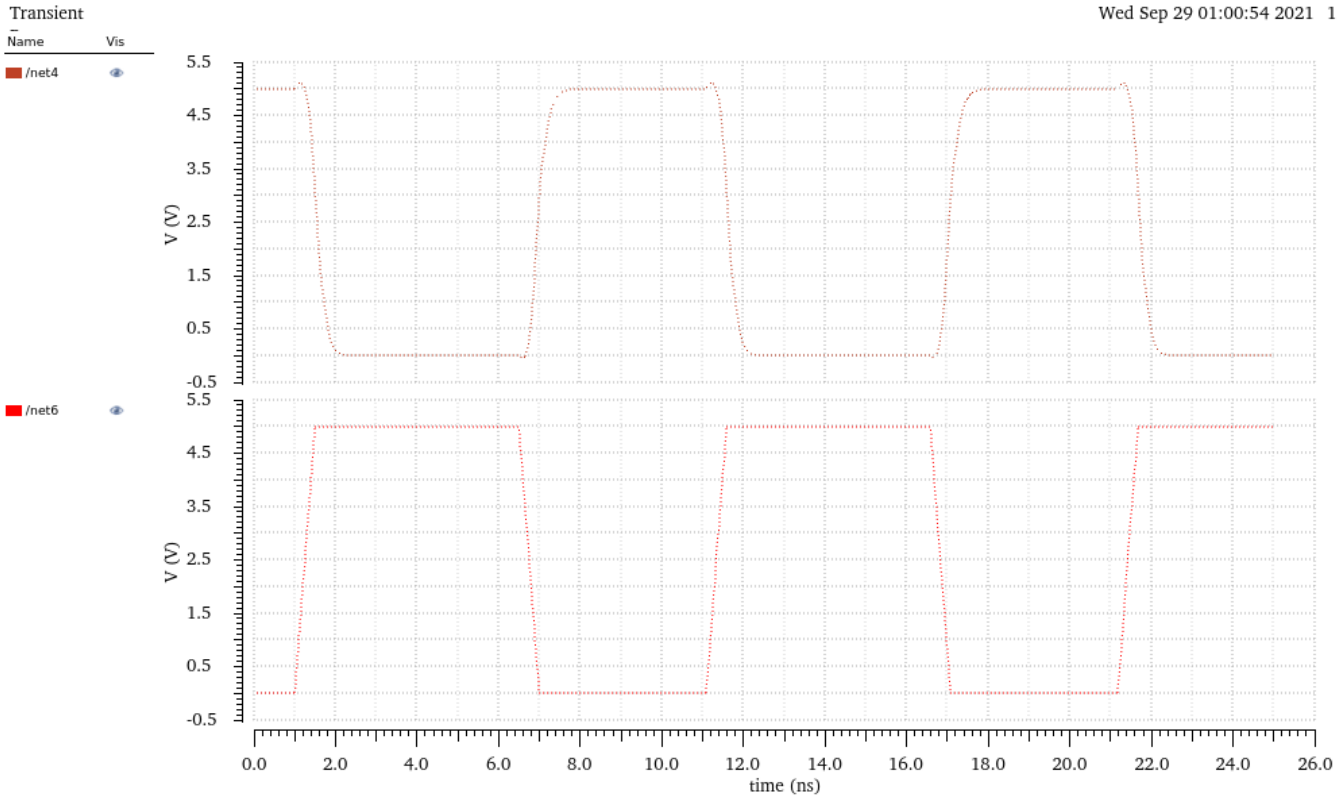

Figure 36: Simulation plot for NAND2x1 driving 4 INVx1

NAND2x1 driving 4 INVx1 flipped:

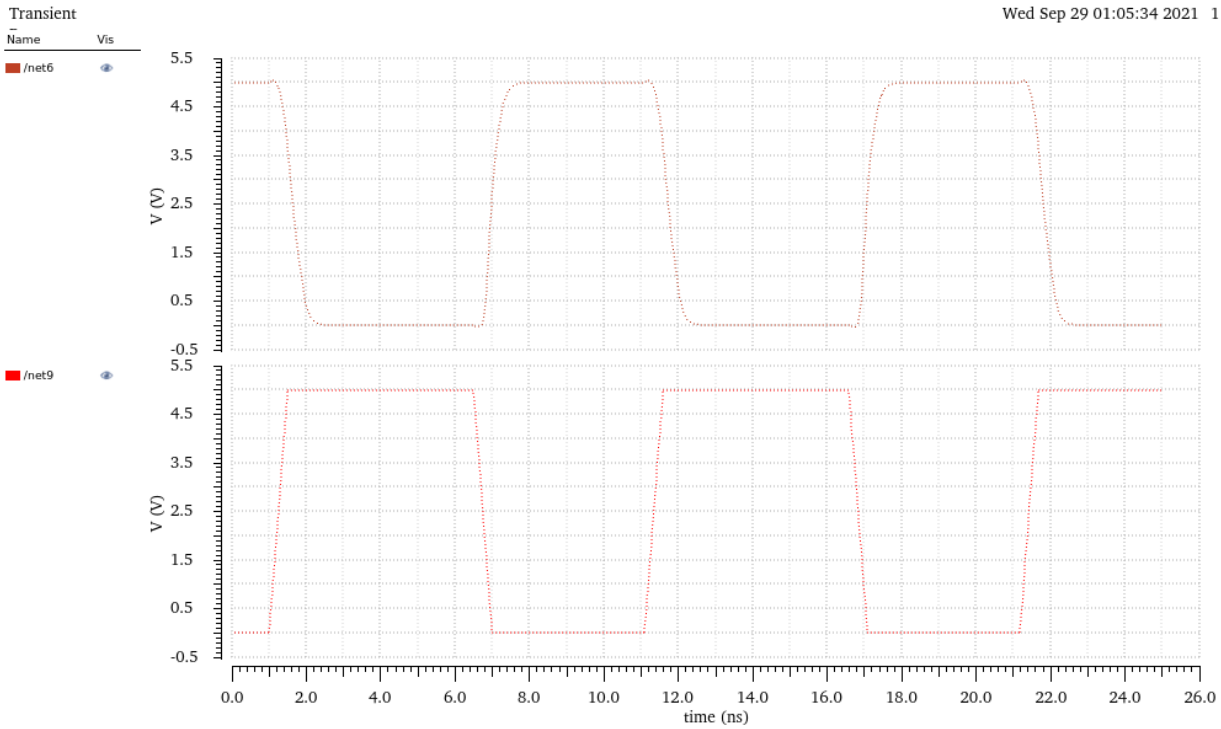

Figure 37: Simulation plot for NAND2x1 driving 4 INVx1 with flipped inputs

Computations:

Fall Time for Inverters:

*****ALL TIME VALUES ARE IN NANOSECONDS (ns) BELOW*****

Table 2: Fall times for each inverter gate with different number of load inverters

Gate	rise 4.5	rise .5	**rise**
INVx1 1	7.01124	6.76348	**0.24776**
INVx1 2	7.08828	6.77789	**0.31039**
INVx1 4	7.23014	6.80113	**0.42901**
INVx1 8	7.50434	6.83804	**0.6663**
INVx1 16	8.05798	6.88727	**1.17071**
INVx2 1	6.95456	6.75383	**0.20073**
INVx2 2	6.99572	6.76074	**0.23498**
INVx2 4	7.06569	6.77315	**0.29254**
INVx2 8	7.1962	6.79556	**0.40064**
INVx2 16	7.44561	6.83056	**0.61505**
INVx4 1	6.93246	6.74836	**0.1841**
INVx4 2	6.94955	6.75138	**0.19817**
INVx4 4	6.98762	6.77835	**0.20927**
INVx4 8	7.05537	6.77065	**0.28472**
INVx4 16	7.18021	6.79188	**0.38833**

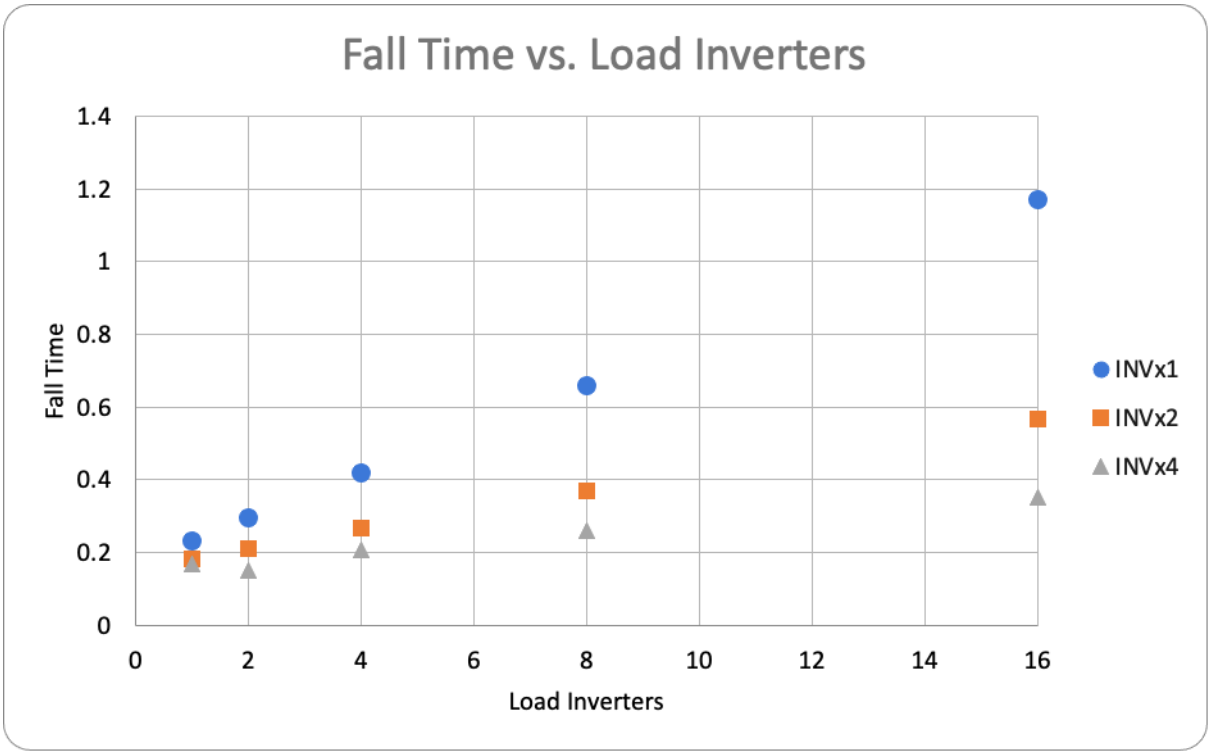

Figure 38: Plot for fall times for each inverter with different number of load inverters

The table and figure above show the fall times for each inverter with different number of load inverters. They clearly show that the width of the pMOS in the inverter heavily influences the fall time of the gate, where the higher the width the lower the fall time. The number of load inverters also has a large effect on the fall time, since when the number of load inverters increase the fall time also increases.

Fall Time Delay for Inverters:

Table 3: Fall time delays for each inverter gate with different number of load inverters

Gate	rise- out	fall- in	**delay fall**
INVx1 1	6.88549	6.75	**0.13549**
INVx1 2	6.91925	6.75	**0.16925**
INVx1 4	6.97745	6.75	**0.22745**
INVx1 8	7.08005	6.75	**0.33005**
INVx1 16	7.29342	6.75	**0.54342**
INVx2 1	6.86229	6.75	**0.11229**
INVx2 2	6.87978	6.75	**0.12978**
INVx2 4	6.91034	6.75	**0.16034**
INVx2 8	6.96353	6.75	**0.21353**
INVx2 16	7.05677	6.75	**0.30677**

INVx4 1	6.85165	6.75	**0.10165**
INVx4 2	6.86065	6.75	**0.11065**
INVx4 4	6.87711	6.75	**0.12711**
INVx4 8	6.90652	6.75	**0.15652**
INVx4 16	6.95696	6.75	**0.20696**

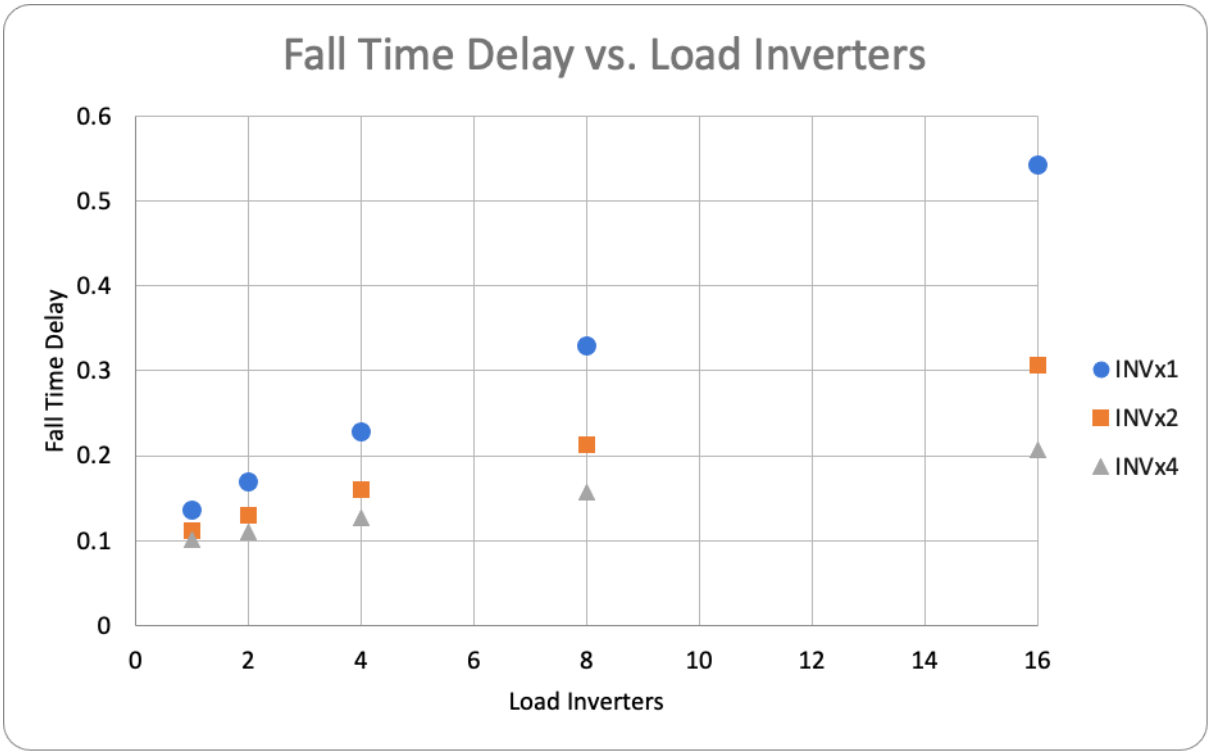

Figure 39: Plot for fall time delays for each inverter with different number of load inverters

The table and figure above show the fall time delays for each inverter with different number of load inverters. They clearly show that the width of the pMOS in the inverter heavily influences the fall time delay of the gate, where the higher the width the lower the fall time delay. The number of load inverters also has a large effect on the fall time delay, since when the number of load inverters increase the fall time delay also increases.

Rise Time for Inverters:

Table 4: Rise times for each inverter gate with different number of load inverters

Gate	fall 4.5	fall .5	**fall**
INVx1 1	1.27454	1.50581	**0.23127**
INVx1 2	1.28747	1.58341	**0.29594**
INVx1 4	1.30956	1.72831	**0.41875**
INVx1 8	1.34477	2.00551	**0.66074**

INVx1 16	1.39312	2.56306	**1.16994**
INVx2 1	1.23987	1.42348	**0.18361**
INVx2 2	1.24639	1.4588	**0.21241**
INVx2 4	1.25844	1.52737	**0.26893**
INVx2 8	1.27911	1.65059	**0.37148**
INVx2 16	1.31206	1.87864	**0.56658**
INVx4 1	1.2219	1.38979	**0.16789**
INVx4 2	1.25519	1.40576	**0.15057**
INVx4 4	1.23153	1.43791	**0.20638**
INVx4 8	1.24307	1.5039	**0.26083**
INVx4 16	1.26307	1.61654	**0.35347**

Figure 40: Plot for rise times for each inverter with different number of load inverters

The table and figure above show the rise times for each inverter with different number of load inverters. They clearly show that the width of the pMOS in the inverter heavily influences the rise time of the gate, where the higher the width the lower the rise time. The number of load inverters also has a large effect on the rise time, since when the number of load inverters increase the rise time also increases.

Rise Time Delay for Inverters:

Table 5: Rise times delays for each inverter gate with different number of load inverters

Gate	fall- out	rise- in	**delay rise**
INVx1 1	1.39771	1.25	**0.14771**
INVx1 2	1.4319	1.25	**0.1819**
INVx1 4	1.49128	1.25	**0.24128**
INVx1 8	1.59865	1.25	**0.34865**
INVx1 16	1.81971	1.25	**0.56971**
INVx2 1	1.34783	1.25	**0.09783**
INVx2 2	1.36516	1.25	**0.11516**
INVx2 4	1.39577	1.25	**0.14577**
INVx2 8	1.44822	1.25	**0.19822**
INVx2 16	1.53681	1.25	**0.28681**
INVx4 1	1.32356	1.25	**0.07356**
INVx4 2	1.33261	1.25	**0.08261**
INVx4 4	1.34919	1.25	**0.09919**
INVx4 8	1.37825	1.25	**0.12825**
INVx4 16	1.42752	1.25	**0.17752**

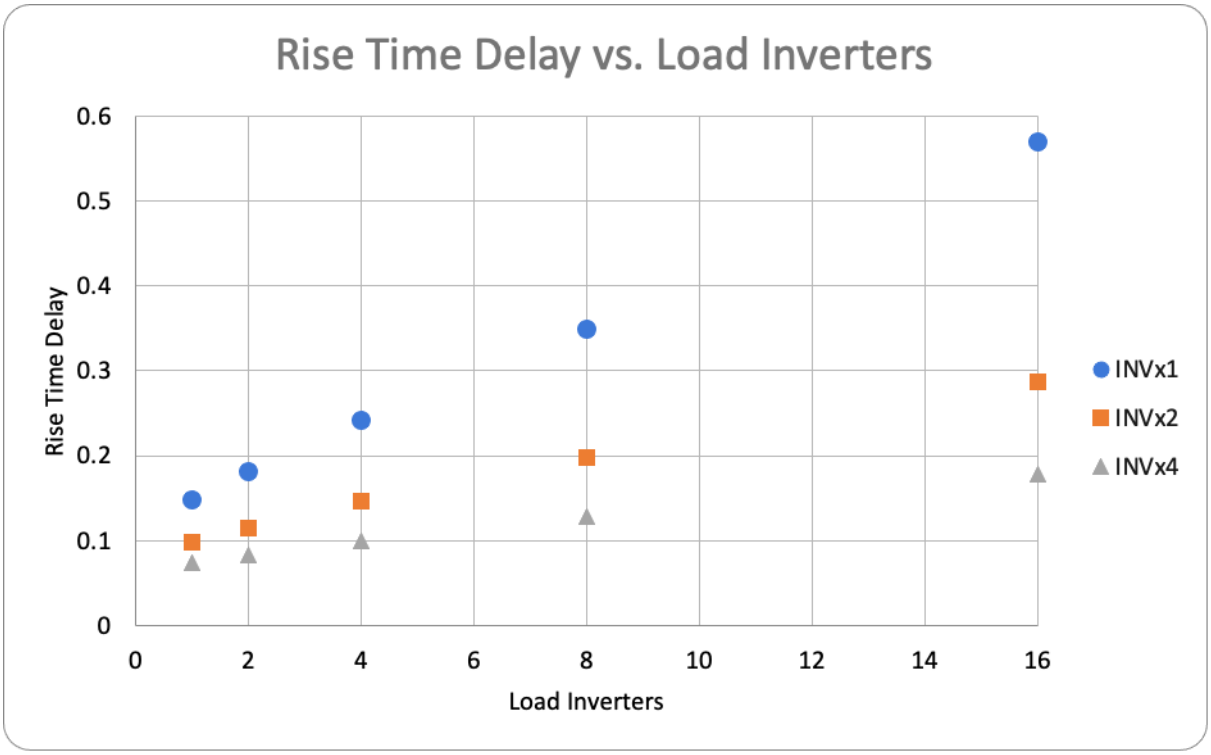

Figure 41: Plot for rise time delays for each inverter with different number of load inverters

The table and figure above show the rise time delay for each inverter with different number of load inverters. They clearly show that the width of the pMOS in the inverter heavily influences the rise time delay of the gate, where the higher the width the lower the rise time delay. The number of load inverters also has a large effect on the rise time delay, since when the number of load inverters increase the rise time delay also increases.

Rise Time for NAND2x1:

Table 6: Rise times for NAND2x1 gate with different number of load inverters

Gate	rise 4.5	rise .5	**rise**
NAND2x1 1	7.20015	6.82202	**0.37813**
NAND2x1 1 flipped	7.09977	6.81934	**0.28043**
NAND2x1 2	7.27132	6.83201	**0.43931**
NAND2x1 2 flipped	7.17397	6.82954	**0.34443**
NAND2x1 4	7.40913	6.84954	**0.55959**
NAND2x1 4 flipped	7.31382	6.84773	**0.46609**

Rise Time for NOR2x1:

Table 7: Rise times for NOR2x1 gate with different number of load inverters

Gate	rise 4.5	rise .5	**rise**
NOR2x1 1	7.07629	6.7504	**0.32589**
NOR2x1 1 flipped	7.10265	6.80123	**0.30142**
NOR2x1 2	7.14097	6.76181	**0.37916**
NOR2x1 2 flipped	7.16478	6.81097	**0.35381**
NOR2x1 4	7.26582	6.78104	**0.48478**
NOR2x1 4 flipped	7.28731	6.82638	**0.46093**

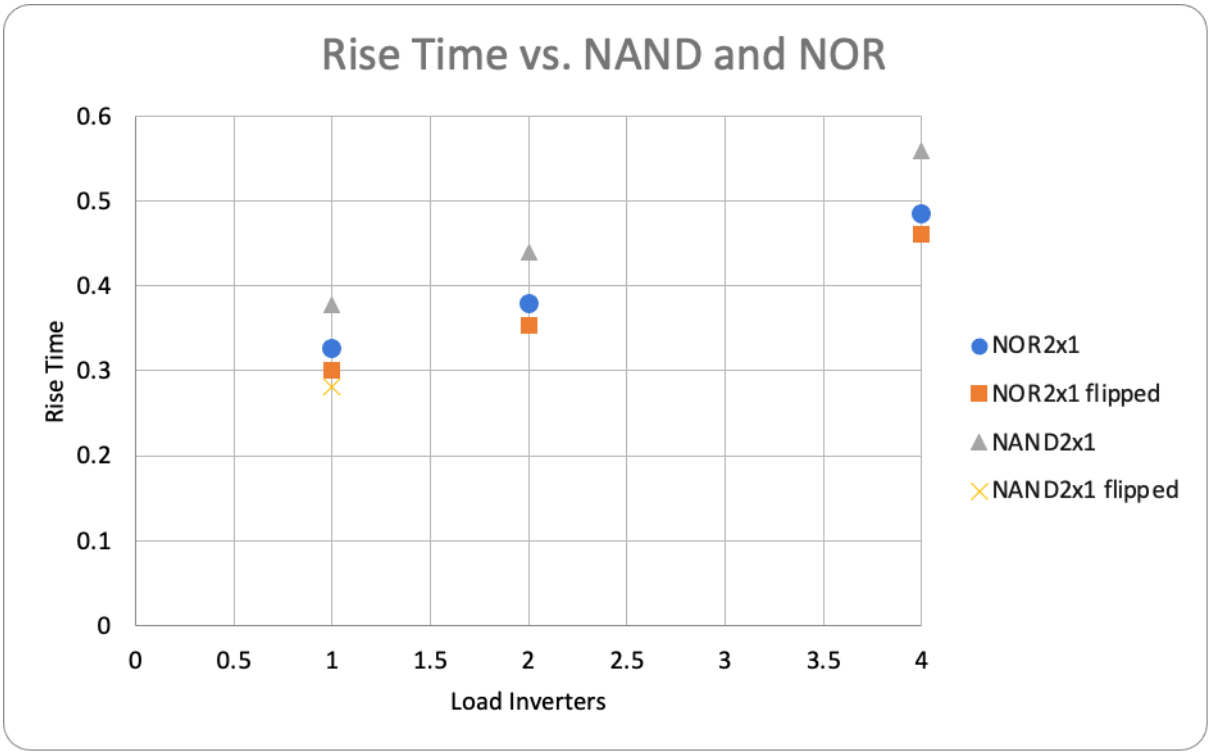

Figure 42: Plot for rise times for NOR2x1 and NAND2x1 with different number of load inverters

Fall Time for NAND2x1:

Table 8: Fall times for NAND2x1 gate with different number of load inverters

Gate	fall 4.5	fall .5	**fall**
NAND2x1 1	1.27119	1.51539	**0.2442**
NAND2x1 1 flipped	1.2399	1.51544	**0.27554**
NAND2x1 2	1.27823	1.56849	**0.29026**
NAND2x1 2 flipped	1.24919	1.57058	**0.32139**
NAND2x1 4	1.29087	1.674	**0.38313**
NAND2x1 4 flipped	1.26577	1.68009	**0.41432**

Fall Time for NOR2x1:

Table 9: Fall times for NOR2x1 gate with different number of load inverters

Gate	fall 4.5	fall .5	**fall**
NOR2x1 1	1.33941	1.59911	**0.2597**
NOR2x1 1 flipped	1.34461	1.75766	**0.41305**
NOR2x1 2	1.34861	1.76487	**0.41626**
NOR2x1 2 flipped	1.35358	1.83064	**0.47706**
NOR2x1 4	1.36515	1.81813	**0.45298**
NOR2x1 4 flipped	1.37015	1.97238	**0.60223**

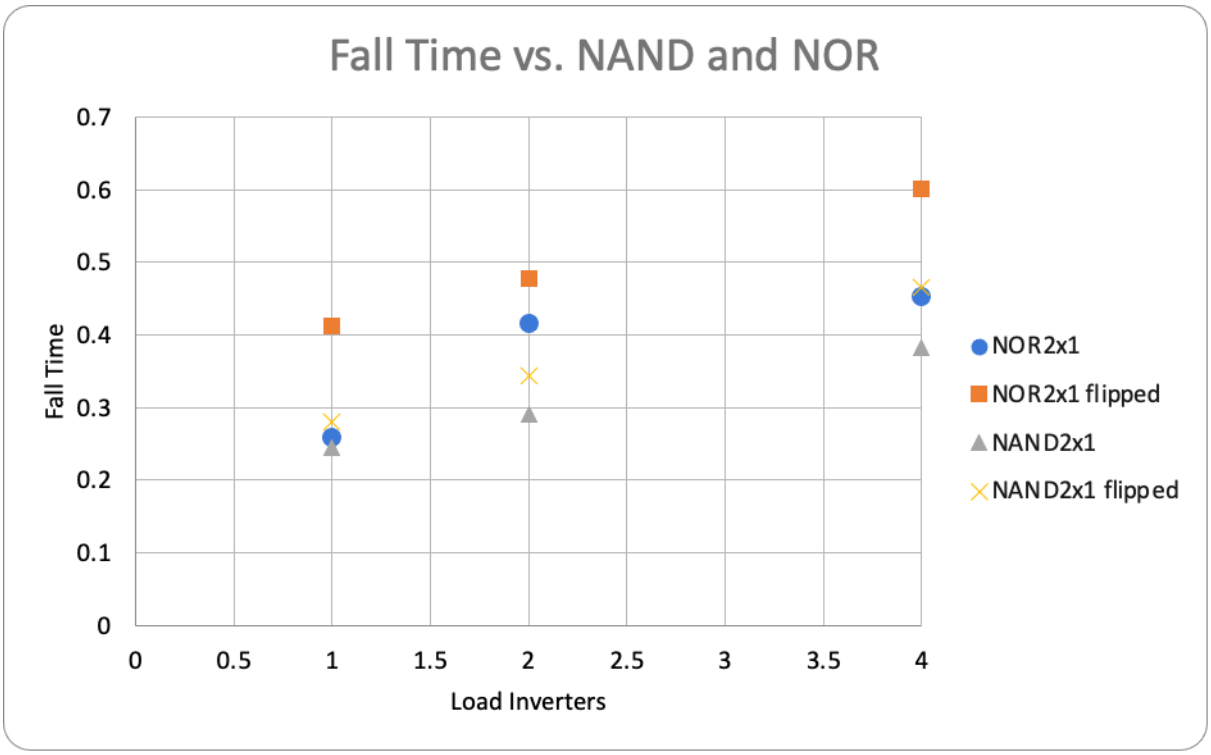

Figure 43: Plot for fall times for NOR2x1 and NAND2x1 with different number of load inverters

The tables and figure above show the rise times for the NAND and NOR gates. They both show that flipped the input has some form of effect on the output. This could be due to the length of wires and how the transistors are set up in the schematics.