# CMPE 315: Principles of VLSI Design Lab Cover Page

Lab#	:5
Lab Title	: Import VHDL, layout and LVS
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Section	:1
Data Cubusittad	10/25/2021
Date Submitted	:10/25/2021
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TA / Grader Use O	nly:
Late Submission Dedu	ction (20% per day late):
Other Deductions:	
Final Lab Grade:	
Comments to student.	

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#### Schematics, Layouts, and LVS outputs

#### 1. Inverter gate

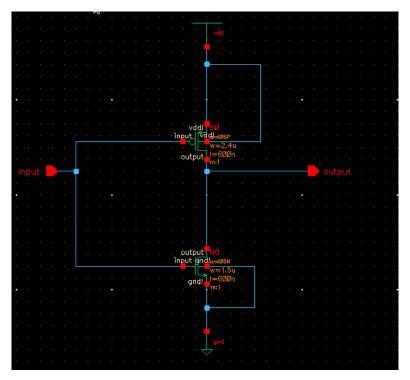


Figure 1: Inverter gate schematic

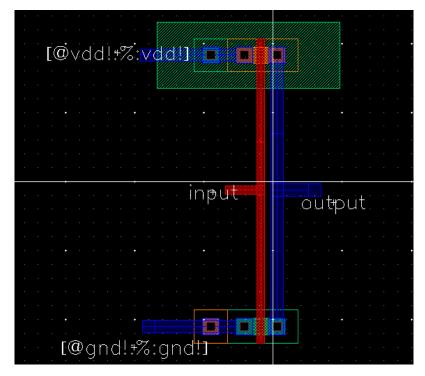


Figure 2: Inverter gate layout

```
The net-lists match.
                            layout schematic
                               instances
       un-matched
                               0
       rewired
                               0
                                       0
       size errors
                               0
                                       0
       pruned
                               0
                                       0
       active
                               2
       total
                               2
                                nets
       un-matched
       merged
pruned
                               0
                                       0
                               0
                                       0
                               4
       active
       total
                               terminals
       un-matched
       matched but
       different type
                               0
                                       0
       total
Probe files from /afs/umbc.edu/users/x/k/xk28378/home/315/LVS/schematic
devbad.out:
netbad.out:
mergenet.out:
termbad.out:
prunenet.out:
prunedev.out:
audit.out:
Probe files from /afs/umbc.edu/users/x/k/xk28378/home/315/LVS/layout
devbad.out:
netbad.out:
mergenet.out:
termbad.out:
prunenet.out:
prunedev.out:
audit.out:
```

Figure 3: Inverter gate LVS output

#### 2. And2 gate

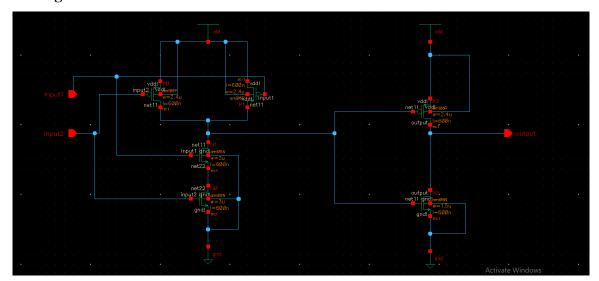


Figure 4: And2 gate schematic

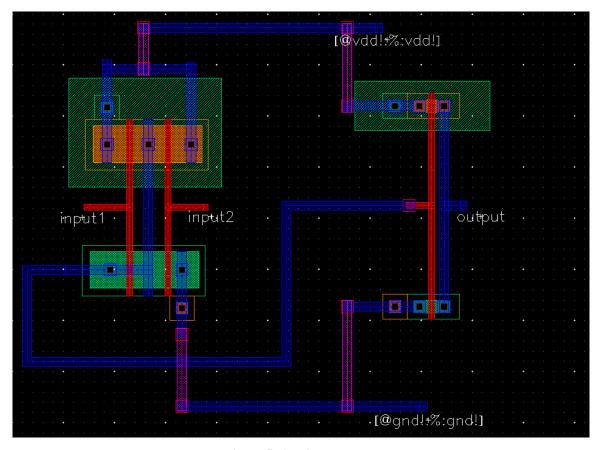


Figure 5: And2 gate layout

audit.out:

	layout	schematic
	instances	
un-matched	0	0
rewired	0	0
size errors	0	0
pruned	0	0
active	6	6
total	6	6
	nets	
un-matched	0	0
merged	0	0
pruned	0	0
active	7	7
total	7	7
	terminals	
un-matched	0	0
matched but		
different type	0	0
total	5	5

```
Probe files from /afs/umbc.edu/users/x/k/xk28378/home/315/LVS/schematic devbad.out:
netbad.out:
mergenet.out:
termbad.out:
prunenet.out:
prunedev.out:
audit.out:

Probe files from /afs/umbc.edu/users/x/k/xk28378/home/315/LVS/layout devbad.out:
netbad.out:
mergenet.out:
termbad.out:
prunenet.out:
prunenet.out:
```

Figure 6: And2 gate LVS output

#### 3. Or3 gate

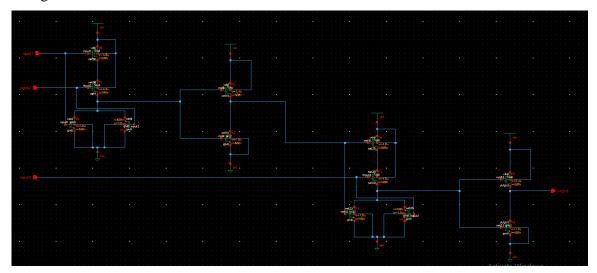


Figure 7: Or3 gate schematic

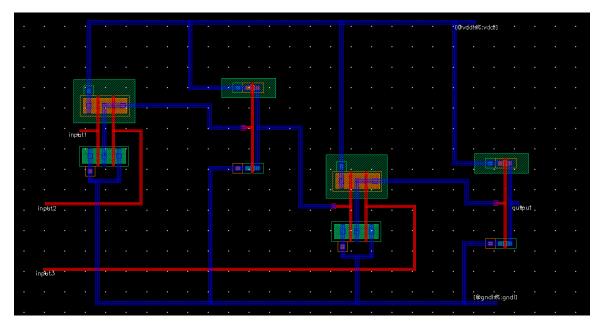


Figure 8: Or3 gate layout

	layout	schematic
	inst	ances
un-matched	0	0
rewired	0	0
size errors	0	0
pruned	0	0
active	12	12
total	12	12
	nets	
un-matched	0	0
merged	0	0
pruned	0	0
active	11	11
total	11	11
	terminals	
un-matched	0	0
matched but		
different type	ø	0
total	6	6
	·	•

```
Probe files from /afs/umbc.edu/users/x/k/xk28378/home/315/LVS/schematic
devbad.out:
netbad.out:
mergenet.out:
termbad.out:
prunenet.out:
prunedev.out:
audit.out:
Probe files from /afs/umbc.edu/users/x/k/xk28378/home/315/LVS/layout
devbad.out:
netbad.out:
mergenet.out:
termbad.out:
prunenet.out:
prunedev.out:
audit.out:
```

Figure 9: Or3 gate LVS output

### 4. Xor2 gate

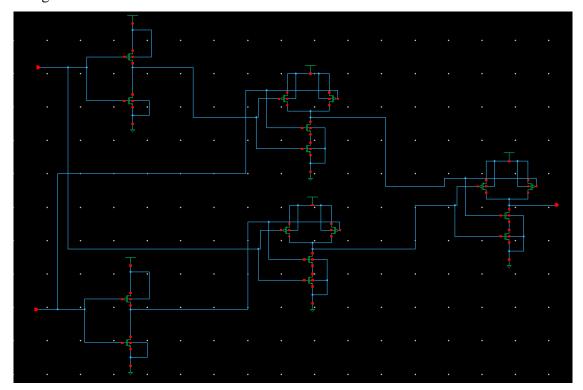


Figure 10: Xor2 gate schematic

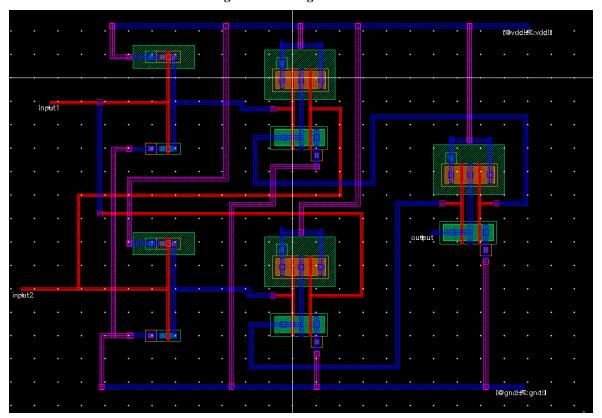


Figure 11: Xor2 gate layout

termbad.out:

prunenet.out:

prunedev.out:

audit.out:

```
layout schematic
                            instances
       un-matched
                            0
                                    0
                           0
       rewired
                                    0
                           0
       size errors
                                    0
                            0
                                    0
       pruned
       active
                            16
                                   16
       total
                            16
                                   16
                             nets
       un-matched
                             0
                                    0
       merged
                            0
                                    0
                            0
       pruned
                                    0
       active
                            12
                                    12
       total
                            12
                                    12
                            terminals
       un-matched
       matched but
       different type
                             0
                                    0
       total
                             5
                                    5
Probe files from /afs/umbc.edu/users/x/k/xk28378/home/315/LVS/schematic
devbad.out:
netbad.out:
mergenet.out:
termbad.out:
prunenet.out:
prunedev.out:
audit.out:
Probe files from /afs/umbc.edu/users/x/k/xk28378/home/315/LVS/layout
devbad.out:
netbad.out:
mergenet.out:
```

Figure 12: Xor2 gate LVS output

#### 5. Mux\_2\_1 gate

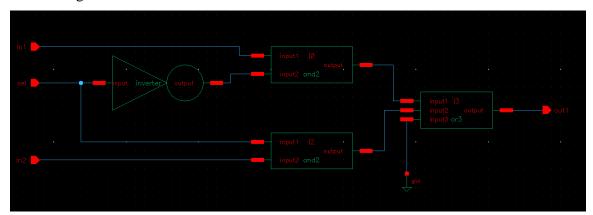


Figure 13: Mux\_2\_1 gate schematic

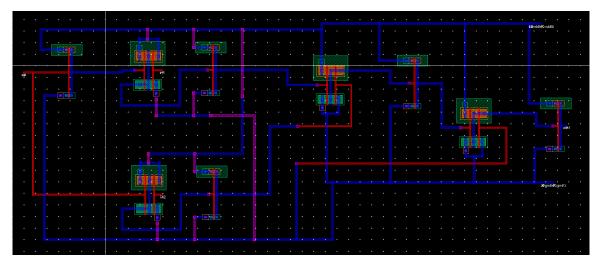


Figure 14: Mux\_2\_1 gate layout

audit.out:

	layout	schematic
	inst	ances
un-matched	0	0
rewired	0	0
size errors	0	0
pruned	0	0
active	26	26
total	26	26
	nets	
un-matched	0	0
merged	0	0
pruned	0	0
active	18	18
total	18	18
	terminals	
un-matched	0	0
matched but		
different type	0	0
total	6	6

Probe files from /afs/umbc.edu/users/x/k/xk28378/home/315/LVS/schematic devbad.out:
netbad.out:
mergenet.out:
termbad.out:
prunenet.out:
prunedev.out:
audit.out:

Probe files from /afs/umbc.edu/users/x/k/xk28378/home/315/LVS/layout devbad.out:
netbad.out:
mergenet.out:
termbad.out:
prunedev.out:

Figure 15: Mux\_2\_1 gate LVS output

#### 6. Mux\_4\_1 gate

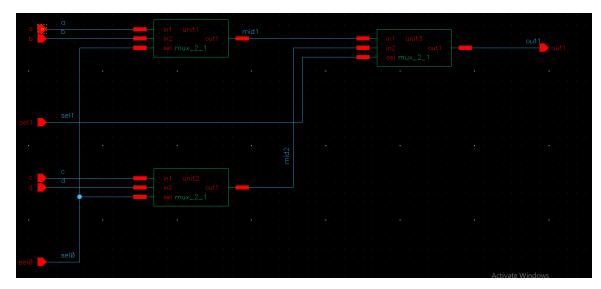


Figure 16: Mux\_4\_1 gate schematic

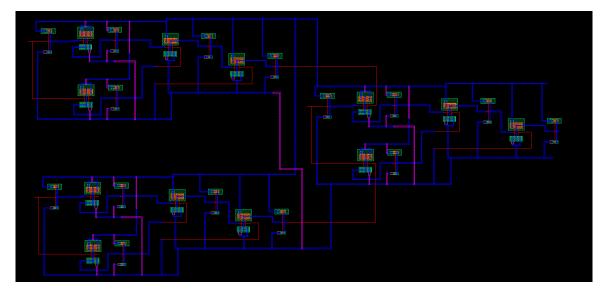


Figure 17: Mux\_4\_1 gate layout

	-	schematic ances
un-matched	0	0
rewired	0	0
size errors	0	0
pruned	0	0
active	78	78
total	78	78
	nets	
un-matched	0	0
merged	0	0
pruned	0	0
active	47	47
total	47	47
		_
	terminals	
un-matched	0	0
matched but		
different type	0	0
total	9	9

Probe files from /afs/umbc.edu/users/x/k/xk28378/home/315/LVS/schematic devbad.out: netbad.out: mergenet.out: termbad.out: prunenet.out: prunedev.out: audit.out: Probe files from /afs/umbc.edu/users/x/k/xk28378/home/315/LVS/layout devbad.out: netbad.out: mergenet.out: termbad.out: prunenet.out: prunedev.out: audit.out:

Figure 18: Mux\_4\_1 gate LVS output

### 7. Mux\_4\_bit gate

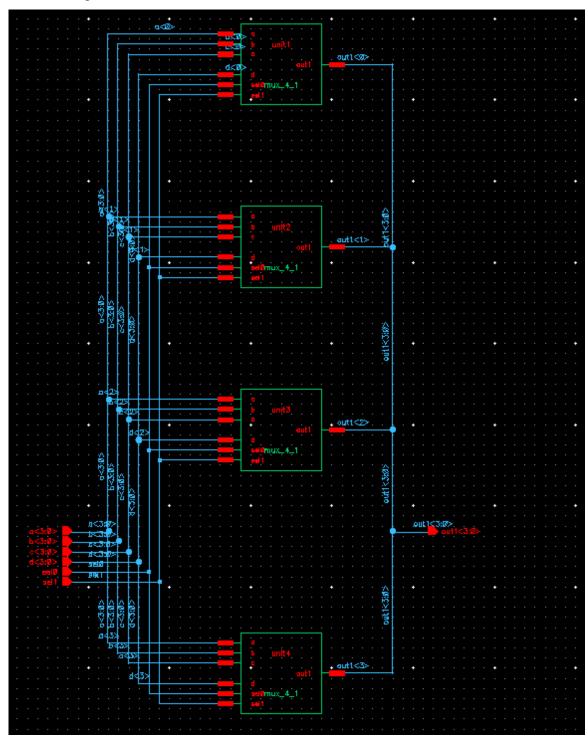


Figure 19: Mux\_4\_bit gate schematic

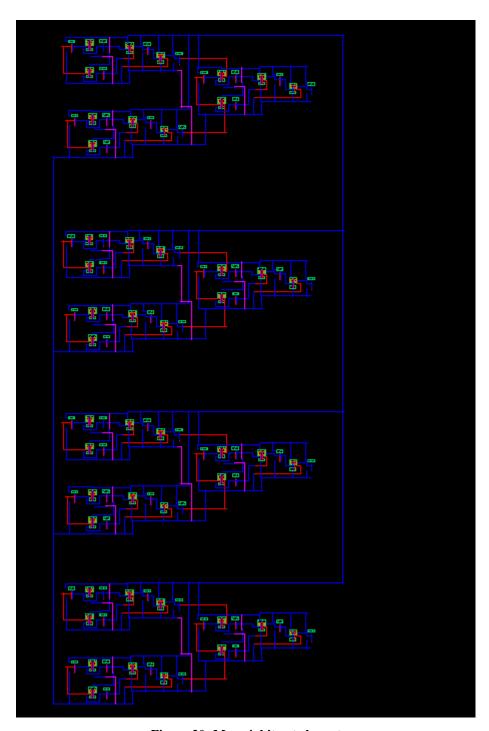


Figure 20: Mux\_4\_bit gate layout

```
layout schematic
                    instances
                    0
un-matched
                           0
                    0
                           0
rewired
size errors
                    0
                            0
pruned
                    0
active
                    312
                            312
total
                    312
                            312
                      nets
un-matched
merged
                     0
                            0
pruned
                     0
                            0
active
                    176
                            176
total
                           176
                    176
                    terminals
un-matched
matched but
different type
                     0
total
                     24
                            24
```

```
Probe files from /afs/umbc.edu/users/x/k/xk28378/home/315/LVS/schematic
devbad.out:
netbad.out:
mergenet.out:
termbad.out:
prunenet.out:
prunedev.out:
audit.out:
Probe files from /afs/umbc.edu/users/x/k/xk28378/home/315/LVS/layout
devbad.out:
netbad.out:
mergenet.out:
termbad.out:
prunenet.out:
prunedev.out:
audit.out:
```

Figure 21: Mux\_4\_bit gate LVS output

#### 8. Adder1

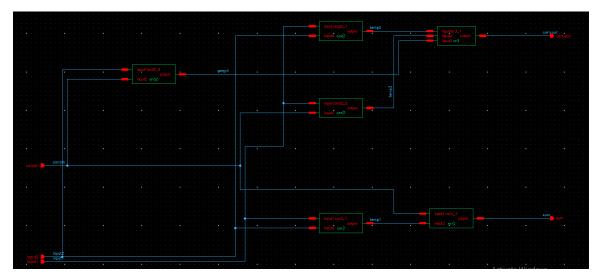


Figure 22: Adder1 gate schematic

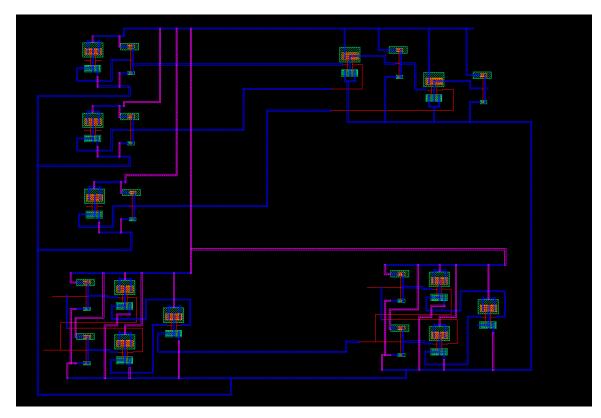


Figure 23: Adder1 gate layout

audit.out:

```
layout schematic
                    instances
un-matched
                    0
                          0
                    0
rewired
                            0
size errors
                    0
                           0
                    0
pruned
                            0
active
                    62
                           62
total
                    62
                            62
                      nets
un-matched
                    0
                            0
merged
                    0
                            0
pruned
                    0
                            0
active
                    36
                            36
total
                    36
                    terminals
un-matched
matched but
different type
                            0
                     0
                            7
```

```
Probe files from /afs/umbc.edu/users/x/k/xk28378/home/315/LVS/schematic devbad.out:
netbad.out:
mergenet.out:
termbad.out:
prunenet.out:
prunedev.out:
audit.out:

Probe files from /afs/umbc.edu/users/x/k/xk28378/home/315/LVS/layout devbad.out:
netbad.out:
mergenet.out:
termbad.out:
prunenet.out:
prunenet.out:
```

Figure 24: Adder1 gate LVS schematic

#### 9. Adder4

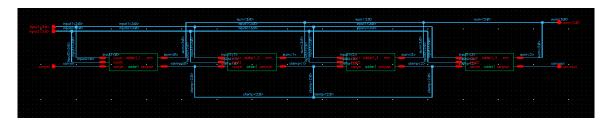


Figure 25: Adder4 gate schematic



Figure 26: Adder gate layout

un-matched rewired size errors pruned active total		schematic ances 0 0 0 0 248 248
total	240	240
	nets	
un-matched	0	0
merged	0	0
pruned	0	0
active	135	135
total	135	135
	terminals	
un-matched matched but	0	0
different type	0	0
total	16	16

```
Probe files from /afs/umbc.edu/users/x/k/xk28378/home/315/LVS/schematic
devbad.out:
netbad.out:
mergenet.out:
termbad.out:
prunenet.out:
prunedev.out:
audit.out:
Probe files from /afs/umbc.edu/users/x/k/xk28378/home/315/LVS/layout
devbad.out:
netbad.out:
mergenet.out:
termbad.out:
prunenet.out:
prunedev.out:
audit.out:
```

Figure 27: Adder4 gate LVS output

#### 10. Alu\_4

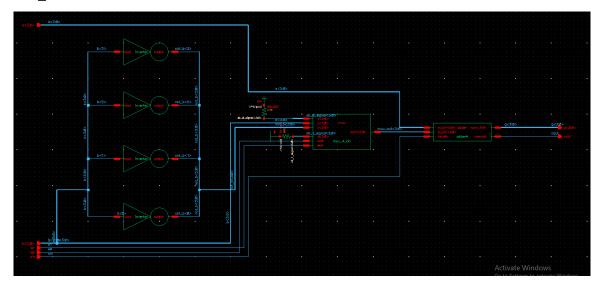


Figure 28: Alu\_4 gate schematic

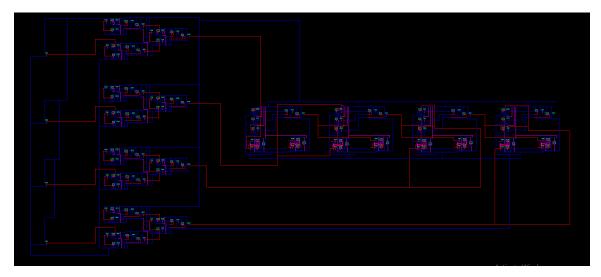


Figure 29: Alu\_4 gate layout

prunedev.out: audit.out:

un-matched

rewired size errors

```
pruned
                               0
                                       0
                               568
                                       568
       active
                               568
                                       568
       total
                                 nets
       un-matched
                               0
                                       0
       merged
                               0
                                       0
       pruned
                               0
                                       0
       active
                               297
                                        297
       total
                               297
                                        297
                               terminals
       un-matched
                               0
       matched but
       different type
                               0
                                       0
       total
                               18
                                       18
Probe files from /afs/umbc.edu/users/x/k/xk28378/home/315/LVS/schematic
devbad.out:
netbad.out:
mergenet.out:
termbad.out:
prunenet.out:
prunedev.out:
audit.out:
Probe files from /afs/umbc.edu/users/x/k/xk28378/home/315/LVS/layout
devbad.out:
netbad.out:
mergenet.out:
termbad.out:
prunenet.out:
```

layout schematic instances

0

0

0

0

Figure 30: Alu\_4 gate LVS output