CMPE 315: Principles of VLSI Design
Lab Cover Page

Lab # : 1
Lab Title : Structural VHDL

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Section : 01

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TA / Grader Use Only:

Late Submission Deduction (20% per day late):

Other Deductions:

Final Lab Grade:

Comments to student:

Lab status and Simulation Procedure:

I was able to fully complete the lab, having it working using file I/O and one printing out to the terminal. My ALU entity ran using three other entities, which were just an adder, inverter and a four bit four to one multiplexer. The four bit four to one multiplexer runs another entity that is a one bit four to one multiplexer, and that entity runs a one bit two to one multiplexer that is called four times. The adder and inverter entities are given to us.

Output Explanation:

The truth table for the ALU is supposed to look like this where A = 3 and B = 2:

S1	S0	Cin	A	B	G	Cout
0	0	0	0011	0010	0011	0
0	1	0	0011	0010	0101	0
1	0	0	0011	0010	0000	1
1	1	0	0011	0010	0010	1
0	0	1	0011	0010	0100	0
0	1	1	0011	0010	0110	0
1	0	1	0011	0010	0001	1
1	1	1	0011	0010	0011	1

This is the input for the file I/O test bench:

0011 //A

0010 //B

0 //S0

0 //S1

0 //Cin

0011

0010

0

1

0

0011

0010

1

0

0

0011

0010

1

1

0

0011

0010

0

0

1

0011

0010

0

1

1

0011

0010

1

0

1

0011

0010

1

1

1

The output for the file I/O test bench is as follows:

0011 //G

0 //Cout

0101

0

0000

1

0010

1

0100

0

0110

0

0001

1

0011

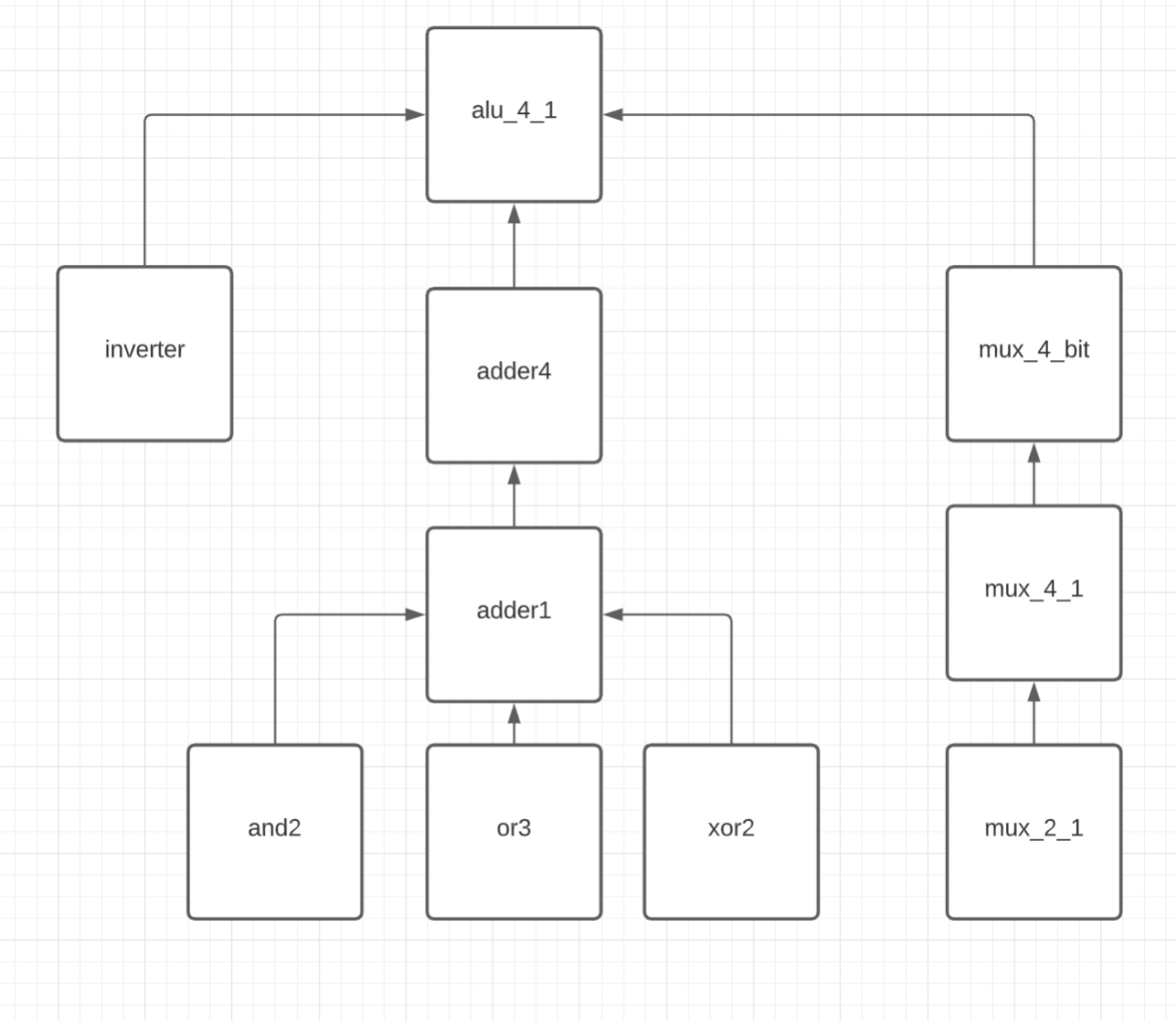
1

This matches the truth table which shows the output is valid. Next is the output for the std out test bench:

```
A:0011 B:0010 S1:0 S0:0 Carry In:0
Output:0011 Carry Out:0

A:0011 B:0010 S1:0 S0:1 Carry In:0
Output:0101 Carry Out:0

A:0011 B:0010 S1:1 S0:0 Carry In:0
Output:0000 Carry Out:1

A:0011 B:0010 S1:1 S0:1 Carry In:0
Output:0010 Carry Out:1

A:0011 B:0010 S1:0 S0:0 Carry In:1
Output:0100 Carry Out:0

A:0011 B:0010 S1:0 S0:1 Carry In:1
Output:0110 Carry Out:0

A:0011 B:0010 S1:1 S0:0 Carry In:1
Output:0001 Carry Out:1

A:0011 B:0010 S1:1 S0:1 Carry In:1
Output:0011 Carry Out:1
```

The output for the std out test bench also matches the truth table which shows it's valid.

Hierarchy of Design Specification



Inverter: flips 1 bit input
Adder4: computes addition with carry to 4-bit inputs and carry in
Adder1: computes addition with a carry for 1-bit inputs and carry in
And2: and gate with 2 inputs
Or3: or gate with 3 inputs
Xor2: xor gate with inputs
Mux_4_bit: 4 to 1 multiplexer with 4-bit inputs and output, takes in all 0s, B, not B, and all 1s
Mux_4_1: 4 to 1 multiplexer with 1-bit inputs and output
Mux_2_1: 2 to 1 multiplexer with 1-bit inputs and output

The ALU entity first uses the inverter entity to invert B. The inverter takes in a 1-bit input, so the inverter entity is called 4 times to flip all four bits of B. From there the two constants, all_0 and

all_1, B, and not_B are sent into the 4 to 1 4-bit multiplexer alongside with two select bits which calls the mux_4_1 entity which is basically a 4 o 1 1-bit multiplexer. It calls it 4 times to get the output value for the 4-bit inputs using the two select bits. The mux_4_1 entity itself also calls another mux_2_1 mux which takes in two 1-bit inputs and uses and, or, and not gates to calculate the output. The output of the mux_4_bit entity is then put into a signal which is then passed to the adder4 entity alongside A and the carry in input. The output of the adder is then outputted as the output of the ALU.

PRINT ALL VHDL CODE USING THE ENSCRIPT COMMAND GIVEN ON THE WEBPAGE AND INCLUDE IT AT THE END OF YOUR REPORT.