CMPE 315: Principles of VLSI Design
Lab Cover Page

Lab #   :   **4**
Lab Title   :   **D Flip-flop layout and simulations**

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Section   :   **1**

Date Submitted   :   **10/15/2021**

TA / Grader Use Only:

Late Submission Deduction (20% per day late):

Other Deductions:

Final Lab Grade:
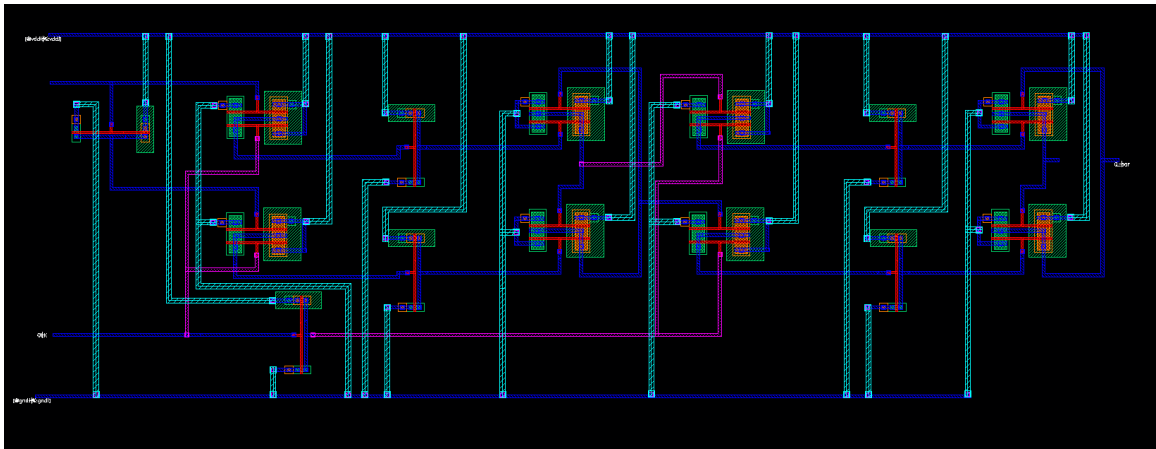
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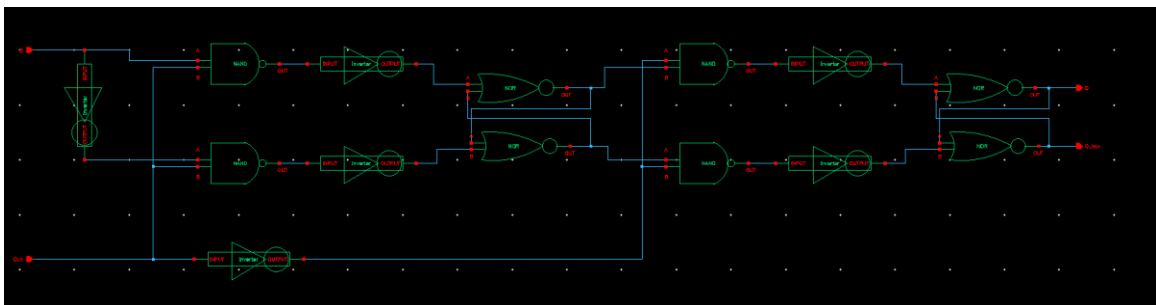
Figure 1: Logic gate D Flip-Flop Layout

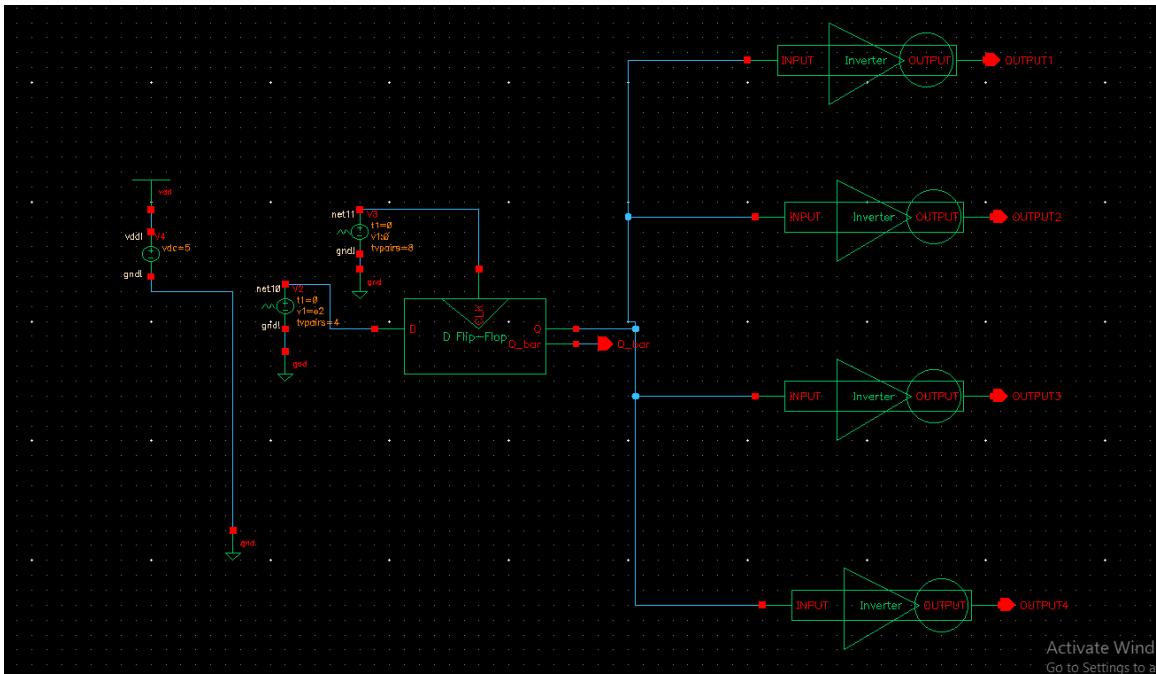**Figure 2: Logic gate D Flip-Flop Schematic**

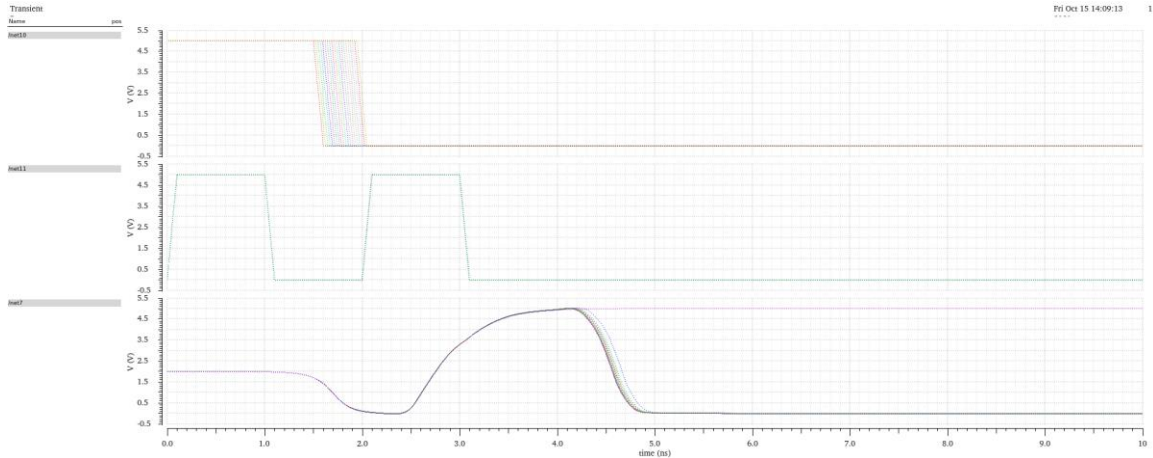**Figure 3: Logic gate D Flip-Flop Simulation Schematic**

Figure 4: Extracted Logic Gate Flip Flop Coarse Sweep Latching 0
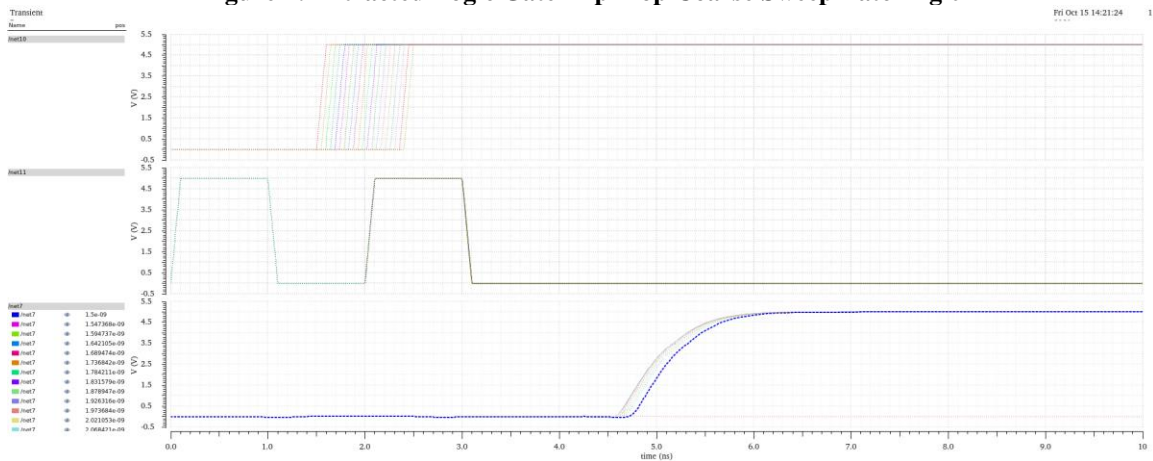

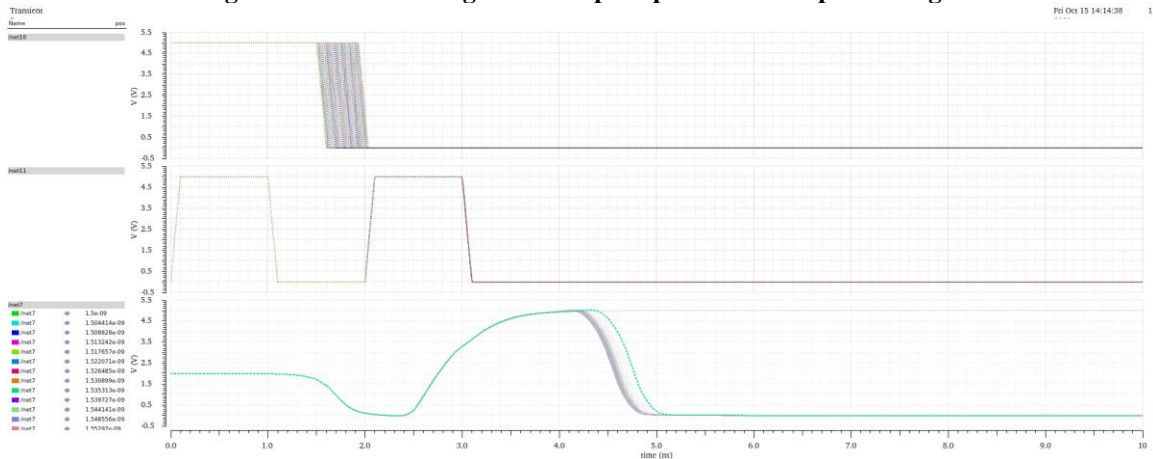**Figure 5: Extracted Logic Gate Flip Flop Coarse Sweep Latching 1**

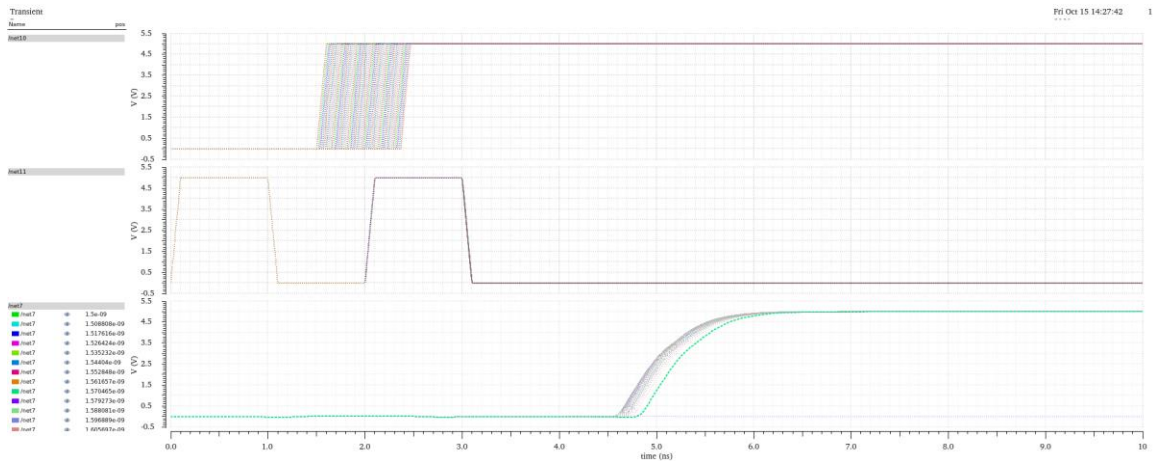**Figure 6: Extracted Logic Gate Flip Flop Fine Sweep Latching 0**

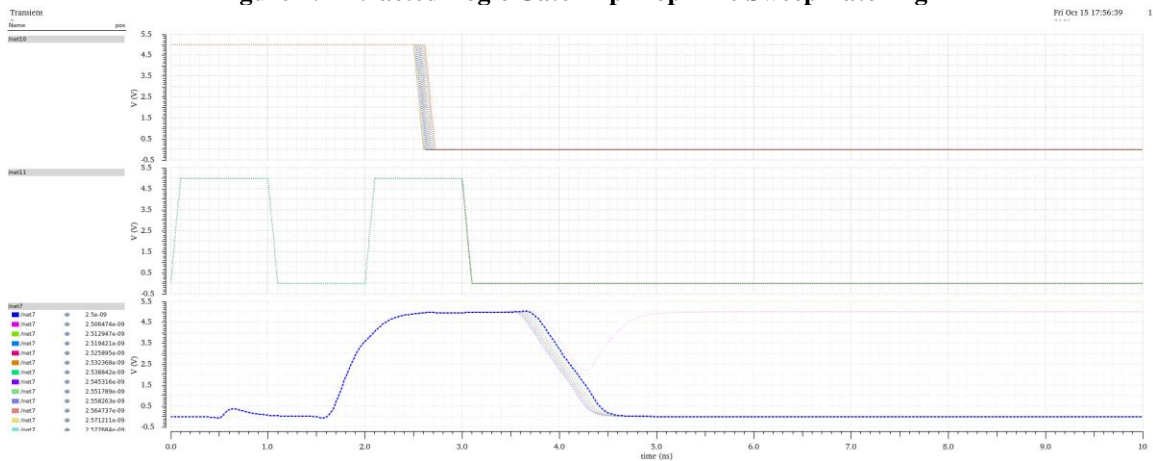**Figure 7: Extracted Logic Gate Flip Flop Fine Sweep Latching 1**

Figure 8: Schematic Logic Gate Flip Flop Coarse Sweep Latching 0
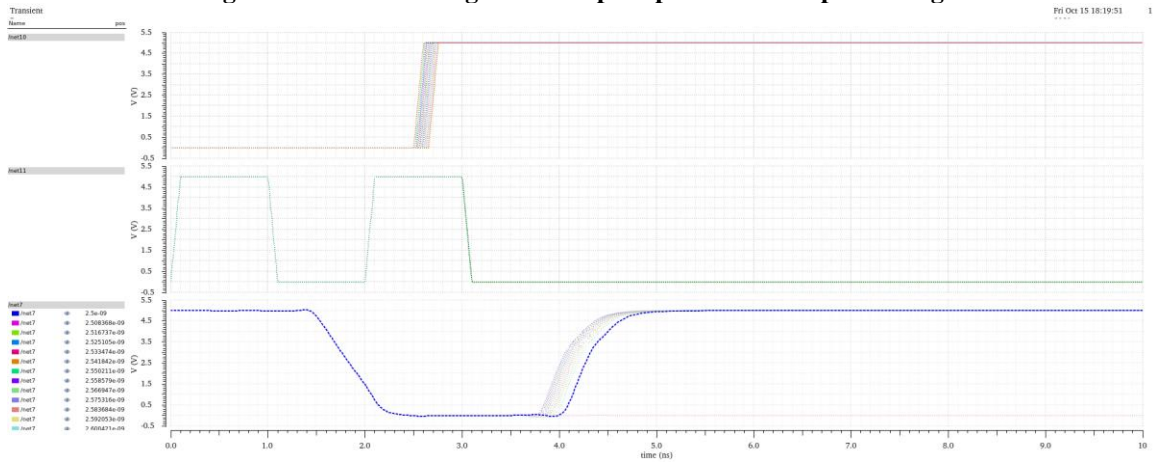

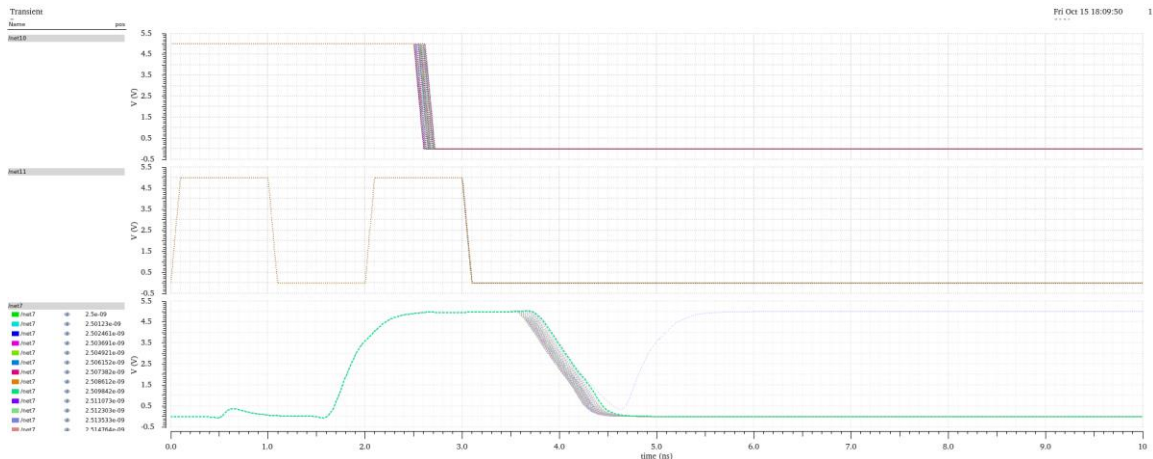**Figure 9: Schematic Logic Gate Flip Flop Coarse Sweep Latching 1**

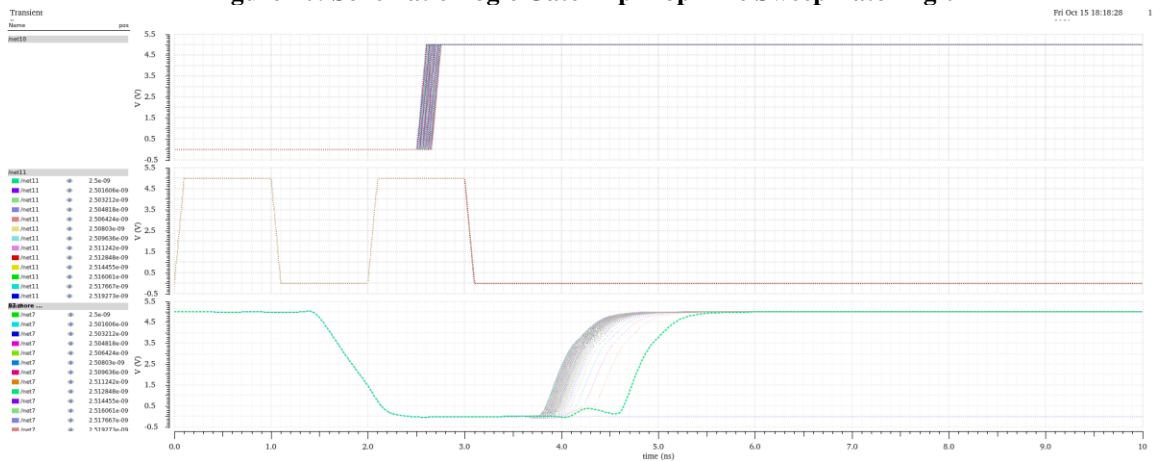**Figure 10: Schematic Logic Gate Flip Flop Fine Sweep Latching 0**

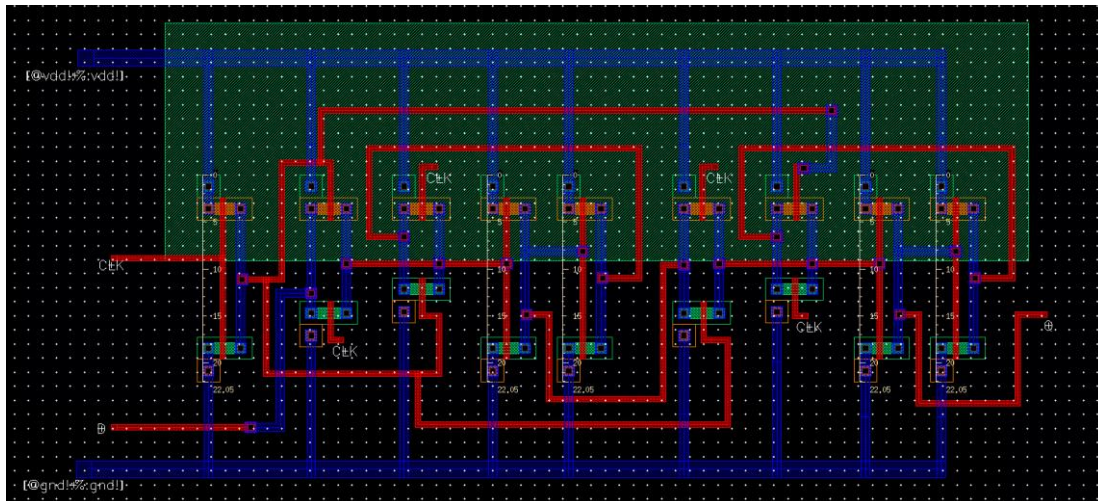**Figure 11: Schematic Logic Gate Flip Flop Fine Sweep Latching 1**

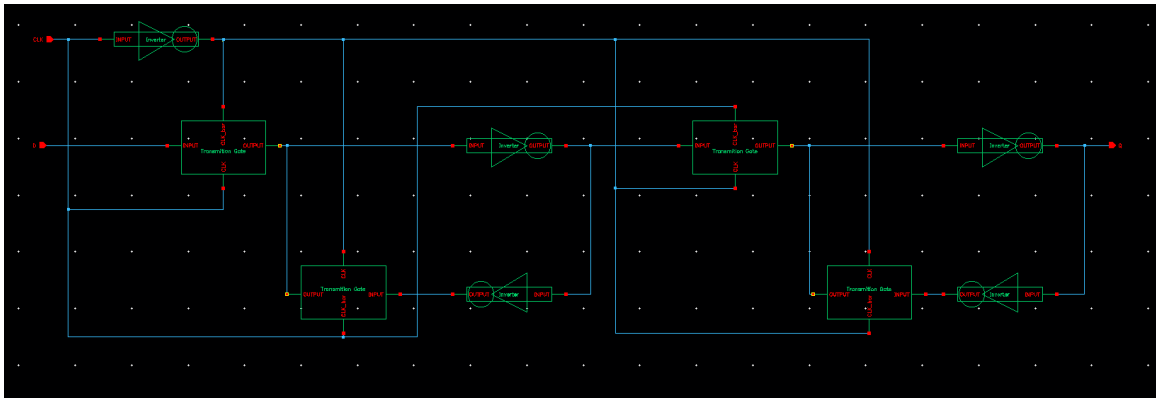**Figure 12: Transmission Gate D Flip-Flop Layout**

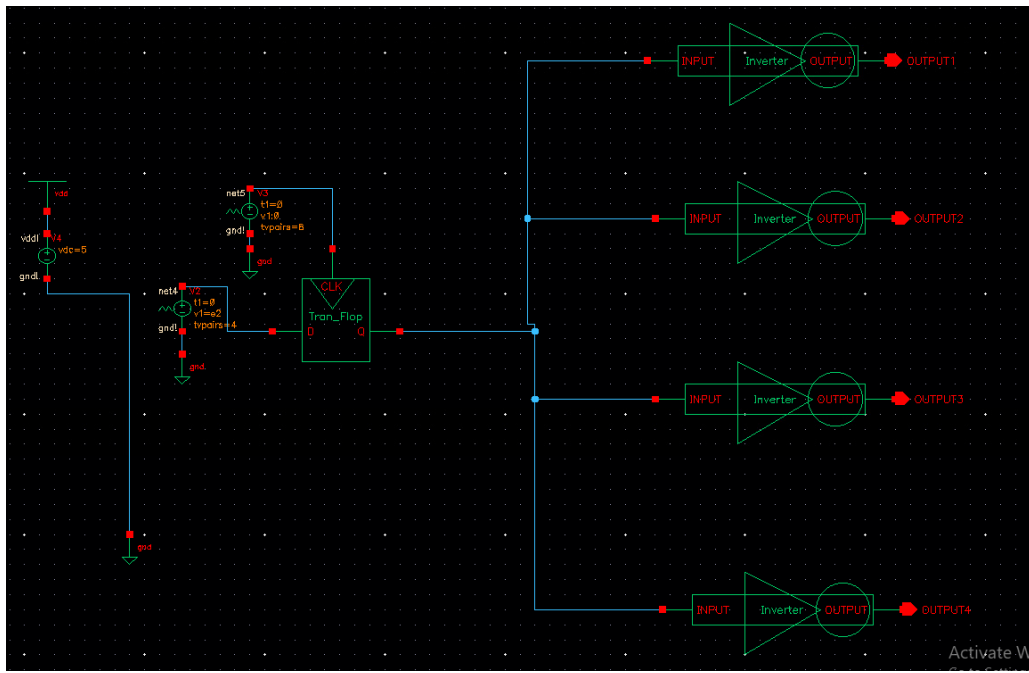**Figure 13: Transmission Gate D Flip-Flop Schematic**

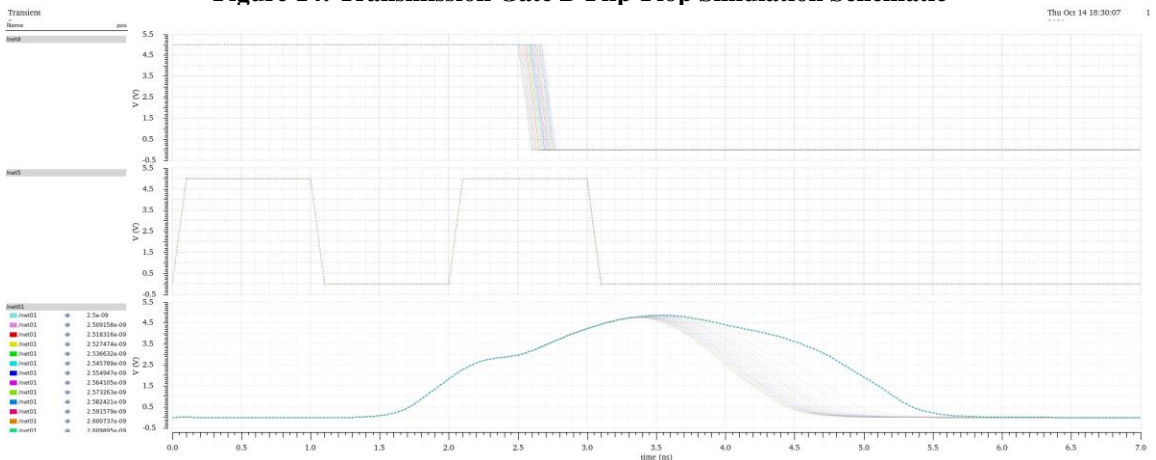**Figure 14: Transmission Gate D Flip-Flop Simulation Schematic**

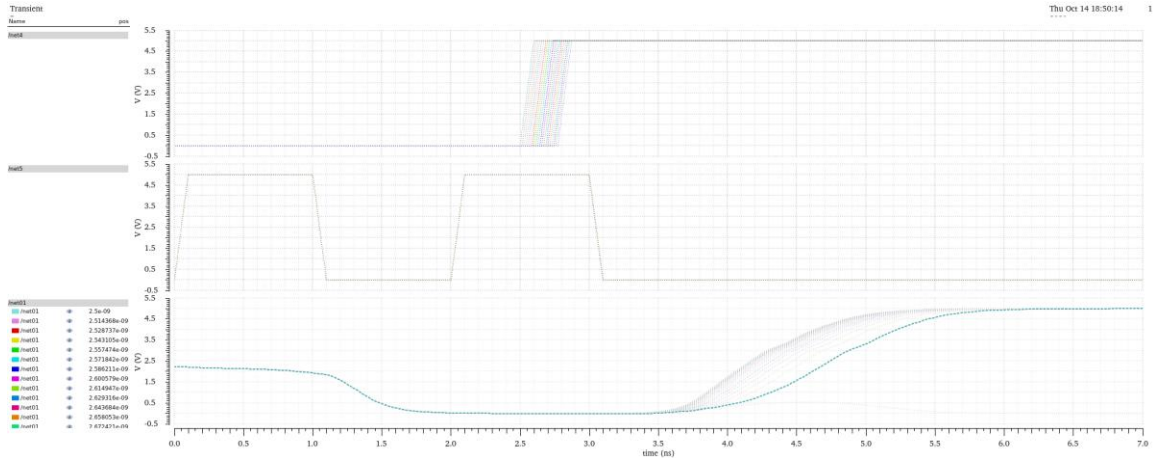**Figure 15: Extracted Transmission Gate Flip Flop Coarse Sweep Latching 0**

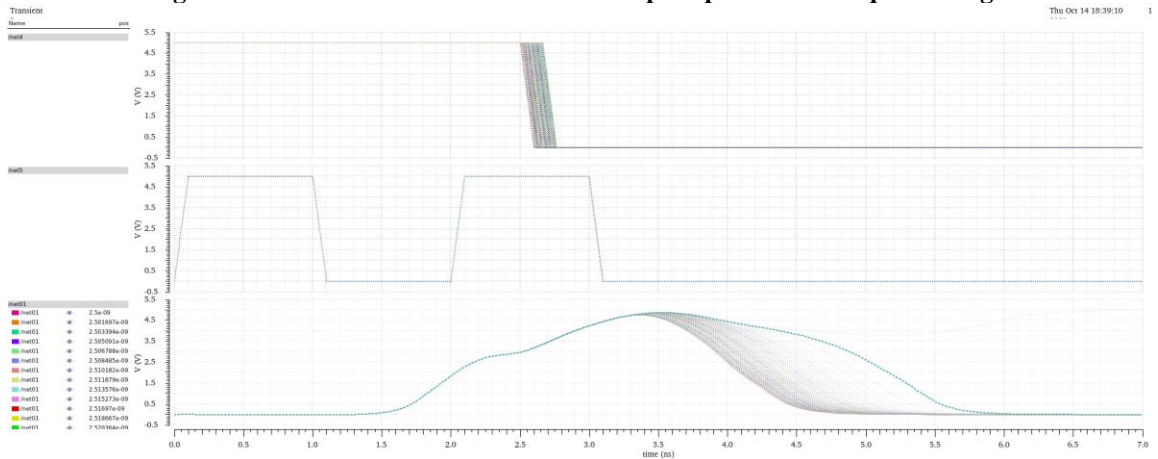**Figure 16: Extracted Transmission Gate Flip Flop Coarse Sweep Latching 1**

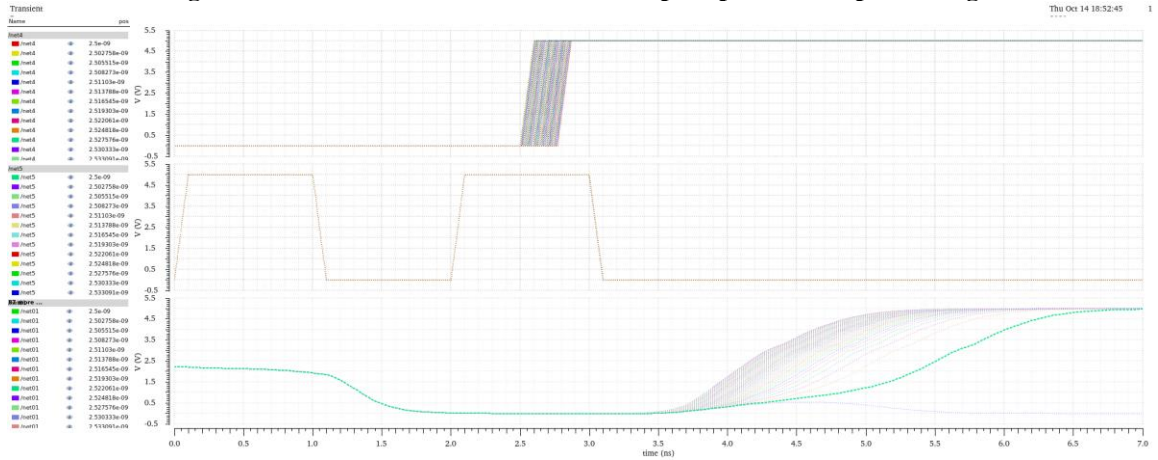**Figure 17: Extracted Transmission Gate Flip Flop Fine Sweep Latching 0**

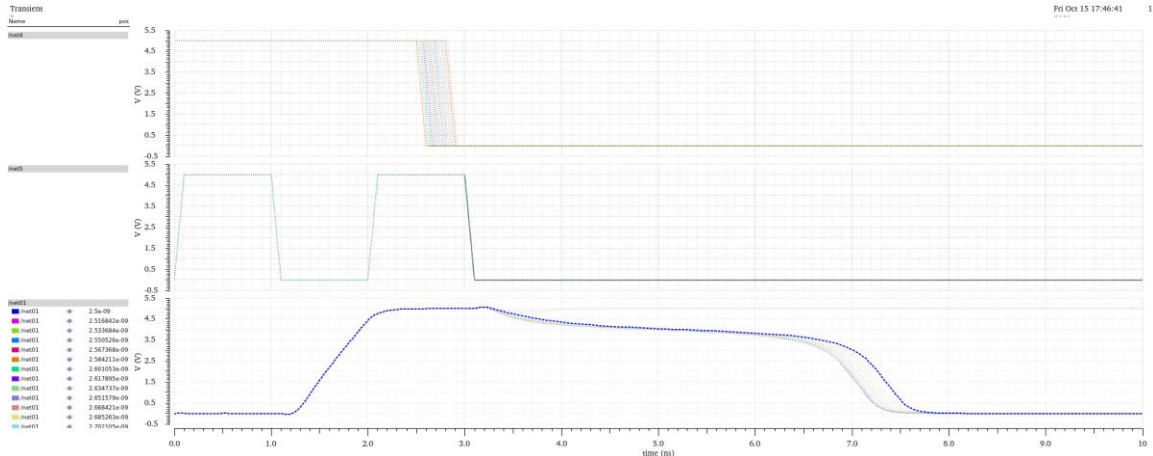**Figure 18: Extracted Transmission Gate Flip Flop Fine Sweep Latching 1**

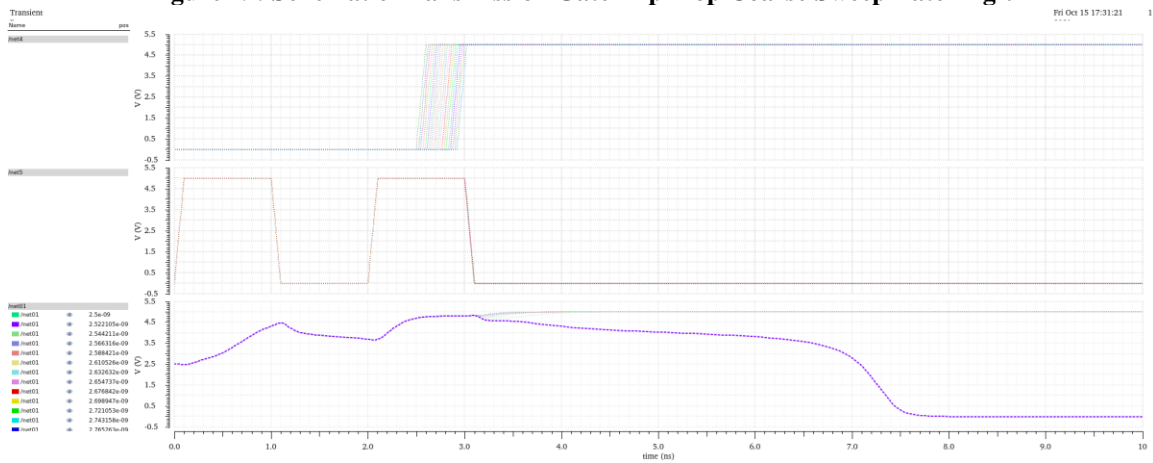**Figure 19: Schematic Transmission Gate Flip Flop Coarse Sweep Latching 0**

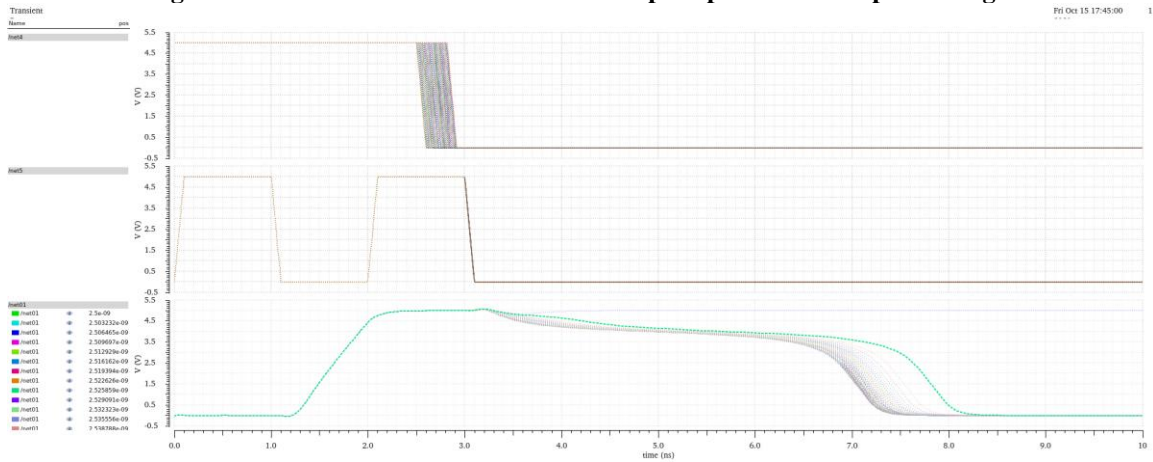**Figure 20: Schematic Transmission Gate Flip Flop Coarse Sweep Latching 1**

Figure 21: Schematic Transmission Gate Flip Flop Fine Sweep Latching 0

Figure 22: Schematic Transmission Gate Flip Flop Fine Sweep Latching 1

Transmission Gate t_{dq} vs t_{dc} latching 1

(y-axis) t_{cq} in seconds — $\times 10^{-10}$, ranging 7 to 12

(x-axis) t_{dc} in seconds — $\times 10^{-10}$, ranging 1.3 to 1.6

Transmission Gate t_{cq} vs t_{dc} latching 0

(y-axis) t_{cq} in seconds — $\times 10^{-9}$, ranging 0.8 to 1.4

(x-axis) t_{dc} in seconds — $\times 10^{-10}$, ranging 1.308 to 1.316

Transmission Gate t_{dq} vs t_{dc} latching 0