Nem Negash

CMPE 415

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HW5 Report

Problem 1:

The adder timing results:

```
create_clock -period 2.155 -name clk -waveform {0.000 1.0775} -add [get_ports clk]
```

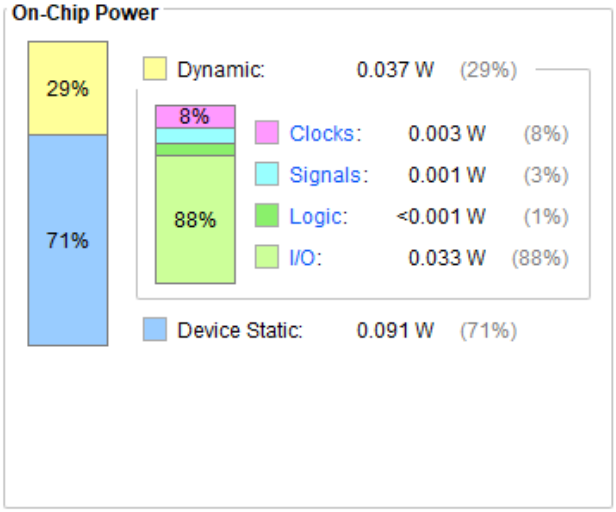
Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	0.163 ns	Worst Hold Slack (WHS):	0.190 ns	Worst Pulse Width Slack (WPWS):	0.000 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	11	Total Number of Endpoints:	11	Total Number of Endpoints:	33

All user specified timing constraints are met.

Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

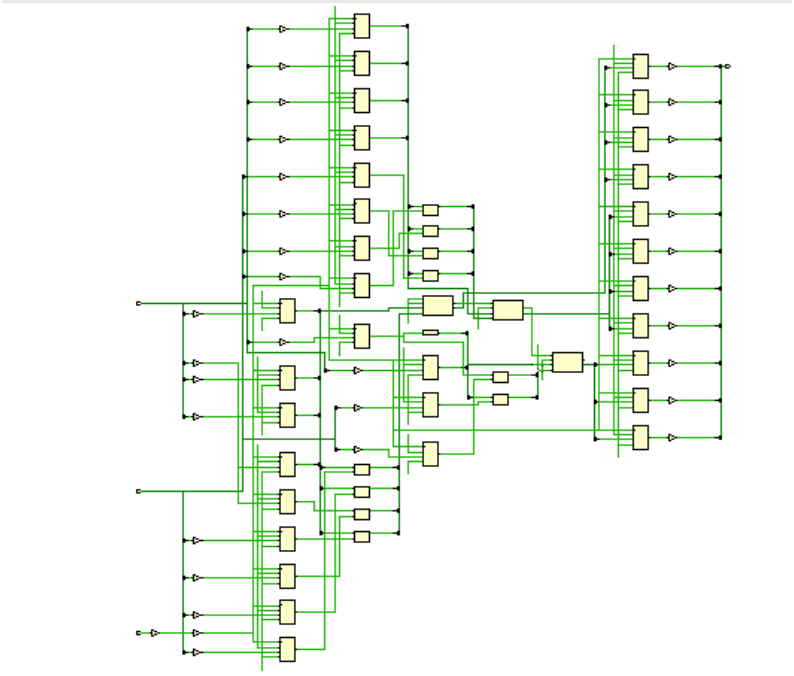
Total On-Chip Power:	**0.128 W**
Design Power Budget:	**Not Specified**
Power Budget Margin:	**N/A**
Junction Temperature:	**25.6°C**
Thermal Margin:	59.4°C (12.9 W)
Effective ϑJA:	4.6°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

Launch Power Constraint Advisor to find and fix invalid switching activity



I couldn't have the negative slack be less than 0.15 because when I had it below my width slack goes into negative.

The schematic:



The multiplier timing results:

```
create_clock -period 12 -name clk -waveform {0.000 6} -add [get_ports clk]
```

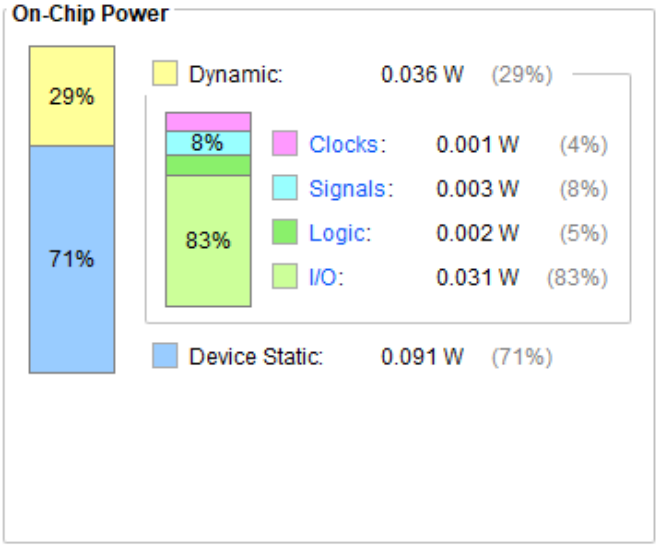
Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	0.017 ns	Worst Hold Slack (WHS):	0.341 ns	Worst Pulse Width Slack (WPWS):	5.500 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	40	Total Number of Endpoints:	40	Total Number of Endpoints:	81

All user specified timing constraints are met.

Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

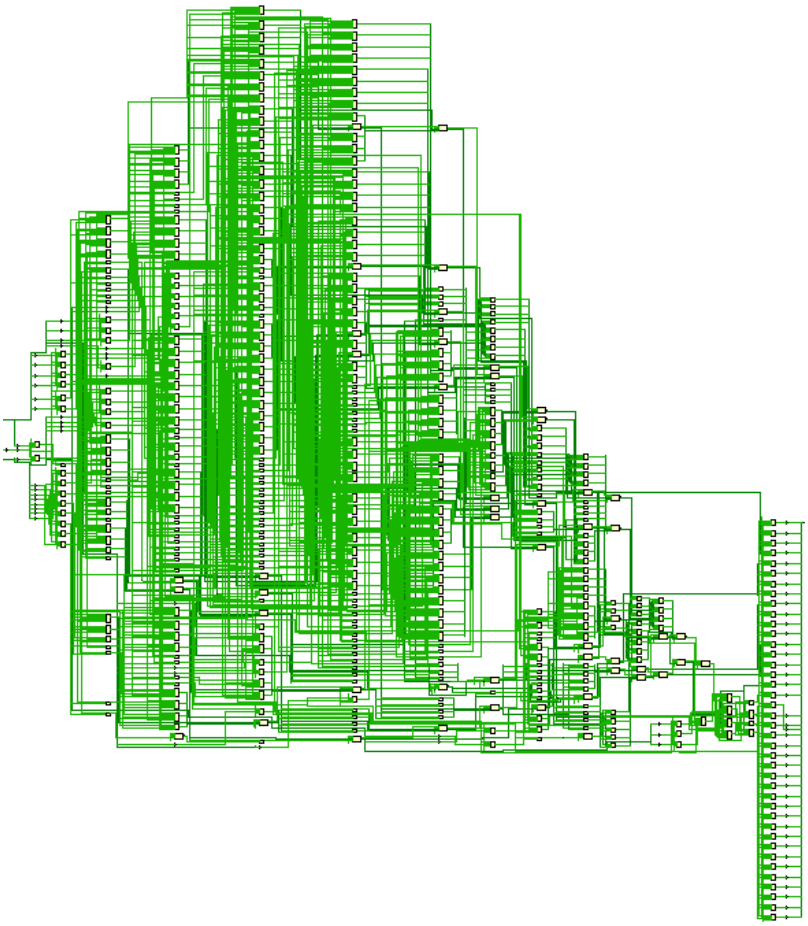
Total On-Chip Power:	**0.128 W**
Design Power Budget:	**Not Specified**
Power Budget Margin:	**N/A**
Junction Temperature:	**25.6°C**
Thermal Margin:	59.4°C (12.9 W)
Effective ϑJA:	4.6°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

Launch Power Constraint Advisor to find and fix invalid switching activity



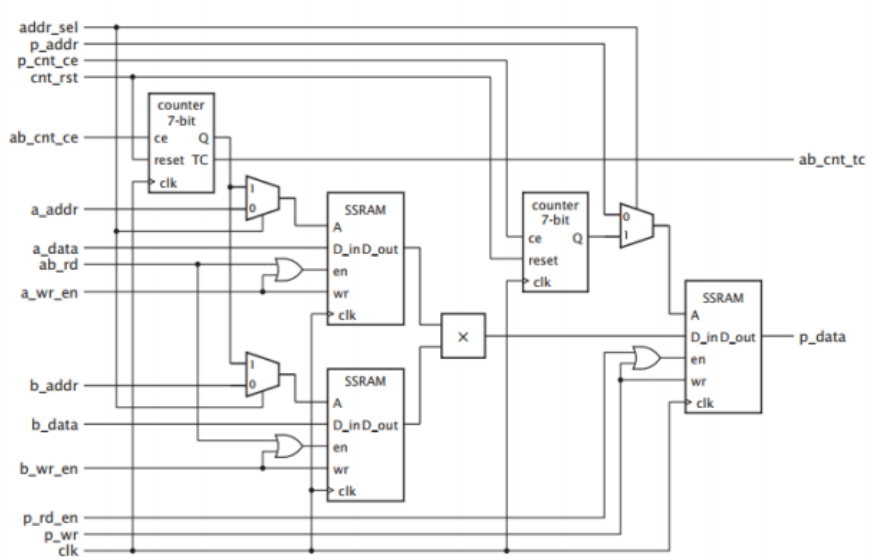
I was able to have the negative slack be less than 0.15.

The schematic:



Problem 2:

Design



state	start	Ab_cn_tc	next	Cnt_rst	Ab_cnt_ce Ab_rd	P_cnt_ce P_wr	done
idle	0	-	idle	1	0	0	0
idle	1	-	Cmp0	0	1	0	0
cmp0	-	-	comp	0	1	1	0
comp	-	0	comp	0	1	1	0
comp	-	1	last	0	1	1	0
last	-	-	Result	0	0	1	0
result	-	-	idle	1	0	0	1

Behavioral Simulations

i. testbench

```
module tb_part2;
//inputs
reg clk,rst, start, a_write_en, b_write_en, p_read_en;
reg [6:0] a_addr, b_addr, p_addr;
reg signed [15:0] a_data, b_data;
integer count = 0;
//fucntion instantiation
part2 test(.clk(clk), .rst(rst), .start(start), .a_write_en(a_write_en), .b_write_en(b_write_en), .p_read_en(p_read_en),
        .a_addr(a_addr), .b_addr(b_addr), .p_addr(p_addr),
        .a_data(a_data), .b_data(b_data),
        .p_data(p_data),
        .done(done));
//clk set up
always#1 clk = !clk;
initial begin
clk = 0;
//reset
rst = 1;
#10
rst = 0;
#5
//Initialize Inputs
start = 1;
a_write_en = 1;
b_write_en = 1;
p_read_en = 1;
a_addr = 0;
b_addr = 0;
p_addr = 0;
a_data = 1;
b_data = 127;
    while(count < 128)begin //change input values
    #10
    a_addr = a_addr + 1;
    b_addr = b_addr + 1;
    p_addr = p_addr + 1;
    a_data = a_data + 1;
    b_data = b_data - 1;
    count = count + 1;
    end
end
endmodule
```

Implementation Results

```
create_clock -period 2.4 -name clk -waveform {0.000 1.2} -add [get_ports clk]
```

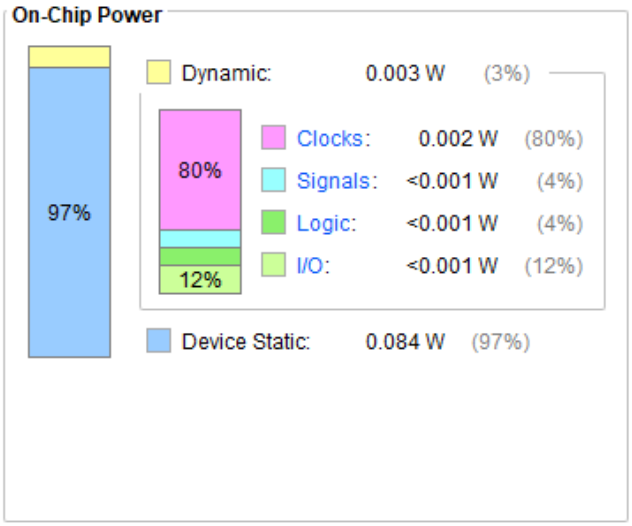
Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	0.022 ns	Worst Hold Slack (WHS):	0.212 ns	Worst Pulse Width Slack (WPWS):	0.245 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	21	Total Number of Endpoints:	21	Total Number of Endpoints:	11

All user specified timing constraints are met.

Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

Total On-Chip Power:	**0.087 W**
Design Power Budget:	**Not Specified**
Power Budget Margin:	**N/A**
Junction Temperature:	**25.4°C**
Thermal Margin:	59.6°C (12.9 W)
Effective ϑJA:	4.6°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Medium

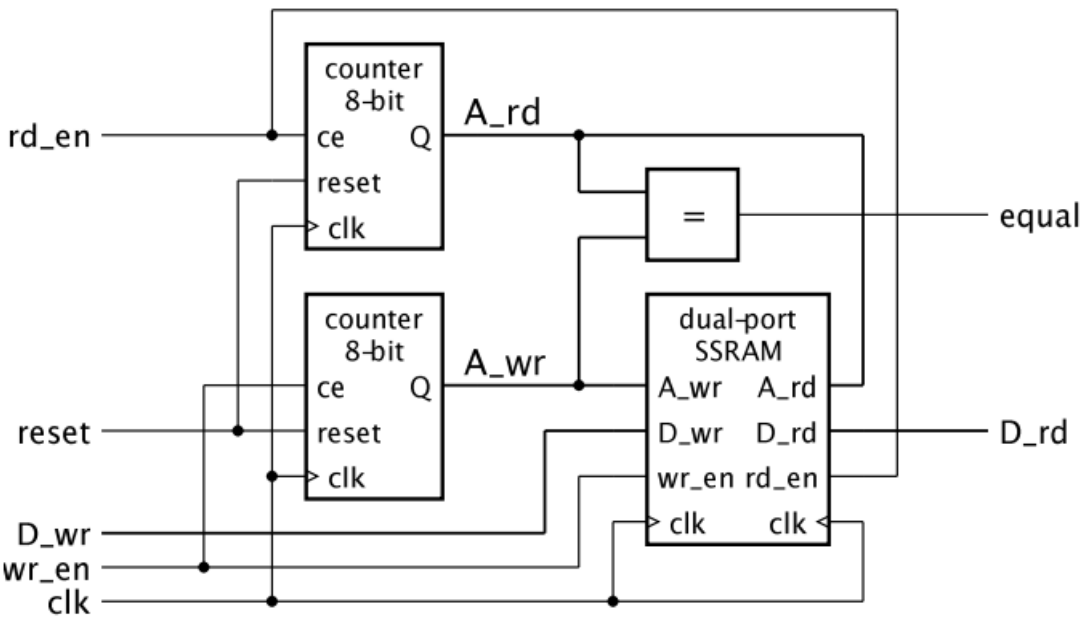
Launch Power Constraint Advisor to find and fix invalid switching activity



Name	Slice LUTs (63400)	Slice Registers (126800)	Slice (15850)	LUT as Logic (63400)	Bonded IOB (210)	BUFGCTRL (32)
part2	14	13	5	14	36	1

Problem 3:

Design



Behavioral Simulations

i. testbench

```
module tb_part3;

reg clk;
reg reset;
reg rd_en;
reg wr_en;
reg [15:0] data_in;


wire full;
wire empty;
wire [15:0] data_out;
integer i,fid_in, fid_out, status;
part3 uut (.clk(clk),.reset(reset),.rd_en(rd_en),.wr_en(wr_en),.full(full),.empty(empty),.data_in(data_in),.data_out(data_out));
always # 10 clk = ~ clk;


initial begin
// Initialize Inputs
clk = 0;
reset = 0;
rd_en = 0;
wr_en = 0;
data_in = 0;

#40;
reset =1;
#90;
reset =0;

for(i=1;i<257;i=i+1)
begin
wr_en=0;
data_in = i;
wr_en=1;
#20;
end
wr_en=0;
#40;
rd_en =1;
#500;
end

endmodule
```

Implementation Results [5pts]

```
create_clock -period 3.5 -name clk -waveform {0.000 1.75} -add [get_ports clk]
```

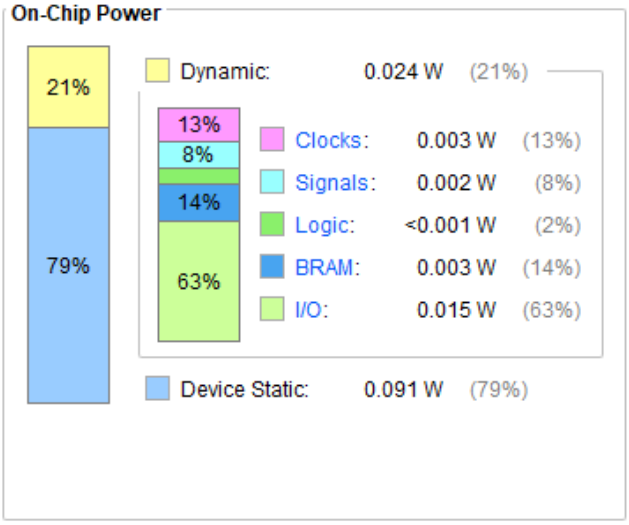
Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	0.021 ns	Worst Hold Slack (WHS):	0.234 ns	Worst Pulse Width Slack (WPWS):	0.556 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	52	Total Number of Endpoints:	52	Total Number of Endpoints:	21

All user specified timing constraints are met.

Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

Total On-Chip Power:	**0.115 W**
Design Power Budget:	**Not Specified**
Power Budget Margin:	**N/A**
Junction Temperature:	**25.5°C**
Thermal Margin:	59.5°C (12.9 W)
Effective ϑJA:	4.6°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

Launch Power Constraint Advisor to find and fix invalid switching activity



Name	Slice LUTs (63400)	Slice Registers (126800)	Slice (15850)	LUT as Logic (63400)	Block RAM Tile (135)	Bonded IOB (210)	BUFGCTRL (32)
N part3	39	18	24	39	0.5	150	1