```
 1: library STD;
 2: library IEEE;
 3: use IEEE.std_logic_1164.all;
 4:
 5: entity mux_4_1 is port(
 6:     a: in std_logic;
 7:     b: in std_logic;
 8:     c: in std_logic;
 9:     d: in std_logic;
10:     sel0: in std_logic;
11:     sel1: in std_logic;
12:     out1: out std_logic);
13: end mux_4_1;
14: architecture structural of mux_4_1 is
15:   component mux_2_1
16:     port(
17:       in1: in std_logic;
18:       in2: in std_logic;
19:       sel: in std_logic;
20:       out1: out std_logic);
21:   end component;
22:   signal mid1, mid2: std_logic;
23: begin
24:   Unit1: mux_2_1 port map(a,b,sel0,mid1);
25:   Unit2: mux_2_1 port map(c,d,sel0,mid2);
26:   Unit3: mux_2_1 port map(mid1,mid2,sel1,out1);
27: end structural;
```