```
 1: library STD;
 2: library IEEE;
 3: use IEEE.std_logic_1164.all;
 4:
 5: entity mux_4_bit is
 6:   port(
 7:     A: in std_logic_vector(3 downto 0);
 8:     B: in std_logic_vector(3 downto 0);
 9:     C: in std_logic_vector(3 downto 0);
10:     D: in std_logic_vector(3 downto 0);
11:     SEL0: in std_logic;
12:     SEL1: in std_logic;
13:     OUT1: out std_logic_vector(3 downto 0));
14: end mux_4_bit;
15:
16: architecture structural of mux_4_bit is
17:   component mux_4_1
18:     port(
19:       a: in std_logic;
20:       b: in std_logic;
21:       c: in std_logic;
22:       d: in std_logic;
23:       sel0: in std_logic;
24:       sel1: in std_logic;
25:       out1: out std_logic);
26:   end component;
27: begin
28:   Unit1: mux_4_1 port map (A(0),B(0),C(0),D(0),SEL0,SEL1,OUT1(0));
29:   Unit2: mux_4_1 port map (A(1),B(1),C(1),D(1),SEL0,SEL1,OUT1(1));
30:   Unit3: mux_4_1 port map (A(2),B(2),C(2),D(2),SEL0,SEL1,OUT1(2));
31:   Unit4: mux_4_1 port map (A(3),B(3),C(3),D(3),SEL0,SEL1,OUT1(3));
32: end structural;
33:
34:
35:
36:
37:
38:
```