CMPE 315: Principles of VLSI Design
Lab Cover Page

Lab # : **3**
Lab Title : **Layout, Extraction and Simulations**

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Section : **1**

Date Submitted : **10/06/2021**

TA / Grader Use Only:

Late Submission Deduction (20% per day late):

Other Deductions:

Final Lab Grade:

Comments to student:

Table of Contents

1. Lab Procedure:

a. Schematics and Layouts

This lab is a continuation of the previous lab where were designed the schematics for the INVx1, NOR2x1, and NAND2x1 gates. We ran simulations for those schematics with different number of load inverters. In this lab we created layout views for those gates and a OAI and AOI layouts with schematics views for those layouts using the gates created from the previous lab. To create the layouts, you would first have to add a layout view to each cell. Form there you would first have to create the nPOS and pMOS components using the cc, nselect, pselect, nactive, pactive, nwell layers. You would then connect those pieces using poly and metal path layers between the ccs. Finally, you would add pins to the output and the input path of the layout. This is done for the INVx1, NOR2x1, and NAND2x1 layouts. To make sure there are no errors in the layout you would run a DRC. If the DRC output shows no errors, then you can procced to extracting the layout which basically creates an actual circuit netlist from the layout. The AOI and OAI layouts are created using the layouts for the INVx1, NAND2x1, and NOR2x1. After setting up all the copies of the layouts for those gates you must flatten them and delete all the pins. This is because pins cannot be used to connect wires between pieces of the layout, and are only used for inputs, outputs, vdd, and gnd. To make connections between pieces of the layout you would need to create vias that connect from one layer to another. The vias that are used for this lab are the ‘M1_POLY’ via which connected a poly layer and metal1 layer using a path of either layer and the ‘M1_M2’ via which connected a metal1 layer with a metal2 layer using a path of either layer. The ‘M1_POLY’ via is mainly used to connect outputs of a gate layout which used the metal1 layer to the inputs of another gate which used the poly layer. The ‘M1_M2’ gate was used when there was a connection in the layout that required metal1 layers to cross but that is not allowed. Instead, you would use a metal2 path to cross over the metal1 path and use the ‘M1_M2’ via to connect it back to a metal1 path. After making all the path connections, you would create vdd and gnd pins that are connected to each gate layout using the metal1 and metal2 paths as needed. Finally, you create an input and output pins for the layout, and DRC the layout to make sure it has no errors. After running the DRC, you would extract the layout to have your extracted view. The schematic view for the AOI and OAI cells were created using the schematic views of the INVx1, NAND2x1, and NOR2x1 gates and connecting them using wires. Finally, input and output pins are added to complete the schematics.

b. Simulations

There are a total of seven simulation schematics for this lab. The first three simulation schematics were the INVx1, NAND2x1, and NOR2x1 extracted views with four INVx1 loads. The final four were the AOI and OAI cells connected to four INVx1 loads where the first two used the schematic view of each cell and the second two used the extracted view of each cell.

2. Schematics, Layouts, and Simulation Plots

a. INVx1 layout and simulation

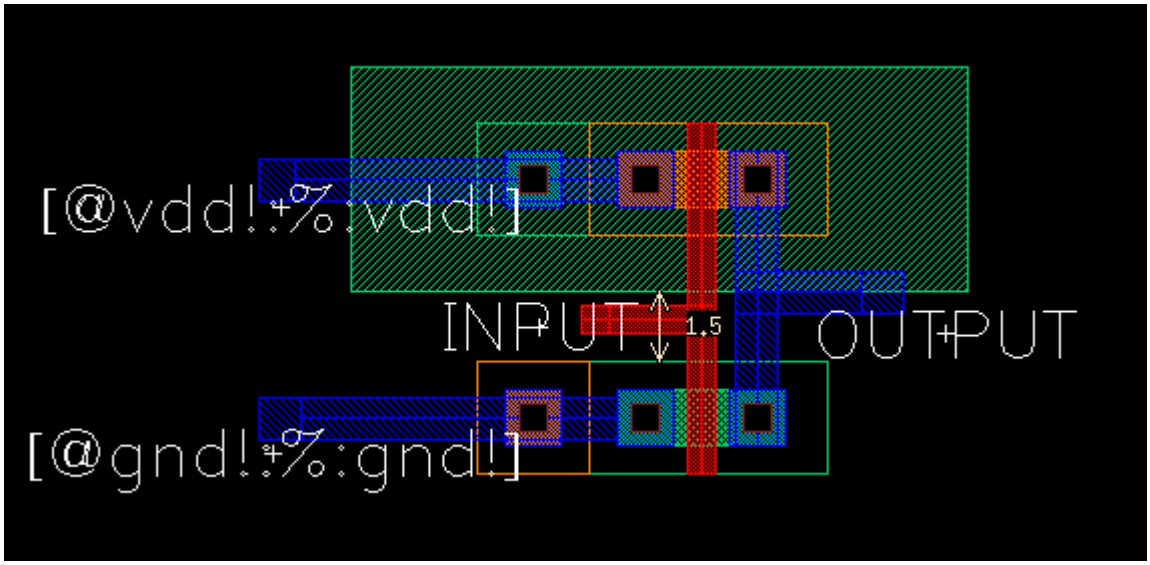

Figure 1: INVx1 cell layout

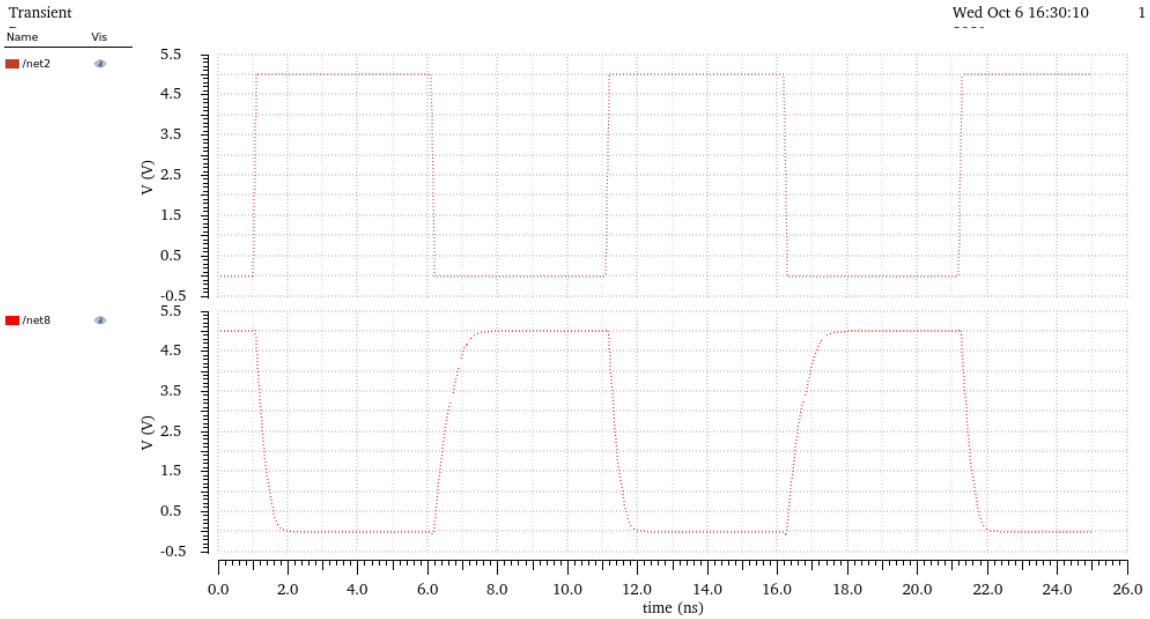

Figure 2: INVx1 with 4 load inverters simulation plot using extracted view

b. NOR2x1 layout and simulation

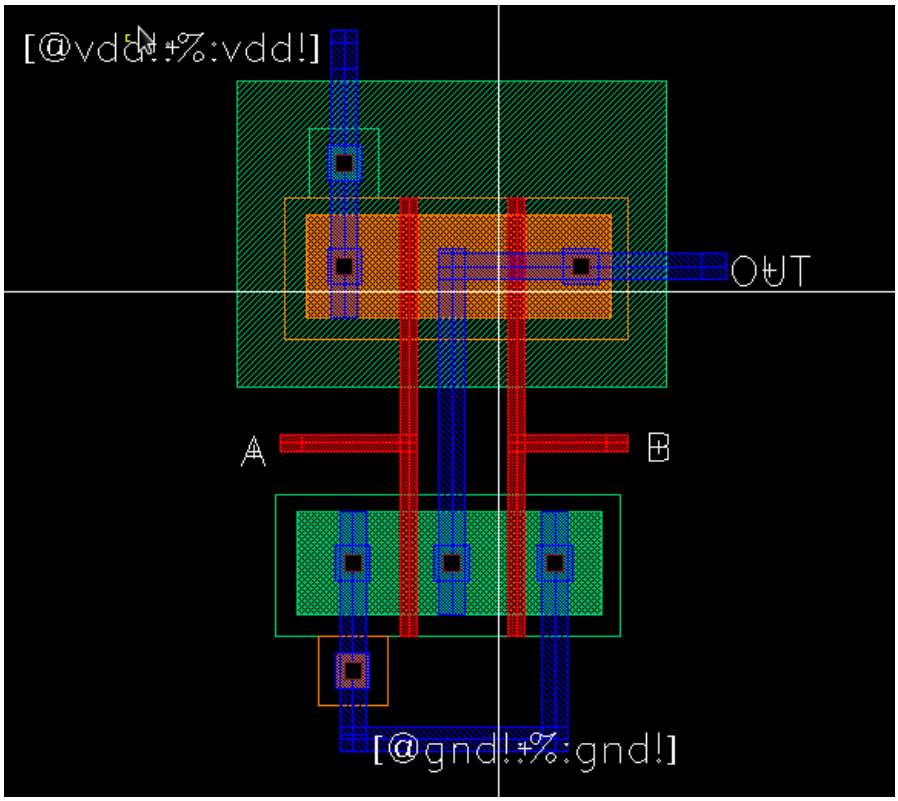

Figure 3: NOR2x1 layout

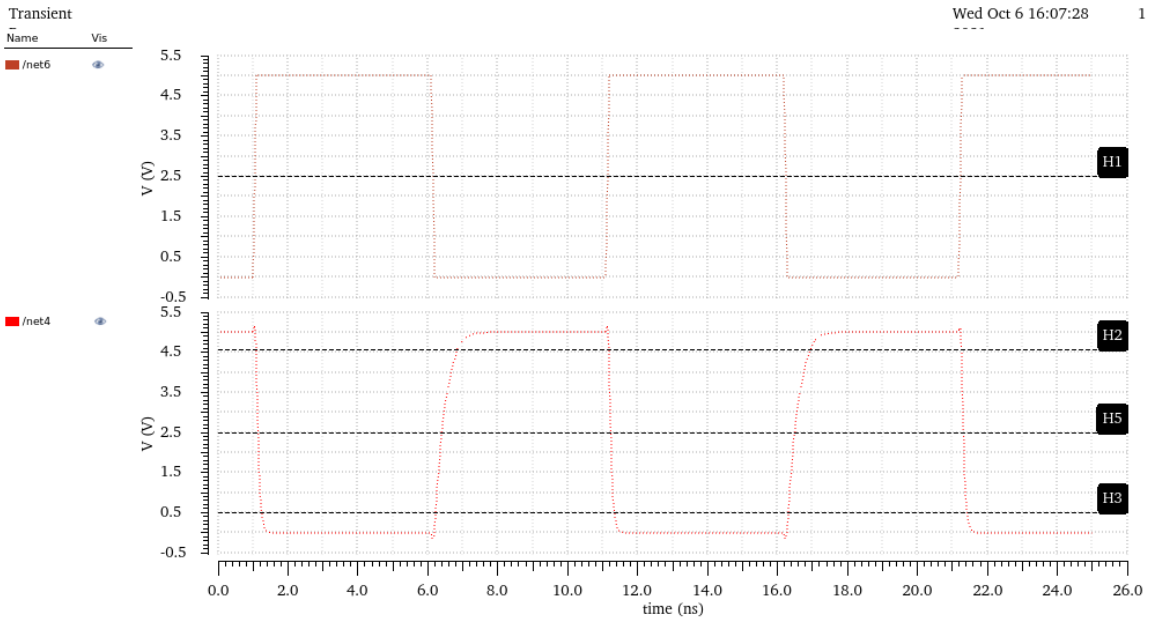

Figure 4: NOR2x1 with 4 load inverters simulation plot using extracted view

c. NAND2x1 layout and simulation

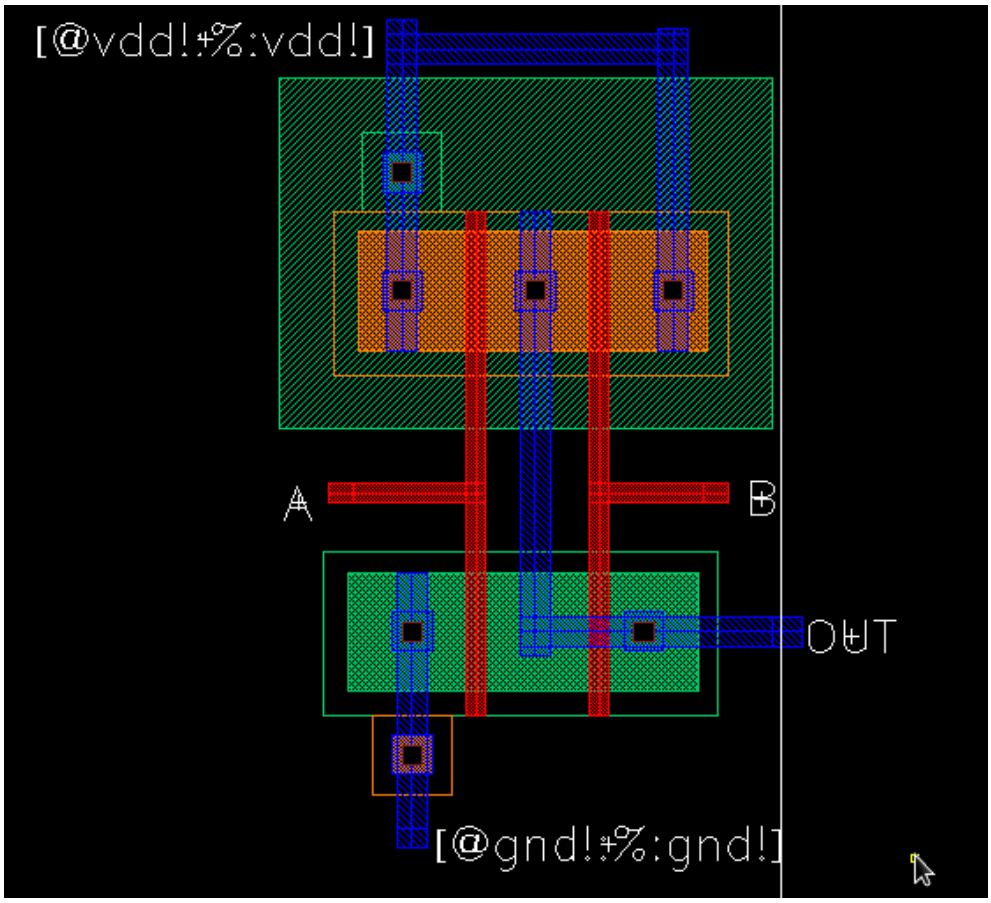

Figure 5: NAND2x1 layout

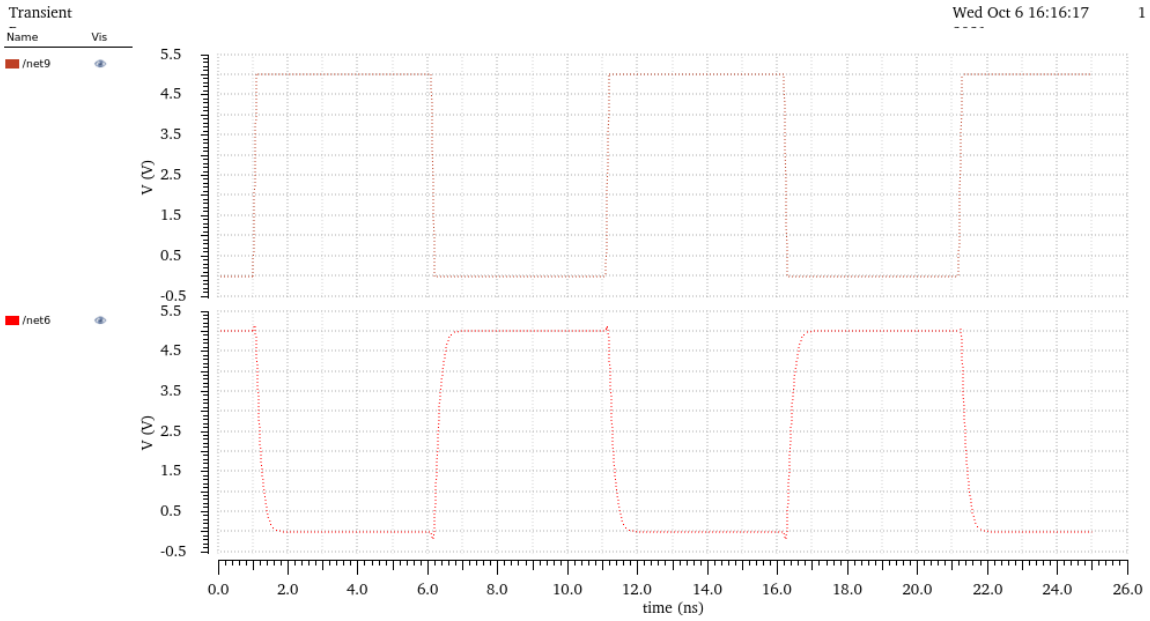

Figure 6: NAND2x1 with 4 load inverters simulation plot using extracted view

d. OAI layout and simulation

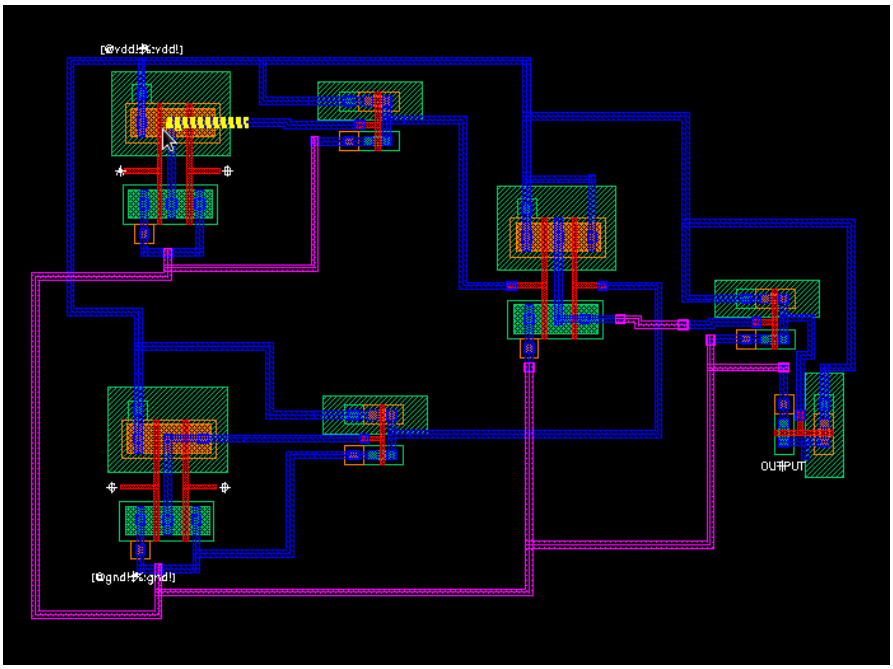

Figure 7: OAI layout

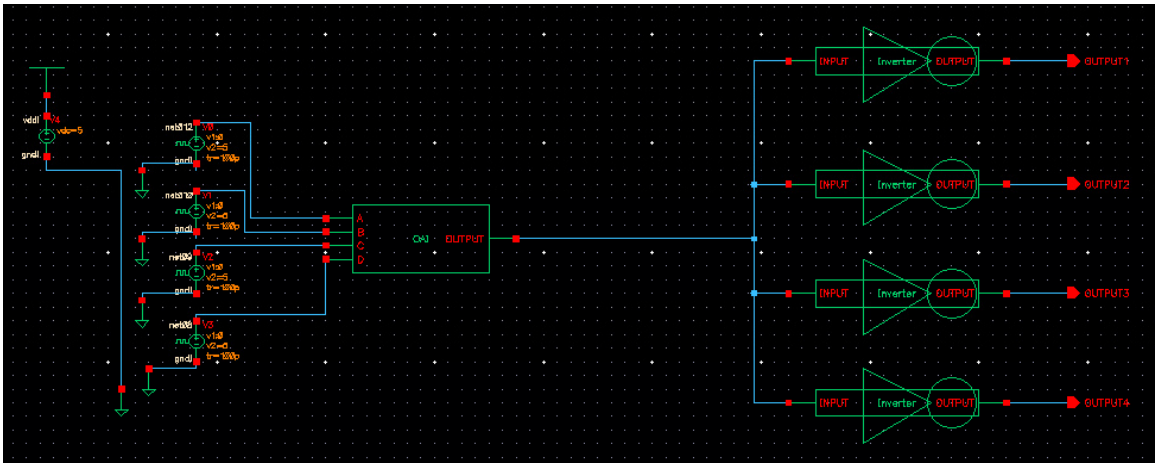

Figure 8: OAI Simulation schematic using extracted view

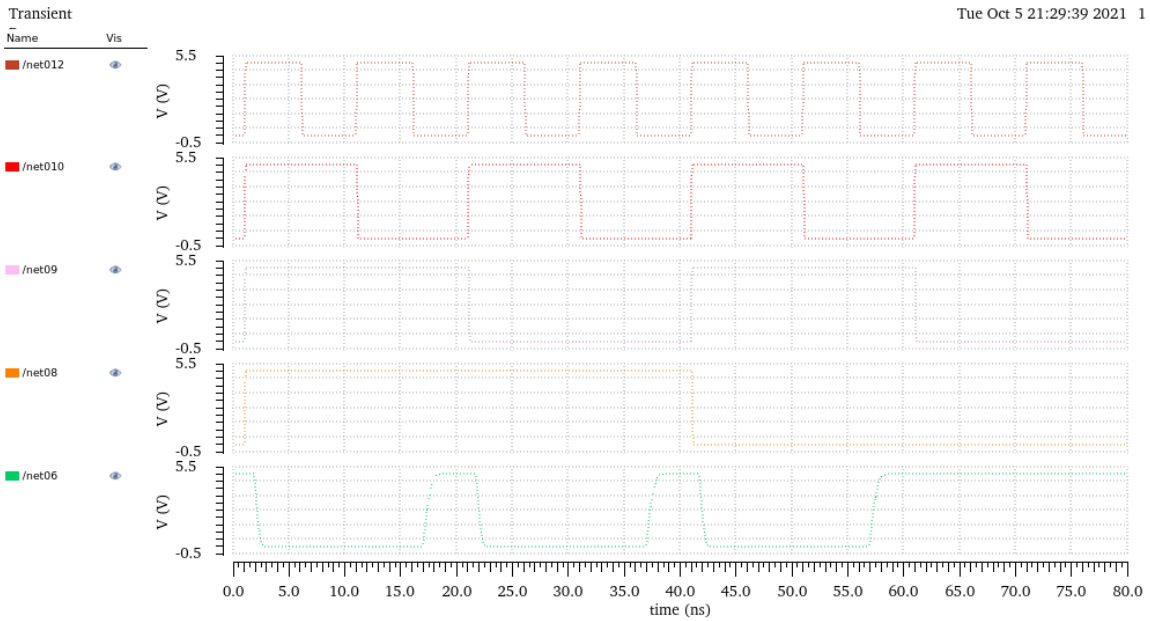

Figure 9: OAI simulation plot using extracted view

e. OAI schematic and simulation

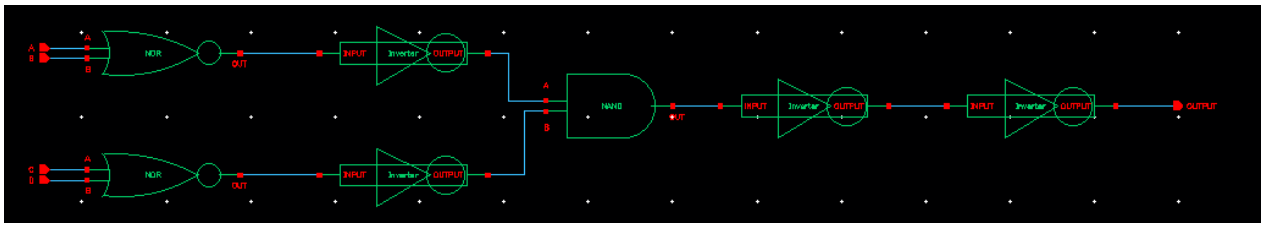

Figure 10: OAI Schematic

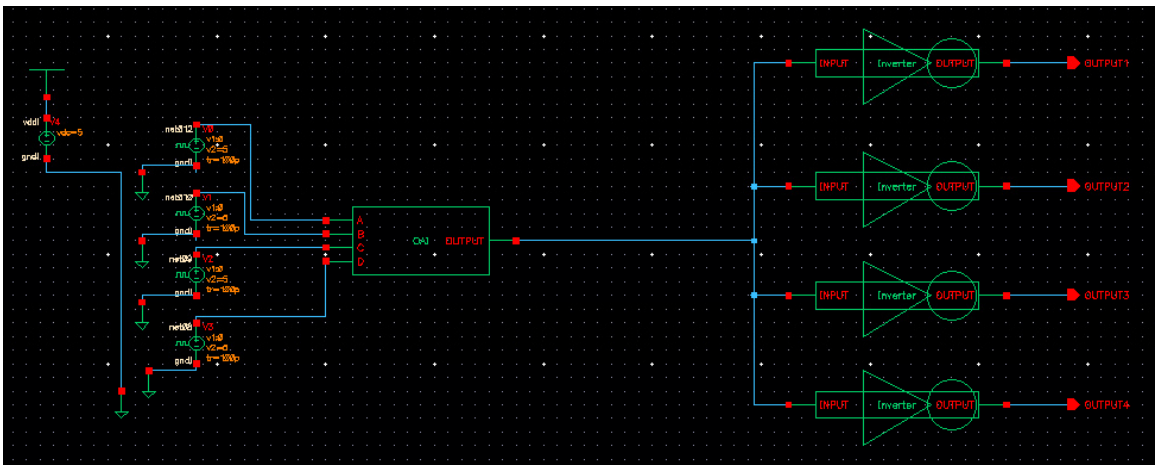

Figure 11: OAI simulation schematic using schematic view

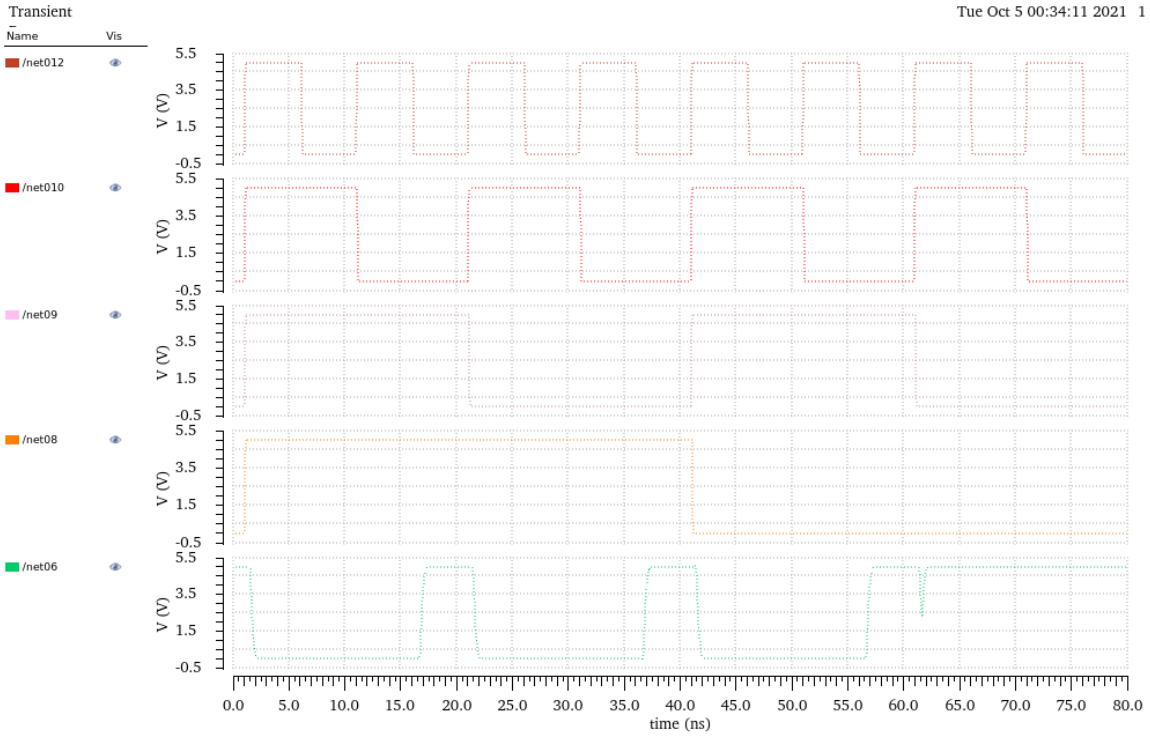

Figure 12: OAI simulation plot using schematic view

f. AOI layout and simulation

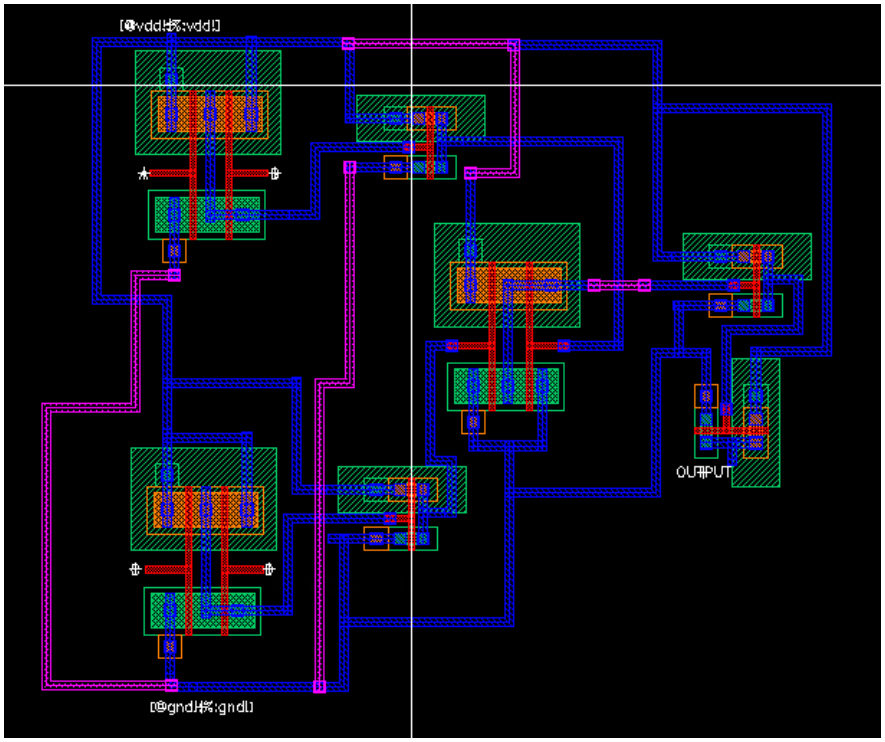

Figure 13: AOI layout

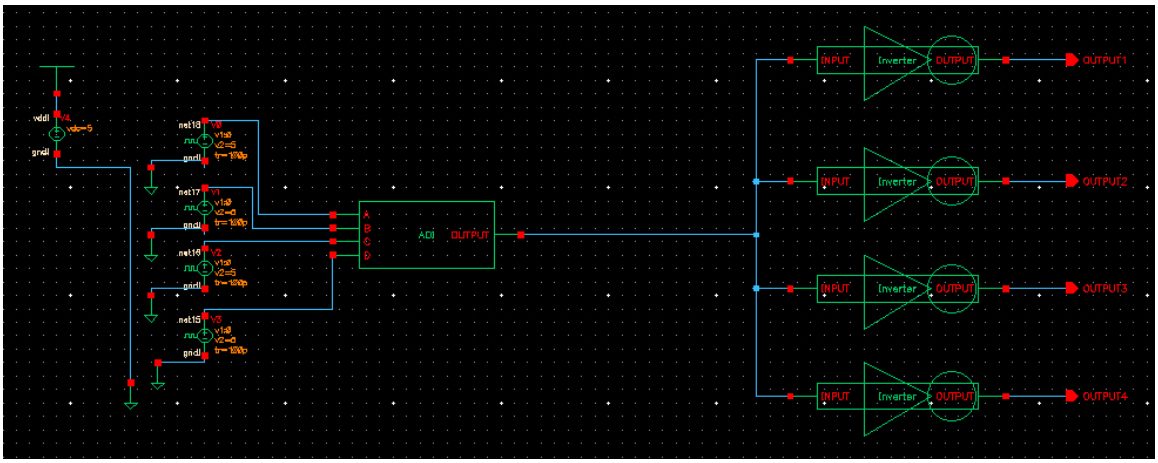

Figure 14: AOI simulation schematic using extracted view

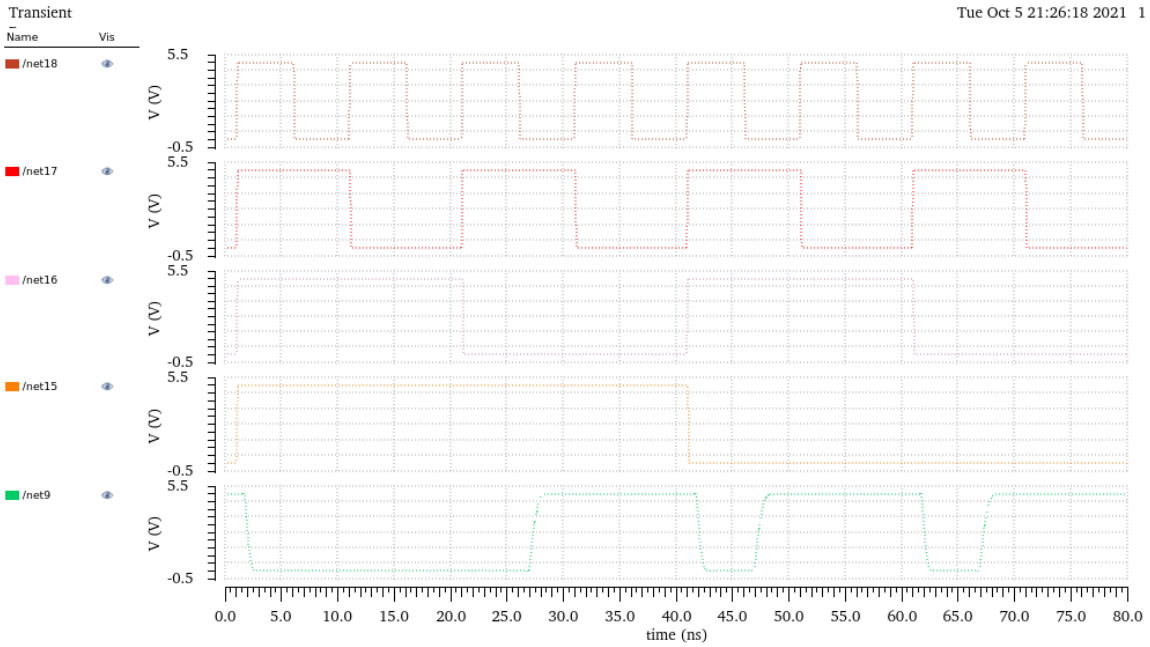

Figure 15: AOI simulation plot using extracted view

g. AOI schematic and simulation

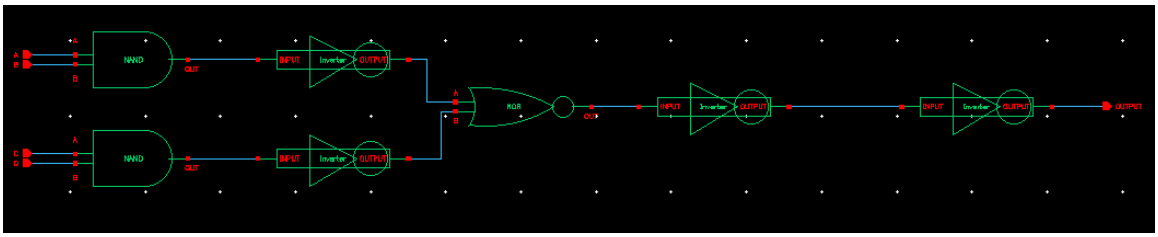

Figure 16: AOI schematic

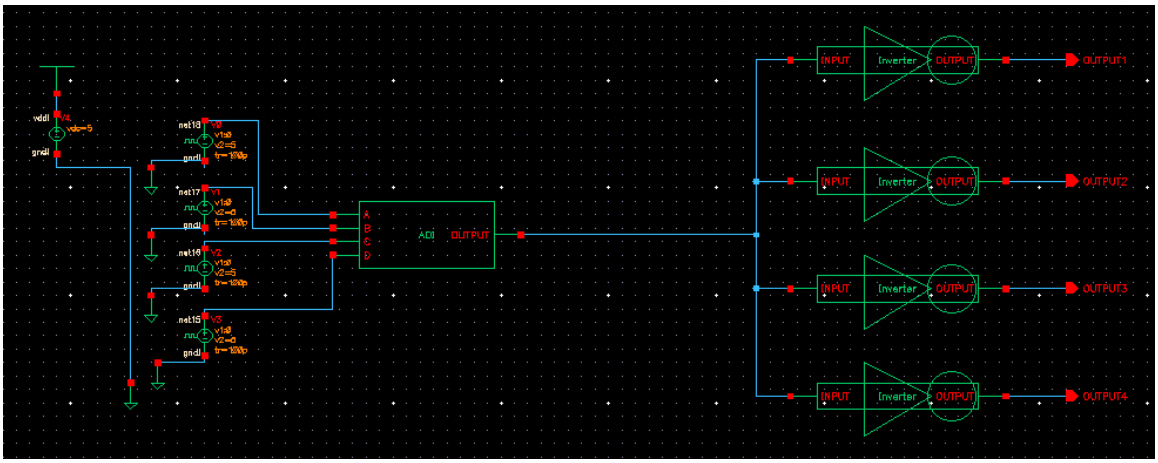

Figure 17: AOI simulation schematic using schematic view

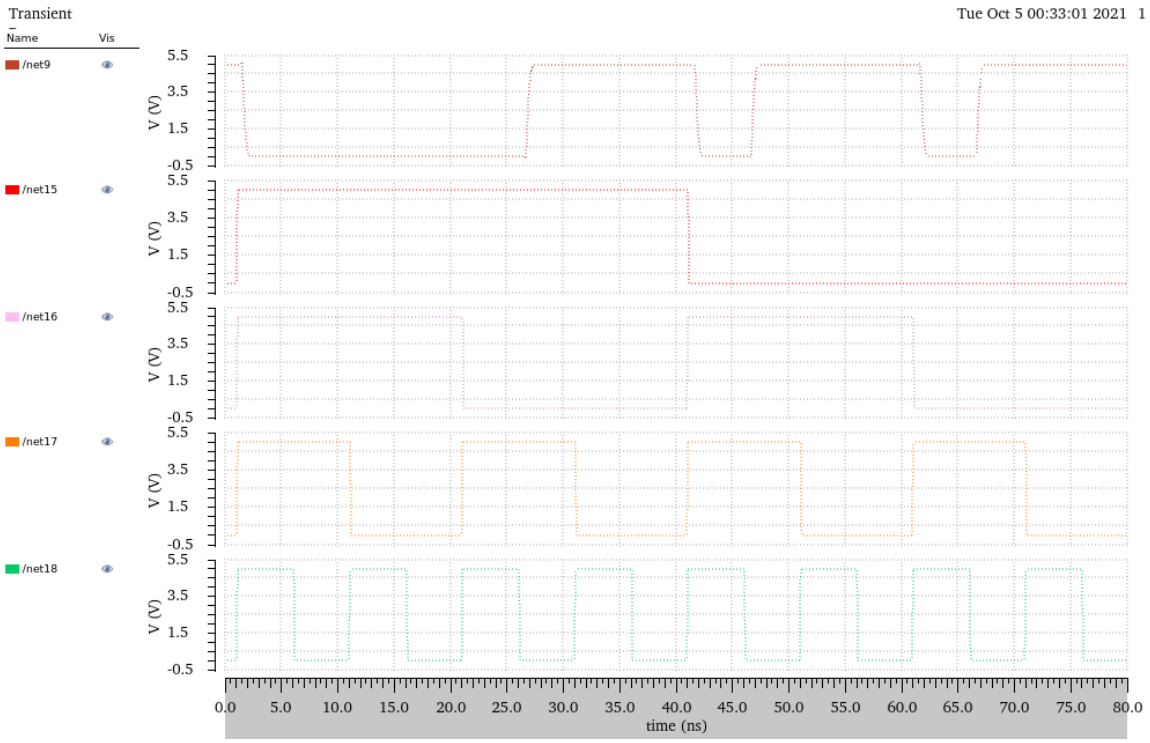

Figure 18: AOI simulation plot using schematic view

3. Fall-Time and Rise-Time Tables

a. Fall-Time table

Gate	fall 4.5	fall .5	**fall**
NOR2x1 layout	1.08455	1.24736	**0.16281**
NAND2x1 layout	1.09859	1.40235	**0.30376**
INVx1 layout	1.10915	1.5812	**0.47205**
AOI layout	1.79096	2.31833	**0.52737**
OAI layout	1.93767	2.4605	**0.52283**
AOI schematic	1.56882	1.94151	**0.37269**
OAI schematic	1.54965	1.92424	**0.37459**

b. Rise-Time table

Gate	rise 4.5	rise .5	**rise**
NOR2x1 layout	6.84614	6.22689	**0.61925**
NAND2x1 layout	6.51289	6.20886	**0.30403**
INVx1 layout	7.02705	6.23469	**0.79236**
AOI layout	27.8817	27.0786	**0.8031**
OAI layout	17.884	17.0847	**0.7993**
AOI schematic	27.1358	26.7562	**0.3796**
OAI schematic	17.1423	16.7638	**0.3785**

c. Fall-Time Delay table

Gate	rise- out	fall- in	**delay fall**
NOR2x1 layout	6.40628	6.15	**0.25628**
NAND2x1 layout	6.3003	6.15	**0.1503**
INVx1 layout	6.49623	6.15	**0.34623**

d. Rise-Time Delay table

Gate	fall- out	rise- in	**delay rise**
NOR2x1 layout	1.14083	1.05	**0.09083**
NAND2x1 layout	1.187	1.05	**0.137**
INVx1 layout	1.27076	1.05	**0.22076**