1-bit 2 to 1 Mux

mux_2_1.vhdl


```
 1: library STD;
 2: library IEEE;
 3: use IEEE.std_logic_1164.all;
 4:
 5: entity mux_2_1 is port (
 6:   in1: in std_logic;
 7:   in2: in std_logic;
 8:   sel: in std_logic;
 9:   out1: out std_logic);
10: end mux_2_1;
11: architecture structural of mux_2_1 is
12:
13: begin
14:
15: out1 <= (in1 and (not sel)) or (in2 and sel);
16:
17: end structural;
```