```
    1: --
    2: -- Entity: xor2
    3: -- Architecture : structural
    4: -- Author: cpatel2
    5: -- Created On: 11/11/2003
    6: --
    7: library STD;
    8: library IEEE;
    9: use IEEE.std_logic_1164.all;
   10:
   11: entity xor2 is
   12:
   13:   port (
   14:     input1   : in  std_logic;
   15:     input2   : in  std_logic;
   16:     output   : out std_logic);
   17: end xor2;
   18:
   19: architecture structural of xor2 is
   20:
   21: begin
   22:
   23:   output <= input2 xor input1;
   24:
   25: end structural;
   26:
   27:
   28: --------------------------------------------------------------------------------
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   29:
   30: --
   31: -- Entity: and2
   32: -- Architecture : structural
   33: -- Author: cpatel2
   34: -- Created On: 11/11/2003
   35: --
   36: library STD;
   37: library IEEE;
   38: use IEEE.std_logic_1164.all;
   39:
   40: entity and2 is
   41:
   42:   port (
   43:     input1   : in  std_logic;
   44:     input2   : in  std_logic;
   45:     output   : out std_logic);
   46: end and2;
   47:
   48: architecture structural of and2 is
   49:
   50: begin
   51:
   52:   output <= input2 and input1;
   53:
   54: end structural;
   55:
   56: --------------------------------------------------------------------------------
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   57:
   58: --
   59: -- Entity: or3
   60: -- Architecture : structural
   61: -- Author: cpatel2
   62: -- Created On: 11/11/2003
   63: --
   64: library STD;
   65: library IEEE;
   66: use IEEE.std_logic_1164.all;
   67:
   68: entity or3 is
   69:
   70:   port (
   71:     input1   : in  std_logic;
   72:     input2   : in  std_logic;
   73:     input3   : in  std_logic;
   74:     output   : out std_logic);
   75: end or3;
   76:
   77: architecture structural of or3 is
   78:
   79: begin
   80:
   81:   output <= input3 or input2 or input1;
   82:
   83: end structural;
   84:
   85:
   86: --------------------------------------------------------------------------------
---------------
   87:
   88: --
   89: -- Entity: adder1
   90: -- Architecture : structural
   91: -- Author: cpatel2
   92: -- Created On: 10/21/2004
   93: --
   94: library STD;
   95: library IEEE;
   96: use IEEE.std_logic_1164.all;
   97:
   98: entity adder1 is
   99:
  100:   port (
  101:     input1   : in  std_logic;
  102:     input2   : in  std_logic;
  103:     carryin  : in  std_logic;
  104:     sum      : out std_logic;
  105:     carryout : out std_logic);
  106: end adder1;
  107:
  108: architecture structural of adder1 is
  109:
  110: component xor2
  111:   port (
  112:     input1   : in  std_logic;
  113:     input2   : in  std_logic;
  114:     output   : out std_logic);
  115: end component;
  116:
  117: component and2
  118:   port (
  119:     input1   : in  std_logic;
  120:     input2   : in  std_logic;
  121:     output   : out std_logic);
```

```
  122: end component;
  123:
  124: component or3
  125:   port (
  126:     input1   : in  std_logic;
  127:     input2   : in  std_logic;
  128:     input3   : in  std_logic;
  129:     output   : out std_logic);
  130: end component;
  131:
  132:
  133: for xor2_1, xor2_2: xor2 use entity work.xor2(structural);
  134: for and2_1, and2_2, and2_3: and2 use entity work.and2(structural);
  135: for or3_1: or3 use entity work.or3(structural);
  136:
  137: signal temp1, temp2, temp3, temp4: std_logic;
  138:
  139: begin
  140:
  141: xor2_1: xor2 port map (input1, input2, temp1);
  142: xor2_2: xor2 port map (carryin, temp1, sum);
  143:
  144: and2_1: and2 port map (input1, input2, temp2);
  145: and2_2: and2 port map (input1, carryin, temp3);
  146: and2_3: and2 port map (input2, carryin, temp4);
  147:
  148: or3_1: or3 port map (temp2, temp3, temp4, carryout);
  149:
  150: end structural;
  151:
  152: --------------------------------------------------------------------------
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  153:
  154: --
  155: -- Entity: adder4
  156: -- Architecture : structural
  157: -- Author: cpatel2
  158: -- Created On: 10/21/2004
  159: --
  160: library STD;
  161: library IEEE;
  162: use IEEE.std_logic_1164.all;
  163:
  164: entity adder4 is
  165:
  166:   port (
  167:     input1   : in  std_logic_vector(3 downto 0);
  168:     input2   : in  std_logic_vector(3 downto 0);
  169:     carryin  : in  std_logic;
  170:     sum      : out std_logic_vector(3 downto 0);
  171:     carryout : out std_logic);
  172: end adder4;
  173:
  174: architecture structural of adder4 is
  175:
  176: component adder1
  177:   port (
  178:     input1   : in  std_logic;
  179:     input2   : in  std_logic;
  180:     carryin  : in  std_logic;
  181:     sum      : out std_logic;
  182:     carryout : out std_logic);
  183: end component;
  184:
  185: for adder1_1, adder1_2, adder1_3, adder1_4: adder1 use entity work.adder1(stru
ctural);
  186:
  187: signal ctemp: std_logic_vector(2 downto 0);
  188:
  189: begin
  190:
  191: adder1_1: adder1 port map (input1(0), input2(0), carryin, sum(0), ctemp(0));
  192: adder1_2: adder1 port map (input1(1), input2(1), ctemp(0), sum(1), ctemp(1));
  193: adder1_3: adder1 port map (input1(2), input2(2), ctemp(1), sum(2), ctemp(2));
  194: adder1_4: adder1 port map (input1(3), input2(3), ctemp(2), sum(3), carryout);
  195: end structural;
  196:
```