```
 1: --
 2: -- Entity: inverter
 3: -- Architecture : structural
 4: -- Author: cpatel2
 5: -- Created On: 10/20/00 at 13:32
 6: --
 7: library STD;
 8: library IEEE;
 9: use IEEE.std_logic_1164.all;
10:
11: entity inverter is
12:
13:   port (
14:     input    : in  std_logic;
15:     output   : out std_logic);
16: end inverter;
17:
18: architecture structural of inverter is
19:
20: begin
21:
22:   output <= not (input);
23:
24: end structural;
25:
26:
27:
28:
29:
30:
31:
32:
33:
34:
35:
36:
37:
```