AP-621

APPLICATION NOTE

Interfacing the MCS® 96 Microcontroller Family with Intel Flash

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1.0 INTRODUCTION

The popularity of the MCS® 96 microcontroller family has grown steadily because of its power and flexibility. The trend continues because this microcontroller family meets the needs of a wide range of computing applications. Some of the applications where the MCS 96 microcontrollers may be found include disk drives, modems, motor control systems, photocopiers, automobile anti-lock brakes, and medical instrumentation. The power of this family lies in the 16-bit architecture, up to 1 KB of on-chip RAM, A/D converters, serial I/O port, and interrupt handling mechanisms. Furthermore, the diversity in this family of controllers continues to grow with lower power and faster versions planned.

Intel Flash meets the memory needs of many 196 applications. Flash offers many advantages over other types of memory including lower power consumption, in-system updateability, and nonvolatility, allowing data retention when power is removed from the device. Not only can a flash solution reduce the cost of a system, but also reduce design time, required board space and, ultimately, improve time-to-market.

The unique characteristics of the MCS 96 microcontroller family and Intel's Flash memory devices represent a powerful solution for many applications when combined. The purpose of this application note is to outline a straightforward method to interface flash memory with a MCS 96 microcontroller. To accomplish this, the 8XC196NP will be examined. Although the timing and specifications for other controllers in the MCS 96 microcontroller family differ, the same principles and analysis may be used.

This application note will start with a brief discussion of the 8XC196NP and Intel's 28F200BX, a high-integration boot block product. Next, the key bus timings for read and write operations will be examined. With this background, the interfacing of flash in both a multiplexed and demultiplexed bus scheme will be explained.

2.0 MCS® 96 MICROCONTROLLER FAMILY

- The 8XC196NP offers both multiplexed and demultiplexed bus
- The 8XC196NP also has 32 I/O lines which multiplex with chip selects and the serial port

There are several varieties of the 196 available. These powerful microcontrollers meet the needs of a wide range of applications, but several of the 196 controllers were designed with a particular market in mind. For example, the 8XC196MCs meets the needs of motor control applications, while the 196KN series tailors to the needs of the automotive industry. The 196KC/KD and 8XC196NP/NU were designed as all-purpose microcontrollers which could be used in a diverse range of applications.

2.1 The 8XC196NP

The 8XC196NP is a powerful and widely-used general purpose microcontroller. With low power versions and various internal memory schemes available, the needs of many applications can be met.

2.1.1 MEMORY AND BUS

The 8XC196NP operates in either an 8- or 16-bit bus width mode. In addition to the bus width flexibility, the 8XC196NP allows direct external addresses up to 1 MB and internal access of on-chip memory. The device comes with an optional 4 KB of on-chip ROM.

New features on the 8XC196NP allow memory to interface with the controller directly. In demultiplexed bus mode, designs may now utilize the 196NP's dedicated address pins to address bus components directly. Alternatively, designs which rely on a multiplexed bus, may synchronize bus activity through the use of Address Latch Enable (ALE).

2.1.2 INPUT AND OUTPUT

Applications can benefit from the 32 I/O port pins available in the 8XC196NP. These I/O ports multiplex with the serial UART, chip selects high-speed I/O event processor, and pulse width modulators.

3.0 INTEL'S FLASH MEMORY

- Flash may be updated in-system
- Flash offers a fast, high-density, low-power, and low-cost solution to many memory requirements

Intel Flash memory offers many advantages over other types of memory and has the potential to satisfy many types of memory requirements. Figure 1 shows how flash embodies the best features of several frequently implemented memory schemes.

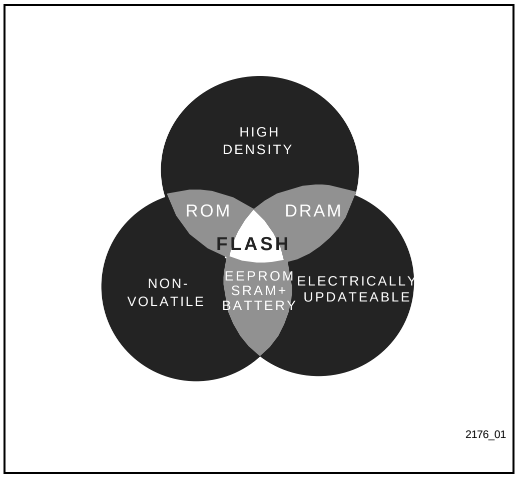


Figure 1. Flash Features the Benefits of Other Popular Types of Memory Schemes

3.1 Updateable Memory

As a nonvolatile form of memory, flash retains data without the need for a constant supply voltage. Once data has been written to flash, power may be removed without risk of data loss. Conventional systems often rely on battery back-ups or slower forms of memory to maintain data, thus increasing cost of system components and design time. Unlike EPROM, flash may be erased electrically and updated in-system. While ROM offers another method for retaining data when power is removed, updating ROM involves a costly process, since it cannot be updated electrically. Flash, on the other hand, allows in-system updates.

3.2 Fast Access, Low Cost, and Density

Flash access times and cost-per-megabit continue to decrease. This trend is related to the lower cost of flash's one transistor memory cell directly. Furthermore, the one transistor cell allows greater densities as well.

3.3 Power Consumption

SmartVoltage flash components provide 2.7V–3.6V, 3.3V ± 0.3V, or 5V read operation and 5V write operations. Furthermore, by connecting the power-down pin to the microcontroller, flash will enter power-down mode along with the controller. Deep power-down mode requires only 0.2 µA of current, typically. The device will also enter a low-power mode, called standby mode, whenever the device is not being accessed—typically drawing only 30 µA of current. Power may also be removed from the V_{PP} pin entirely, thus reducing battery load.

4.0 SUMMARY

The Intel 8XC196NP and Intel's Flash memory provide a dynamic low-power, low-cost solution for many applications. Flash's nonvolatile design allows code and data storage in the same device, while reducing the number of required components in the system.

5.0 THE 8XC196NP/FLASH MEMORY INTERFACE

Many factors must be considered when interfacing memory to a microcontroller. The physical connections and timing of the bus depend on the memory interface scheme.

One of two bus interfacing schemes may be used on the 80C196NP: the multiplexed or demultiplexed bus. In multiplexed mode, address and data signals share the same bus. As shown in Figure 2, at the beginning of the bus cycle the address must be latched by memory. After the address is removed from the bus, data may then be exchanged.

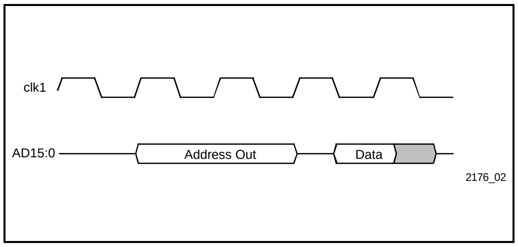


Figure 2. In a Multiplexed Bus, Data Is Exchanged across the Same Pins as the Address

In demultiplexed mode, address and data have dedicated pins. Thus, as shown in Figure 3, data may be exchanged prior to the removal of the address from the bus. By using the demultiplexed bus interface, data exchange can be achieved faster, with fewer "glue-logic" components.

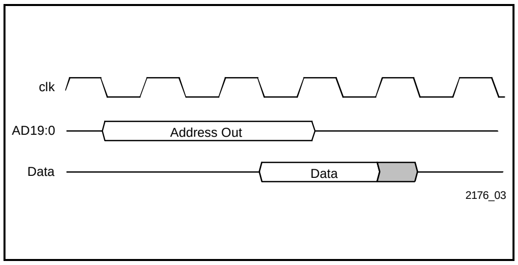


Figure 3. The Address and Data May be Exchanged Simultaneously on a Demultiplexed Bus

To select the desired bus configuration, program the BUSCONx register. As shown in Figure 4, BUSCONx.7 sets the bus mode. When BUSCONx.7 is set to 1, the 8XC196NP operates in demultiplexed mode; if BUSCONx.7 is cleared to 0, the chip operates in multiplexed mode. The BUSCONx register also controls wait-states and bus width.

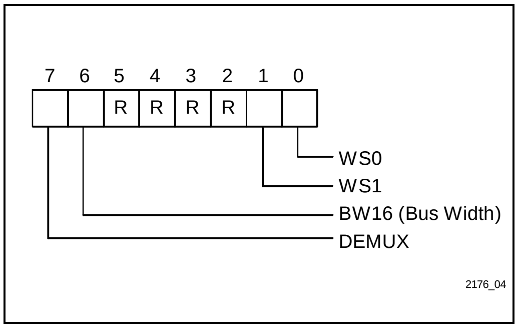


Figure 4. Program the BUSCONx Register to Set Demultiplexed Mode, Bus Width, and the Number of Wait-States

5.1 The Demultiplexed Bus

On a demultiplexed bus the 8XC196NP control signals directly interface with flash memory. Figure 5 shows the mapping structure and corresponding names for control signals from the 8XC196NP to flash.

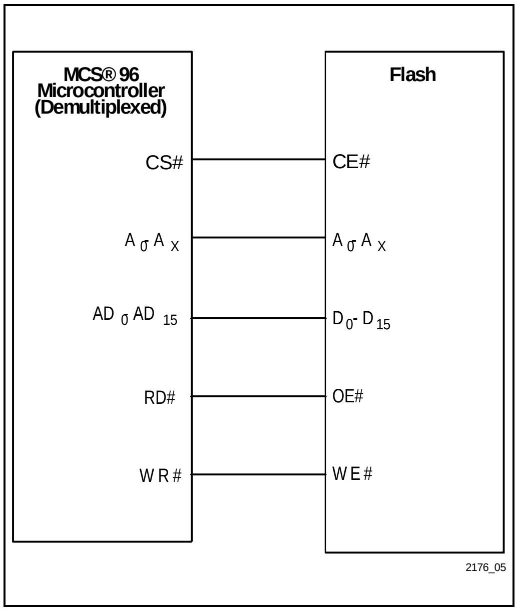


Figure 5. The 8XC196NP's Demultiplexed Bus Signals Correspond to Flash Directly

5.1.1 THE ZERO WAIT-STATE READ CYCLE

The 80C196NP demultiplexed read cycle begins with chip select and ends after the latching of valid data into the 80C196NP. Several specifications should be examined to ensure that signal timings are met. Table 1 lists four of the critical specifications which must be met by the flash device and the corresponding 196 specifications. For purposes of demonstration, a comparison of a 80C196NP, running at 3V and 14 MHz, and a 28F200BV-80 (V_{CC} = 3.3V, extended temperature) will be examined. Use similar analysis for other 196 controllers and flash devices.

Since each of the key specifications are met for these two devices, zero wait-state read operation is guaranteed. Interfacing between these two devices does not require any glue logic. Figure 6 shows the timing diagram of the 80C196NP demultiplexed bus for a data read.

Table 1. Critical Read Timing Specifications for a Demultiplexed Bus with Zero Wait-States

Timing Description	80C196NP	28F200BV-80	Timing Specification Met?
Address to Valid Data	t_{AVDV} = 213 ns	t_{AVQV} = 110 ns	Yes
RD#/OE# to Data Valid	t_{RLDV} = 109 ns	t_{GLQV} = 65 ns	Yes
End of RD#/OE# to High Impedance Data Bus	t_{RHDZ} = 66 ns	t_{GHQZ} = 45 ns	Yes
Output Hold after RD#/OE# Inactive	t_{RXDX} = 0 ns	t_{OH} = 0 ns	Yes

NOTE:
28F200BV-80 and 80C196NP-14 MHz

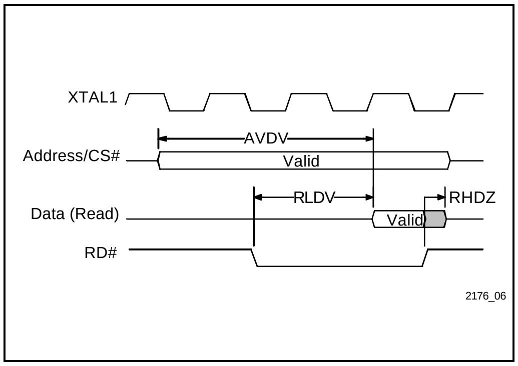


Figure 6. Key Timing Specifications for Intel Flash and the 8XC196NP during a Read Cycle

5.1.2 THE WAIT-STATE READ CYCLE

Slower flash devices may require the insertion of wait-states. To illustrate this point, suppose a 28F200BV-120 (V_{CC} = 5V, commercial temperature) is used in place of the 28F200BV-80 from the previous example. Table 2 compares the 8XC196NP (25 MHz, V_{CC} = 5V) with 120 ns flash device.

Since t_{AVQV} violates the MCS 96 microcontroller t_{AVDV} specification, a wait-state must be inserted into the bus cycle. Wait-states add ($2T_{OSC}$ x n)ns to t_{AVDV} and t_{RLDV}, where n is the number of inserted wait-states. Thus, t_{AVDV} equals

$$110 \text{ ns} + (2 \text{ x } 40 \text{ ns x } 1 \text{ ws}) = 190 \text{ ns}$$

To add wait-states, modify the two least significant bits of the BUSCONx register. In this example, adding one wait-state is sufficient. Thus the two least significant bits of the BUSCONx register should be set to 01.

Table 2. Read Timing for a Demultiplexed Bus Requiring Wait-States

Timing Description	8XC196NP	28F200BV-120	Timing Specification Met?
Address to Valid Data	t_{AVDV} = 110 ns	t_{AVQV} = 120 ns	No
RD#/OE# to Data Valid	t_{RLDV} = 55 ns	t_{GLQV} = 40 ns	Yes
End of RD#/OE# to High Impedance Data Bus	t_{RHDZ} = 35 ns	t_{GHQZ} = 30 ns	Yes
Output Hold after RD#/OE# Inactive	t_{RXDX} = 0 ns	t_{OH} = 0 ns	Yes

5.1.3 THE WRITE CYCLE

Similar analysis must be undertaken for the write cycle. Table 3 shows the key specifications which guarantee proper write execution.

6.0 THE MULTIPLEXED BUS

Interfacing flash to the 80C196NP multiplexed bus can also be straightforward. An additional signal, ALE, provides the timing necessary for a common address/data bus. The multiplexed bus also supports a READY signal to force wait-states for slower memory devices. However, since the MCS 96 microcontroller family has the BUSCONx register, the READY signal may be ignored. Figure 7 shows a block diagram for one possible method of interfacing memory using this bus scheme.

As discussed, data is returned on the same bus that the address is delivered. Thus some mechanism must be used to hold the address while flash retrieves data. In this solution, a transparent latch is used to hold the address so the bus may become available for data. ALE provides the timing mechanism for latching the address into the transparent latch. As shown in Figure 8, the falling edge of ALE triggers the latching of the address.

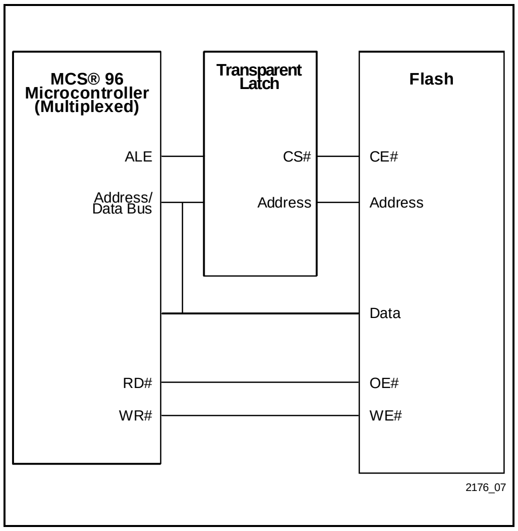


Figure 7. A Latch Should be Used on a Multiplexed Bus to Interface with Memory

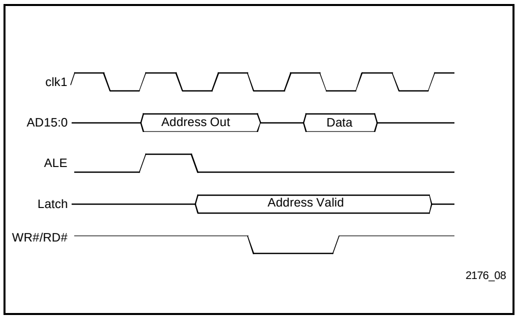


Figure 8. Use ALE to Latch the Valid Address into an Octal Buffer or Transparent Latch

Table 3. Key Write Timing Specifications for Interfacing the 80C196NP to the 28F200BV

Timing Description	8XC196NP	28F200BV	Timing Specification Met?
Data Valid/Setup before WR#/WE# High	t_{QVWH} = 83 ns	t_{DVWH} = 50 ns	Yes
WR#/WE# Pulse Width	t_{WLWH} = 70 ns	t_{WLWH} = 50 ns	Yes
Address Hold from WR#/WE# High	t_{WHAX} = 0 ns	t_{WHAX} = 0 ns	Yes
Data Hold from WR#/WE# High	t_{WHQX} = 20 ns	t_{WHDX} = 0 ns	Yes
WR#/WE# Pulse Width High	>35 ns	t_{WHWL} = 30 ns	Yes

NOTE:

For timing violations during the write cycle, add wait-states by modifying the BUSCONx register.

The timing analysis for the multiplexed bus is similar to the analysis of the demultiplexed bus. Since ALE signals a valid address, the added delay of the valid address to ALE must be taken into account. For the flash device, t_{AVQV} must be greater than the MCS 96 microcontroller's ($t_{QVWH} - t_{AVLL}$), or in other words, the flash access time must be faster than address valid minus address valid to ALE low.

> To ensure proper multiplexed bus operation, the following specification must be met:
>
> $$t_{AVQV} > (t_{QVWH} - t_{AVLL})$$

A 25 MHz 8XC196NP requires one wait-state if interfaced with a 28F200BV-80. This is shown from the above equation. Since t_{AVQV} = 80 ns, t_{QVWH} equals 80 ns, and t_{AVLL} equals 25 ns,

$$(t_{QVWH} - t_{AVLL}) = 55 \text{ ns}$$

Thus, this configuration violates the bus timing specification and a wait-state must be inserted to ensure proper operation.

7.0 PARTITIONING MEMORY

Several different memory configurations may be used with the MCS 96 microcontroller family. For memory configurations composed of only one memory device and where power consumption is not critical to the design, flash's CE# may be tied to ground. The bus of the 8XC196NP also allows designs with several memory chips residing on the bus.

7.1 The Chip Select Signal

- Each device on the bus has an associated BUSCONx, ADDRCOMx, and ADDRMSKx
- ADDRCOMx stores the 12 most significant bit of the base address
- ADDRMSKx stores the size of the bus device

The CS# signal generated by the 80C196NP can be tied to the flash device's CE# directly. When asserted, the flash device powers the sense amplifiers and other internal circuitry on chip. Thus, without assertion of this signal, flash cannot drive the data bus.

Along with BUSCONx, two other registers configure the memory interface: ADDRCOMx and ADDRMSKx.

These 12 bit registers allow the 8XC196NP to address several memory devices of different sizes on the same bus.

Each chip select has an associated BUSCONx, ADDRCOMx, and ADDRMSKx. ADDRCOMx defines the base address of the memory device whereas ADDRMSKx defines the size of the device. For example, a 28F200BV connected to CS1 occupies the memory space from 080000H to 0BFFFFH. ADDRCOM1 stores the 12 most significant bits of the base address. In this case, 0800H.

ADDRMSK1 stores the size of the addressing space. To calculate the value that must be placed in this register, subtract the base two exponent that corresponds to the size of the memory device from 20 and set the resulting number of most significant bits in the ADDRMSKx register. Thus, in this example, since a two megabit chip = 2^{18} bytes, the number of set bits = (20 – 18) = 2. ADDRMSK1 should be set to 0C00H, as shown in Figure 9.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	R	1	1	0	0	0	0	0	0	0	0	0	0

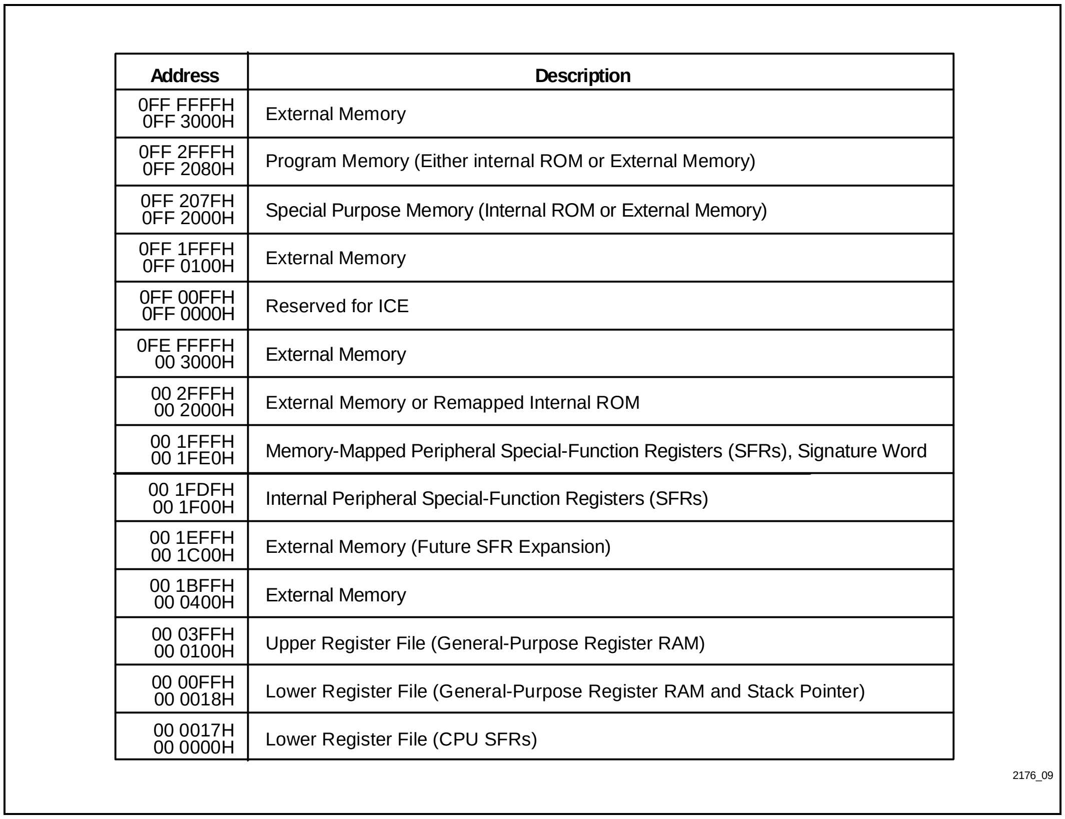
2176_09

Figure 9. The Contents of ADDRMSKx Register to Address Two Megabits of memory

This process should be repeated for each memory device on the bus. The corresponding BUSCONx register should also be set according to the memory device's configuration.

7.2 MCS® 96 Memory Map and Internal Memory

The 80C196NP has a 24-bit internal address bus, but only 20 of these address lines are bonded out. Thus a total of one megabyte of external memory may be addressed directly while the remaining address space is reserved for internal ROM or register memory. Figure 10 shows the memory map for the 80C196NP.



Address	Description
0FF FFFFH 0FF 3000H	External Memory
0FF 2FFFH 0FF 2080H	Program Memory (Either internal ROM or External Memory)
0FF 207FH 0FF 2000H	Special Purpose Memory (Internal ROM or External Memory)
0FF 1FFFH 0FF 0100H	External Memory
0FF 00FFH 0FF 0000H	Reserved for ICE
0FE FFFFH 00 3000H	External Memory
00 2FFFH 00 2000H	External Memory or Remapped Internal ROM
00 1FFFH 00 1FE0H	Memory-Mapped Peripheral Special-Function Registers (SFRs), Signature Word
00 1FDFH 00 1F00H	Internal Peripheral Special-Function Registers (SFRs)
00 1EFFH 00 1C00H	External Memory (Future SFR Expansion)
00 1BFFH 00 0400H	External Memory
00 03FFH 00 0100H	Upper Register File (General-Purpose Register RAM)
00 00FFH 00 0018H	Lower Register File (General-Purpose Register RAM and Stack Pointer)
00 0017H 00 0000H	Lower Register File (CPU SFRs)

Figure 10. Only 20 of the 24 Internal Address Lines are Bonded out of the 80C196NP. Access Internal Memory between 0FF2000H and 0FF2FFFH.

Since the 8XC196NP external addresses contain only 20 bits, external accesses may be differentiated from internal accesses through the use of the chip select unit. To address internal ROM (83C196NP only), simply address memory within the range of 0FF2000H to 0FF2FFFH. When accessing this internal memory, the external address pins will show an address between 0F2000H and 0F2FFFH. The chip selects will remain deasserted during an internal access.

8.0 RESET CONSIDERATIONS

- The peripheral devices should complete reset sequence prior to the microcontroller
- Boot block protection may be achieved while booting from 0FF2080H

Two methods may be used to reset the MCS 96 microcontroller family. To cause a reset, the system may either pull the RESET# pin low for at least four system clocks or issue the RST instruction. Both reset methods activate internal pull-down transistors, which hold the RESET# signal low for 32 system clock cycles. During reset, the controller forces all of the I/O pins, control pins, and registers to their reset states. The controller will fetch the chip configuration bytes followed by the first instruction fetch. Several considerations should be made when designing the reset circuitry. First, the peripheral devices should complete reset sequence prior to the controller, especially the external boot device. Second, since the MCS 96 microcontroller family boots from memory location 0FF2080H, how can boot block protection be obtained when booting from a flash boot block device?

8.1 Memory Reset Timing

After reset, the external boot device must become available before the controller fetches its first instruction. To verify that flash will become available prior to the microcontroller's initial fetch, analysis similar to the following example should be performed.

Suppose an 80C196NP is interfaced with a 28F400BV-120 operating at 3V V_{CC}. The earliest this flash device will be able to deliver code to the microcontroller is 800 ns, as specified by t_{PHQV}. The 80C196NP operating at 14 MHz, on the other hand, may require register data from memory as early as three clock cycles, or 214 ns. Because the 8XC196NP may require an instruction before flash is ready, a delay circuit should be inserted to postpone the microcontroller's reset sequence. A circuit such as the one shown in Figure 11 must be implemented for a predictable reset.

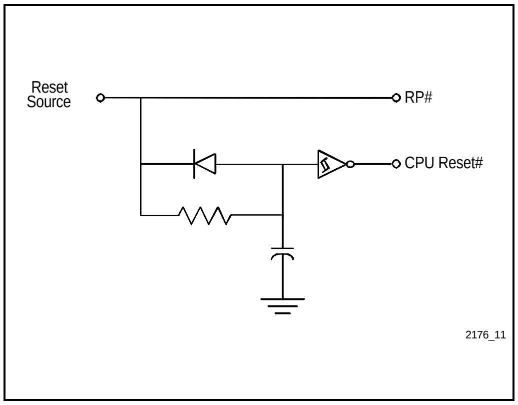


Figure 11. Implement This Circuit if the Flash Device Reset Timing Does Not Meet the Microcontroller's Initial Instruction Fetch Timing

The Reset Source input, in Figure 11, could represent a number of signals. For example, a PowerGood signal or user initiated reset may be connected to this input. Create the delay by choosing appropriate resistor and capacitor values. The Schmitt trigger will ensure clean edges to the microcontroller input and the diode allows fast discharge of the capacitor when the Reset Source input switches from logic high to a logic low input.

To calculate the resistor and capacitor values, use the equation:

$$V_C(t) = V_S + (V_0 - V_S)e^{-t/RC}$$

Analyzing the 80C196NP and 28F400BV as above, a minimum delay of 586 ns must be inserted to ensure valid data upon reset or power-up. If the Schmitt trigger switches from logic low to logic high at V_{T+} = 0.8V and the source voltage V_S = 5V, calculate the following:

$$0.8V = 5V - 5Ve^{-800\ ns/RC}$$

Solving for RC yields 4.59 µs. Since this value represents the minimum RC requirement, larger values may be chosen for guardband.

8.2 Booting from the Boot Block

Immediately after reset or power-up, 8XC196NP reads chip configuration data from the boot device. Next, the processor fetches its first instruction. By default, the 196 boots from 0FF2080H. Since many applications require boot block protection, fetching boot instructions and data from the boot block is required. This may be accomplished by inverting the high address bits, thus booting from 2080H. Figure 12 shows the interconnections of a 28F200BV with the 8XC196NP, including the necessary inverters.

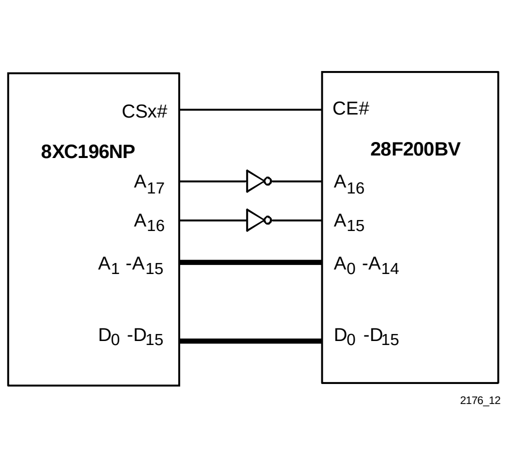


Figure 12. To Boot from the Boot Block, Invert the Upper Address Lines

With the upper address lines inverted, the initial instruction fetch now falls within the 16-Kbyte boot block.

9.0 UPGRADING MEMORY

Many of today's systems could benefit from current product upgrades or from future flash devices. For example, systems which currently use two 28F010 to gain 16-bit data exchange could lower system cost and system power consumption by replacing the two one-megabit chips with a single 28F200BV. Upgrading decreases system cost, the number of chips in the design, and the complexity of the design.

Multi-site layouts provide flexibility to systems by allowing memory upgrades when code becomes too large for the existing design. The SmartVoltage family of boot block products, however, provides a single-socket that allows for a 2-, 4-, and 8-Mbit density upgrade path. Multi-site layouts may be designed to allow the use of alternate components, ensuring production if availability becomes constrained. Figure 13 shows a multi-site layout that may be used to migrate from a 28F010 to 28F200BV. Contact an Intel representative or Intel's BBS system for multi-site layout files for specific applications.

10.0 SUMMARY

Intel Flash and the MCS 96 microcontroller family offer a powerful solution for many applications. Intel Flash's fast access times, low power consumption, and electrical updateability fit well with the various MCS 96 controllers. Zero wait-state operation may be achieved through proper device selection and interfacing. On the 80C196NP, the BUSCONx register sets the bus width, number of wait-states, and bus mode. Other registers control the chip select unit and the mapping of each memory unit on the bus. Mismatches in the reset timing may be corrected with simple circuitry. Finally, multi-site layouts may be used to allow memory density upgrade path.

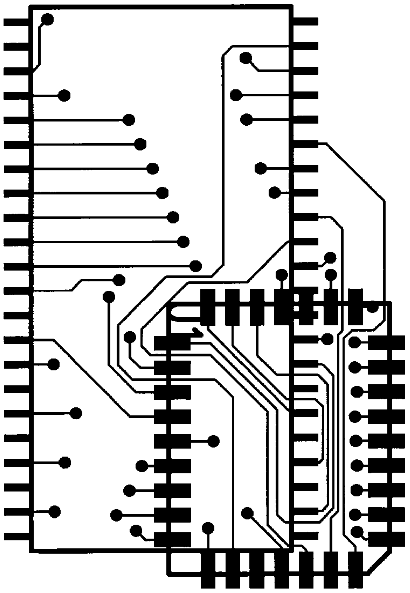


Figure 13. Multi-Site Layouts Allow Flexibility and Offer a Cost-Effective Upgrade Path.

11.0 ADDITIONAL INFORMATION

11.1 References

Order Number	Document
272109	MCS® 96 Architectural Overview
272459	8XC196NP Commercial CHMOS 16-bit Controller Datasheet
290531	2-Mbit SmartVoltage Boot Block Flash Memory Family Datasheet
290530	4-Mbit SmartVoltage Boot Block Flash Memory Family Datasheet
290539	8-Mbit SmartVoltage Boot Block Flash Memory Family Datasheet
292130	AB-57, “Boot Block Architecture for Safe Firmware Updates
292154	AB-60, “2-/4-/8-Mbit SmartVoltage Boot Block Flash Memory

11.2 Revision History

Number	Item
001	Original Version

Filename:	292176_1.DOC
Directory:	C:\TESTDOCS
Template:	C:\WINDOWS\WINWORD6\TEMPLATE\ZAN____1.DOT
Title: E	
Subject:	
Author:	M. Castillo
Keywords:	
Comments:	
Creation Date:	07/11/95 1:38 PM
Revision Number:	164
Last Saved On:	01/19/96 10:42 AM
Last Saved By:	Ward McQueen
Total Editing Time:	2,006 Minutes
Last Printed On:	01/19/96 10:42 AM
As of Last Complete Printing	
Number of Pages:	12
Number of Words:	3,585 (approx.)
Number of Characters:	20,436 (approx.)