AN4649
Application note

Migration of microcontroller applications from STM32F1 to STM32L4 series

Introduction

For designers of STM32 microcontroller applications, it is important to be able to easily replace one microcontroller type by another one in the same product family. Migrating an application to a different microcontroller is often needed, when product requirements grow, putting extra demands on memory size, or increasing the number of I/Os. On the other hand, cost reduction objectives may force you to switch to smaller components and shrink the PCB area.

This application note is written to help analyzing the steps required to migrate an existing design from STM32F1 to STM32L4. It groups together all the most important information and lists the vital aspects that need to be addressed.

This document lists the “full set” of features available for the STM32F1 and STM32L4 series (some products may have less features depending on their part number).

In order to migrate an application from STM32F1 series to STM32L4 series, these three aspects need to be considered: the hardware migration, the peripheral migration and the firmware migration.

To fully benefit from the information in this application note, the user should be familiar with the STM32 microcontroller documentation available on *www.st.com*, with a particular focus on.

The STM32F1 family reference manual (RM0008), the STM32F1 datasheets, and the STM32F1 Flash programming manuals (PM0068, PM0075).

The STM32L4 family reference manuals

- RM0351 (STM32L4x6)

The STM32L4 datasheets.

Table 1. Applicable products

Type	Applicable products
Microcontrollers	STM32F1 Series, STM32L4 Series.

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1 STM32L4 family overview

The STM32L4 platform forms a perfect fit in terms of ultra-low-power, performances, memory size, and peripherals at a cost effective price.

In particular, the STM32L4 family allows high frequency/performance operation, including a Cortex™-M4 @80 MHz and optimized Flash memory access through the adaptive real-time memory accelerator (ART Accelerator™).

The detailed list of available features and packages for each product can be found in the respective datasheet.

The STM32L4 series include a larger set of peripherals with advanced features than the STM32F1 series.

- Advanced encryption hardware accelerator (AES)
- Touch sensing controller (TSC)
- Single Wire Protocol Interface(SWPMI)
- Serial Audio Interface (SAI)
- Low Power UART (LPUART)
- Infrared Interface (IRTIM)
- Low Power Timer (LPTIM)
- Liquid Crystal Display controller (LCD)
- Digital Filter for Sigma Delta modulators (DFSDM)
- Operational Amplifiers (OPAMP)
- Comparators (COMP)
- Voltage Reference Buffer (VREFBUF)
- QuadSPI interface (QUADSPI)
- Flexible Memory Controller (FMC) (FSMC on F1 serie)
- Firewall (FW)
- Additional SRAM2 (32Kbytes) with data preservation in Standby mode
- Random Number Generator (RNG)

It also provides optimized power consumption and an enriched set of low-power mode.

2 Hardware migration

Only LQFP64, LQFP100 and LQFP144 are available on both families. The other packages available on STM32F1 family are not available on STM32L4 family.

The ultra-low-power STM32L4 and STM32F1 families present a high level of pin compatibility. Most peripherals shares the same pins in the two families.

The transition from the STM32F1 series to the STM32L4 series is easy since only a few pins are different (refer to *Table 2*).

Table 2. STM32F1 series and STM32L4 series pinout differences (QFP)

STM32F1 series				STM32L4 series			
QFP64	**QFP100**	**QFP144**	**Pinout**	**QFP64**	**QFP100**	**QFP144**	**Pinout**
5	-	-	PD0-OSC_IN	5	-	-	PH0-OSC_IN
6	-	-	PD1-OSC_OUT	6	-	-	PH1-OSC_OUT
-	73	106	NC	-	73	106	VDDUSB
48	-	-	VDD	48	-	-	VDDUSB
-	-	95	VDD	-	-	95	VDDIO2(1)
-	-	131	VDD	-	-	131	VDDIO2(1)

1. VDDIO2 pin can be connected externally to V_{DD}.

Recommendations to migrate from F1 board to a L4 board

On STM32L4 there is no PD0 and PD1 pins, they are replaced by PH0 and PH1 respectively.

A dedicated V_{DDUSB} supply is used on STM32L4. It should be connected to pin VDDUSB (pin 48 on QFP64, pin 73 on QFP100, pin 106 on QFP144). On STM32F1 the pin was not connected (QFP100, QFP144) or connected to V_{DD} (QFP64).

The figures below show examples of board designs migrating from F1 to L4 series.

Figure 1. Compatible board design: LQFP144

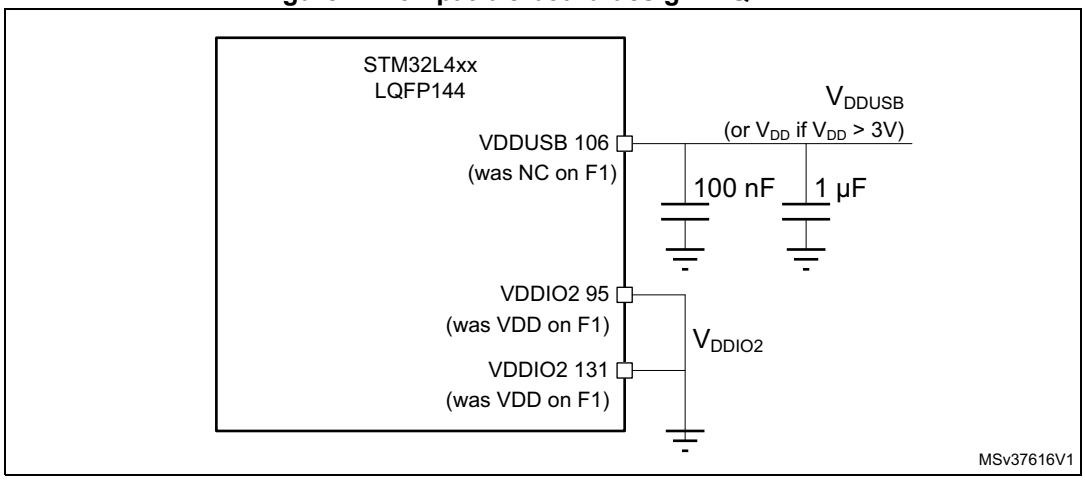


Figure 2. Compatible board design: LQFP100

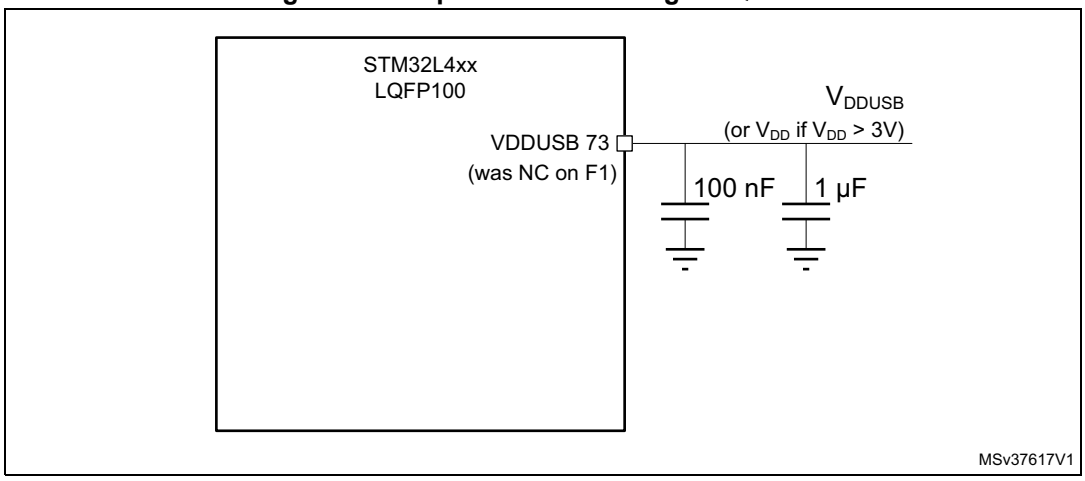
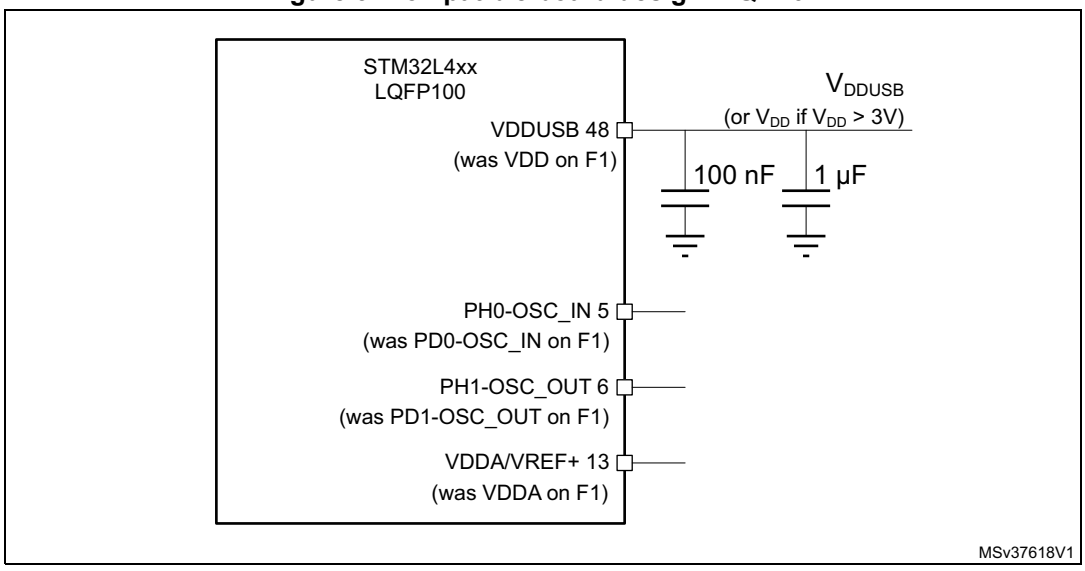


Figure 3. Compatible board design: LQFP64



3 Boot Mode Selection

The way to select the boot mode differs between the F1 and the L4 family. On the F1 family the boot mode is selected with two pins. On L4 family the boot mode is selected with one pin and the nBOOT1 option bit located in the user option bytes at memory address 0x1FFF7800. For both F1 and L4, the boot mode can be selected among these three options: boot from main Flash memory, boot from SRAM or boot from system memory.

Table 3 summarizes the different configurations available for selecting the boot mode.

Table 3. Boot modes

L4/F1 boot mode selection		Boot mode	Aliasing
BOOT1(1)	BOOT0		
x	0	Main Flash memory	Main Flash memory is selected as boot space
0	1	System memory	System memory is selected as boot space
1	1	Embedded SRAM	Embedded SRAM is selected as boot space

1. The BOOT1 value is the opposite of the nBOOT1 option bit.

Embedded boot loader:

The embedded boot loader is located in the system memory, programmed by ST during production. It is used to reprogram the Flash memory using one of the following serial interfaces:

Table 4. Bootloader interfaces

Periph	Pin	STM32F1			STM32L4
		STM32F10xxx	STM32F105xx /107xx	STM32F10xxx XL-density(1)	
DFU	USB_DM (PA11) USB_DP (PA12)	-	X	-	X
CAN2	CAN2_RX (PB5) CAN2_TX (PB6)	-	X	-	-
USART1	USART1_TX (PA9) USART1_RX (PA10)	X	X	X	X
USART2	USART2_TX (PD5) USART2_RX (PD6)	-	X	X	-
USART3	USART3_TX (PC10) USART3_RX (PC11)	-	-	-	X
I2C1	I2C1_SCL (PB6) I2C1_SDA (PB7)	-	-	-	X

Table 4. Bootloader interfaces (continued)

Periph	Pin	STM32F1			STM32L4
		STM32F10xxx	STM32F105xx /107xx	STM32F10xxx XL-density(1)	
I2C2	I2C2_SCL (PB10) I2C2_SDA (PB11)	-	-	-	X
I2C3	I2C3_SCL (PC0) I2C3_SDA (PC1)	-	-	-	X
SPI1	SPI1_NSS (PA4) SPI1_SCK (PA5) SPI1_MISO (PA6) SPI1_MOSI (PA7)	-	-	-	X
SPI2	SPI2_NSS (PB12) SPI2_SCK (PB13) SPI2_MISO (PB14) SPI2_MOSI (PB15)	-	-	-	X
SPI3	SPI3_NSS (PA15) SPI3_SCK (PC10) SPI3_MISO (PC11) SPI3_MOSI (PC12)	-	-	-	X

1. STM32F101xx and STM32F103xx microcontrollers where the Flash memory density ranges between 768 Kbyte and 1 Mbyte.

Please refer to AN2606 for more detail on BootLoader.

4 Peripheral migration

4.1 STM32 product cross-compatibility

The STM32 series embeds a set of peripherals which can be classed in three categories:

- The first category is for the peripherals that are common to all products. Those peripherals are identical on all products, so they have the same structure, registers and control bits. There is no need to perform any firmware change to keep the same functionality at the application level after migration. All the features and behavior remain the same.
- The second category is for the peripherals that present minor differences from one product to another (usually differences due to the support of new features). Migrating from one product to another is very easy and does not require any significant new development effort.
- The third category is for peripherals which have been considerably modified from one product to another (new architecture, new features...). For this category of peripherals, migration will require new development at application level.

Table 5 gives a general overview of this classification.

The “SW compatibility” mentioned in the table below only refers to the register description for “low level” drivers.

The STMCube™ hardware abstraction layer (HAL) between F1 and L4 is compatible.

Table 5. STM32 peripheral compatibility analysis F1 versus L4 series

Peripheral	Nb inst. in F1(1)	Nb Inst. in L4(1)	Compatibility (migrating from F1 to L4)		
			SW	Pinout	Comments
SPI **I2S (full duplex)**	3(1) 3(1)	3 0	Partial Compatibility	Full Compatibility (SPI)	I2S is no more supported by SPI but replaced by dedicated Serial Audio Interface (SAI) in L4. SPI1/SPI2/SPI3 mapped on same GPIO.
WWDG	1	1	Full Compatibility	NA	-
IWDG	1	1	Full Compatibility	NA	Additional read only Window Register (IWDG_WINR) in L4.
DBGMCU	1	1	Full Compatibility	NA	-
CRC	1	1	Partial Compatibility	NA	Additional features in L4.
EXTI	1	1	Partial Compatibility	Partial Compatibility	PG[0:15] GPIO not available as EXTI input on L4.
USB OTG FS	1	1	Partial Compatibility	Partial Compatibility	More endpoints on L4. A few register control are different. VDDUSB merged with VDD on F1. Some F1 devices do not support OTG.
DMA	2	2	No Compatibility	NA	Similar features but DMA mapping requests differ (see section 5.4 DMA)

Table 5. STM32 peripheral compatibility analysis F1 versus L4 series (continued)

Peripheral	Nb inst. in F1(1)	Nb Inst. in L4(1)	Compatibility (migrating from F1 to L4)		
			SW	Pinout	Comments
TIM Basic General P. Advanced Low Power	14 2 10 2 0	13 2 7 2 2	Full Compatibility	Partial Compatibility	Some pins not mapped on same GPIO. Timer instance name may differ. Internal connections may differ.
SDIO/ SDMMC	1	1	Partial Compatibility	Full Compatibility	CE-ATA devices not supported on L4. On F1 SDIO is an AHB peripheral, while it is an APB peripheral on L4.
FSMC/ FMC	1	1	Partial Compatibility	Partial Compatibility	PC card interface not supported on L4. Only 1 bank of NAND Flash supported on L4 (2 on F1).
PWR	1	1	Partial Compatibility	NA	-
RCC	1	1	Partial Compatibility	NA	-
USART	3	3	Partial Compatibility	Full Compatibility	Additional features in L4
UART	2	2 1 (LP)	Partial Compatibility	Full Compatibility	Additional features in L4. Additional LPUART on L4.
I2C	2	3	No Compatibility	Partial Compatibility	Pinout fully compatible for I2C2. I2C1 mapped on different GPIOs. Additional features in L4.
DAC	2	2	Partial Compatibility	Partial Compatibility	Additional features in L4.
ADC	3	3	No Compatibility	Partial Compatibility	Additional features in L4.
RTC	1	1	No Compatibility	Full Compatibility	Additional features in L4.
FLASH	1	1	No Compatibility	NA	New peripheral.
GPIO	142 (1)	114 (1)	Full compatibility	Full Compatibility	At reset, F1 configured in input floating mode, L4 in analog mode.
bxCAN	2	1	Partial Compatibility	Full Compatibility	CAN1 pins fully compatible. CAN2 not available on L4.
ETH	1	0	NA	NA	Ethernet peripheral not available on L4.

Color key:

= No compatibility (new feature or new architecture)

= Partial compatibility (minor changes)

= Full Compatibility (from F1 to L4)

= not applicable

1. Maximum number of instances.

4.2 Memory mapping

The peripheral address mapping has been changed in the L4 series versus the F1 series.

The table below provides the peripheral address mapping correspondence between F1 and L4 series.

Table 6. Peripheral address mapping differences between STM32F1 and STM32L4 series

Peripheral	STM32F1 series		STM32L4 series	
	Bus	Base address	Bus	Base address
FSMC/FMC	AHB	0xA000 0000	AHB3	0xA000 0000
USB OTG FS		0x5000 0000	AHB2	0x5000 0000
ETHERNET MAC		0x4002 8000	NA	
CRC		0x4002 3000	AHB1	0x4002 3000
Flash Interface Reg		0x4002 2000		0x4002 2000
RCC		0x4002 1000		0x4002 1000
DMA2		0x4002 0400		0x4002 0400
DMA1		0x4002 0000		0x4002 0000
SDIO/SDMMC		0x4001 8000	APB2	0x4001 2800
TIM11	APB2	0x4001 5400	NA	
TIM10		0x4001 5000		
TIM9		0x4001 4C00		
ADC3		0x4001 3C00	AHB2	0x5004 0200
USART1		0x4001 3800	APB2	0x4001 3800
TIM8		0x4001 3400		0x4001 3400
SPI1		0x4001 3000		0x4001 3000
TIM1		0x4001 2C00		0x4001 2C00
ADC2		0x4001 2800	AHB2	0x5004 0100
ADC1		0x4001 2400		0x5004 0000
GPIOG		0x4001 2000		0x4800 1800
GPIOF		0x4001 1C00		0x4800 1400
GPIOE		0x4001 1800		0x4800 1000
GPIOD		0x4001 1400		0x4800 0C00
GPIOC		0x4001 1000		0x4800 0800
GPIOB		0x4001 0C00		0x4800 0400
GPIOA	APB2	0x4001 0800	AHB2	0x4800 0000
EXTI		0x4001 0400	APB2	0x4001 0400
AFIO		0x4001 0000	NA	

Table 6. Peripheral address mapping differences between STM32F1 and STM32L4 series (continued)

Peripheral	STM32F1 series		STM32L4 series	
	Bus	Base address	Bus	Base address
DAC	APB1	0x4000 7400	APB1	0x4000 7400
PWR		0x4000 7000		0x4000 7000
Backup registers (BKP)		0x4000 6C00	NA	
bxCAN1		0x4000 6400	APB1	0x4000 6400
bxCAN2		0x4000 6800	NA	
Shared USB/CAN SRAM 512 bytes		0x4000 6000		
USB device FS registers		0x4000 5C00		
I2C2		0x4000 5800	APB1	0x4000 5800
I2C1		0x4000 5400		0x4000 5400
UART5		0x4000 5000		0x4000 5000
UART4		0x4000 4C00		0x4000 4C00
USART3		0x4000 4800		0x4000 4800
USART2		0x4000 4400		0x4000 4400
SPI3/I2S		0x4000 3C00		0x4000 3C00
SPI2/I2S		0x4000 3800		0x4000 3800
IWDG		0x4000 3000		0x4000 3000
WWDG		0x4000 2C00		0x4000 2C00
RTC (inc. BKP registers on L4)		0x4000 2800		0x4000 2800
TIM14		0x4000 2000	NA	
TIM13		0x4000 1C00		
TIM12		0x4000 1800		
TIM7		0x4000 1400	APB1	0x4000 1400
TIM6		0x4000 1000		0x4000 1000
TIM5		0x4000 0C00		0x4000 0C00
TIM4		0x4000 0800		0x4000 0800
TIM3		0x4000 0400		0x4000 0400
TIM2		0x4000 0000		0x4000 0000
Periph on L4 not available on F1				
TSC	NA		AHB1	0x4002 4000
RNG			AHB2	0x5006 0800
CRYP/AES				0x5006 0000

Table 6. Peripheral address mapping differences between STM32F1 and STM32L4 series (continued)

Peripheral	STM32F1 series		STM32L4 series	
	Bus	Base address	Bus	Base address
GPIOH	NA		AHB2	0x4002 1C00
QUADSPI			AHB3	0xA000 1000
SYSCFG			APB2	0x4001 0000
DFSDM				0x4001 6000
SAI1				0x4001 5400
SAI2				0x4001 5800
TIM17				0x4001 4800
TIM16				0x4001 4400
TIM15				0x4001 4000
FIREWALL				0x4001 1C00
VREF				0x4001 0030
COMP				0x4001 0200
OPAMP			APB1	0x4000 7800
I2C3				0x4000 5C00
LCD				0x4000 2400
LPTIM2				0x4000 9400
SWPMI1				0x4000 8800
LPUART1				0x4000 8000
LPTIM1				0x4000 7C00
Color key: = base address or bus change = not applicable				

The system memory mapping has been updated between STM32F1 and STM32L4, please refer to reference manual or datasheet for more details.

The L4 series features an additional SRAM (SRAM2) of 32 Kbytes. The SRAM2 includes additional features listed below:

- Maximum performance through ICode bus access without physical remap.
- Parity check option (32-bit + 4-bit parity check)
- Write protection with 1 Kbyte granularity
- Read Protection (RDP)
- Erase by system reset (option byte) or by software
- Content is preserved in Low-power run, Low-power sleep, Stop 0, Stop 1, Stop 2 mode
- **Content can be preserved (RRS bit set in PWR_CR3 register) in Standby mode (not the case for SRAM1**)

4.3 DMA

STM32F1 and STM32L4 series implement the same DMA IP.

The current consumption of the STM32L4 DMA has been slightly improved and it includes option registers.

The table below presents the correspondence between the DMA requests of the peripherals in STM32F1 series and STM32L4 series.

Table 7. DMA request differences migrating STM32F1 series to STM32L4 series

Peripheral	DMA request	STM32F1 series	STM32L4 series
ADC1	**ADC1**	DMA1_Channel1	DMA1_Channel1 DMA2_Channel3
ADC3	**ADC3**	DMA2_Channel5	NA
DAC	**DAC1** **DAC2**	DMA2_Channel3 DMA2_Channel4	DMA1_Channel3 DMA2_Channel4 DMA1_Channel4 DMA2_Channel5
SPI1	**SPI1_Rx** **SPI1_Tx**	DMA1_Channel2 DMA1_Channel3	DMA1_Channel2 DMA2_Channel3 DMA1_Channel3 DMA2_Channel4
SPI2	**SPI2_Rx** **SPI2_Tx**	DMA1_Channel4 DMA1_Channel5	DMA1_Channel4 DMA1_Channel5
SPI3	**SPI3_Rx** **SPI3_Tx**	DMA2_Channel1 DMA2_Channel2	DMA2_Channel1 DMA2_Channel2
USART1	**USART1_Rx** **USART1_Tx**	DMA1_Channel5 DMA1_Channel4	DMA1_Channel5 DMA2_Channel7 DMA1_Channel4 DMA2_Channel6
USART2	**USART2_Rx** **USART2_Tx**	DMA1_Channel6 DMA1_Channel7	DMA1_Channel6 DMA1_Channel7
USART3	**USART3_Rx** **USART3_Tx**	DMA1_Channel3 DMA1_Channel2	DMA1_Channel3 DMA1_Channel2
UART4	**UART4_Rx** **UART4_Tx**	DMA2_Channel3 DMA2_Channel5	DMA2_Channel5 DMA2_Channel3
UART5	**UART5_Rx** **UART5_Tx**	NA	DMA2_Channel2 DMA2_Channel1
I2C1	**I2C1_Rx** **I2C1_Tx**	DMA1_Channel7 DMA1_Channel6	DMA1_Channel7 DMA2_Channel6 DMA1_Channel6 DMA2_Channel7

Table 7. DMA request differences migrating STM32F1 series to STM32L4 series (continued)

Peripheral	DMA request	STM32F1 series	STM32L4 series
I2C2	**I2C2_Rx** **I2C2_Tx**	DMA1_Channel5 DMA1_Channel4	DMA1_Channel5 DMA1_Channel4
I2C3	**I2C3_Rx** **I2C3_Tx**	NA	DMA1_Channel3 DMA1_Channel2
SDIO **SDMMC**	**SDIO** **SDMMC**	DMA2_Channel4	NA NA DMA2_Channel4 DMA2_Channel5
TIM1	**TIM1_UP** **TIM1_TRIG** **TIM1_COM** **TIM1_CH1** **TIM1_CH3** **TIM1_CH4**	DMA1_Channel5 DMA1_Channel4 DMA1_Channel4 DMA1_Channel2 DMA1_Channel6 DMA1_Channel4	NA
TIM2	**TIM2_UP** **TIM2_CH1** **TIM2_CH2** **TIM2_CH3** **TIM2_CH4**	DMA1_Channel2 DMA1_Channel5 DMA1_Channel7 DMA1_Channel1 DMA1_Channel7	DMA1_Channel2 DMA1_Channel5 DMA1_Channel7 DMA1_Channel1 DMA1_Channel7
TIM3	**TIM3_UP** **TIM3_TRIG** **TIM3_CH1** **TIM3_CH3** **TIM3_CH4**	DMA1_Channel3 DMA1_Channel6 DMA1_Channel6 DMA1_Channel2 DMA1_Channel3	DMA1_Channel3 DMA1_Channel6 DMA1_Channel6 DMA1_Channel2 DMA1_Channel3
TIM4	**TIM4_UP** **TIM4_CH1** **TIM4_CH2** **TIM4_CH3**	DMA1_Channel7 DMA1_Channel1 DMA1_Channel4 DMA1_Channel5	DMA1_Channel7 DMA1_Channel1 DMA1_Channel4 DMA1_Channel5
TIM5	**TIM5_UP** **TIM5_CH1** **TIM5_CH2** **TIM5_CH3** **TIM5_CH4** **TIM5_TRIG** **TIM5_COM**	DMA2_Channel2 DMA2_Channel5 DMA2_Channel4 DMA2_Channel2 DMA2_Channel1 DMA2_Channel1 NA	DMA2_Channel2 DMA2_Channel5 DMA2_Channel4 DMA2_Channel2 DMA2_Channel1 DMA2_Channel1 DMA2_Channel1
TIM6	**TIM6_UP**	DMA2_Channel3	DMA1_Channel3 DMA2_Channel4

Table 7. DMA request differences migrating STM32F1 series to STM32L4 series (continued)

Peripheral	DMA request	STM32F1 series	STM32L4 series
TIM7	**TIM7_UP**	DMA2_Channel4	DMA1_Channel4 DMA2_Channel5
TIM8	**TIM8_UP** **TIM8_CH1** **TIM8_CH2** **TIM8_CH3** **TIM8_CH4** **TIM8_TRIG** **TIM8_COM**	DMA2_Channel1 DMA2_Channel3 DMA2_Channel5 DMA2_Channel1 DMA2_Channel2 DMA2_Channel2 DMA2_Channel2	NA
AES	**AES_OUT** **AES_IN**	NA	DMA2_Channel3 DMA2_Channel2 DMA2_Channel5 DMA2_Channel1
Color key: = Feature not available (NA) = Difference between F1 and L4 highlight			

4.4 Interrupts

The table below presents the interrupt vectors in STM32L4 series versus STM32F1 series.

The changes in the interrupt vectors impact only a few peripherals:

Table 8. Interrupt vector differences between STM32F1 series and STM32L4 series

Position	STM32F1 series			STM32L4 series
	Connectivity line [1]	XL density[2]	Other devices	
0	WWDG			WWDG
1	PVD			PVD / PVM
2	TAMPER			TAMPER / CSS
3	RTC			RTC_WKUP
4	FLASH			FLASH
5	RCC			RCC
6	EXTI0			EXTI0
7	EXTI1			EXTI1
8	EXTI2			EXTI2
9	EXTI3			EXTI3
10	EXTI4			EXTI4
11	DMA1_Channel1			DMA1_Channel1
12	DMA1_Channel2			DMA1_Channel2
13	DMA1_Channel3			DMA1_Channel3
14	DMA1_Channel4			DMA1_Channel4
15	DMA1_Channel5			DMA1_Channel5
16	DMA1_Channel6			DMA1_Channel6
17	DMA1_Channel7			DMA1_Channel7
18	ADC1_2			ADC1_2
19	CAN1_TX	USB_HP / CAN_TX		CAN1_TX
20	CAN1_RX0	USB_LP /CAN_RX0		CAN1_RX0
21	CAN1_RX1		CAN_RX1	CAN1_RX1
22	CAN1_SCE		CAN_SCE	CAN1_SCE
23	EXTI9_5			EXTI9_5
24	TIM1_BRK	TIM1_BRK / TIM9	TIM1_BRK	TIM1_BRK / TIM15
25	TIM1_UP	TIM1_UP / TIM10	TIM1_UP	TIM1_UP / TIM16
26	TIM1_TRG_COM	TIM1_TRG_COM / TIM11	TIM1_TRG_COM	TIM1_TRG_COM /TIM17
27	TIM1_CC			TIM1_CC

Table 8. Interrupt vector differences between STM32F1 series and STM32L4 series (continued)

Position	STM32F1 series			STM32L4 series
	Connectivity line [1]	XL density[2]	Other devices	
28	TIM2			TIM2
29	TIM3			TIM3
30	TIM4			TIM4
31	I2C1_EV			I2C1_EV
32	I2C1_ER			I2C1_ER
33	I2C2_EV			I2C2_EV
34	I2C2_ER			I2C2_ER
35	SPI1			SPI1
36	SPI2			SPI2
37	USART1			USART1
38	USART2			USART2
39	USART3			USART3
40	EXTI15_10			EXTI15_10
41	RTC_Alarm			RTC_Alarm
42	USB_FS_WKUP	USBWakeup		DFSDM
43	NA	TIM8_BRK / TIM12	TIM8_BRK	TIM8_BRK
44		TIM8_UP / TIM13	TIM8_UP	TIM8_UP
45		TIM8_TRG_COM / TIM14	TIM8_TRG_COM	TIM8_TRG_COM
46		TIM8_CC		TIM8_CC
47		ADC3		ADC3
48		FSMC		FMC
49		SDIO		SDMMC
50	TIM5			TIM5
51	SPI3			SPI3
52	UART4			UART4
53	UART5			UART5
54	TIM6			TIM6_DACUNDER
55	TIM7			TIM7
56	DMA2_Channel1			DMA2_Channel1
57	DMA2_Channel2			DMA2_Channel2
58	DMA2_Channel3			DMA2_Channel3
59	DMA2_Channel4	DMA2_Channel4_5		DMA2_Channel4

Table 8. Interrupt vector differences between STM32F1 series and STM32L4 series (continued)

Position	STM32F1 series			STM32L4 series
	Connectivity line [1]	XL density[2]	Other devices	
60	DMA2_Channel5	NA		DMA2_Channel5
61	ETH			DFSDM1
62	ETH_WKUP			DFSDM2
63	CAN2_TX			DFSDM3
64	CAN2_RX0			COMP
65	CAN2_RX1			LPTIM1
66	CAN2_SCE			LPTIM2
67	OTG_FS			OTG_FS
68	NA			DMA2_CH6
69				DMA2_CH7
70				LPUART1
71				QUADSPI
72				I2C3_EV
73				I2C3_ER
74				SAI1
75				SAI2
76				SWPMI1
77				TSC
78				LCD
79				AES
80				RNG
81				FPU

Color key:

= Same feature, but specification change or enhancement

= Feature not available (NA)

= Difference between F1 and L4 highlight

1. **Connectivity line devices** are STM32F105xx and STM32F107xx microcontrollers.
2. **XL-density devices** are STM32F101xx and STM32F103xx microcontrollers where the Flash memory density ranges between 768 Kbyte and 1 Mbyte.

4.5 RCC

The main differences related to the RCC (reset and clock controller) in the STM32L4 series and the STM32F1 series, are presented in the table below.

Table 9. RCC differences between STM32F1 and STM32L4 series

RCC	STM32F1 series	STM32L4 series
MSI	NA	MSI is a low power oscillator with programmable frequency up to 48 MHz. It can replace PLLs as system clock (faster wakeup, lower consumption). It can be used as USB device clock (no need for external high speed crystal oscillator). Multi speed RC factory and user trimmed (100 kHz, 200 kHz, 400 kHz, 800 kHz, 1 MHz, 2 MHz, 4 MHz (default value), 8 MHz, 16 MHz, 24 MHz, 32 MHz and 48 MHz). Auto calibration from LSE.
HSI	8 MHz RC factory and user trimmed	16 MHz RC factory and user trimmed
LSI	40 kHz RC	32 kHz RC Lower consumption, higher accuracy (refer to product datasheet)
HSE	Connectivity line:(1) 3 - 25 MHz Other lines: 4 - 16 MHz (up to 25 MHz in bypass mode)	4 - 48 MHz
LSE	32.768 kHz (up to 1 MHz in bypass mode) Available in backup domain (VBAT)	32.768 kHz (up to 1 MHz in bypass mode) Configurable drive/consumption Available in backup domain (VBAT)
PLL	Connectivity line:(1) 3 PLLs Main PLL sources: HSI/2, HSE, PLL2 (through divider) PLL2, PLL3 clocked by HSE through divider Other lines: 1 PLL The PLL sources are HSI, HSE.	– Main PLL for system – 2 PLLs for SAI1/2, ADC, RNG, SDMMC and OTG FS clock. Each PLL can provide up to 3 independent outputs. The PLL sources are MSI, HSI16, HSE.
System clock source	HSI, HSE or PLL	MSI, HSI16, HSE or PLL
System clock frequency	Up to 72 MHz 8 MHz after reset using HSI	up to 80 MHz 4 MHz after reset using MSI
AHB frequency	up to 72 MHz	up to 80 MHz
APB1 frequency	up to 36 MHz	up to 80 MHz
APB2 frequency	up to 72 MHz	up to 80 MHz

Table 9. RCC differences between STM32F1 and STM32L4 series (continued)

RCC	STM32F1 series	STM32L4 series
RTC clock source	LSI, LSE or HSE/128	LSI, LSE or HSE/32
MCO clock source	– MCO1 pin (PA8): (max 50 MHz) Connectivity line:(1) HSI, HSE, SYSCLK, PLLCLK/2, PLL2, PLL3/2, XT1 ext 3-25 MHz, PLL3 Other lines: HSI, HSE, SYSCLK, PLLCLK/2	– MCO pin (PA8): SYSCLK, HSI16, HSE, PLLCLK, MSI, LSE or LSI With configurable prescaler, 1, 2, 4, 8 or 16 for each output.
CSS	CSS (Clock Security System)	CSS (Clock Security System) CSS on LSE
Internal oscillator measurement / calibration	– LSE connected to TIM5 CH4 IC: can measure HSI with respect to LSE clock high precision – LSI connected to TIM5 CH4 IC: can measure LSI with respect to HSI or HSE clock precision – HSE connected to TIM11 CH1 IC: can measure HSE with respect to LSE/HSI clock	– LSE connected to TIM15 or TIM16 CH1 IC: can measure HSI16 or MSI with respect to LSE clock high precision – LSI connected to TIM16 CH1 IC: can measure LSI with respect to HSI16 or HSE clock precision – HSE/32 connected to TIM17 CH1 IC: can measure HSE with respect to LSE/HSI16 clock – MSI connected to TIM17 CH1 IC: can measure MSI with respect to HSI16/HSE clock
Interrupt	– CSS (linked to NMI IRQ) – LSIRDY, LSERDY, HSIRDY, HSERDY, PLLRDY (linked to RCC global IRQ)	– CSS (linked to NMI IRQ) – LSECSS, LSIRDY, LSERDY, HSIRDY, MSIRDY, HSERDY, PLLRDY, *PLLSAI1RDY, PLLSAI2RDY* (linked to RCC global IRQ)
Color key: = New feature or new architecture (difference between F1 and L4) = Same feature, but specification change or enhancement = Feature not available (NA) = Difference between F1 and L4 highlight		

1. **Connectivity line devices** are STM32F105xx and STM32F107xx microcontrollers.

In addition to the differences described in the table above, the following additional adaptation steps may be needed for the migration:

4.5.1 Maximum clock frequency versus Flash wait state:

On STM32L4 the maximum system clock frequency and number of Flash memory wait state depend on the selected voltage range V_{CORE}.

Table 10. STM32L4 Performance versus V_{CORE} ranges

CPU performance	Power performance	V_{CORE} range	Typical value (V)	Max frequency (MHz)				
				4 WS	3 WS	2 WS	1 WS	0 WS
High	Medium	1	1.2	80	64	48	32	16
Medium	High	2	1.0	26	26	18	12	6

On STM32F1 the maximum system clock frequency and number of Flash memory wait state are linked by the below conditions:

- zero wait state, if 0 < SYSCLK ≤ 24 MHz
- one wait state, if 24 MHz < SYSCLK ≤ 48 MHz
- two wait states, if 48 MHz < SYSCLK ≤ 72 MHz

4.5.2 Peripheral access configuration

Since the address mapping of some peripherals has been changed in L4 series versus F1 series, different registers need to be used to [enable/disable] or [enter/exit] the peripheral [clock] or [from reset mode].

Table 11. RCC registers used for peripheral access configuration

Bus	Register F1 series	Register L4 series	Comments
AHB	RCC_AHBRSTR	RCC_AHB1RSTR (AHB1) RCC_AHB2RSTR (AHB2) RCC_AHB3RSTR (AHB3)	Used to [enter/exit] the AHB peripheral from reset
	RCC_AHBENR	RCC_AHB1ENR (AHB1) RCC_AHB2ENR (AHB2) RCC_AHB3ENR (AHB3)	Used to [enable/disable] the AHB peripheral clock
	NA	RCC_AHB1SMENR (AHB1) RCC_AHB2SMENR (AHB2) RCC_AHB3SMENR (AHB3)	Used to [enable/disable] the AHB peripheral clock in Sleep mode
APB1	RCC_APB1RSTR	RCC_APB1RSTR1 RCC_APB1RSTR2	Used to [enter/exit] the APB1 peripheral from reset
	RCC_APB1ENR	RCC_APB1ENR1 RCC_APB1ENR2	Used to [enable/disable] the APB1 peripheral clock
	NA	RCC_APB1SMENR1 RCC_APB1SMENR2	Used to [enable/disable] the APB1 peripheral clock in Sleep mode

Table 11. RCC registers used for peripheral access configuration (continued)

Bus	Register F1 series	Register L4 series	Comments
APB2	RCC_APB2RSTR		Used to [enter/exit] the APB2 peripheral from reset
	RCC_APB2ENR		Used to [enable/disable] the APB2 peripheral clock
	NA	RCC_APB2SMENR	Used to [enable/disable] the APB2 peripheral clock in Sleep mode
Color key: = Feature not available (NA)			-

The configuration to access a given peripheral involves:

- identify the bus to which the peripheral is connected, refer to *Table 6 on page 12*
- selecting the right register according the needed action, refer to *Table 11* above.

For example, USART1 is connected to APB2 bus. In order to enable the USART1 clock, the RCC_APB2ENR register needs to be configured as follows:

```
__HAL_RCC_USART1_CLK_ENABLE();
```

with STM32Cube HAL driver RCC API.

In order to disable the USART1 clock during Sleep mode (to reduce power consumption) the RCC_APB2SMENR register needs to be configured as follows:

```
__HAL_RCC_USART1_CLK_SLEEP_ENABLE();
```

with STM32Cube HAL driver RCC API.

4.5.3 Peripheral clock configuration:

Some peripherals have a dedicated clock source independent from the system clock, and used to generate the clock required for their operation:

- *USB:*

  In STM32F1 series (connectivity device only), The USB 48 MHz clock is derived from the main PLL VCO output.

  In STM32L4 series, the USB 48 MHz clock is derived from one of the three following sources:

  – Main PLL VCO (PLLUSB1CLK)
  – PLLSAI1 VCO (PLLUSB2CLK)
  – MSI clock (when the MSI clock is auto-trimmed with the LSE, it can be used by the USB OTG FS device)

- *SDIO/SDMMC:*

  In STM32F1 series (not present on connectivity device), the SDIO AHB interface clock (SDIOCLK) is derived from the system clock and is equal to HLCK/2 (HCLK = AHB clock), while the SDIO adapter clock equals HCLK.

In STM32L4 series, the SDMMC clock is derived from one of the three following sources:

– Main PLL VCO (PLLUSB1CLK)
– PLLSAI1 VCO (PLLUSB2CLK)
– MSI clock

- RTC:
  – In STM32 F1 series, the RTC clock is derived from one of the three following sources: LSE
  – LSI
  – HSE divided by 128

  In STM32L4 series, the RTC (and LCD glass clock) is derived from one of the three following sources:
  – LSE clock
  – LSI clock
  – HSE clock divided by 32 (PCLK frequency should always be greater than or equal to RTC Clock frequency)
- *ADC:*

  In STM32F1 series, the ADC clock is the PCLK2 clock divided by a programmable factor (2, 4, 6, 8)

  In STM32L4 series, the input clock of the two ADCs (master and slave) can be selected between two different clock sources:
  – The ADCs clock can be derived (selected by software) from one of the three following sources: system clock (SYSCLK), PLLSAI1 VCO (PLLADC1CLK), PLLSAI2 VCO (PLLADC2CLK). In this mode, a programmable divider factor can be selected (1, 2, … 256 according to bits PREC[3:0]).
  – The ADC clock can be derived from the AHB clock of the ADC bus interface, divided by a programmable factor (1, 2 or 4). In this mode, a programmable divider factor can be selected (1, 2 or 4 according to bits CKMODE[1:0]). See reference manuals for more details.
- DAC:

  In STM32L4 series, the LSI clock is used for the sample and hold operation in addition to the PCLK1 clock.
- U(S)ARTs:

  In STM32F1 series, the U(S)ART clock is APB1 or APB2 clock (depending on which APB bus the U(S)ART) is mapped to.

  In STM32L4 series, the U(S)ART clock is derived from one of the four following sources: system clock (SYSCLK), HSI16, LSE, APB1 or APB2 clock (depending on which APB bus is mapped the U(S)ART).

  Using a source clock independent from the system clock (ex: HSI16) allows to change the system clock on the fly without need to reconfigure U(S)ART peripheral baud rate pre-scalers.
- I2Cs:

  In STM32F1 series, the I2C clock is APB1 clock (PCLK1).

  In STM32L4 series, the I2C clock is derived from one of the three following sources:
  – System clock (SYSCLK)

  - HSI16
  - APB1 (PCLK1)

  Using a source clock independent from the system clock (example HSI16) allows to change the system clock on the fly without need to reconfigure I2C peripheral timing register.

- I2S/SAI:

  In STM32F1 series, the I2S clocks are derived from one of the two following sources:
  - SYSCLK (system clock)
  - PLL3VCO (= 2x PLL3CLK) (only on connectivity devices).

  In STM32L4 series, the I2S peripherals are not available and replaced by SAIs.

  The SAI clocks are derived from one of the four following sources:
  - An external clock mapped on SAI1_EXTCLK or SAI2_EXTCLK
  - PLLSAI1 VCO (PLLSAI1CLK)
  - PLLSAI2 VCO (PLLSAI2CLK)
  - Main PLL VCO (PLLSAI3CLK)
- IWDG:

  In STM32F1 and STM32L4 series, the IWDG clock is LSI.

Ethernet clocks are not available on STM32L4 compared to STM32F1 (no Ethernet peripheral on STM32L4).

4.6 PWR

In STM32L4 series the PWR controller presents some differences versus STM32F1 series, these differences are summarized in the table below.

Table 12. PWR differences between STM32F1 series and STM32L4 series

PWR	STM32F1 series	STM32L4 series
Power supplies	V_{DD} = 2.0 to 3.6 V: external power supply for I/Os, Flash memory and internal regulator. It is provided externally through V_{DD} pins.	V_{DD} = 1.71 to 3.6 V: external power supply for I/Os and internal regulator. It is provided externally through V_{DD} pins.
	V_{CORE} = 1.8 V V_{CORE} is the power supply for digital peripherals, SRAM and Flash memory. It is generated by an internal voltage regulator. In Stop mode the regulator supplies low-power preserving contents of registers and SRAM.	V_{CORE} = 1.0 to 1.2 V V_{CORE} is the power supply for digital peripherals, SRAM and Flash memory. It is generated by an internal voltage regulator. Two V_{CORE} ranges can be selected by software depending on target frequency.
	V_{BAT} = 1.8 to 3.6 V: power supply for RTC, external clock 32 kHz oscillator and backup registers (through power switch) when V_{DD} is not present.	V_{BAT} = 1.55 to 3.6 V: power supply for RTC, external clock 32 kHz oscillator and backup registers (through power switch) when V_{DD} is not present.
	V_{DD} and V_{DDA} must be at the same voltage value.	Independent power supplies (V_{DDA}, V_{DDUSB}, V_{DDIO2}) allow to improve power consumption by running MCU at lower supply voltage than analog and USB.
	V_{SSA}, V_{DDA}: 2.0 V to 3.6 V V_{DDA} is the external analog power supply for A/D and D/A converters. V_{DDA} and V_{SSA} must be connected to V_{DD} and V_{SS} respectively.	V_{SSA}, V_{DDA} = 1.62 V (ADCs/COMPs) to 3.6 V 1.8 V (DACs/OPAMPs) to 3.6 V 2.4 V (VREFBUF) to 3.6 V V_{DDA} is the external analog power supply for A/D and D/A converters, voltage reference buffer, operational amplifiers and comparators. The V_{DDA} voltage level is independent from the V_{DD} voltage.
	NA	V_{LCD} = 2.5 to 3.6 V The LCD controller can be powered either externally through the V_{LCD} pin or internally from an internal voltage generated by the embedded step-up converter.
	N/A USB powered by V_{DD}. V_{DD} should be > 3.0 V (or degraded electrical characteristic between 2.7 V to 3 V)	V_{DDUSB} = 3.0 to 3.6 V V_{DDUSB} is the external independent power supply for USB transceivers. The V_{DDUSB} voltage level is independent from the V_{DD} voltage.
	N/A No VDDIO2 supply on STM32F1 products.	V_{DDIO2} = 1.08 V to 3.6 V V_{DDIO2} is the external power supply for 14 I/Os (Port G[15:2]). The V_{DDIO2} voltage level is independent from the V_{DD} voltage.

Table 12. PWR differences between STM32F1 series and STM32L4 series (continued)

PWR	STM32F1 series	STM32L4 series
Battery backup domain	RTC with backup registers LSE PC13 to PC15 I/Os	RTC with backup registers LSE PC13 to PC15 I/Os Data retention on SRAM2 during Standby
Power supply supervisor	Integrated POR / PDR circuitry Programmable voltage detector (PVD)	Integrated POR / PDR circuitry Programmable voltage detector (PVD)
	NA	Brownout reset (BOR) BOR is always enabled, except in Shutdown mode
		4 Peripheral Voltage Monitoring (PVM) – PVM1 for V_{DDUSB} – PVM2 for V_{DDIO2} – PVM3/PVM4 for V_{DDA} (~1.65 V/ ~2.2 V)
Low-power modes	Sleep mode	Sleep mode
	NA	Low-power run mode (up to 2 MHz)(1) Low-power sleep mode (up to 2 MHz)(1) System clock is limited to 2 MHz but I2C and U(S)ART/LPUART can be clocked with HSI16 at 16 MHz.
	Stop mode (all clocks are stopped)	Stop 0, Stop1 and Stop2 mode Some additional functional peripherals (see wakeup source)
	Standby mode (V_{CORE} domain powered off)	Standby mode (V_{CORE} domain powered off) with new features: – BOR is always ON – SRAM2 content can be preserved – Pull-up or pull-down can be applied on each I/O
	NA	Shutdown mode (V_{CORE} domain powered off and power monitoring off)

Table 12. PWR differences between STM32F1 series and STM32L4 series (continued)

PWR	STM32F1 series	STM32L4 series
Wake-up sources	Sleep mode – Any peripheral interrupt/wakeup event	Sleep mode – Any peripheral interrupt/wakeup event
	Stop mode – Any EXTI line event/interrupt – PVD, RTC	Stop 0, Stop 1 and Stop 2 mode – Any EXTI line event/interrupt – BOR, PVD, PVM, COMP, RTC, USB, IWDG, U(S)ART, LPUART, I2C, SWP, LPTIM, LCD
	Standby mode – WKUP pin (PA0) rising edge – RTC event – External reset in NRST pin – IWDG reset	Standby mode – 5 WKUP pins rising or falling edge – RTC event – External reset in NRST pin – IWDG reset
	NA	Shutdown mode – 5 WKUP pins rising or falling edge – RTC event – External reset in NRST pin
Configuration	-	In L4 the registers are different: From 2 registers on F1 to 23 registers in L4 – 4 control registers – 2 status registers – 1 status clear register – 2 registers per GPIO port (A,B,..H) for controlling pull-up and pull-down (16 registers) Most configuration bits from F1 can be found on L4 (but sometime may have different programming mode)

Color key:

= New feature or new architecture (difference between F1 and L4)

= Same feature, but specification change or enhancement

= Feature not available (NA)

= Difference between F1 and L4 highlight

1. U(S)ART, LPUART, I2C, SWP, LPTIM up to 16 MHz peripheral independent clock.

4.7 RTC

The STM32L4 and STM32F1 series implement different RTC versions.

The table below shows the differences.

Table 13. RTC differences between STM32F1 series and STM32L4 series

RTC	STM32F1 series	STM32L4 series
Feature	32-bit programmable counter. Programmable prescaler (divider up to 2^{20}). 32bit programmable Alarm register. Alarm interrupt, Second interrupt for periodic interrupt signal, Overflow interrupt.	Calendar with sub-seconds, seconds, minutes, hours, day, date, month, year. Programmable alarm with interrupt function. The alarm can be triggered by any combination of the calendar fields. Automatic wakeup unit. Includes 32x32 backup registers. Enhanced precision, digital calibration circuit (0.95ppm accuracy). Time-stamp for event saving. Tamper detection event.
Configuration	Registers are very different on F1 and L4.	
Color key: = New feature or new architecture (difference between F1 and L4) = Difference between F1 and L4 highlight		

For more information about STM32L4 RTC features, please refer to RTC section of STM32L4 reference manuals.

4.8 GPIO

The STM32L4 GPIO peripheral embeds identical features compared to F1 series.

Minor adaptation of the code written for the F1 series using the GPIO may be required on L4 due to:

- Mapping of particular function on different GPIOs (see pinout difference in *Section 2: Hardware migration*
- Alternate function selection differences (AFSELy[3:0] in registers GPIOx_AFRL and GPIOx_AFRH).

Below ar the main GPIO features:

- GPIO mapped on AHB bus for better performance
- I/O pin multiplexer and mapping: pins are connected to on-chip peripherals/modules through a multiplexer that allows only one peripheral alternate function (AF) connected to an I/O pin at a time. In this way, there cannot be any conflict between peripherals sharing the same I/O pin
- More possibilities and features for I/O configuration.

For more information about STM32L4 GPIO programming and usage, please refer to the "I/O pin multiplexer and mapping" subsection in the GPIO section of the STM32L4 reference manuals and to the product datasheet for detailed description of the pinout and alternate function mapping.

4.9 EXTI

The external interrupt/event controller (EXTI) is very similar on both STM32F1 and STM32L4. The table below shows the main differences.

Table 14. EXTI differences between STM32F1 series and STM32L4 series

EXTI	STM32F1 series	STM32L4 series
Nb of event/interrupt lines	Up to 20 configurable lines (4 direct, 16 configurable)	Up to 40 lines (14 direct, 26 configurable)
Configuration	-	Registers are slightly different to cope with different number of interrupts.
Color key: = Same feature, but specification change or enhancement		

4.10 FLASH

The table below presents the difference between the FLASH interface of STM32F1 series and STM32L4 series.

The STM32L4 instantiates a different FLASH module both in terms of architecture/technology and interface, consequently the L4 Flash programming procedures and registers are different from the F1 series, and any code written for the Flash memory interface in the F1 series needs to be rewritten to run on L4 series.

For more information on programming, erasing and protection of the L4 Flash memory, please refer to the STM32L4 reference manuals.

Table 15. FLASH differences between STM32F1 series and STM32L4 series

FLASH	STM32F1 series	STM32L4 series
Main/Program memory	0x0800 0000 – up to 0x080F FFFF	0x0800 0000 - up to 0x080F FFFF
	For XL-density devices: Up to 1 Mbyte Split in 2 banks Each bank: 256 pages of 2 Kbyte Each page: 8 rows of 256 Byte (other devices have smaller memory size and only 1 bank, see RM0008 for details) Programming granularity: 16 bits Read granularity: 128 bits	Up to 1 Mbyte Split in 2 banks Each bank: 256 pages of 2 Kbyte Each page: 8 rows of 256 Byte Programming and read granularity: 72bits (incl 8 ECC bits)
Feature	for XL-density device: Read while write (RWW) Dual bank boot	Read while write (RWW) Dual bank boot
Wait State	up to 2 (depending on the frequency)	up to 4 (depending on the core voltage and frequency)
ART Accelerator™	NA	Allowing 0 wait state when executing from the cache.
One Time programmable (OTP)		1K OTP bytes (bank1)

Table 15. FLASH differences between STM32F1 series and STM32L4 series (continued)

FLASH	STM32F1 series	STM32L4 series
Flash interface (FLITF)	Read interface with prefetch buffer (2x64-bit) Option byte loader Flash program / erase operation Read / write protection	Flash memory read operations Option byte loader Flash program / erase operations Read protection by option byte 4 write protection areas (2 per bank) 2 proprietary code read protection areas (1 per bank) Prefetch on ICODE Instruction cache: (1 KB RAM) Data Cache: (256 B RAM) Error code correction: 8 bits for 64-bit Low-power mode
Erase granularity	Page erase (1 Kbyte or 2 Kbyte) and mass erase.	Page erase (2Kbytes), bank erase and mass erase (both banks)
Read Protection (RDP)	No protection: RDP = 0x00A5, nRDP = 0xFF5A Protection: RDP = 0xFF = nRDP	Level 0 no protection RDP = 0xAA
		Level 1 memory protection RDP ≠ (Level 2 & Level 0)
		Level 2 RDP = 0xCC (1)
Proprietary Code Readout Protection (PCROP)	NA	2 PCROP areas (1 per bank) Granularity: 64 bit PCROP_RDP option: PCROP area preserved when RDP level decreased.
Write protection (WRP)	Granularity: low, medium density devices: – 4 pages other devices: – 2 pages from page 0 to 61 – remaining pages from page 62 as a whole	4 write protection areas (2 per bank) Granularity: 2 Kbyte

Table 15. FLASH differences between STM32F1 series and STM32L4 series (continued)

FLASH	STM32F1 series	STM32L4 series
User option bytes	nRST_STOP	nRST_STOP
	nRST_STDBY	nRST_STDBY
	NA	nRST_SHDW
	WDG_SW	IWDG_SW
	NA	IWDG_STOP, IWDG_STDBY
		WWDG_SW
		BOR_LEV[2:0]
	BFB2 (for XL-density devices only)	BFB2
	NA	nBOOT1
		SRAM2_RST, SRAM2_PE
		DUAL BANK

Color key:

= New feature or new architecture (difference between F1 and L4)

= Same feature, but specification change or enhancement

= Feature not available (NA)

= Difference between F1 and L4 highlight

Memory read protection Level 2 is an irreversible operation. When Level 2 is activated, the level of protection cannot be decreased to Level 0 or Level 1.

4.11 U(S)ART

The STM32L4 implement several new features on the U(S)ART compared to STM32F1.

The table below shows the differences.

Table 16. U(S)ART differences between STM32F1 series and STM32L4 series

U(S)ART	STM32F1 series	STM32L4 series
Instances	up to 3 x USART up to 2 x UART	3xUSART 2xUART 1xLPUART
Baud rate	up to 4.5 Mbit/s	up to 10 Mbit/s (when the clock frequency is 80 MHz and oversampling is by 8)
Clock	Single clock domain	Dual clock domain allowing: – UART functionality and wakeup from stop mode – Convenient baud rate programming independent from the PCLK reprogramming
Data	**word length**: Programmable (8 or 9 bits)	**word length**: Programmable (7, 8 or 9 bits) Programmable data order with MSB-first or LSB-first shifting
interrupt	11 interrupt sources with flags	14 interrupt sources with flags

Table 16. U(S)ART differences between STM32F1 series and STM32L4 series (continued)

U(S)ART	STM32F1 series	STM32L4 series
Feature	Hardware flow control (CTS/RTS) Continuous communication using DMA Multiprocessor communication Single-wire half-duplex communication IrDA SIR ENDEC block LIN mode SPI Master	
	Smartcard mode T = 0 and T = 1 is to be implemented by software Number of stop bits: 0.5, 1, 1.5, 2	Smartcard mode T = 0 and T = 1 supported (features are added to support T = 1 such as receiver timeout, block length, end of block detection, binary data inversion, etc…) Number of stop bits: 1, 1.5, 2
	NA	Wakeup from STOP mode (Start Bit, Received Byte, Address match) Support for ModBus communication – Timeout feature – CR/LF character recognition Receiver timeout interrupt Auto baud rate detection Driver Enable Swappable Tx/Rx pin configuration LPUART does not support Synchronous mode (SPI Master), Smartcard mode, IrDA, LIN, ModBus, Receiver timeout interrupt, Auto baud rate detection.
Configuration	-	F1 registers and associated bits are not identical in L4. Please refer to STM32L4 reference manuals for details

Color key:

= New feature or new architecture (difference between F1 and L4)

= Same feature, but specification change or enhancement

= Difference between F1 and L4 highlight

4.12 I2C

The STM32L4 and STM32F1 series implement almost the same feature on the I2C.

The table below shows the differences.

Table 17. I2C differences between STM32F1 series and STM32L4 series

I2C	STM32F1 series	STM32L4 series
Instances	x2	x3
Features	7-bit and 10-bit addressing mode SMBus Standard mode (Sm, up to 100 kHz) Fast mode (Fm, up to 400 kHz)	
	NA	Fast mode Plus (Fm+, up to 1 MHz) Independent clock Wakeup from STOP on address match
Configuration	-	Register configuration is very different on F1 and L4. Please refer to STM32L4 reference manuals for details

Color key:

= New feature or new architecture (difference between F1 and L4)

= Same feature, but specification change or enhancement

= Difference between F1 and L4 highlight

4.13 SPI/I2S

The STM32L4 and STM32F1 series implement almost the same features on the SPI (apart from I2S).

The table below shows the differences.

Table 18. SPI differences between STM32F1 series and STM32L4 series

SPI	STM32F1 series	STM32L4 series
Instances	x3 (up to)	x3
Features	SPI + I2S	I2S feature is not supported by SPI on L4, 2 SAI interfaces are available instead
Data size	Fixed, configurable to 8 or 16 bits	Programmable from 4 to 16-bit
Data buffer	Tx & Rx 16-bit buffers (single data frame)	32-bit Tx & Rx FIFOs (up to 4 data frames)
Data packing	No (16-bit access only)	Yes (8-bit, 16-bit or 32-bit data access, programmable FIFOs data thresholds)
Mode	SPI Motorola mode	SPI TI SPI Motorola mode NSSP mode
Speed	up to 36Mbits/s (core at 72 MHz)	TBD
Configuration	-	The data size and Tx/Rx flow handling are different on F1 and L4 hence requiring different SW sequence.

Color key:

= New feature or new architecture (difference between F1 and L4)

= Same feature, but specification change or enhancement

= Difference between F1 and L4 highlight

Migrating from I2S to SAI:

STM32L4 does not include I2S interface part of the SPI peripheral, instead it includes 2 serial audio Interfaces.

The table below shows main differences between I2S and SAI.

Table 19. I2S/SAI differences between STM32F1 series and STM32L4 series

I2S/SAI	STM32F1 series (I2S)	STM32L4 series (SAI)
Instances	x3	x2 (SAI1, SAI2)
Features	Half-duplex communication	Two independent audio sub-blocks (per SAI) which can be transmitters or receivers with their respective FIFO.
	Master or slave operations	Synchronous or asynchronous mode between the audio sub-blocks. Possible synchronization between multiple SAIs. Master or slave configuration independent for both audio sub-blocks.
	8-bit programmable linear pre-scaler to reach accurate audio sample frequencies (from 8 kHz to 192 kHz)	Clock generator for each audio block to target independent audio frequency sampling when both audio sub-blocks are configured in master mode.
	Data format may be 16-bit, 24-bit or 32-bit Data direction is always MSB first	Data size configurable: 8-, 10-, 16-, 20-, 24-, 32-bit. First active bit position in the slot is configurable. LSB first or MSB first for data transfer.
	Channel Length is fixed to 16-bit (16-bit data size) or 32-bit (16-bit, 24-bit, 32-bit data size) by audio channel	Up to 16 slots available with configurable size. Number of bits by frame can be configurable Frame synchronization active level configurable (offset, bit length, level). Stereo/mono audio frame capability.
	Programmable clock polarity (steady state)	Communication clock strobing edge configurable (SCK).
	16-bit register for transmission and reception with one data register for both channel sides.	8-word integrated FIFOs for each audio sub-block. (facilitating interrupt mode).
	Supported I2S protocols: – I2S Phillps standard – MSB-justified standard (left-justified) – LSB-justified standard (right-justified) – PCM standard (with short and long frame synchronization on 16-bit channel frame or 16-bit data frame extended to 32-bit channel frame)	Audio protocol: I2S, LSB or MSB-justified, PCM/DSP, TDM (up to 16 channels), AC'97 SPDIF output Mute mode.
	DMA capability for transmission and reception (16-bit wide)	2-channel DMA interface.

Table 19. I2S/SAI differences between STM32F1 series and STM32L4 series (continued)

I2S/SAI	STM32F1 series (I2S)	STM32L4 series (SAI)
Features	Master clock may be output to drive an external audio component. Ratio is fixed at 256 × FS (where FS is the audio sampling frequency)	
	Interruption sources when enabled: – Errors – Tx Buffer Empty, Rx Buffer not Empty.	Interruption sources when enabled: – Errors – FIFO requests.
	Error flags with associated interrupts if enabled respectively. – Overrun and underrun detection – Anticipated frame synchronization signal detection in slave mode – Late frame synchronization signal detection in slave mode.	Idem F1 + Protection against misalignment in case of underrun and overrun.
Configuration	-	There is no compatibility between STM32F1 I2S and STM32L4 SAI. User will have to configure the SAI interface for the target protocol. Please refer to STM32L4 reference manuals for details.
Color key: = New feature or new architecture (difference between F1 and L4) = Same feature, but specification change or enhancement = Difference between F1 and L4 highlight		

The SAI peripheral improves robustness of communication in Slave mode compared to I2S peripheral (in case of data clock glitch for example)

In master mode, while migrating an application from F1 to L4, the user should review the possible master clock (MCLK), data bit clock (SCK) and frame synchronization (FS) frequency reachable using STM32L4 PLL multiplication factors and SAI internal clock divider for a given external oscillator which can be different than with STM32F1 I2S.

On STM32L4, the SAI1 and SAI2 input clocks are derived (selected by software) from one of the four following sources:

- An external clock mapped on SAI1_EXTCLK for SAI1 and SAI2_EXTCLK for SAI2
- PLLSAI1 (P) divider output (PLLSAI1CLK)
- PLLSAI2 (P) divider output (PLLSAI2CLK)
- Main PLL (P) divider output (PLLSAI3CLK)

When the clock is derived from one of the 3 internal PLLs, the 3 PLL inputs are either HSI16, HSE or MSI (between 4 and 8 MHz) divided by a programmable factor PLLM (from 1 to 8). This input is then multiplied by PLLN (from 8 to 86) to reach PLL VCO frequency (should be between 64 and 344 MHz). It is finally divided by PLLP (7 or 17) to provide the input clock of SAI (max. 80 MHz)

When the master clock MCLK is used by the external slave audio peripheral, the PLL output is divided by SAI internal master clock divider factor (1, 2, 4, 6, 8, ..., 30) to provide the master clock (MCLK). The data bit clock is then derived from MCLK following the formula:

$$SCK = MCLK \times (FRL + 1)/256$$

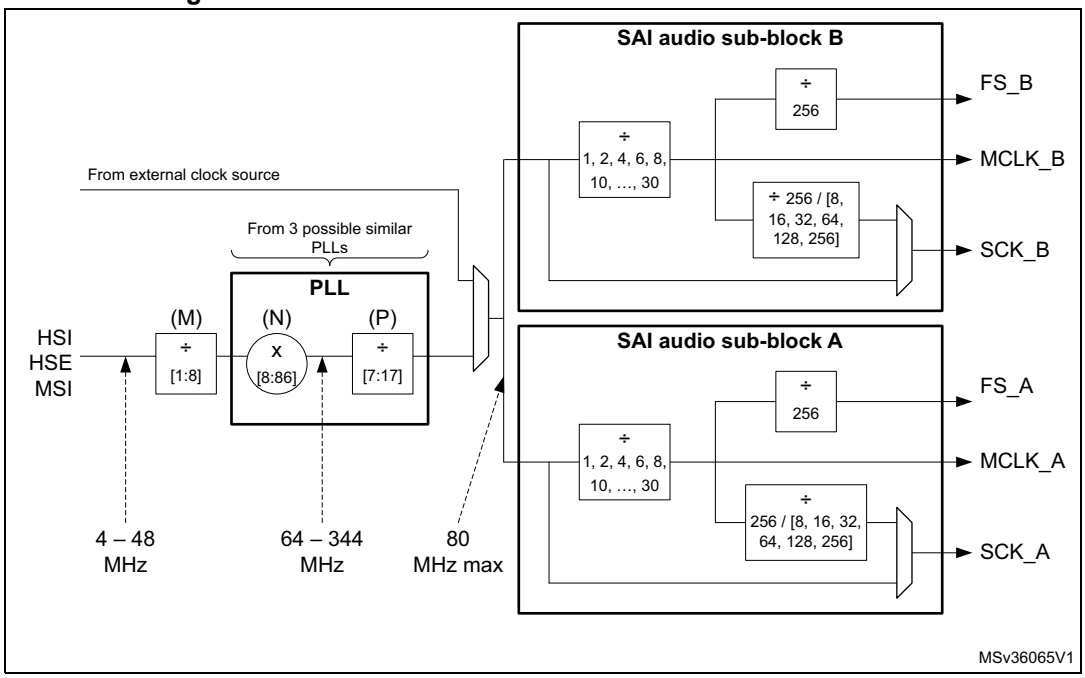
where (FRL + 1) = 8, 16, 32, 64, 128, 256:

- FRL is the number of bit clock cycles - 1 in the audio frame.
- (FRL+ 1) should be a power of 2 higher or equal to 8.

SCK can also be directly connected to input clock of SAI when MCLK output is not needed.

The Frame Synchronization (FS) frequency is always MCLK / 256.

Figure 4. STM32L4 Generation of Clock for SAI Master mode



Please refer to the STM32L4 reference manuals for more details.

4.14 CRC

The STM32L4 implements very similar CRC (cyclic redundancy check) calculation unit as STM32F1.

The table below shows the differences.

Table 20. CRC differences between STM32F1 series and STM32L4 series

CRC	STM32F1 series	STM32L4 series
Feature	Single input/output 32-bit data register CRC computation done in 4 AHB clock cycles (HCLK) for the 32-bit data size General-purpose 8-bit register (can be used for temporary storage)	
	Uses CRC-32 (Ethernet) polynomial: 0x4C11DB7 Handles 32-bit data size	Fully programmable polynomial with programmable size (7, 8, 16, 32bits) Handles 8-,16-, 32-bit data size Programmable CRC initial value Input buffer to avoid bus stall during calculation Reversibility option on I/O data
Configuration	-	Configuration registers on F1 are identical on L4. L4 includes additional registers for new features. Please refer to the STM32L4 reference manuals for details.
Color key: = New feature or new architecture (difference between F1 and L4)		

4.15 bxCAN

The STM32L4 implements same bxCAN (basic extended CAN interface) as STM32F1.

Table 21. bxCAN differences between STM32F1 series and STM32L4 series

bxCAN	STM32F1 series	STM32L4 series
Instances	x2 (up to)	x1
Feature	Supports CAN protocol version 2.0 A, B Active Bit rates up to 1 Mbit/s Supports the time triggered communication option Tx: 3 transmit mailboxes, configurable priority, time stamp on SOF transmission. Rx: 2 receive FIFOs with 3 stages, scalable filter banks, identifier list, configurable FIFO overrun, time stamp on SOF reception. Time-triggered communication option: – Disable automatic retransmission mode – 16-bit free running timer – Time Stamp sent in last two data bytes Management – Maskable interrupts – Software-efficient mailbox mapping at a unique address space	
	Dual CAN (connectivity line only)	NA
Configuration	-	Configuration registers on F1 are identical on L4. Please refer to the STM32L4 reference manuals for details.

Color key:

= Same feature, but specification change or enhancement

= Difference between F1 and L4 highlight

4.16 USB OTG FS

The STM32L4xx and STM32F105xx/107xx series implement very similar USB OTG FS peripherals.

Other STM32F1xx devices only implements a USB FS device interface.

Most features supported by STM32F1xx are also supported by STM32L4xx.

The key differences are listed below.

Table 22. USB OTG FS differences between STM32F105xx/107xx series and STM32L4 series

USB	STM32F1 series	STM32L4 series
Features	Universal Serial Bus Revision 2.0 Full support for the USB On-The-Go (USB OTG).	
	FS mode: 1 bidirectional control endpoint 3 IN endpoints (Bulk, Interrupt, Isochronous) 3 OUT endpoints (Bulk, Interrupt, Isochronous)	FS mode: 1 bidirectional control endpoint 5 IN endpoints (Bulk, Interrupt, Isochronous) 5 OUT endpoints (Bulk, Interrupt, Isochronous)
	USB internal connect/disconnect feature with an internal pull-up resistor on the USB D + (USB_DP) line.	
	-	Attach detection protocol (ADP) Battery charging detection (BCD)
		Independent V_{DDUSB} power supply allowing lower V_{DDCORE} while using USB.
Mapping	AHB	AHB2
Buffer memory	1.25 Kbyte data FIFOs Management of up to 4 Tx FIFOs (1 for each IN end point) + 1 Rx FIFO.	1.25 Kbyte data FIFOs Management of up to 6 Tx FIFOs (1 for each IN end point) + 1 Rx FIFO.
Low-power modes	USB suspend and resume	USB suspend and resume Link power management (LPM) support
Configuration	-	In L4 the registers are different. Please refer to the STM32L4 reference manuals for details.

Color key:

= New feature or new architecture (difference between F1 and L4)

= Same feature, but specification change or enhancement

= Difference between F1 and L4 highlight

Table 23. USB FS differences between STM32F1 series and STM32L4 series

USB	STM32F1 series	STM32L4 series
Features	Universal serial bus revision 2.0.	Universal serial bus revision 2.0, including link power management (LPM) support
	NA	Full support for the USB on-the-go (USB OTG).
	FS mode: 1 bidirectional control endpoint 7 IN endpoints (bulk, interrupt, isochronous) 7 OUT endpoints (bulk, interrupt, isochronous)	FS mode: 1 bidirectional control endpoint 5 IN endpoints (bulk, interrupt, isochronous) 5 OUT endpoints (bulk, interrupt, isochronous)
	USB internal connect/disconnect feature with an internal pull-up resistor on the USB D+ (USB_DP) line.	
	NA	Attach detection protocol (ADP) Battery charging detection (BCD)
		Independent V_{DDUSB} power supply allowing lower V_{DDCORE} while using USB.
Mapping	APB1	AHB2
Buffer memory	512 byte (endpoint buffers and buffer descriptors structure) Shared with bxCAN interface (cannot use both CAN and USB FS simultaneously)	1.25 Kbyte data FIFOs Management of up to 6 Tx FIFOs (1 for each IN end point) + 1 Rx FIFO.
Low-power modes	USB suspend and resume	USB suspend and resume Link power management (LPM) support
Configuration	-	In L4 the registers are different. Please refer to the STM32L4 reference manuals for details.

Color key:

= New feature or new architecture (difference between F1 and L4)

= Same feature, but specification change or enhancement

= Feature not available (NA)

= Difference between F1 and L4 highlight

4.17 ADC

The table below presents the differences between the ADC peripheral of STM32F1 series and STM32L4 series, these differences are the following:

- New digital interface
- New architecture and new features.

Table 24. ADC differences between STM32F1 series and STM32L4 series

ADC	STM32F1 series		STM32L4 series	
ADC Type	SAR structure			
Instances	up to 3 instances (STM32F103xC/D/E/F/G)		3 instances	
Max Sampling freq	up to 2 Msps in interleaved mode (STM32F105/107xx)		5.1 Msps (Fast channels) 4.8 Msps (Slow channels)	
Number of channels	up to 21 channels (STM32F103xC/D/E/F/G)		Up to 19 channels per ADC	
Resolution	12-bit		12-bit + digital oversampling up to 16-bit	
Conversion Modes	Single / continuous / scan / discontinuous Dual mode			
DMA	Yes			
External Trigger	Yes			
	External event for regular group: For ADC1/ADC2: TIM1 CC1 TIM1 CC2 TIM1 CC3 TIM2 CC2 TIM3 TRGO TIM4 CC4 EXTI line 11 TIM8_TRGO SWSTART For ADC3: TIM3_CC1 TIM2_CC3 TIM1_CC3 TIM8_CC1 TIM8_TRGO TIM5_CC1 TIM5_CC3 SWSTART	External event for injected group: For ADC1/ADC2: TIM1_TRGO TIM1_CC4 TIM2_TRGO TIM2_CC1 TIM3_CC4 TIM4_TRGO EXTI line 15 TIM8_CC4 For ADC3: TIM1_CC4 TIM1_TRGO TIM4_CC3 TIM8_CC2 TIM8_CC4 TIM5_TRGO TIM5_CC4 JWSTART	External event for regular group: TIM1 CC1 TIM1 CC2 TIM1 CC3 TIM2 CC2 TIM3 TRGO TIM4 CC4 EXTI line 11 TIM8_TRGO TIM8_TRGO2 TIM1_TRGO TIM1_TRGO2 TIM2_TRGO TIM4_TRGO TIM6_TRGO TIM15_TRGO TIM3_CC4	External event for injected group: TIM1 TRGO TIM1 CC4 TIM2 TRGO TIM2 CC1 TIM3 CC4 TIM4 TRGO EXTI line15 TIM8_CC4 TIM1_TRGO2 TIM8_TRGO TIM8_TRGO2 TIM3_CC3 TIM3_TRGO TIM3_CC1 TIM6_TRGO TIM15_TRGO

Table 24. ADC differences between STM32F1 series and STM32L4 series (continued)

ADC	STM32F1 series	STM32L4 series
Supply requirement	2.4 V to 3.6	1.62 V to 3.6 V Independent power supply (V_{DDA})
Reference Voltage	External 2.4 V to V_{DDA}	External (2.0 V to V_{DDA}) or Internal (2.048 V or 2.5 V)
Electrical Parameters	160 µA (Typ) on V_{REF} DC current 0.8 mA (Typ) on V_{DDA} DC current	Consumption proportional to conversion speed: 200 µA/Msps
Input range	$V_{REF-} \leq V_{IN} \leq V_{REF+}$	$V_{REF-} \leq V_{IN} \leq V_{REF+}$
Color key: = New feature or new architecture (difference between F1 and L4) = Same feature, but specification change or enhancement		

4.18 DAC

The STM32L4 series implement some enhanced DACs compared to STM32F1 series.

The table below shows the differences.

Table 25. DAC differences between STM32F1 series and STM32L4 series

DAC	STM32F1 series	STM32L4 series
Instances	x2	
Resolution	12-bit	
Features	Left or right data alignment in 12-bit mode Noise-wave and triangular-wave generation Dual DAC channel for independent or simultaneous conversions	
	NA	Buffer offset calibration DAC_OUTx can be disconnected from output pin Sample and hold mode for low power operation in Stop mode
DMA	Yes	Yes
External Trigger	Yes	Yes
	TIM2 TRGO TIM4 TRGO TIM5 TRGO TIM6 TRGO TIM7 TRGO TIM8 TRGO (TIM3 TRGO on connectivity devices) EXTI line9 SW TRIG	TIM6 TRGO TIM8 TRGO TIM7 TRGO TIM5 TRGO TIM2 TRGO TIM4 TRGO EXTI line9 SW TRIG
Supply requirement	2.4 V to 3.6 V	1.8 V to 3.6 V Independent power supply (V_{DDA})
Reference Voltage	External 2.4 V ≤ V_{REF+} ≤ V_{DDA}	External (1.8 V to V_{DDA}) or internal (2.048 V or 2.5 V)
Configuration	-	SW compatible except for output buffer management.

Color key:

= New feature or new architecture (difference between F1 and L4)

= Same feature, but specification change or enhancement

= Feature not available (NA)

= Difference between F1 and L4 highlight

5 Revision history

Table 26. Document revision history

Date	Revision	Changes
11-Jun-2015	1	Initial release.
23-Nov-2015	2	*Section 4.2: Memory mapping* updated: Stop 0 mode added for content preservation *Table 12: PWR differences between STM32F1 series and STM32L4 series* updated: Stop 0 mode added