ENR-325/325L Principles of Digital Electronics and Laboratory

Xiang Li

Fall 2025

COE COLLEGE

A homemade MOSFET by Sam Zeloof in 2021:

- https://www.youtube.com/watch?v=IS5ycm7VfXg

Also check:
https://sam.zeloof.xyz/category/semiconductor/

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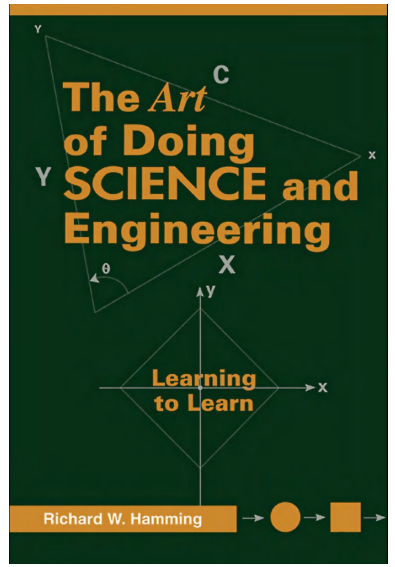
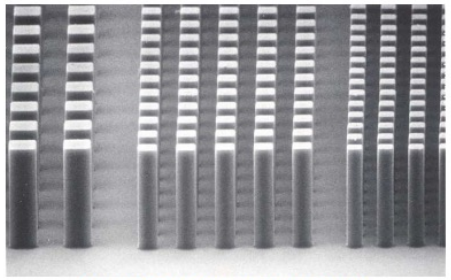
Making CMOS is in the realm of process engineering

In science if you know what you are doing you should not be doing it.
In engineering if you do not know what you are doing you should not be doing it.

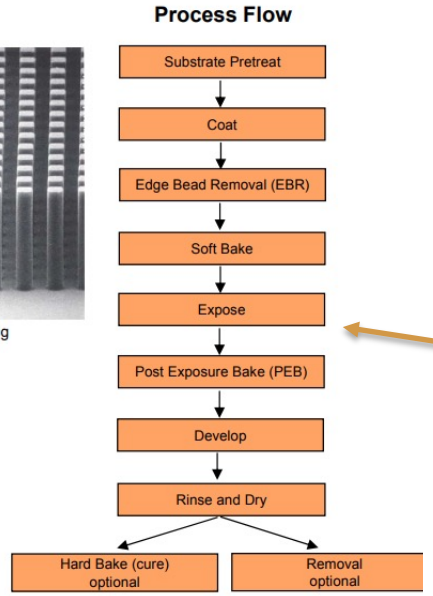


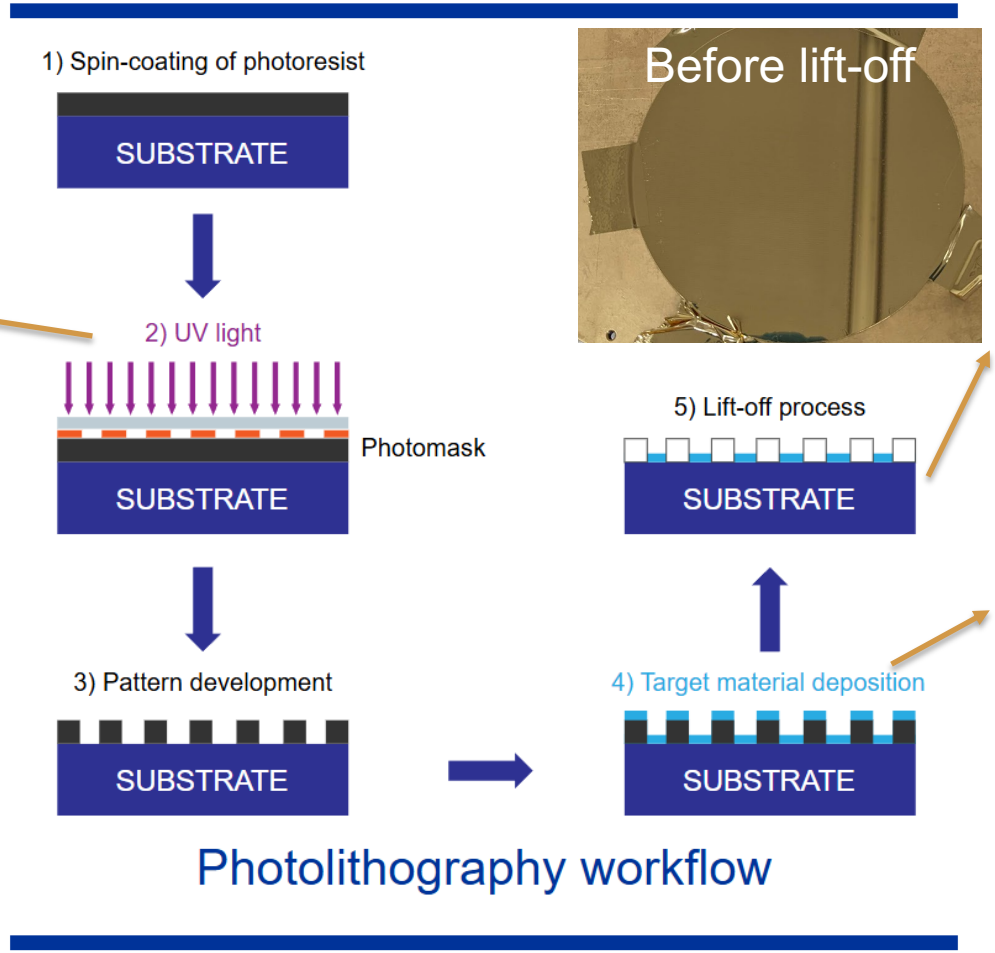
The realm of process engineering

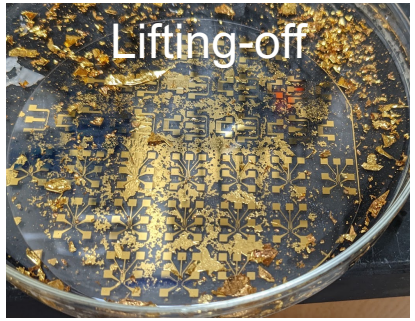
Photolithography example: lift-off



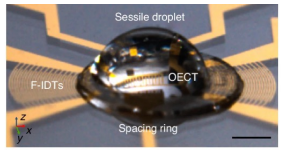
10 um features, 50 um SU-8 2000 coating







Vacuum chamber



Integrated POCT sensor

Data sheet and process flow from Kayaku and Kurt J. Lesker
Fabrication process at Indiana University cleanroom, 2021
Device shown was for Alzheimer's detection: https://doi.org/10.1038/s41378-025-00916-4

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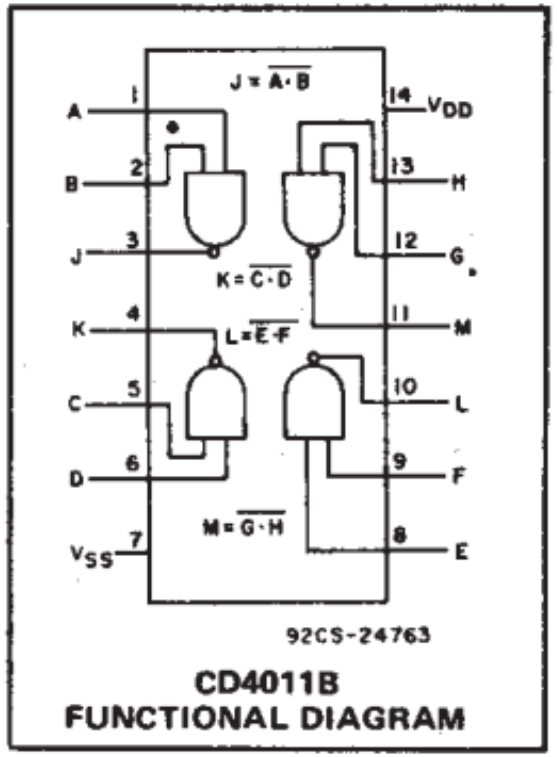
CMOS NAND gate IRL:

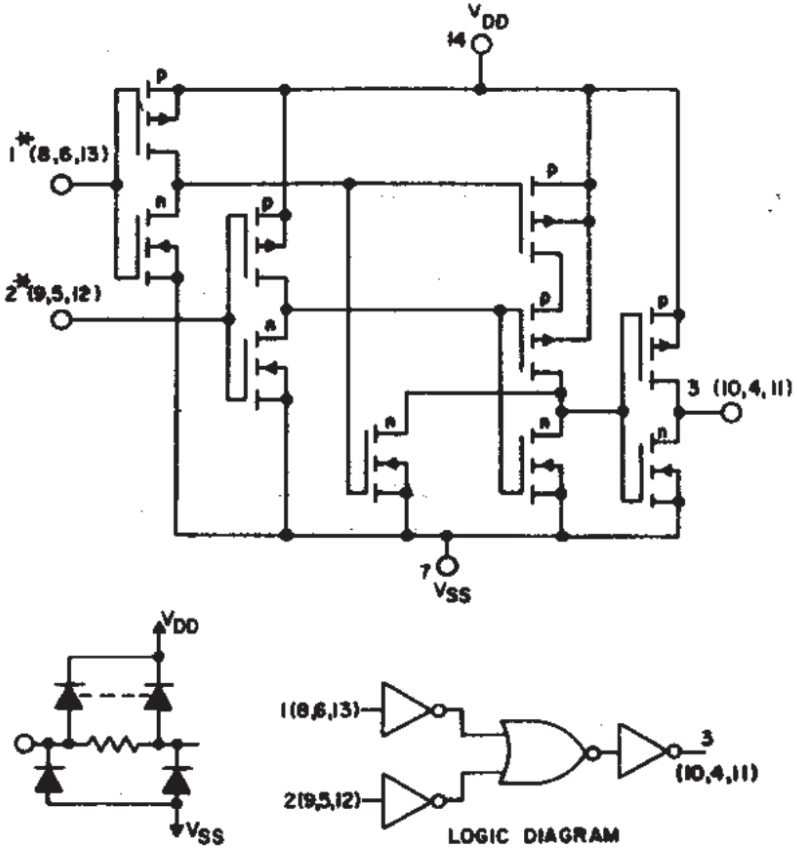
TEXAS INSTRUMENTS

Data sheet acquired from Harris Semiconductor
SCHS021D – Revised September 2003

CMOS NAND GATES



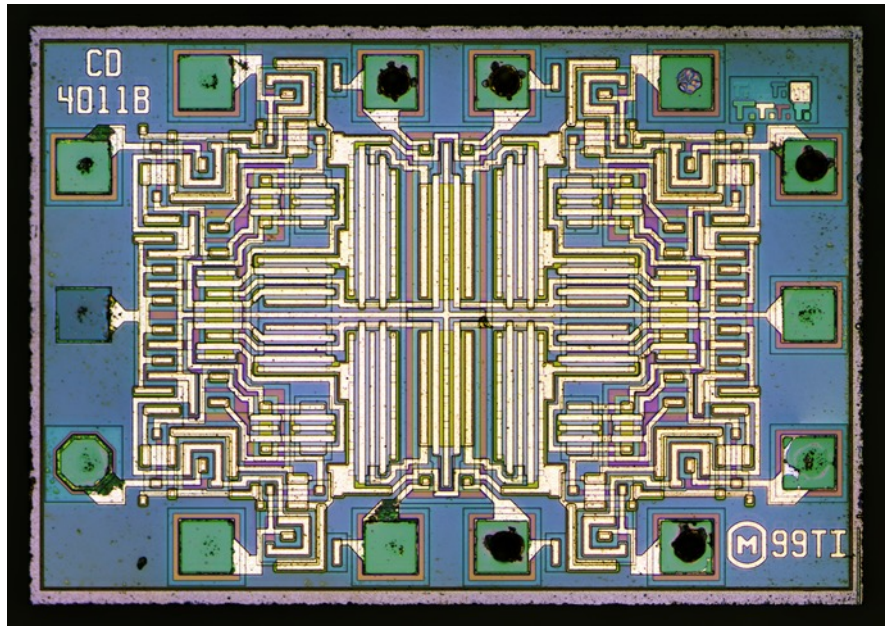
CD4011B
FUNCTIONAL DIAGRAM



* ALL INPUTS ARE PROTECTED BY CMOS PROTECTION NETWORK

1 OF 4 GATES (NUMBERS IN PARENTHESES ARE TERMINAL NUMBERS FOR OTHER GATES)

Fig.7 – Schematic and logic diagrams for CD4011B.



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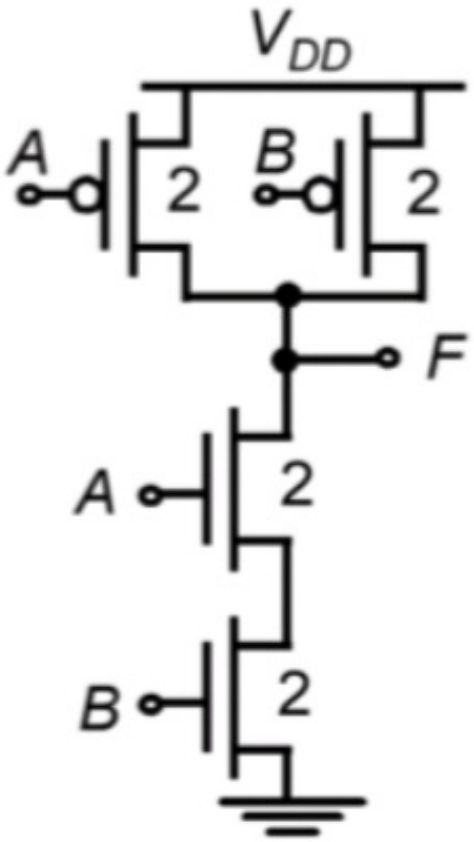
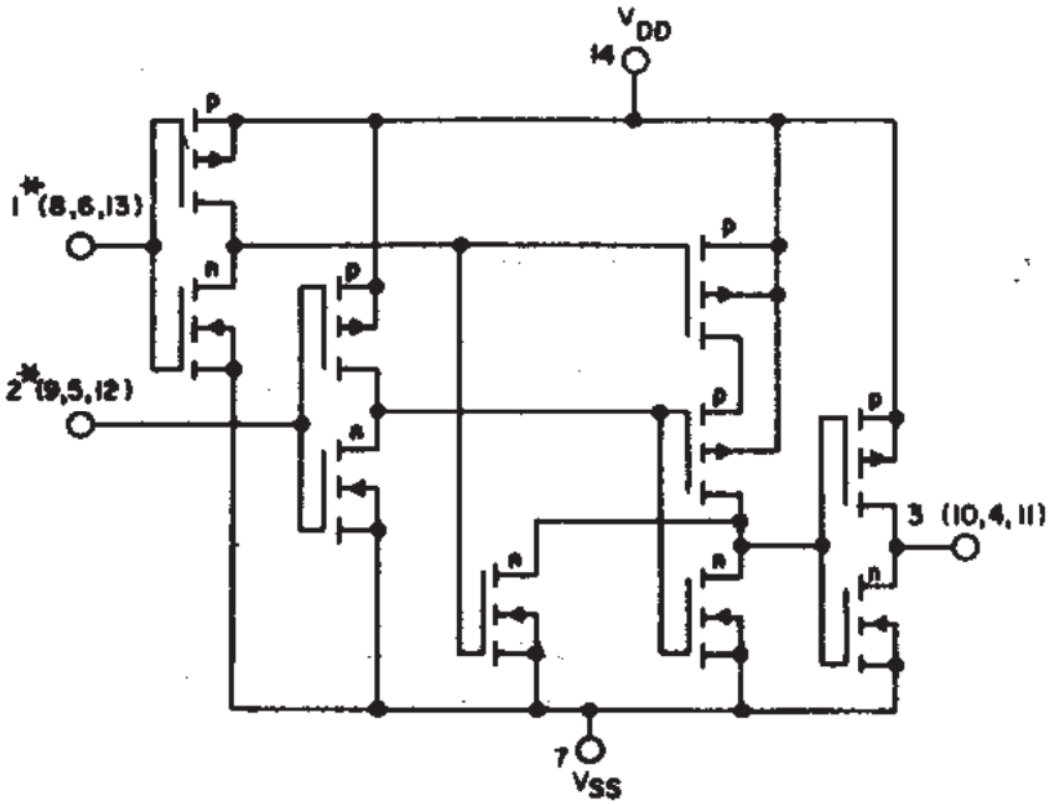
Little class exercise: identify the NAND gate





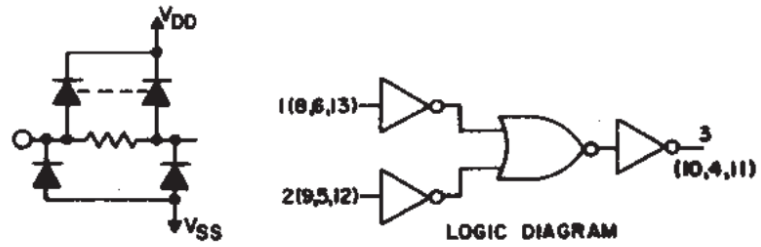


Fig. 7 – Schematic and logic diagrams for CD4011B.

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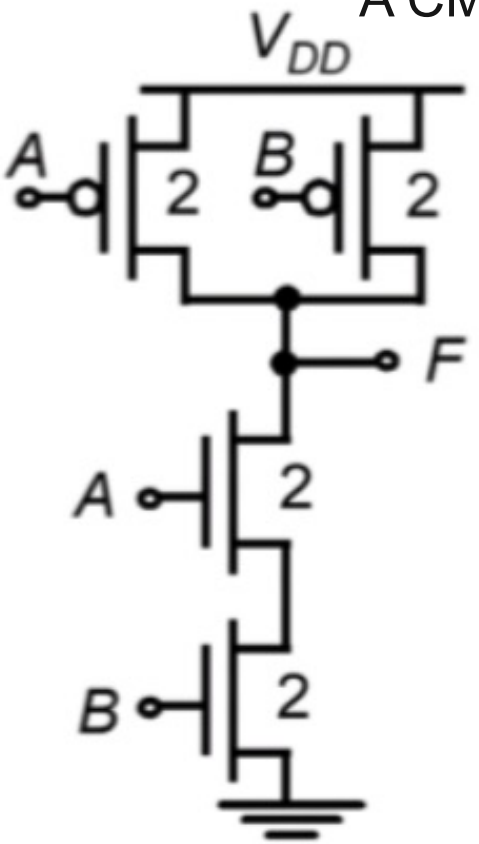
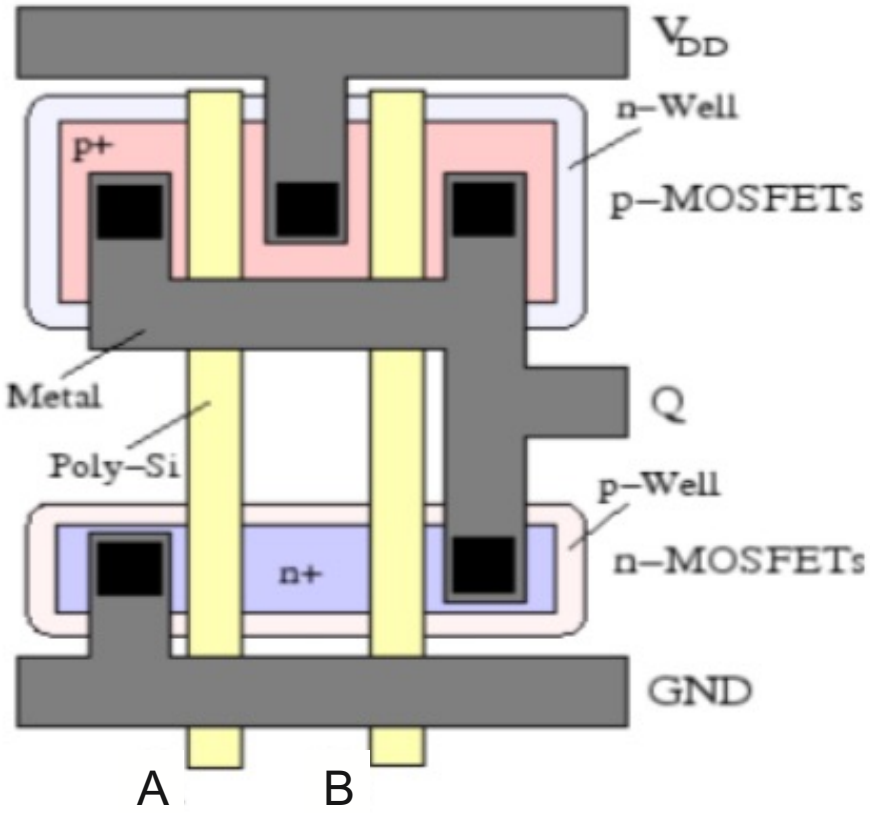
Built in IC: from schematics to layered design

A CMOS NAND gate





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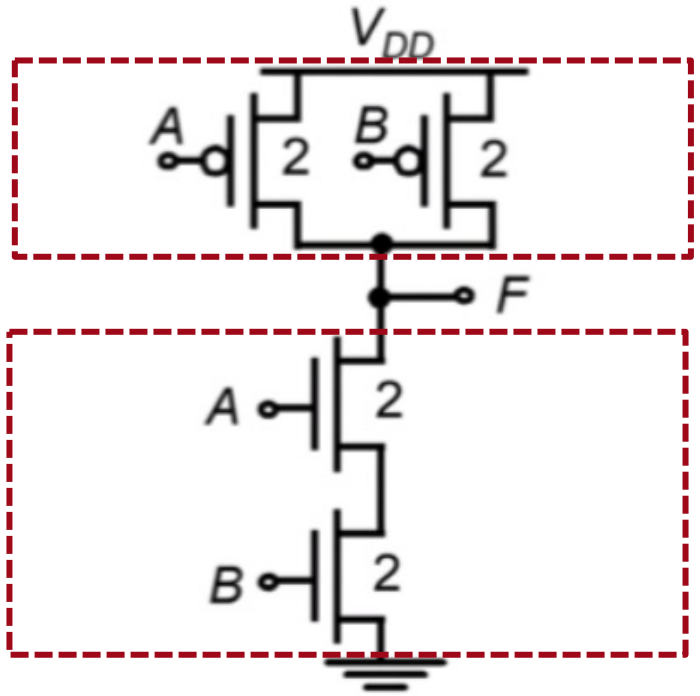
https://www.tutorialspoint.com/vlsi_design/vlsi_design_combinational_mos_logic_circuits.htm

Built in IC: schematics

Logic for NAND: $\overline{A \times B} = \bar{A} + \bar{B}$

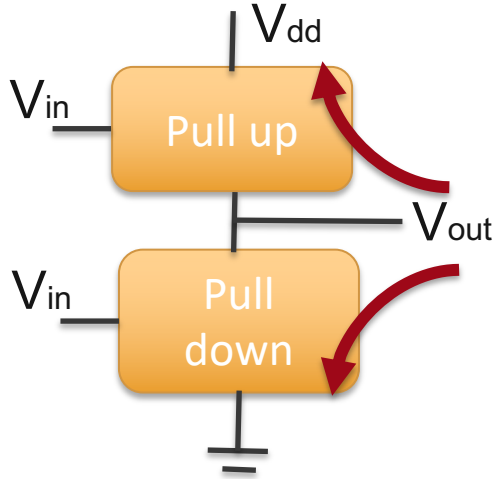


Actual function in the PMOS block

ON: $\bar{A} + \bar{B}$

Actual function in the NMOS block

ON: $A \times B$



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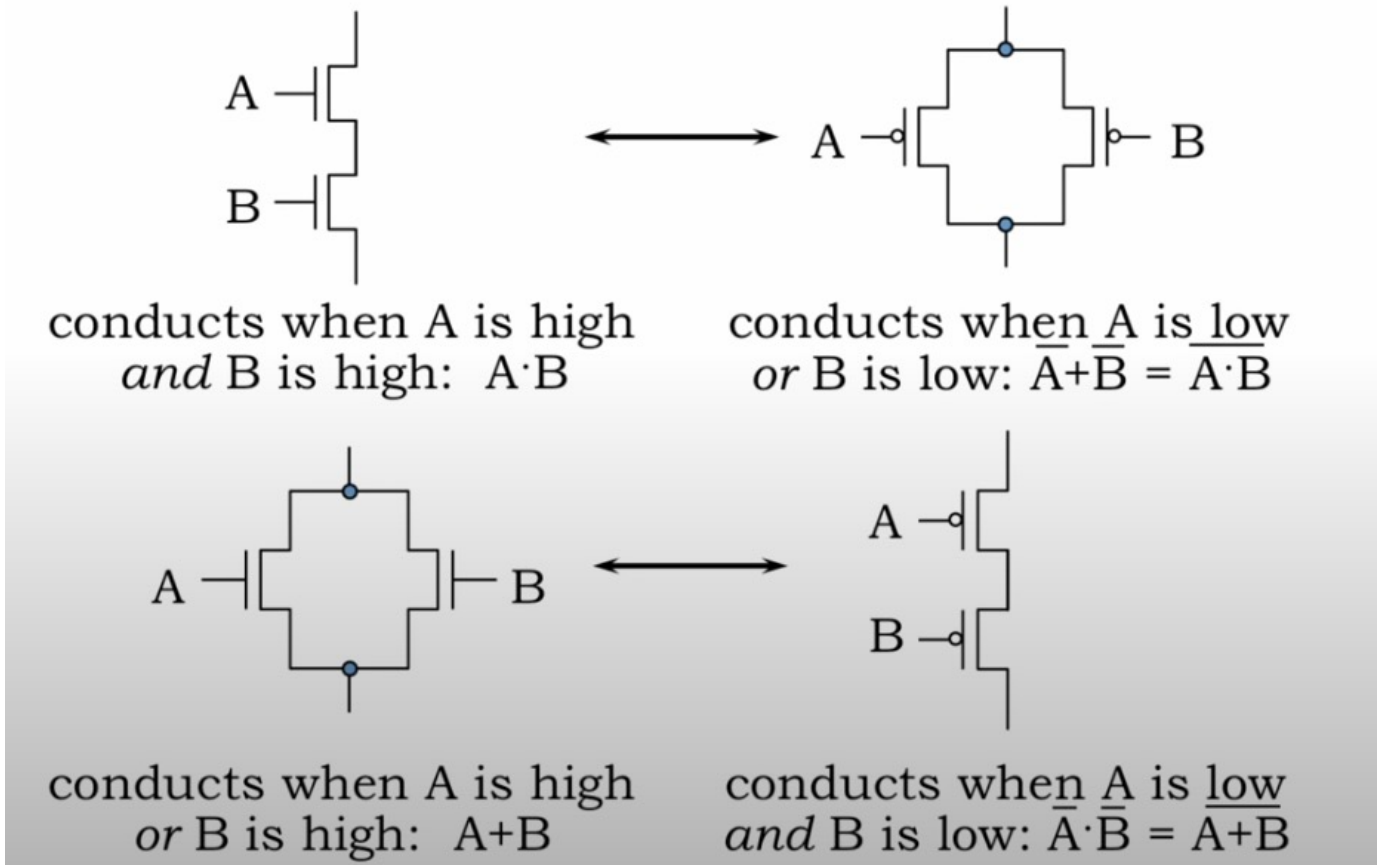
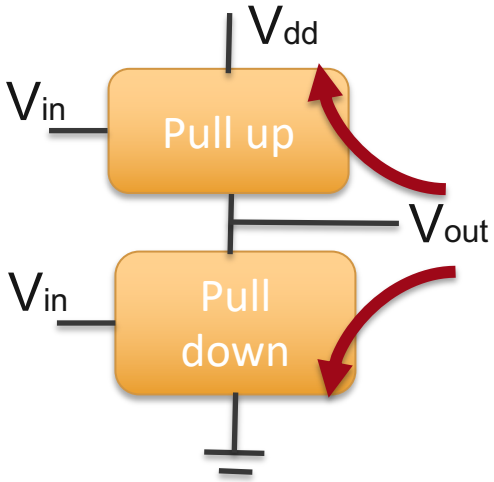
CMOS schematic design is so confined, there's no need for truth table.

Reminder: C is for complimentary



CMOS schematic design, no need for truth table

Target logic operation: $O = \overline{(A+B)\cdot C}$

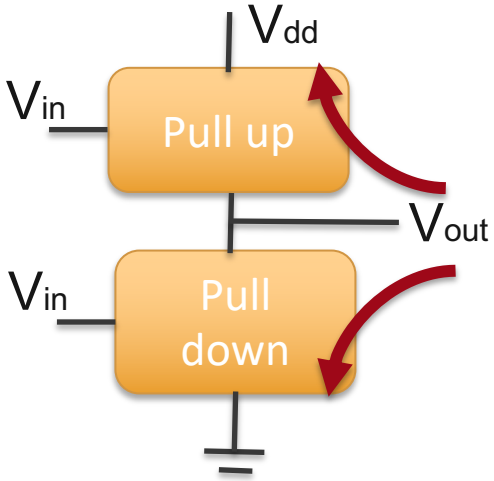


Step 1 (PMOS block): operate for logic high, but with all $\bar{X}$

Step 2 (NMOS block): operate for logic low, thus we are solving for $\overline{O}$

CMOS schematic design, no need for truth table

Target logic operation: $O = \overline{(A+B)\cdot C}$

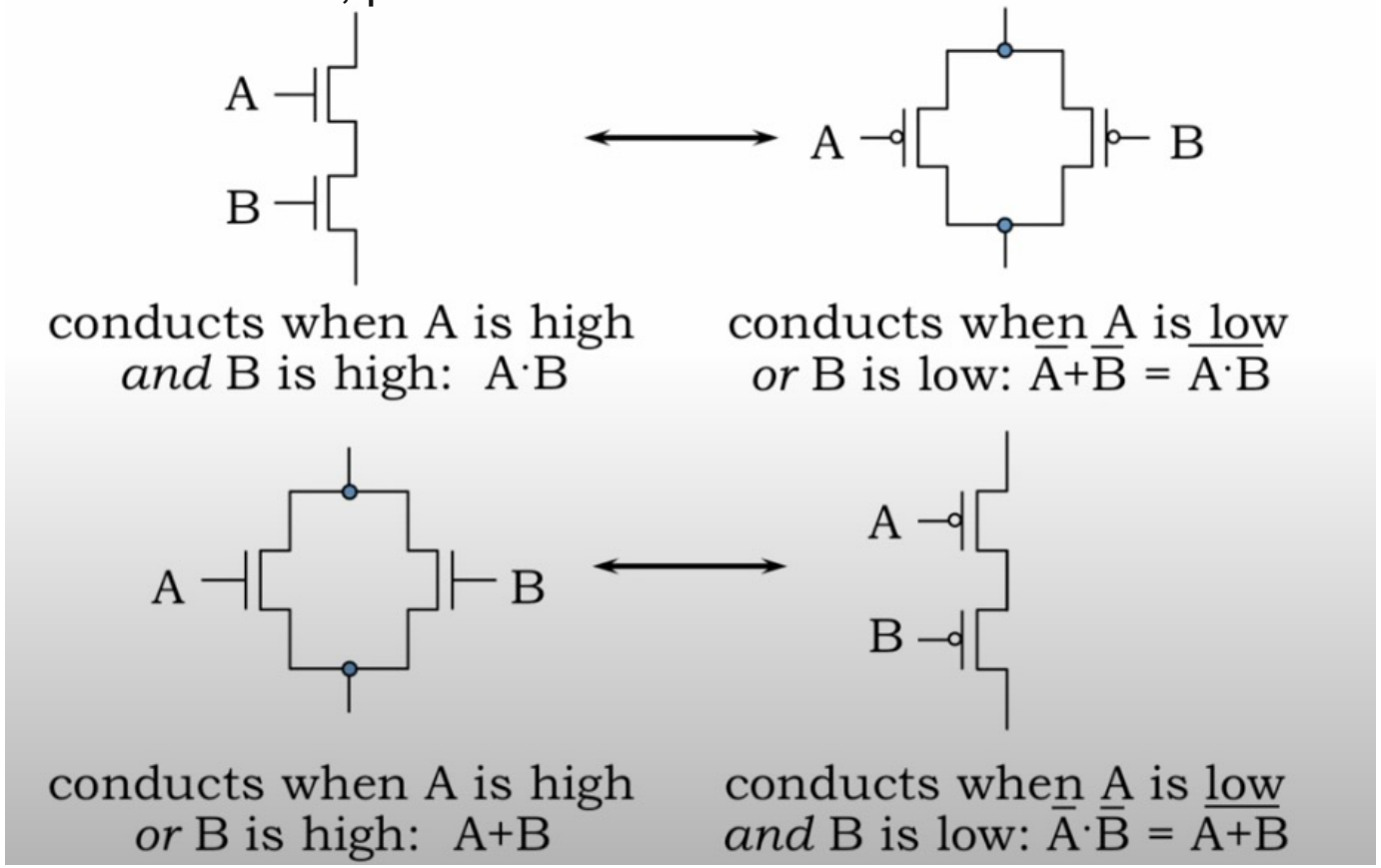


Step 1 (PMOS block): operate for logic high, but with all $\bar{X}$ $\overline{(A\cdot B)}+\overline{C}$

Step 2 (NMOS block): operate for logic low, thus we are solving for $\bar{O}$ $\bar{O} = (A+B)\cdot C$

Or quicker way if we remembered the complimentary rules:

The complimentary rule:
Parallel in NMOS, serial in PMOS
Serial in NMOS, parallel in PMOS



$$O = \overline{(A+B)\cdot C}$$

Step 1:
Pull down (NMOS) $\overline{O} = (A+B)\cdot C$

Step 2:
Pull up (PMOS), just De Morgan it: $\overline{A}\,\overline{B}$ $+\,\overline{C}$

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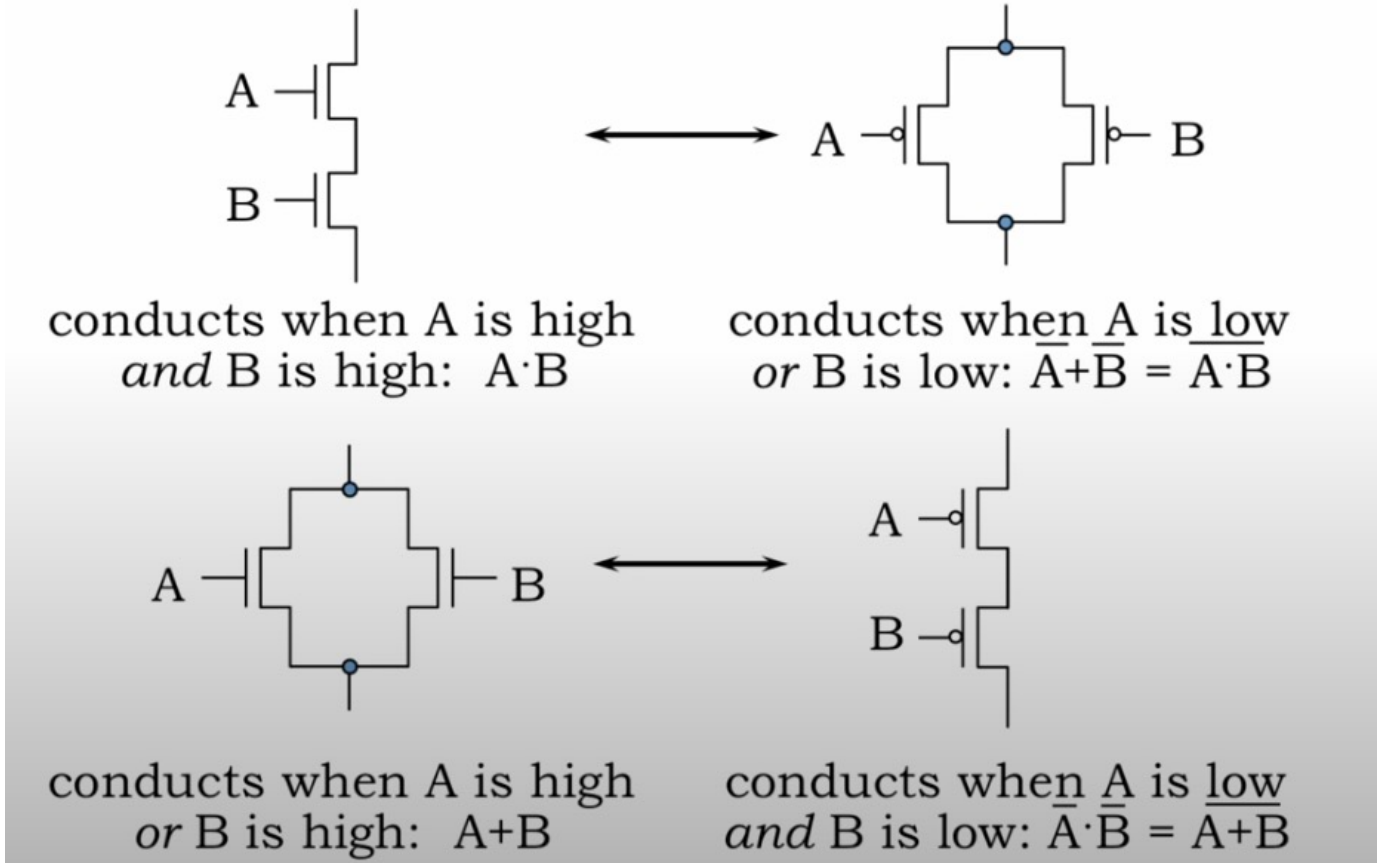
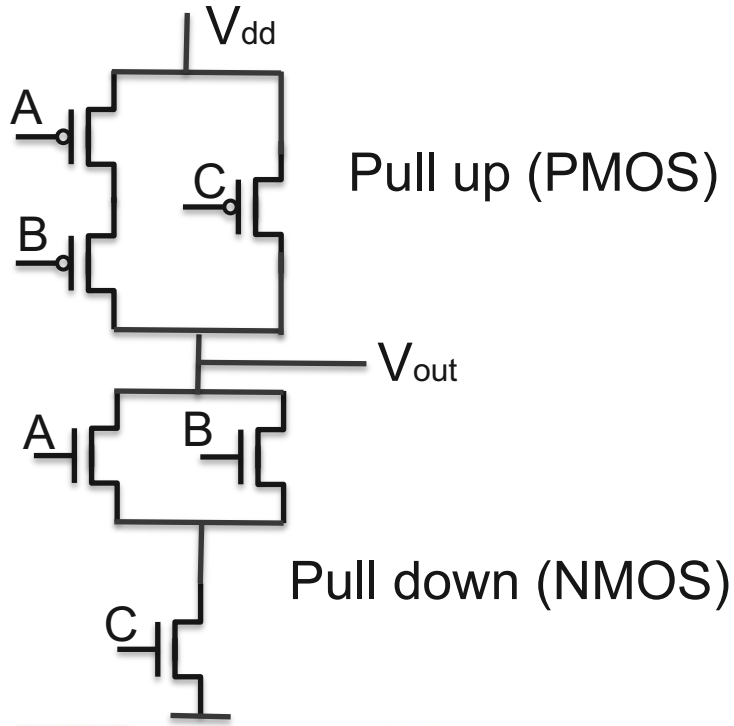
Just write it down, no truth table

The complimentary rule:
Parallel in NMOS, serial in PMOS
Serial in NMOS, parallel in PMOS



CMOS design without truth table

$O = \overline{(A+B) \cdot C}$



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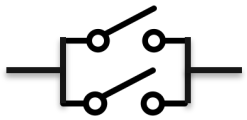
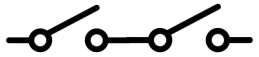
Improved cheat sheet for CMOS design

AND OR logic expressed in mechanical Switches:

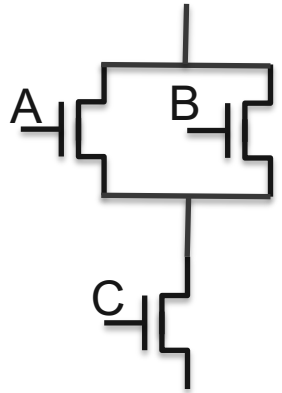
OR: A+B 

AND: A·B 

$$O = \overline{(A+B)\cdot C}$$

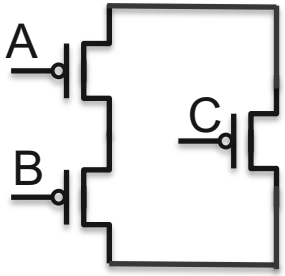
Step 1 NMOS, solve for $\overline{O}$

$$\overline{O} = (A+B)\cdot C$$



As if they are mechanical switches!

Step 2 PMOS, use the complimentary rule:
Parallel in NMOS, serial in PMOS
Serial in NMOS, parallel in PMOS



Step 3 add everything else (I/O, Vdd, GND and wires)

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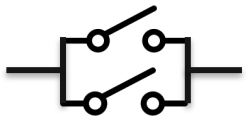
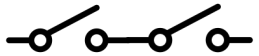
CMOS design, in-class exercise

AND OR logic expressed in mechanical Switches:

$$O = \overline{(A \cdot B + C) \cdot D + E}$$

OR: A+B 

AND: A·B 

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Built in IC: to layered design

https://app.siliwiz.com/

- Introduction to SiliWiz
  How SiliWiz helps you get an understanding of how semiconductors work and are manufactured
- Draw a Resistor
  Learn the basics of SiliWiz while creating a component
- Parasitics
  How we get unwanted parasitics in circuits and what that means
- Voltage Divider
  Divide a number with 2 resistors
- Draw a capacitor
  Understand how capacitance changes and using DRC to check your design
- Draw an N MOSFET
  Active components: draw a MOSFET and make measurements
- Making a logic inverter
  Create a logic gate and discover its shortcomings
- Draw a P type MOSFET
  Learn about the N type MOSFET's complement, the P type MOSFET
- Draw a CMOS inverter
  Understand the benefit of CMOS and explore standard cells

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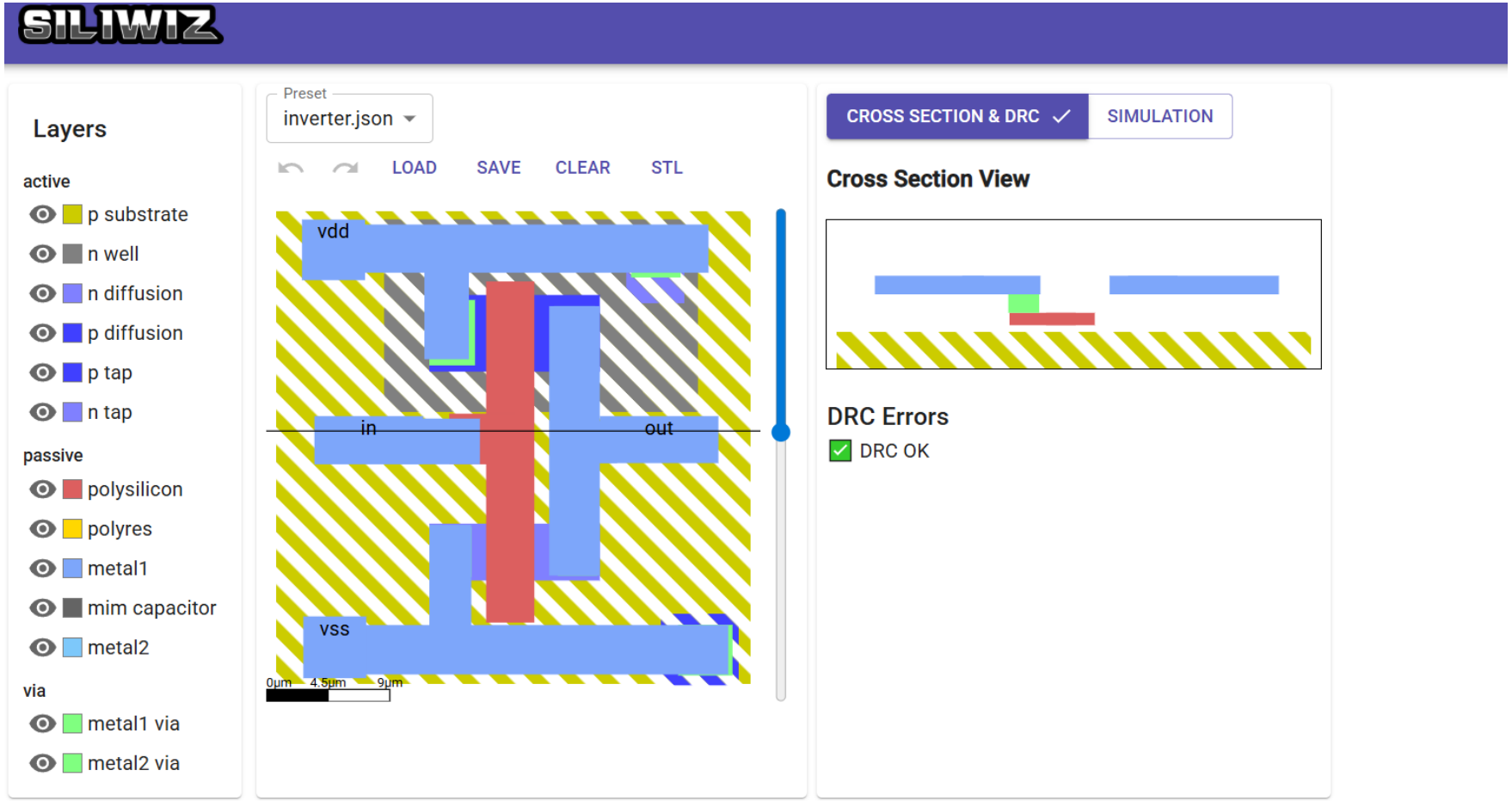
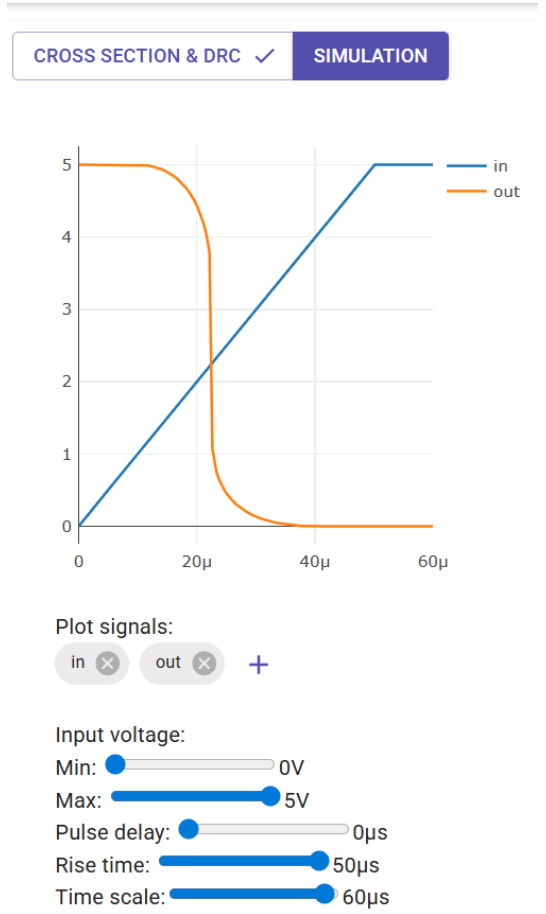
Built in IC: to layered design

https://app.siliwiz.com/





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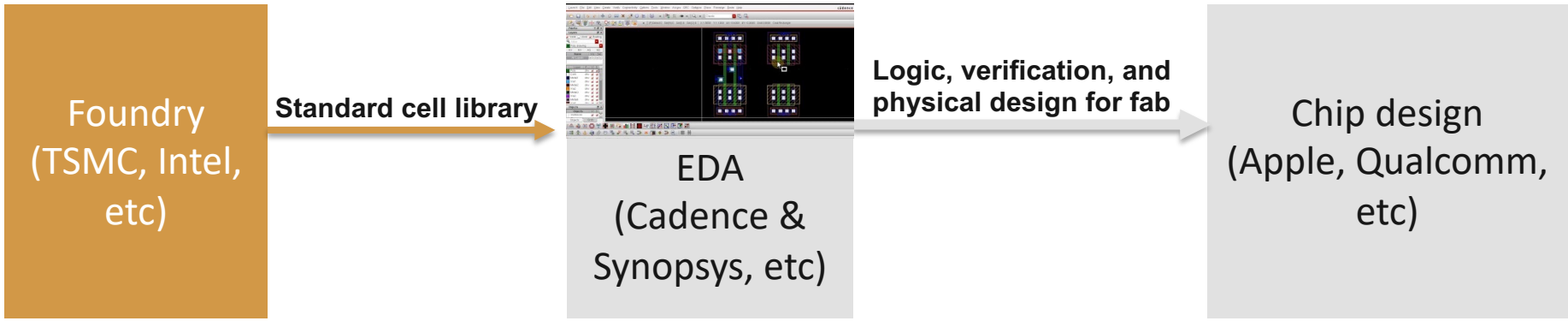
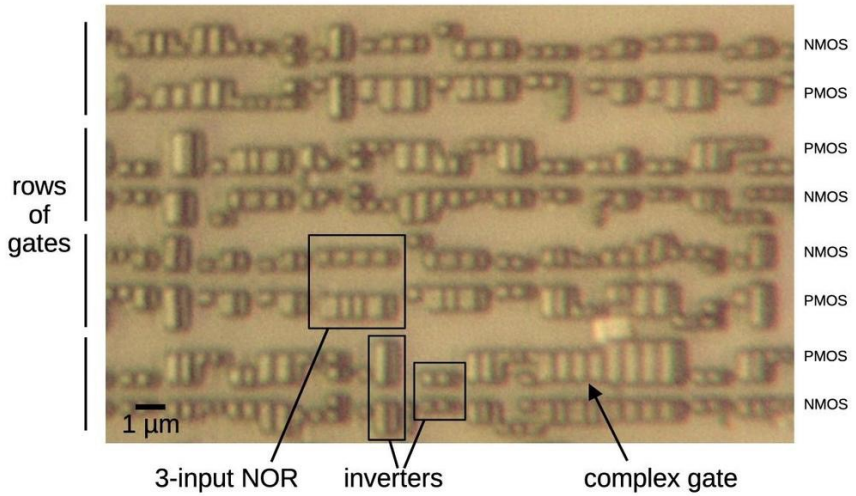
CMOS design for large circuitry



Standard cell logic form a 180 nm CMOS chip in the 90s



https://www.righto.com/2024/06/montreal-mifare-ultralight-nfc.html

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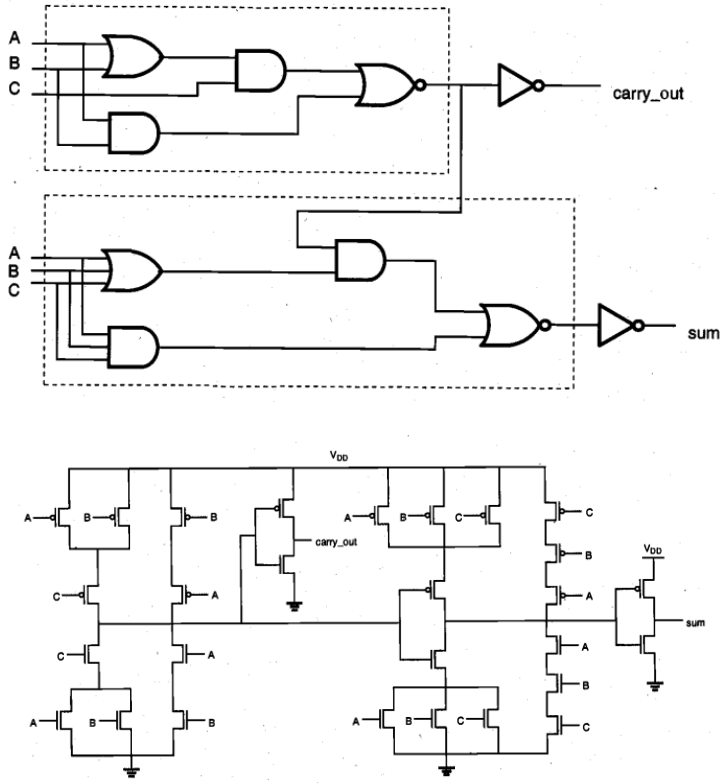
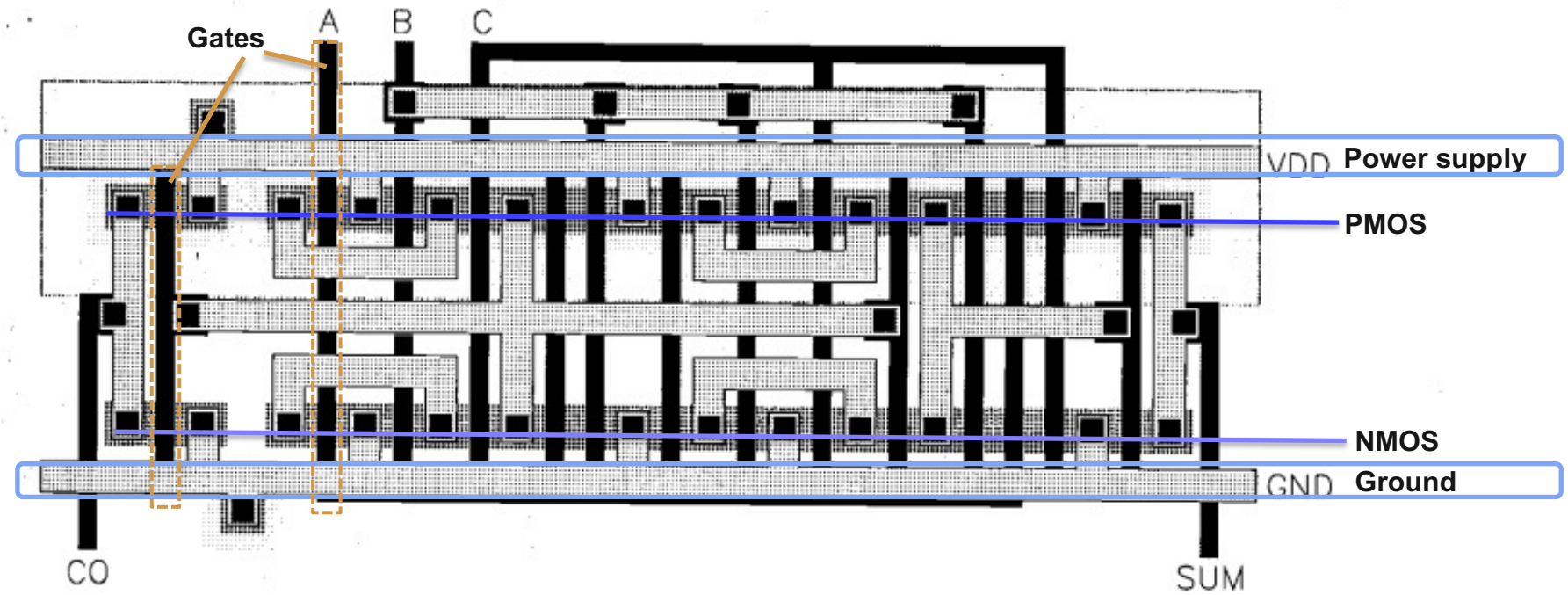
CMOS design rules shown as a full-adder



of being easily adaptable to computer-aided design (CAD). The silicon area occupied by this full-adder layout is (21 μm x 54 μm) = 1134 μm^2.



Mano, M. Morris. *Digital logic and computer design*. 1979

Figure 1.10. Initial layout of the full-adder circuit using minimum-size transistors.

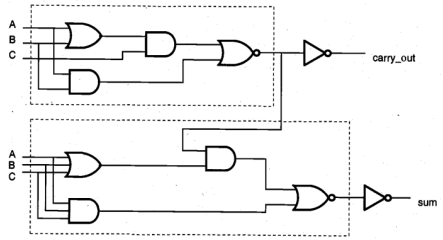
Design our own IC, yes we can!

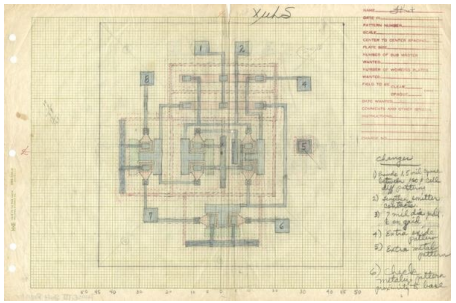
The general process flow

IC spec → Circuits design → Physical design → Test and sign off

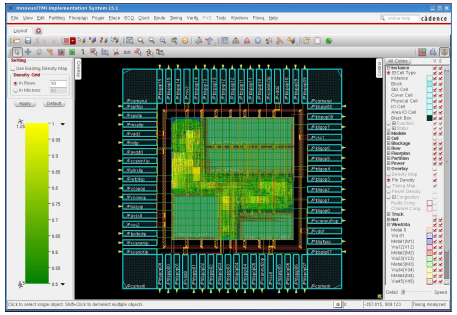
- **High level requirements**
- **Customer needs**

- **Logic circuits**
- **Memory circuits**
- **Netlist of every groupings**





Hand draw mask layout, Fairchild 1960
https://www.computerhistory.org/revolution/digital-logic/12/287



cadence

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Design our own IC, yes we can!

https://tinytapeout.com/siliwiz/
https://app.siliwiz.com/
https://github.com/ncsu-eda/FreePDK3

Google + skywater TECHNOLOGY

FOSS 130nm Production PDK
github.com/google/skywater-pdk

FreePDK3

Design Rule Manual

Revision: 1.0

Process Node: 3nm

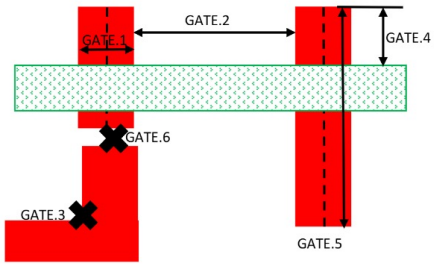
Release Date: August 30, 2021

- PDK are design rules set by the foundry. With opensource support, it is technically possible to generate a design file (GDS) and get your IC chips fabricated.

Example of design rules from FreePDK3 by NCSU, 2021

2.6 Gate Layer

Rule	Value	Description
GATE.1	15 nm	GATE exact horizontal width
GATE.2	27 nm	Minimum horizontal spacing between GATE or DUMMY layers
GATE.3		GATE may not bend
GATE.4	21.5 nm	GATE min extension past ACT
GATE.5	40 nm	GATE minimum vertical length
GATE.6		GATE may not be discontinuous along the vertical axis. Use GCUT layer to mark cuts in the GATE
GATE.7		ACT layer vertical edge may not lie inside, or coincide with, the GATE layer
GATE.8	6 nm	Minimum horizontal spacing between ACT and GATE (not cut by GCUT and not interacting with ACT)



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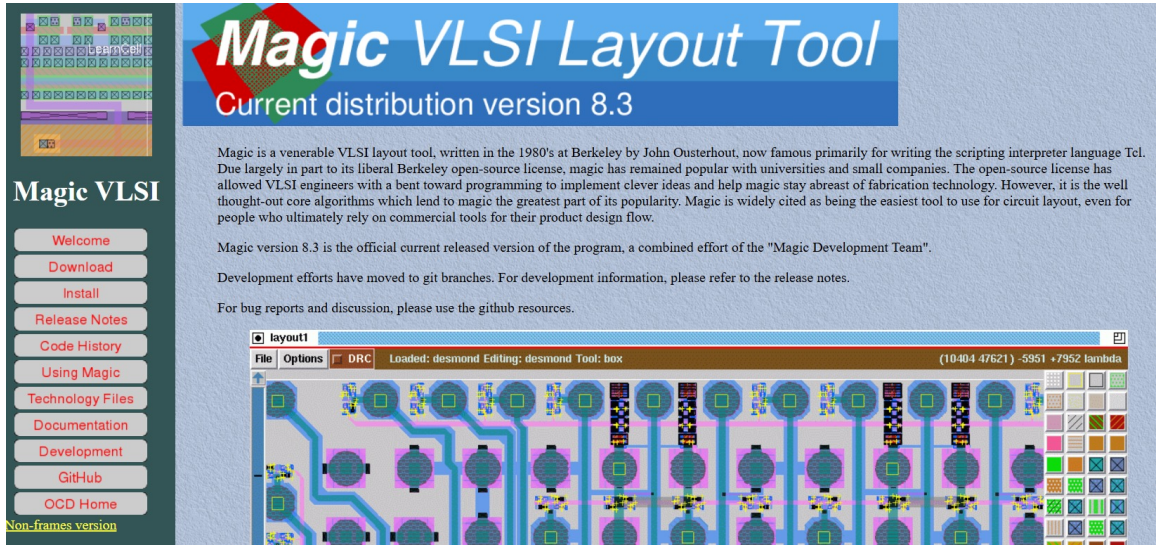
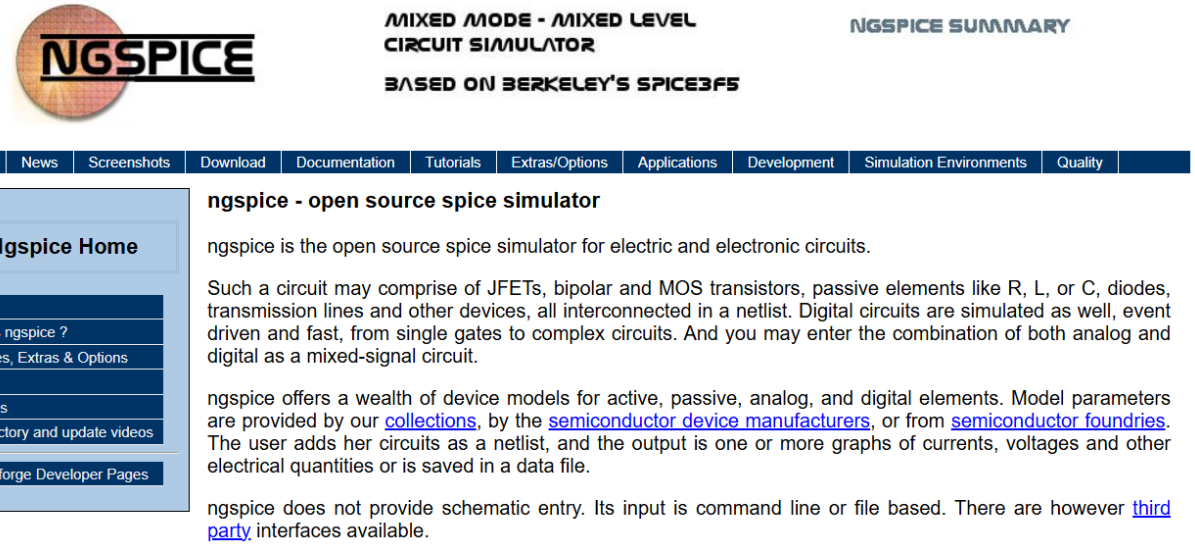
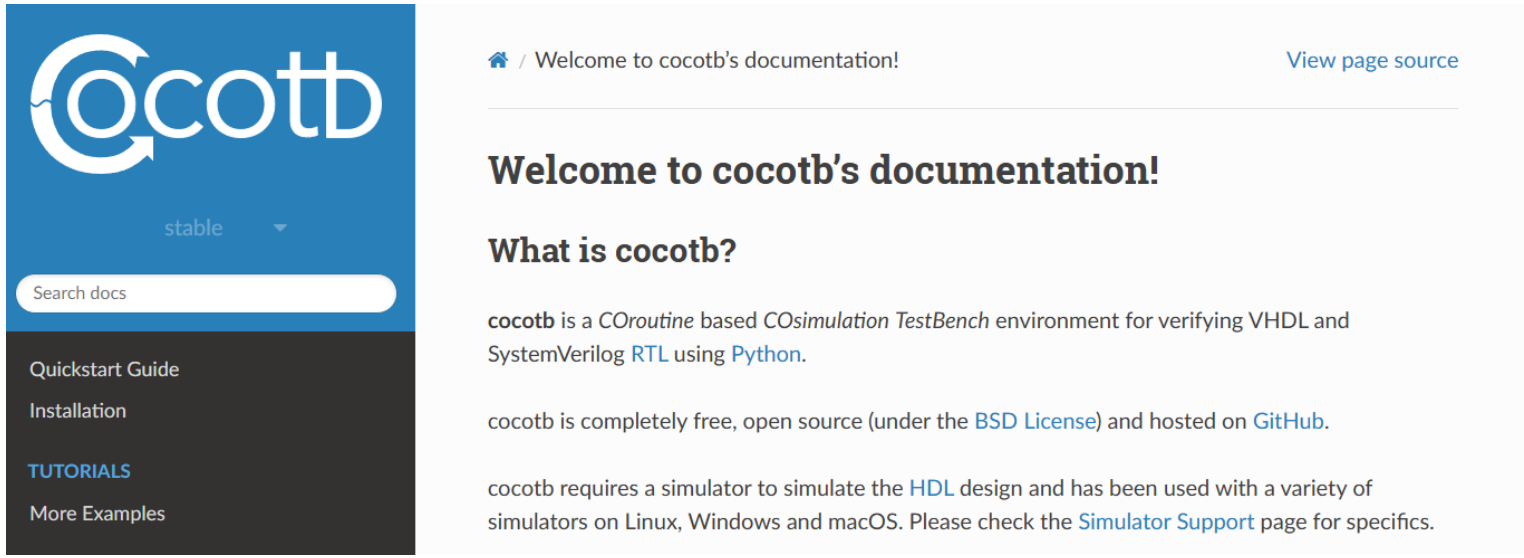
Into the realm of digital design







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The state of the art for CMOS:

The "nm" race

MOSFET scaling (process nodes)

- 20 µm – 1968
- 10 µm – 1971
- 6 µm – 1974
- 3 µm – 1977
- 1.5 µm – 1981
- 1 µm – 1984
- 800 nm – 1987 ← First FinFET fabrication by Hitachi
- 600 nm – 1990
- 350 nm – 1993
- 250 nm – 1996
- 180 nm – 1999
- 130 nm – 2001
- 90 nm – 2003
- 65 nm – 2005
- 45 nm – 2007
- 32 nm – 2009
- 28 nm – 2010
- 22 nm – 2012 ← First FinFET chip by Intel
- 14 nm – 2014 ← TSMC starting chip supply (SoC) to Apple
- 10 nm – 2016
- 7 nm – 2018 ← GlobalFoundries (AMD) stopping R&D
- 5 nm – 2020
- 3 nm – 2022 ← TSMC FinFET mass rollout

Future

- 2 nm ~ 2025 ← TSMC leading
- 1 nm ~ 2027

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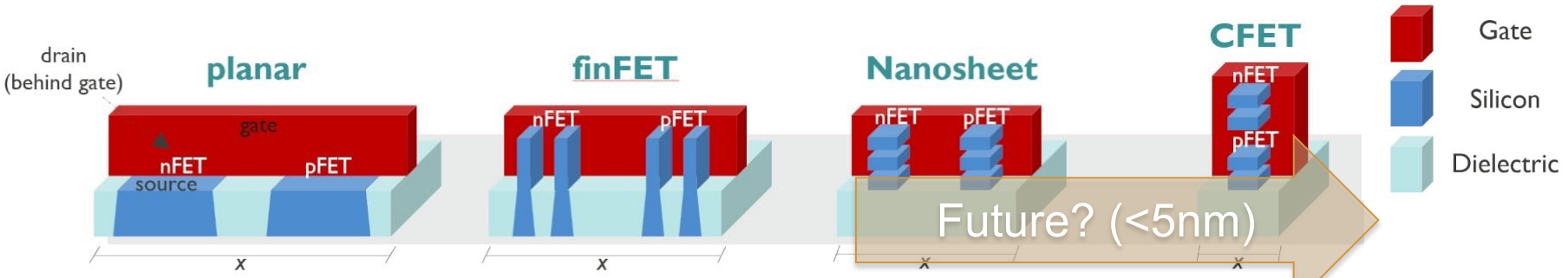
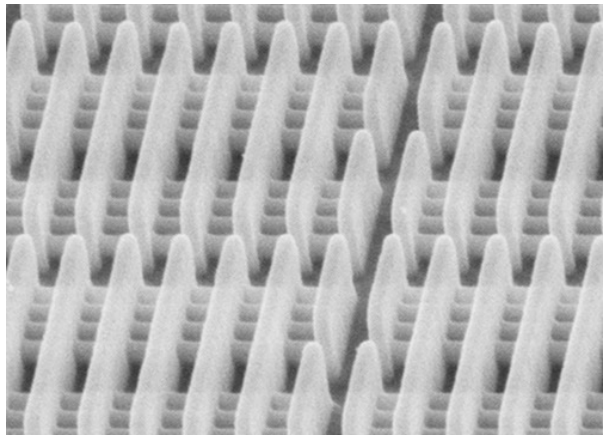
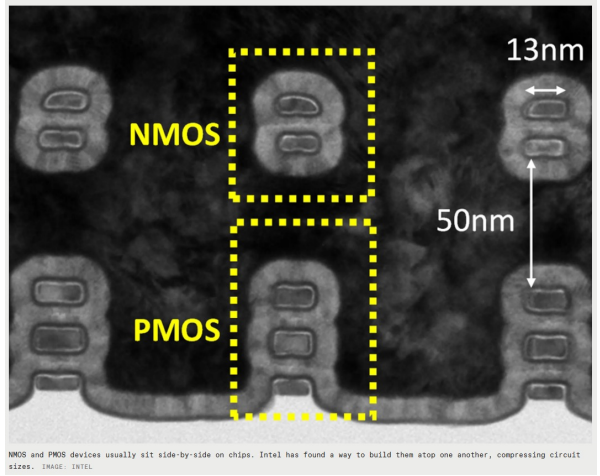


https://www.electronicdesign.com/

16nm Fin Field Effect Transistor, TSMC



Nanosheet inverter, Intel reported in 2020



https://spectrum.ieee.org/

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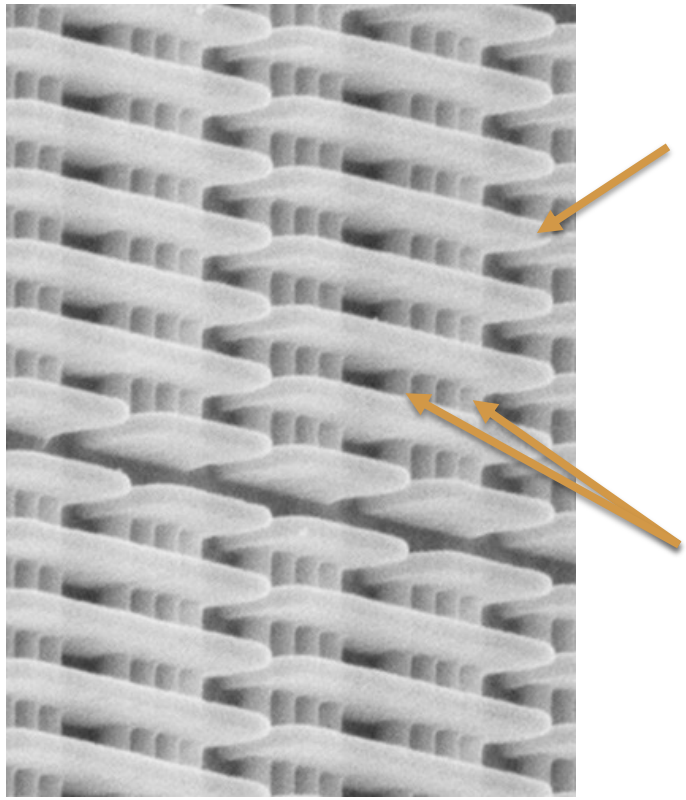
FinFET



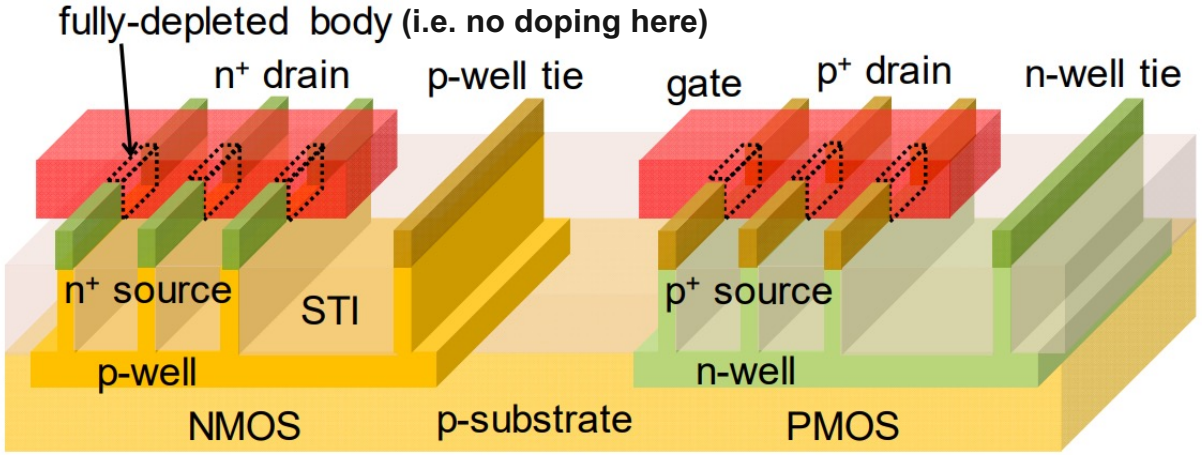


Fig. 1. Fully depleted bulk CMOS finFETs. DOI:10.1109/CICC.2018.8357060

- The dimension of the fin is confined by the foundry (TSMC).
- The number of the fin can be adjusted to get different gate current.
- The fin stacks and gate can then be cut or connected.

CMOS inverter layout example

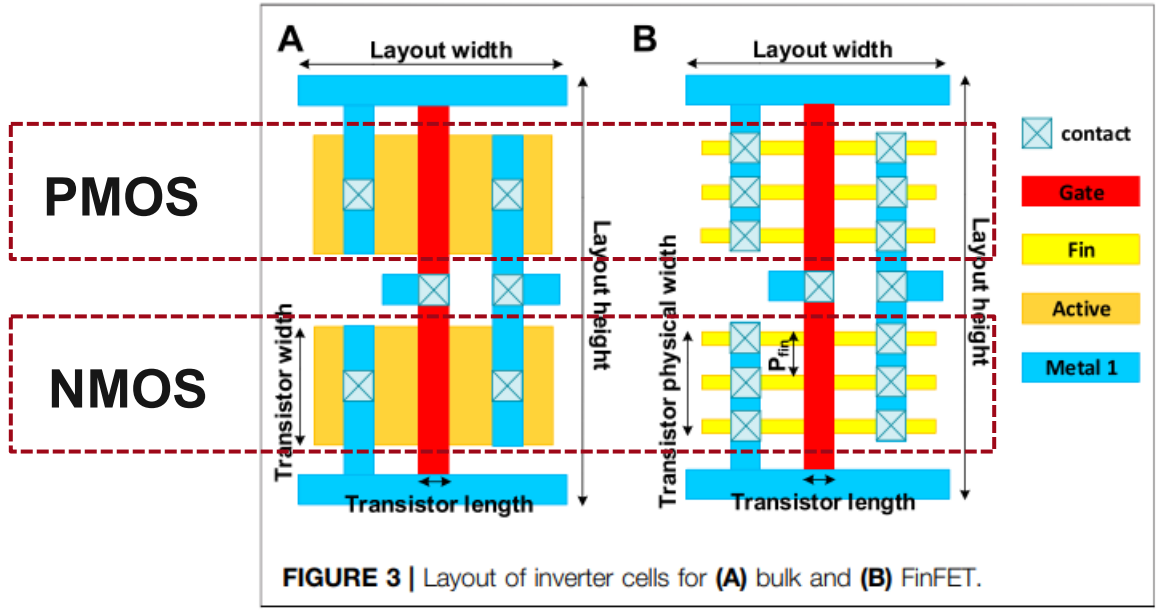
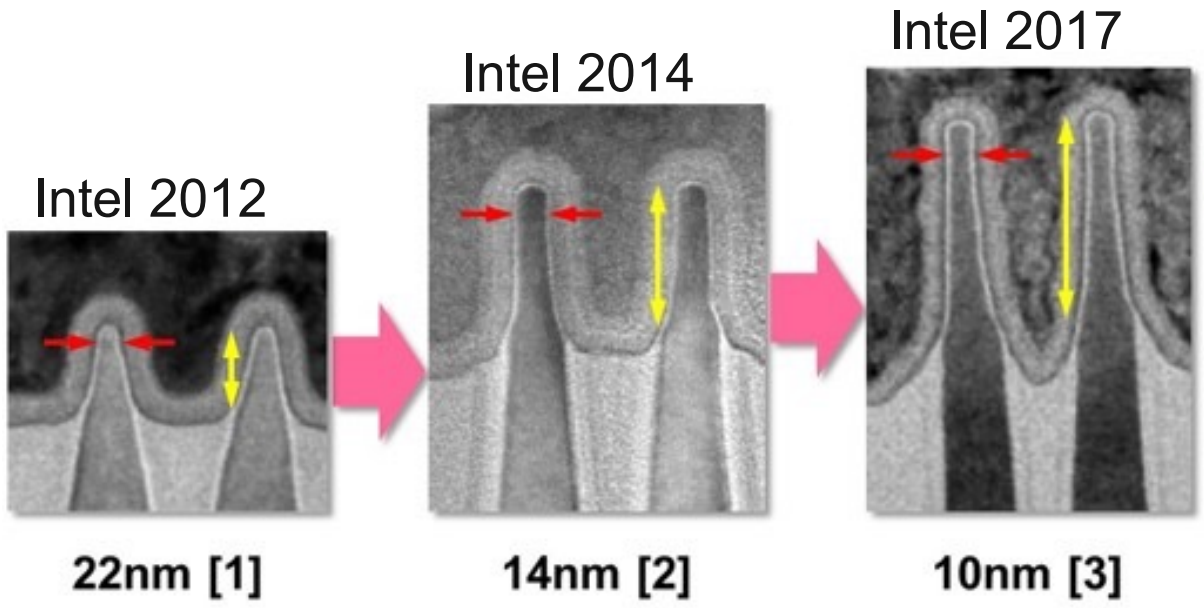


FIGURE 3 | Layout of inverter cells for (A) bulk and (B) FinFET.

DOI: 10.3389/frai.2021.659060

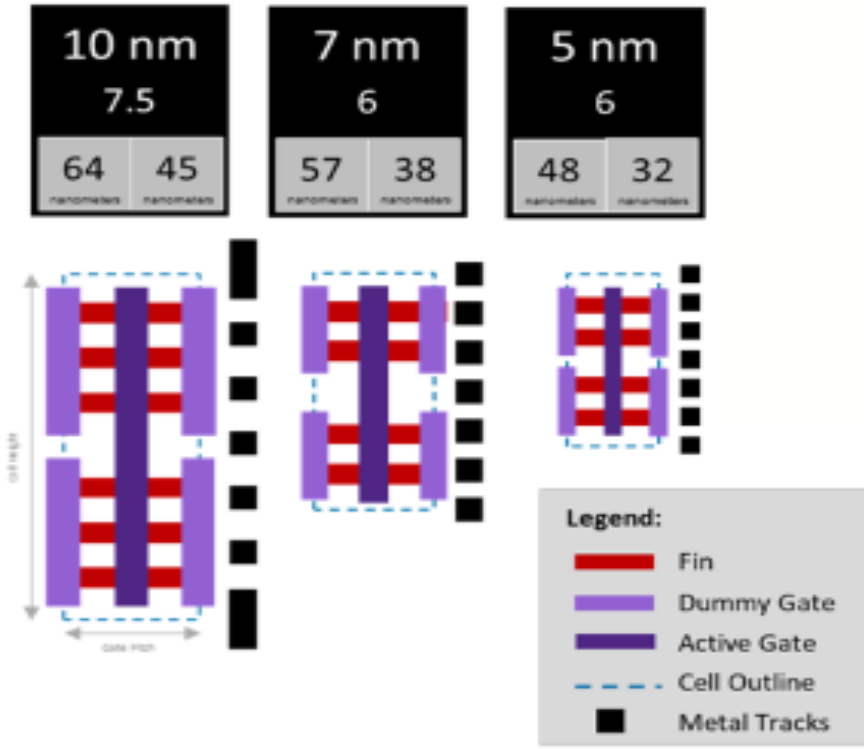
FinFET iteration

Tall fin



https://semiengineering.com/selective-removal-for-stronger-fins/

Fin depopulation



https://www.eetimes.com/what-to-expect-at-5-nm-and-beyond-and-what-that-means-for-eda/

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