ENR-325/325L Principles of Digital Electronics and Laboratory

Xiang Li

Fall 2025

COE COLLEGE

Digital electronics: the multi-staged abstraction:

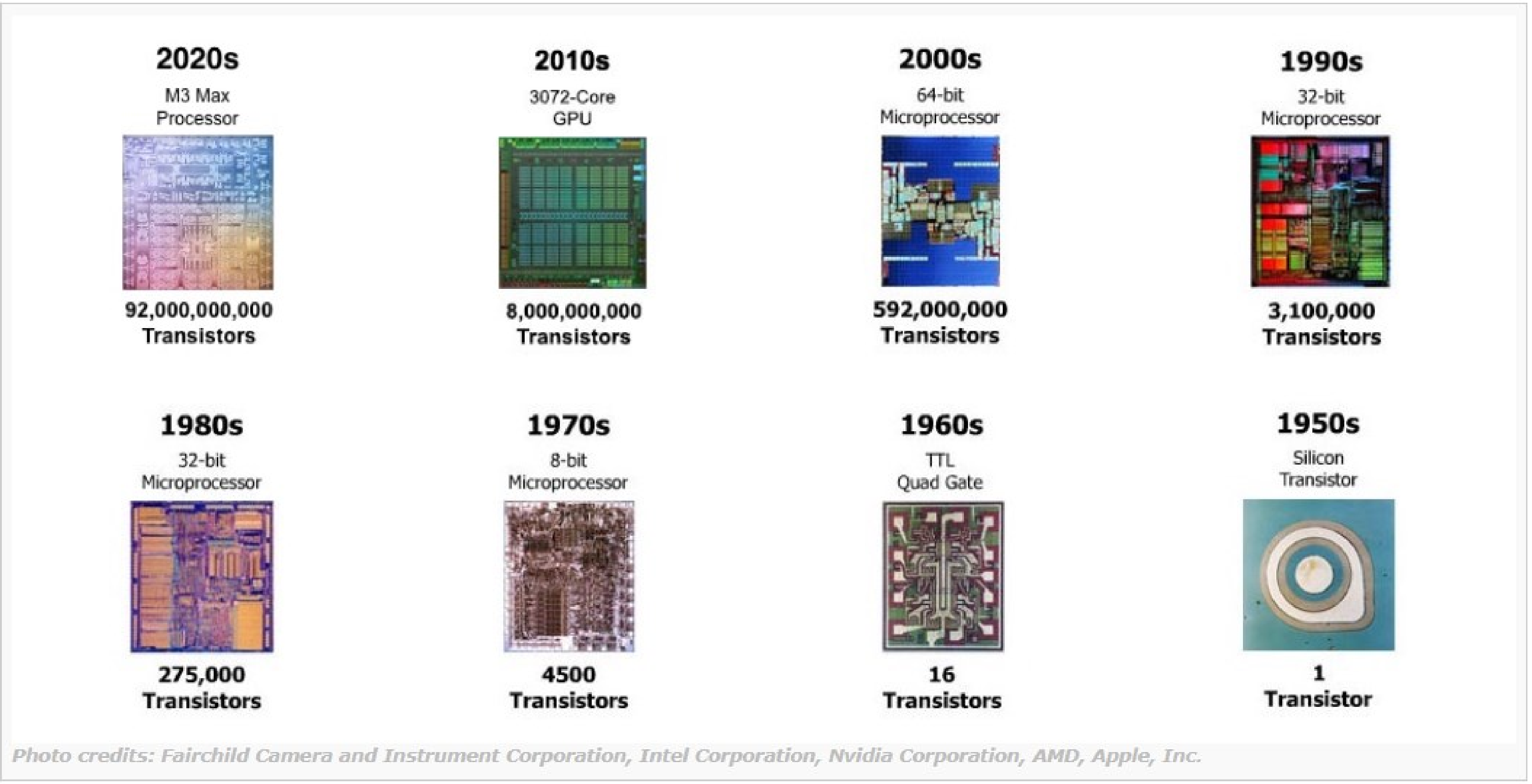
Application	EE	CE	MicroE

E PROTECTED BY
ION NETWORK

ams for CD4001B.

https://www.ti.com/product/CD4001B/part-details/CD4001BM

How the arithmetic and logic functions are physically realized



https://www.computerhistory.org/siliconengine/timeline/

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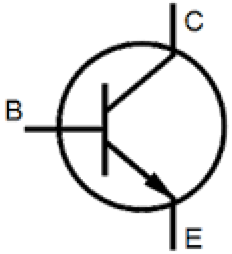
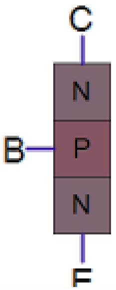
…and it's very different from the macro world

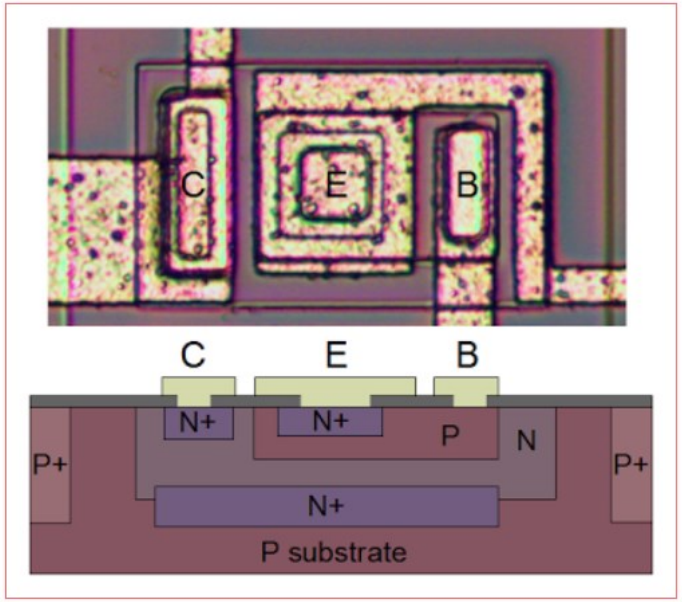
- Example: how op amps chips ACTUALLY works:

NPN BJT in theory:

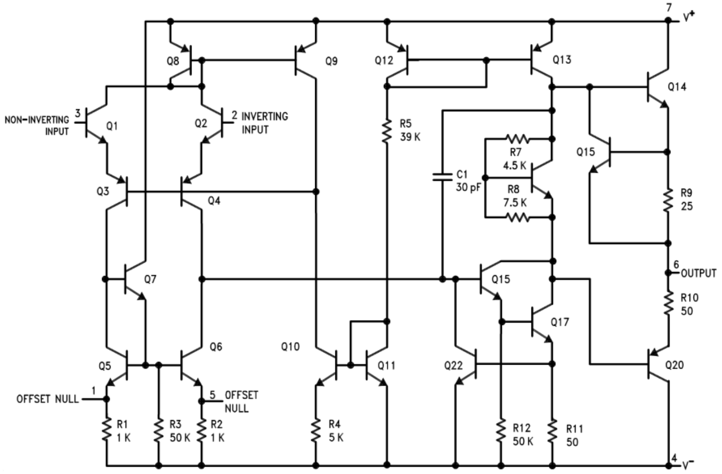


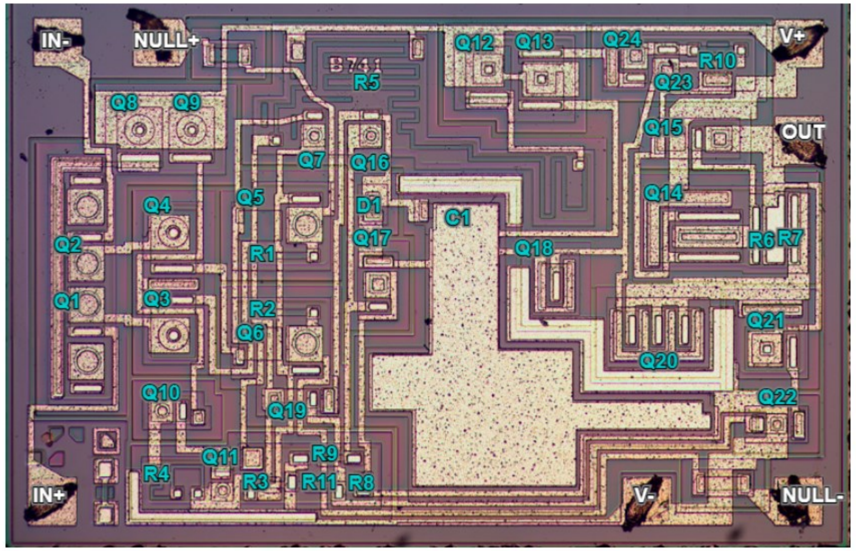


NPN BJT in IC:



7.2 Functional Block Diagram

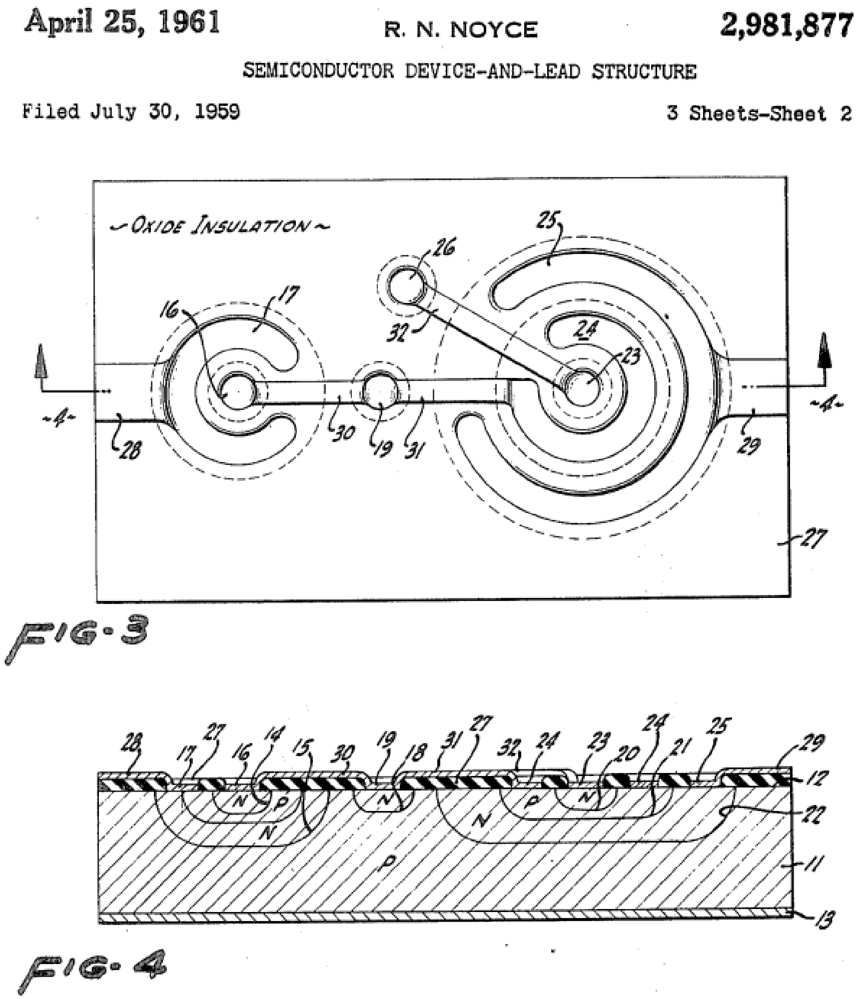


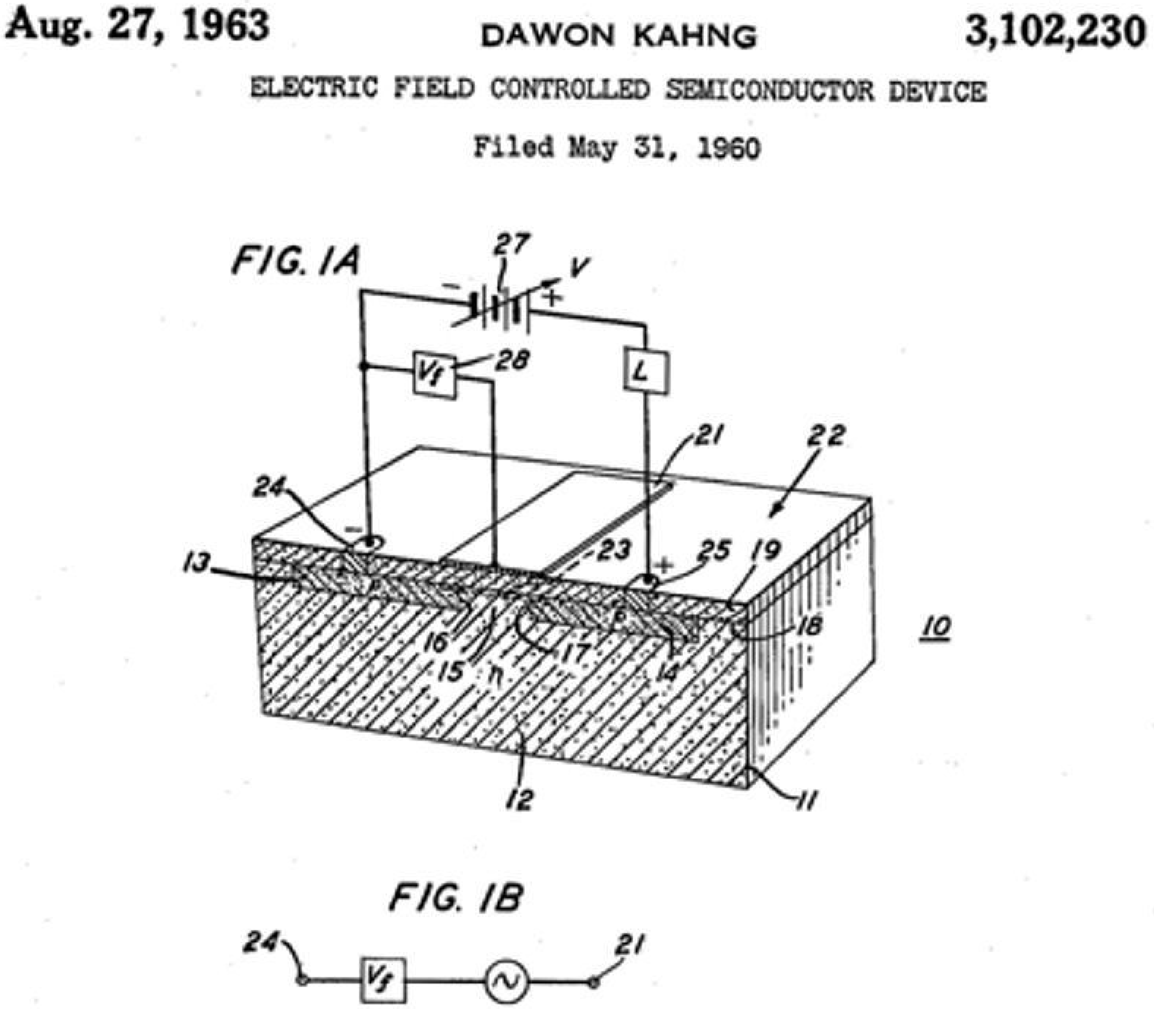


https://www.righto.com/2015/10/inside-ubiquitous-741-op-amp-circuits.html

The MOSFET revolution

Robert Noyce, inventor of silicon IC and “mayor of silicon valley”

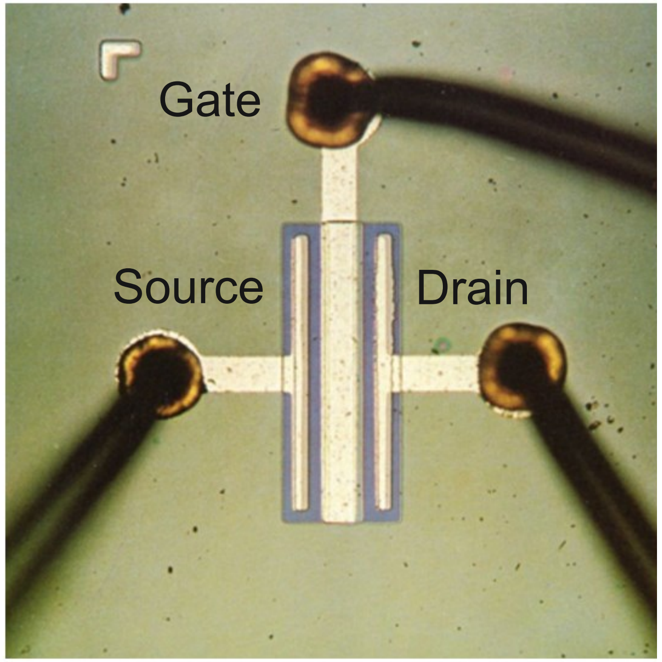




Mohamed Atalla and Dawon Kahng’s MOS transistor patent. At the time it was 100 times slower than BJT.

The MOSFET revolution

MOS works on “surface physics”:
Solid state, band gap theories, tunneling effects…



Fairchild FI 100 p-channel MOS switching transistor
Credit: Fairchild Camera & Instrument Corporation

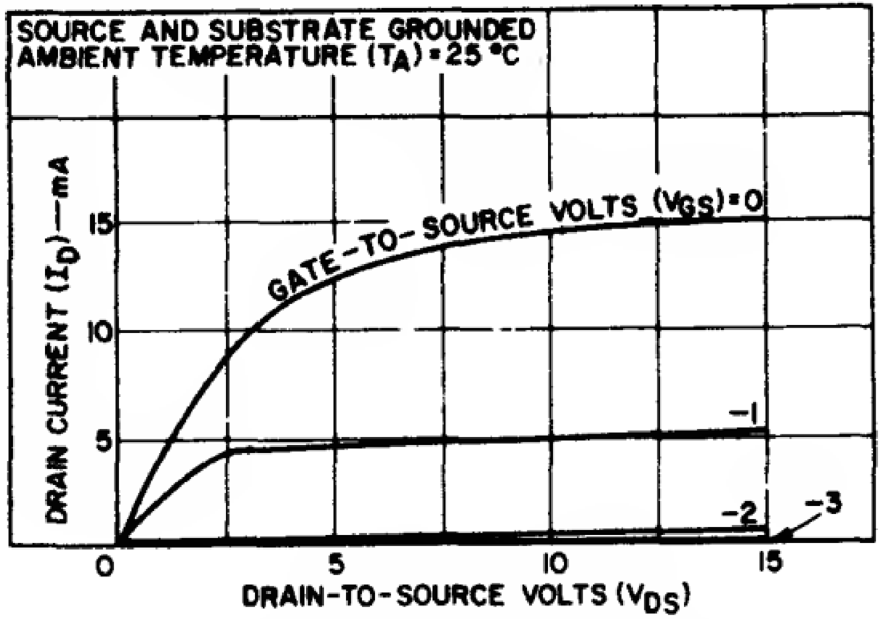


Fig. 1 - Transfer characteristics for the RCA 3N128 vhf MOS transistor.

RCA IC and MOSFET Applications Notes, 1983

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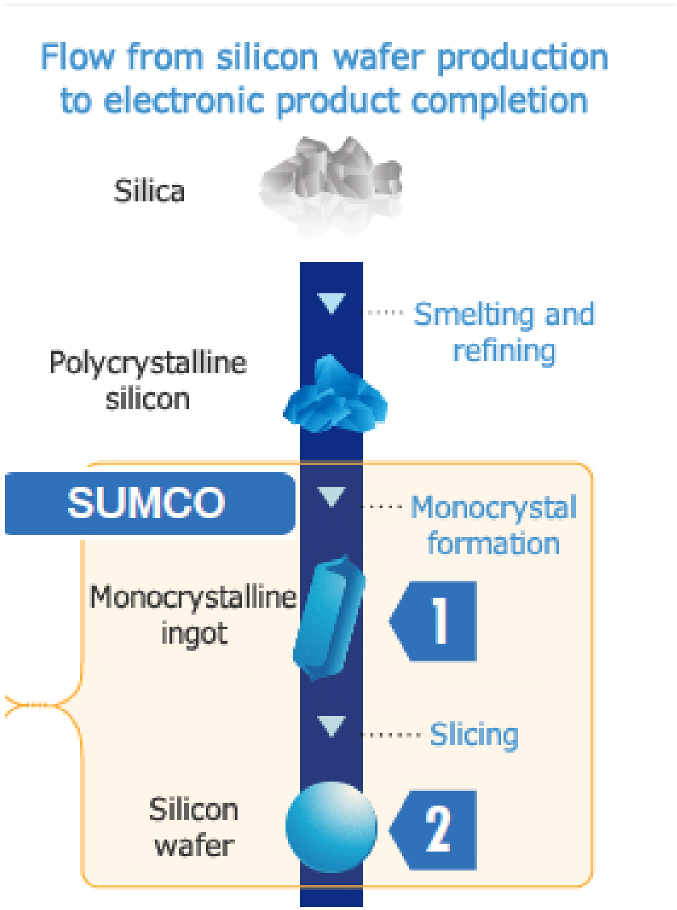
https://www.computerhistory.org/siliconengine/timeline/

Bonus slide: how silicon wafer is made



https://www.sumcosi.com/

Czochralski Process

Sliced and polished wafer

Bonus slide: how silicon wafer is sold:

https://order.universitywafer.com/default.aspx?cat=Silicon

Qty	ID ↑	Price Per Qty	Diam ↓	Type ↑	Dopant ↑	Orien ↑	Res (Ohm-cm)	Thick (um)	Polish ↑	Grade ↑
100 ▾	3105	$11.22	25.4mm	P	B	<100>	.01-.05	500um	DSP	Test
10 ▾	4170	$92.00	300mm	P	B	<100>	1-100ohm.cm	775um	DSP	Dummy
500 ▾	704	$10.09	200mm					750um	SSP	MECH

The MOSFET fabrication

It was made with…

Surface modification like photolithography

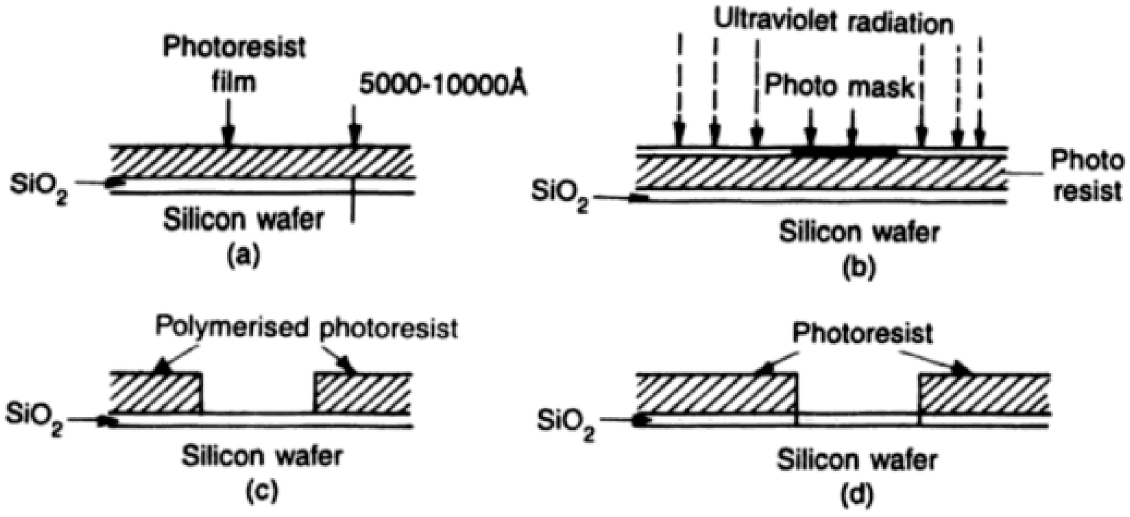
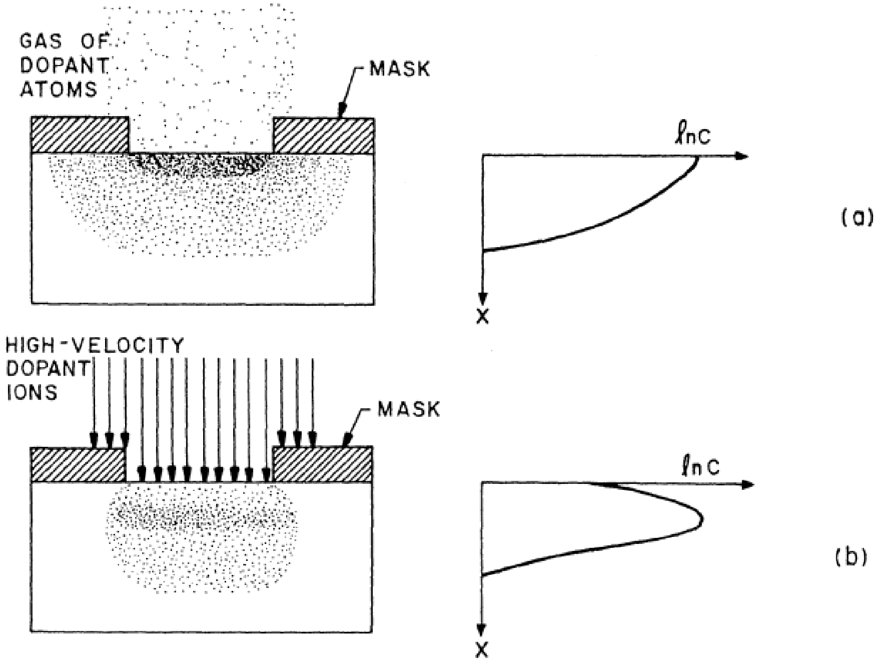


Fig. 1.8 Various steps for photo-etching

Roy, D. Choudhury. *Linear integrated circuits*. New Age International, 2003.

Surface chemistry like doping of impurities



AP 6120, Chapter 8 Diffusion, CCHK

1 A = 0.1 nm
1 nm = 0.001 um
1 um = 0.001 mm

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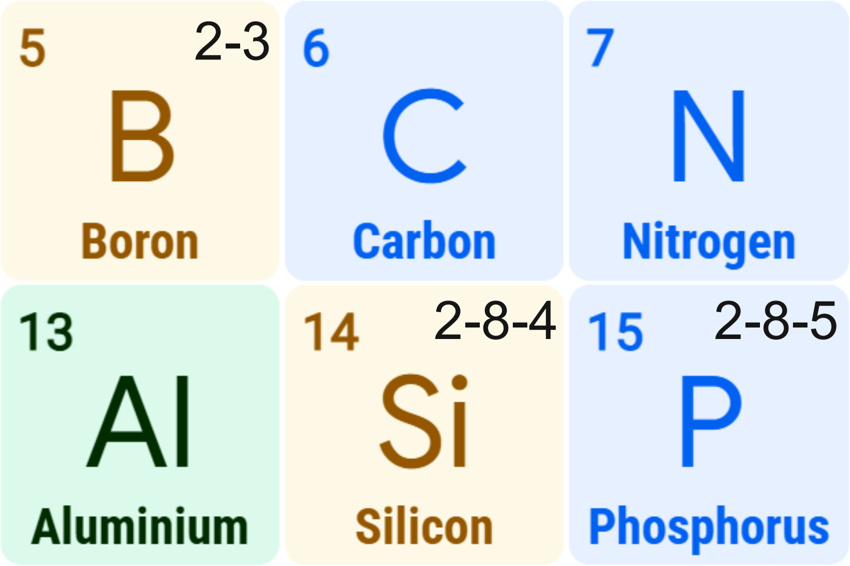
Why doping?

Because intrinsic silicon is **electrically** uninteresting:

- ~1.08e10 electrons turn conductive per cm^3
- Total electrons: 10e22
- That's one in a trillion odds escaping bonds.

- +B to make P type (additional holes h+)
- +P to make N type (additional electrons e-)



Both holes and electrons can be utilized as carriers.

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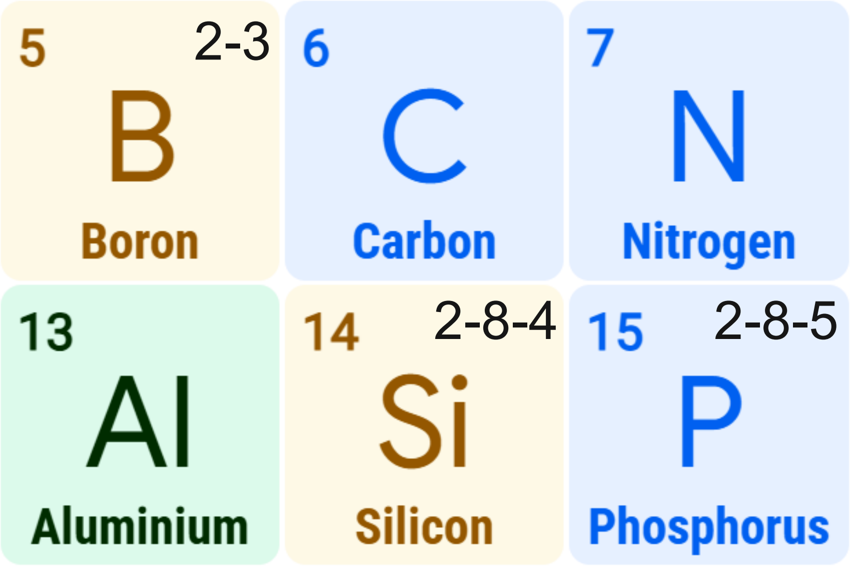

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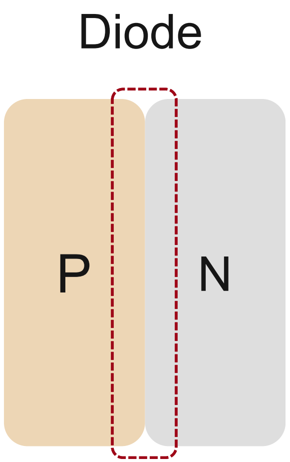
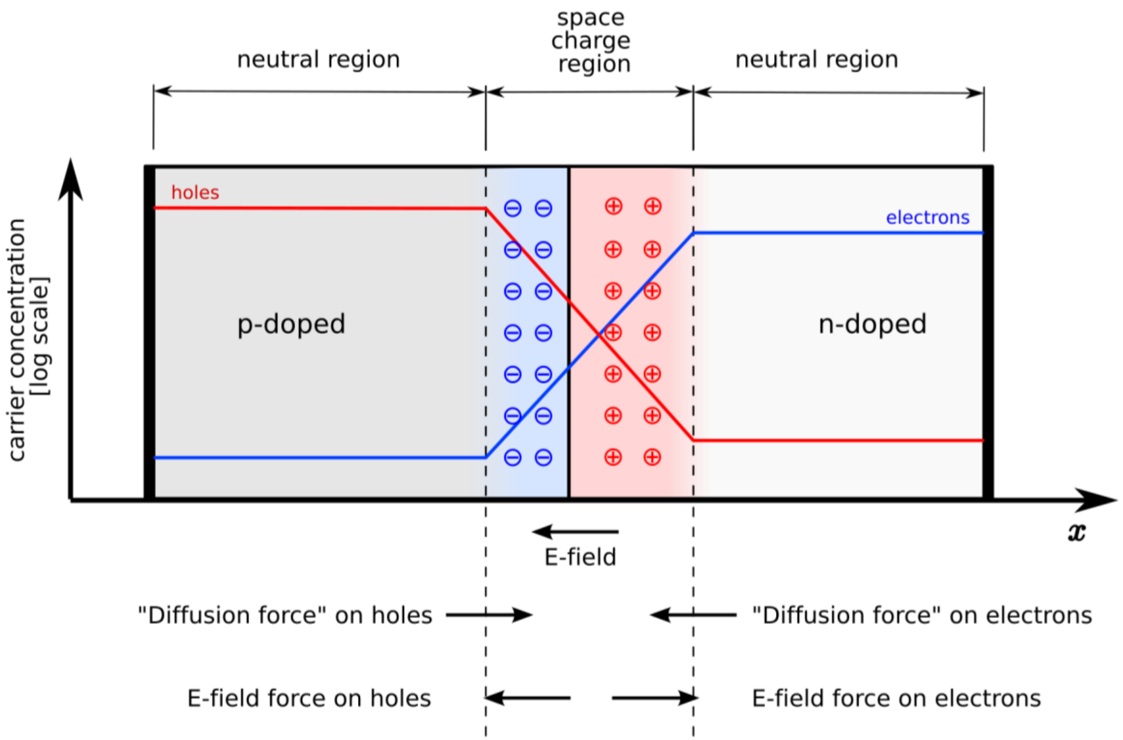
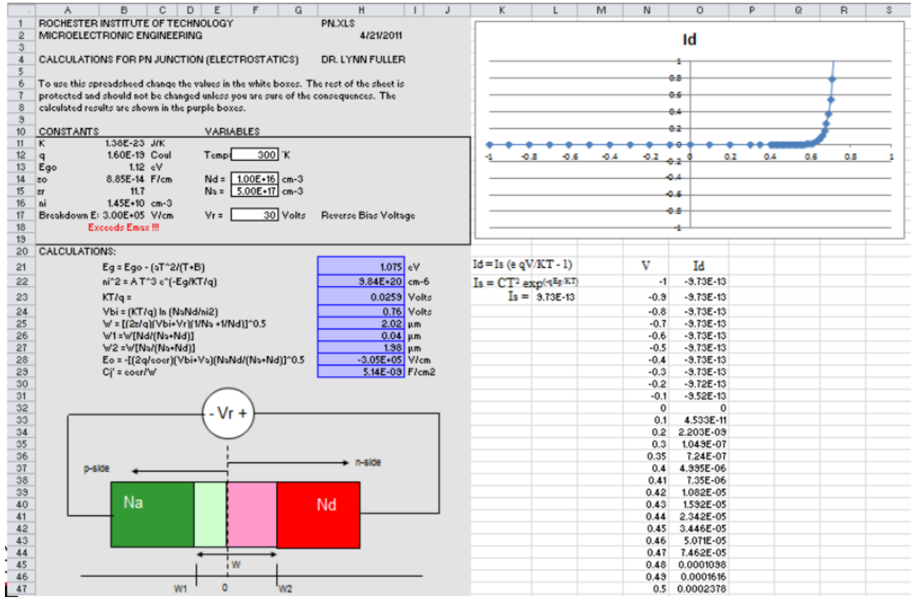
Empirical Device Models





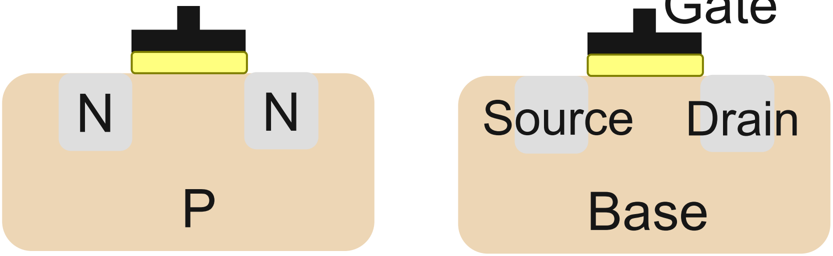
https://en.wikipedia.org/wiki/P%E2%80%93n_junction



MOSFET is a four terminal system

NMOS

What is doped What is named



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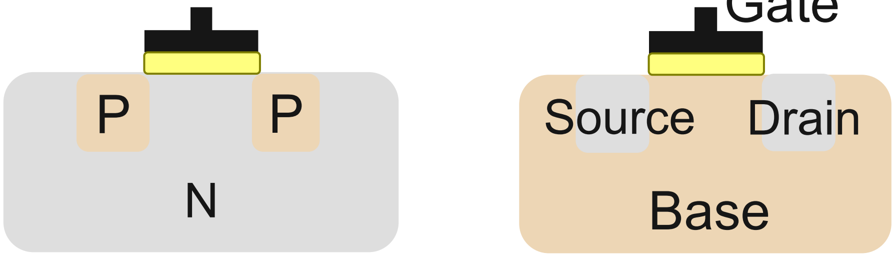
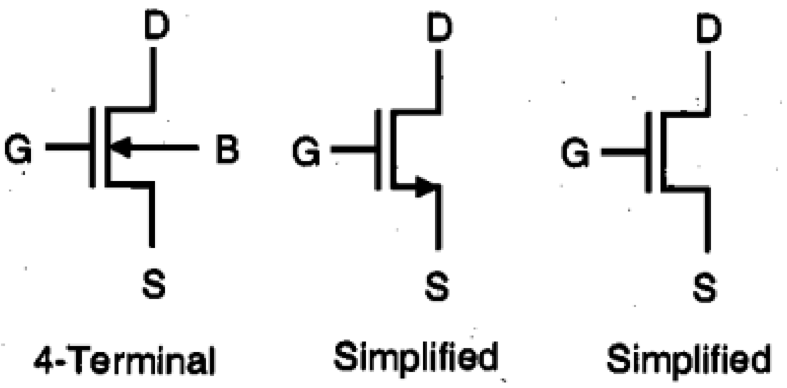
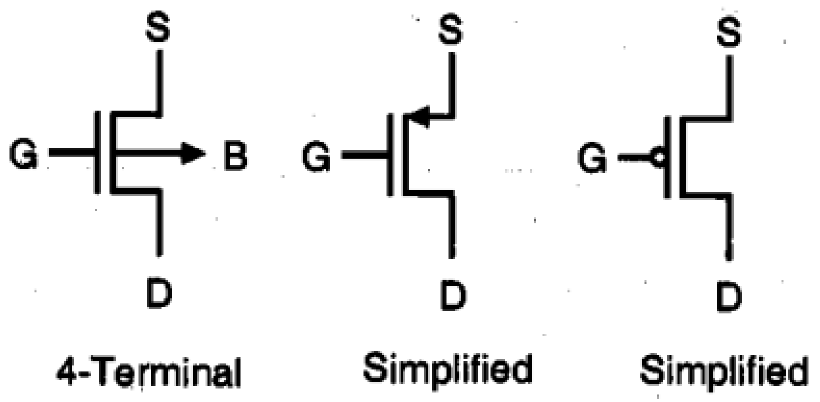




n-channel MOSFET



p-channel MOSFET

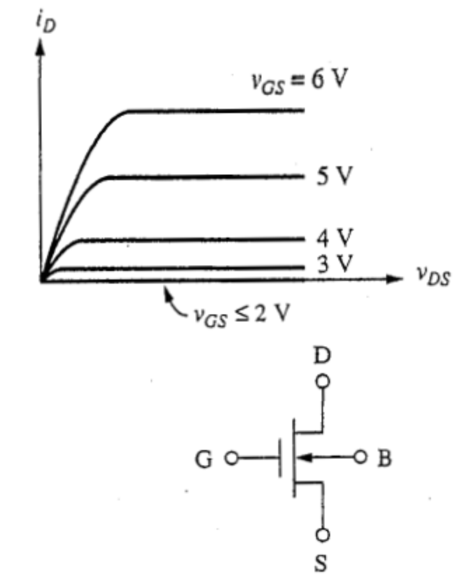
And its symbol system is quite confusing, all above are all legit in IEEE standard.

MOSFET physics is complicated

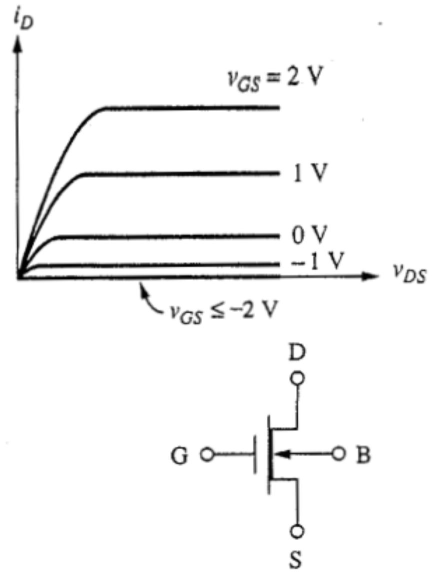
By adjusting doping level:
Enhancement mode: when gate is zero-bias, no conductive channel region.
This is the “normally off” condition.
Depletion mode: when gate is zero-bias, already has a conductive channel region.
I.e., the “normally on” condition.

NMOS

Enhancement mode

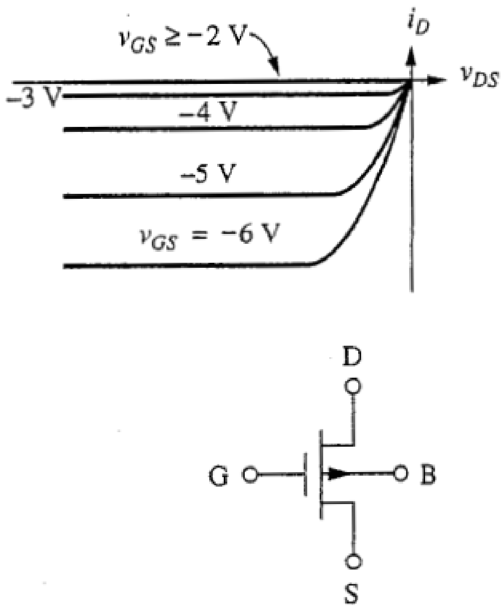


Depletion mode

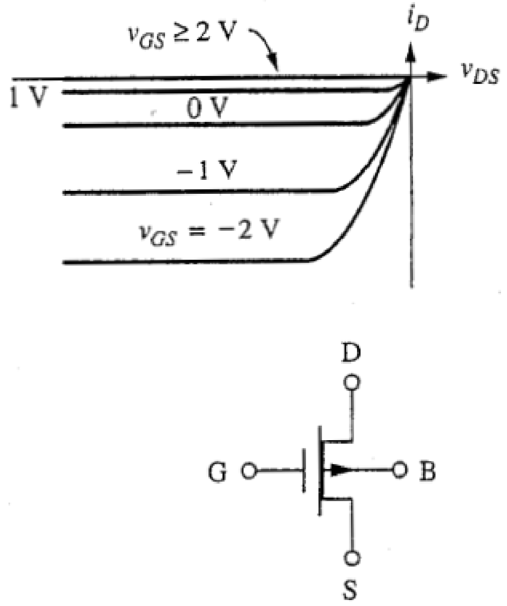


PMOS

Enhancement mode



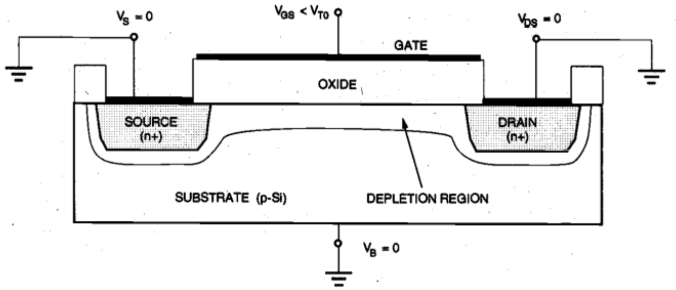
Depletion mode

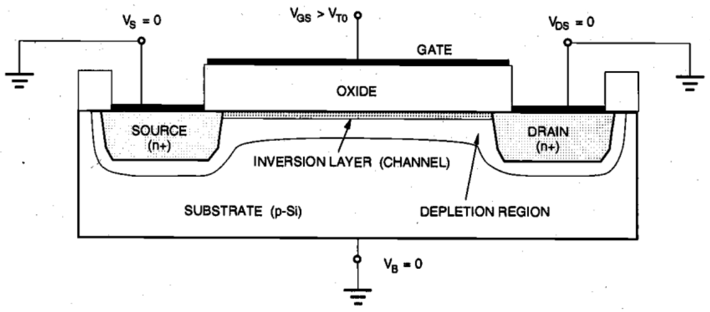


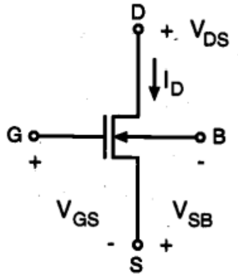
Fonstad, Clifton G. *Microelectronic devices and circuits*. McGraw-Hill, Inc., 2006

MOSFET physics is complicated, more example

Four terminal means many bias arrangements (but mostly we manipulate V_{GS} and V_{DS}):







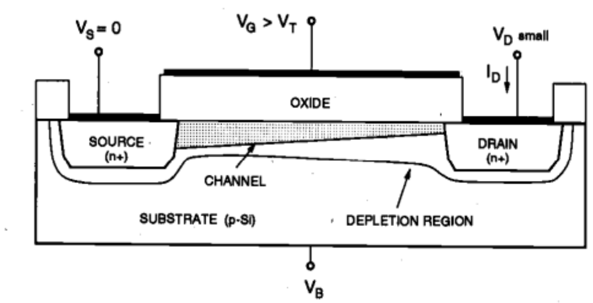
n-channel MOSFET

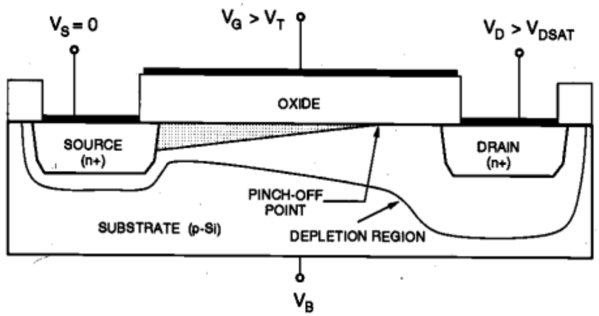
Current-voltage equations of the n-channel MOSFET :

$$I_D = 0, \quad for \quad V_{GS} < V_T \tag{3.54}$$

$$I_D(lin) = \frac{\mu_n \cdot C_{ox}}{2} \cdot \frac{W}{L} \cdot \left[2 \cdot (V_{GS} - V_T)V_{DS} - V_{DS}^2\right] \quad for \quad V_{GS} \geq V_T \quad and \quad V_{DS} < V_{GS} - V_T \tag{3.55}$$

$$I_D(sat) = \frac{\mu_n \cdot C_{ox}}{2} \cdot \frac{W}{L} \cdot (V_{GS} - V_T)^2 \cdot (1 + \lambda \cdot V_{DS}) \quad for \quad V_{GS} \geq V_T \quad and \quad V_{DS} \geq V_{GS} - V_T \tag{3.56}$$





Kang, Sung Mo, and Yusuf Leblebici. *CMOS digital integrated circuits*. New York, NY, USA:: MacGraw-Hill, 2003.

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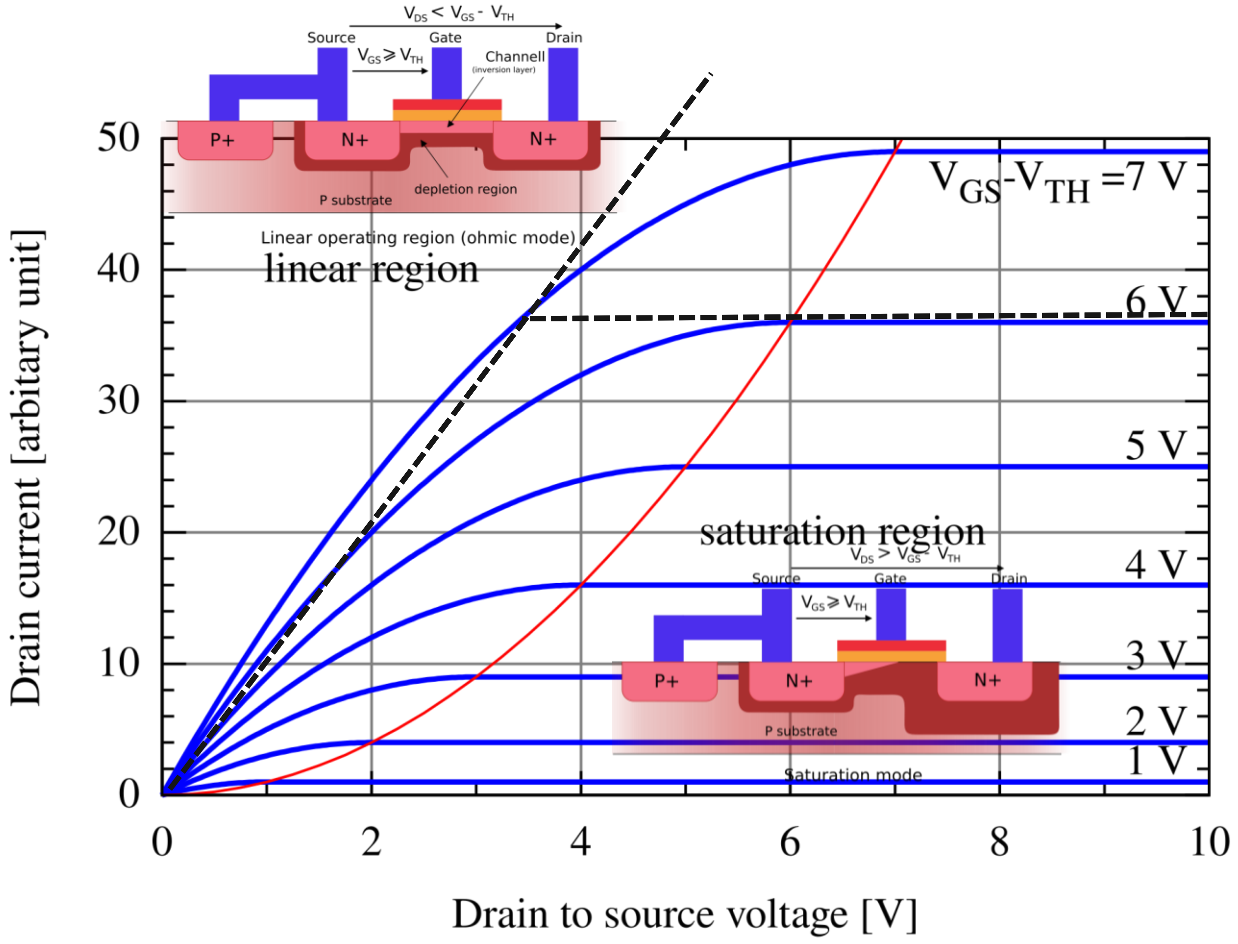
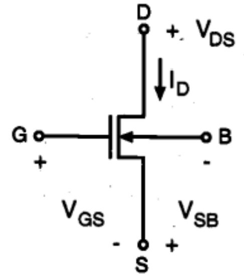


https://en.wikipedia.org/wiki/MOSFET, this is a simulated graph



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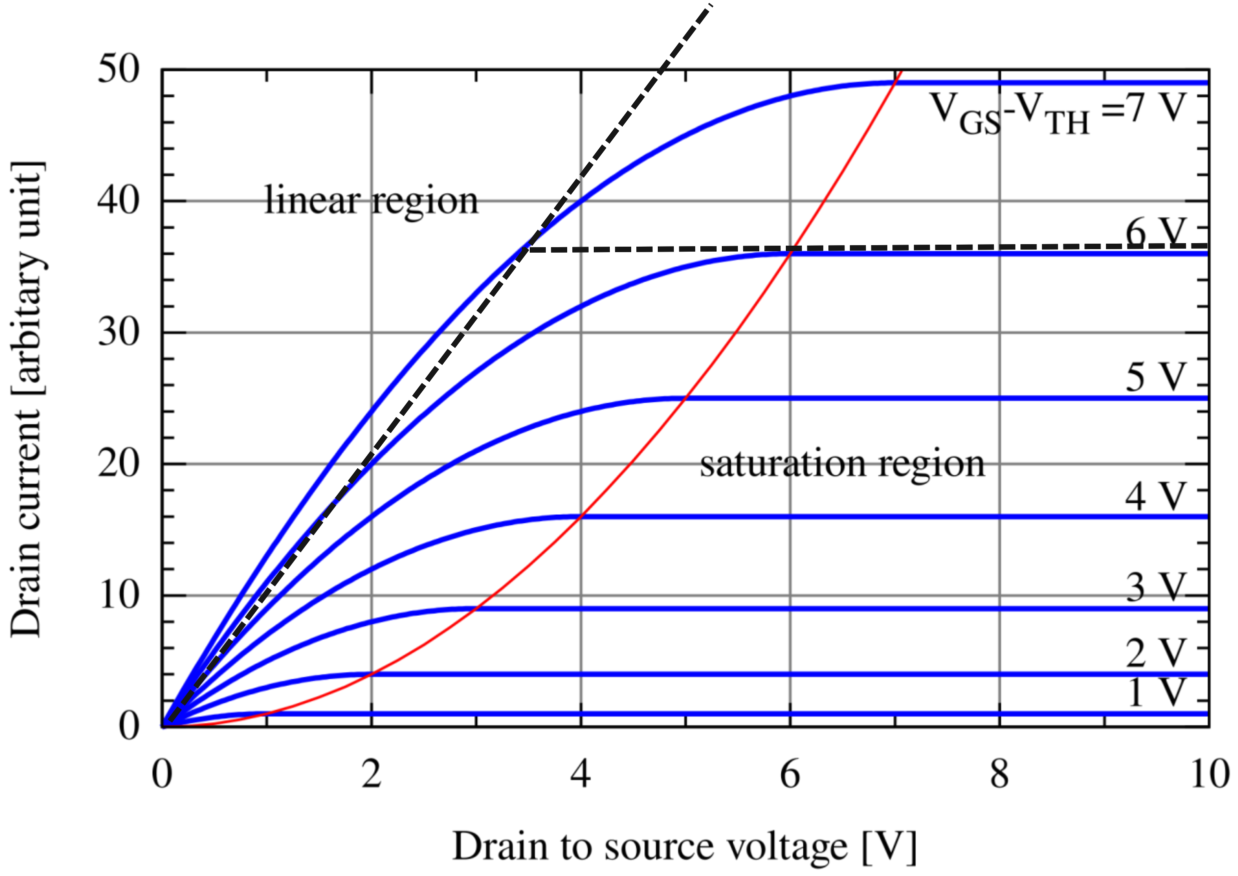
Empirical Device Models

This is a simulated graph



https://en.wikipedia.org/wiki/MOSFET

This is a “better” simulated graph

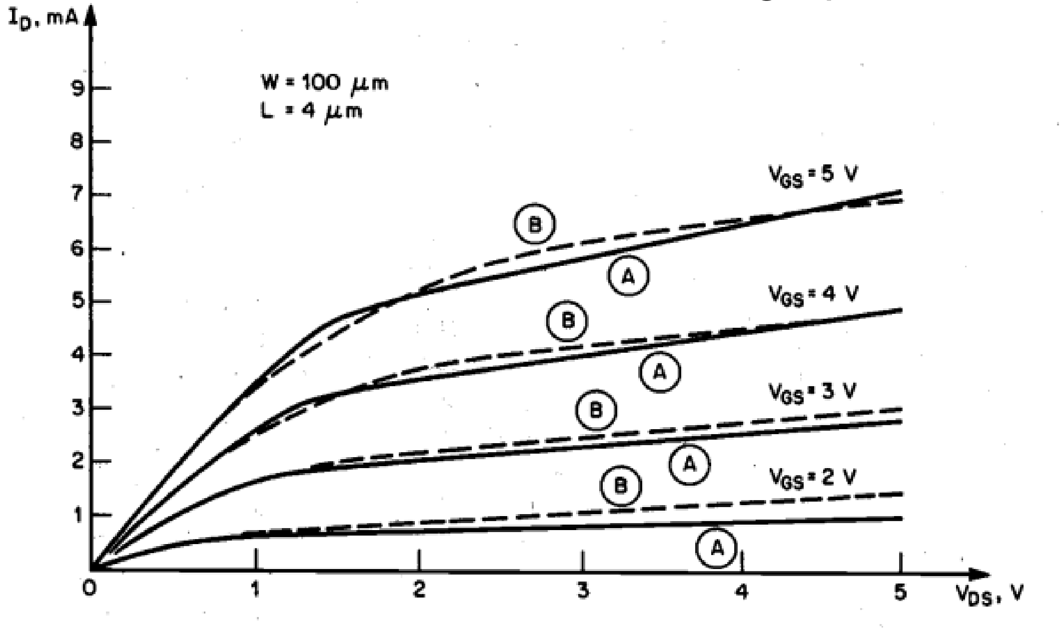
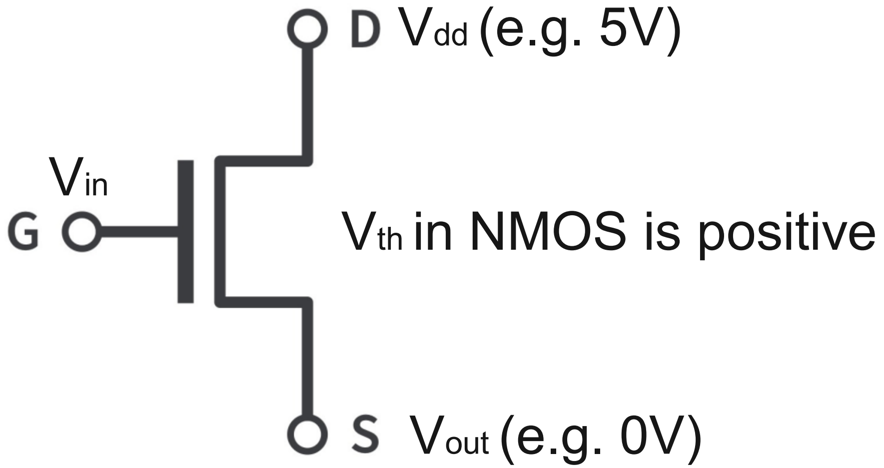


Figure 4.9. Drain current versus drain voltage characteristics of an n-channel MOSFET calculated with the LEVEL 2 model (A) and the LEVEL 3 model (B) (Copyright © 1988 by McGraw-Hill, Inc.).
The parameters common for both models are : VTO = 1, XJ = 1.0E-6, LD = 0.8E-6.
The parameters of the LEVEL 2 model are : UO = 800, UCRIT = 5.0E4, UEXP = 0.15.
The parameters of the LEVEL 3 model are : UO = 850, THETA = 0.04.

Kang, Sung Mo, and Yusuf Leblebici. *CMOS digital integrated circuits*. New York, NY, USA:: MacGraw-Hill, 2003.

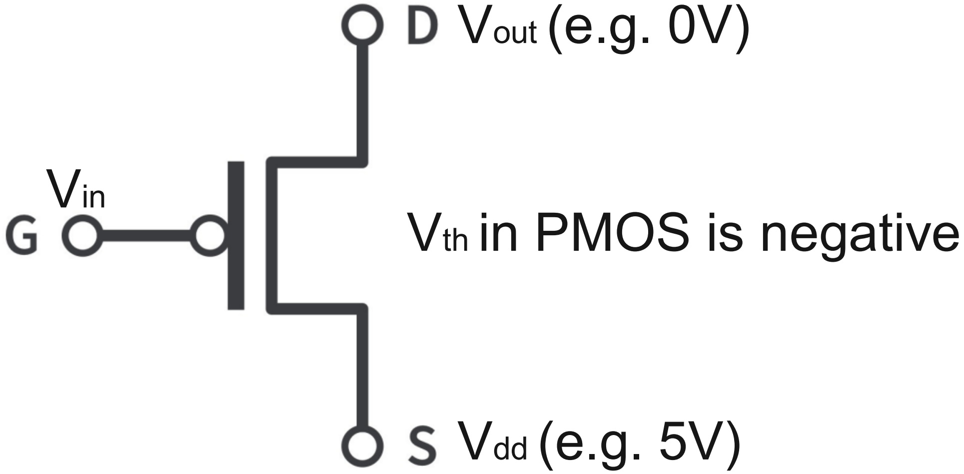
MOSFET as voltage controlled switches:

NMOS as pulldown



Switch	Input
On ($V_{GS}>V_{th}$)	**High**
Off ($V_{GS}<V_{th}$)	**Low**

PMOS as pullup



Switch	Input
On ($V_{GS}<V_{th}$)	**Low**
Off ($V_{GS}>V_{th}$)	**High**

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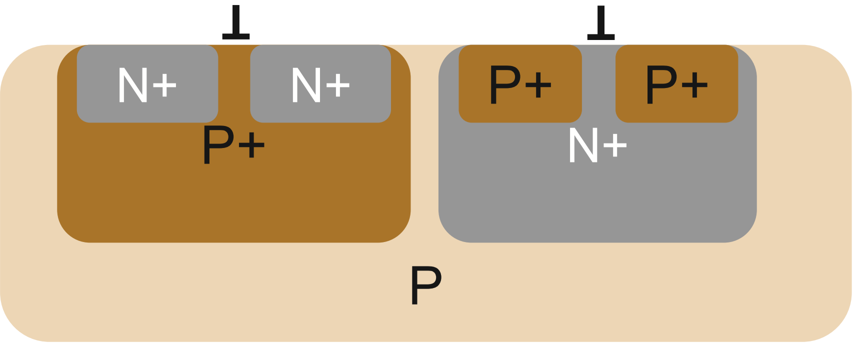
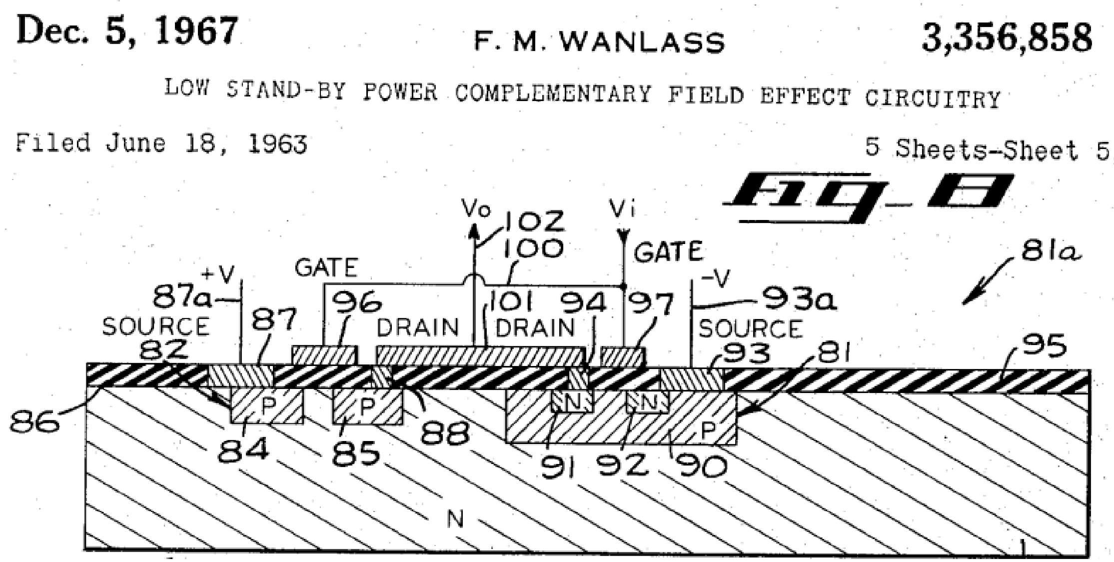
Entering the CMOS





Accordingly, an object of the present invention is to provide circuits in which power losses are minimized.

Another object of the present invention is to provide logic circuits in which power dissipation is reduced during stand-by periods.

Another object of the present invention is to provide a transistor circuit employing field-effect semiconductor devices wherein a field-effect semiconductor device of one carrier type is used as the active load for the field-effect semiconductor device of the opposite carrier type.

Another object of the present invention is to provide a transistor circuit in which an inverter action is produced without employing any passive load element.

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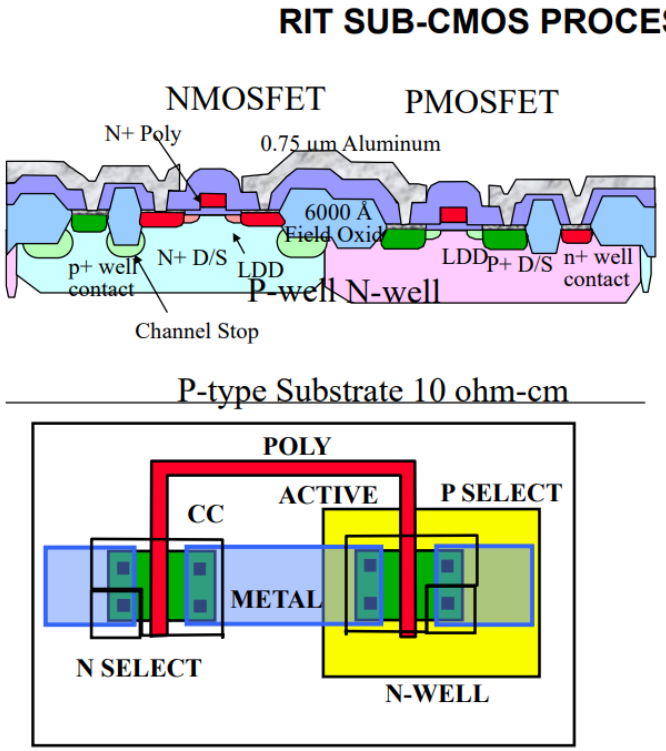
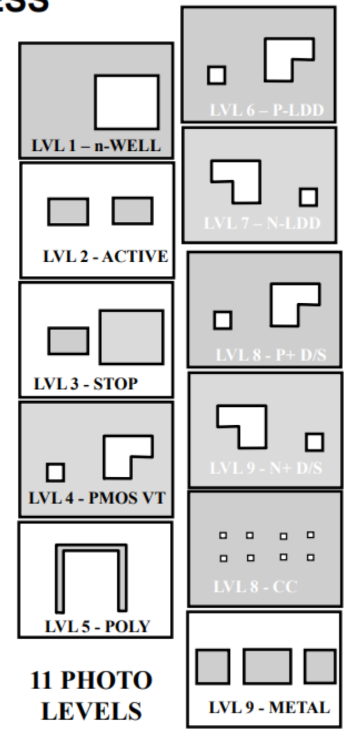
Entering the CMOS

11 photomasks and 150 fabrication steps, easy!





SUB-CMOS 150 PROCESS

SUB-CMOS Versions 150

1. CL01
2. OX05--- pad oxide, Tube 4
3. CV02- Si3N4-1500Å
4. PH03 –1- JG nwell
5. ET29 – Nitride Etch
6. IM01 – n-well
7. ET07 – Resist Strip
8. CL01
9. OX04 – well oxide, Tube 1
10. ET19 – Hot Phos Si3N4
11. IM01 – p-well
12. OX06 – well drive, Tube 1
13. ET06 - Oxide Etch
14. CL01
15. OX05 – pad oxide, Tube 4
16. CV02 – Si3N4 -1500 Å
17. PH03 – 2 – JG Active
18. ET29 – Nitride Etch
19. ET07 – Resist Strip
20. PH03 - -Pwell Stop
21. IM01- stop
22. ET07 Resist Strip
23. CL01
24. OX04 – field, Tube 1
25. ET19 – Hot Phos Si3N4
26. ET06 – Oxide Etch
27. OX04 – Kooi, Tube 1
28. IM01 – Blanket Vt
29. PH03 – 4-PMOS Vt Adjust
30. IM01 - Vt
31. ET07 – Resist Strip
32. ET06 – Oxide Etch
33. CL01
34. OX06 – gate, Tube 4
35. CV01 – Poly 5000A
36. IM01 - dope poly
37. OX08 – Anneal, Tube 3
38. DE01 – 4 pt Probe
39. PH03-5-JG poly
40. ET08 – Poly Etch
41. ET07 – Resist Strip
42. PH03 – 6 - n-LDD
43. IM01
44. ET07 – Resist Strip
45. PH03 – 7 - p-LDD
46. IM01
47. ET07 – Resist Strip
48. CL01
49. CV03 –TEOS, 5000A
50. ET10 - Spacer Etch
51. PH03 – 8 - N+D/S
52. IM01 – N+D/S
53. ET07 – Resist Strip
54. PH03 – 9 P+ D/S
55. IM01 – P+ D/S
56. ET07 – Resist Strip
57. CL01 Special - No HF Dip
58. OX08 – DS Anneal, Tube 2
59. CV03 – TEOS, 4000A
60. PH03 – 10 CC
61. ET26 - CC Etch
62. ET07 – Resist Strip
63. CL01 Special - Two HF Dips
64. ME01 – Metal 1 Dep
65. PH03 -11- metal
66. ET15 – plasma Etch Al
67. ET07 Resist Strip
68. SI01 - Sinter
69. CV03 – TEOS- 4000Å
70. PH03 – VIA
71. ET26 – Via Etch
72. ET07 – Resist Strop
73. ME01 – Metal 2 Dep
74. PH03- M2
75. ET15 – plasma Etch Al
76. ET07 - Resist Strip
77. SEM1
78. TE01
79. TE02
80. TE03

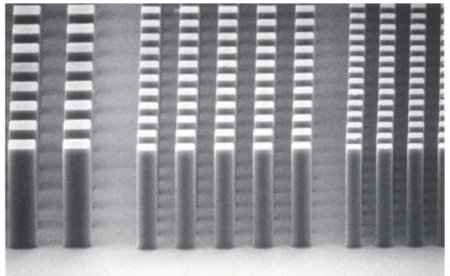
Dr. Lynn Fuller's CMOS and MEMS class, RIT 2015

A homemade MOSFET:

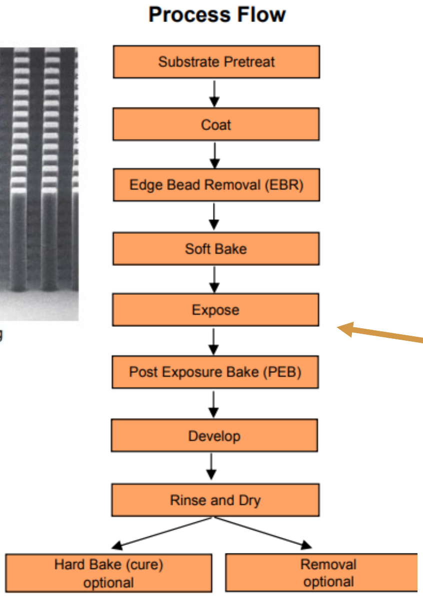
- https://www.youtube.com/watch?v=IS5ycm7VfXg

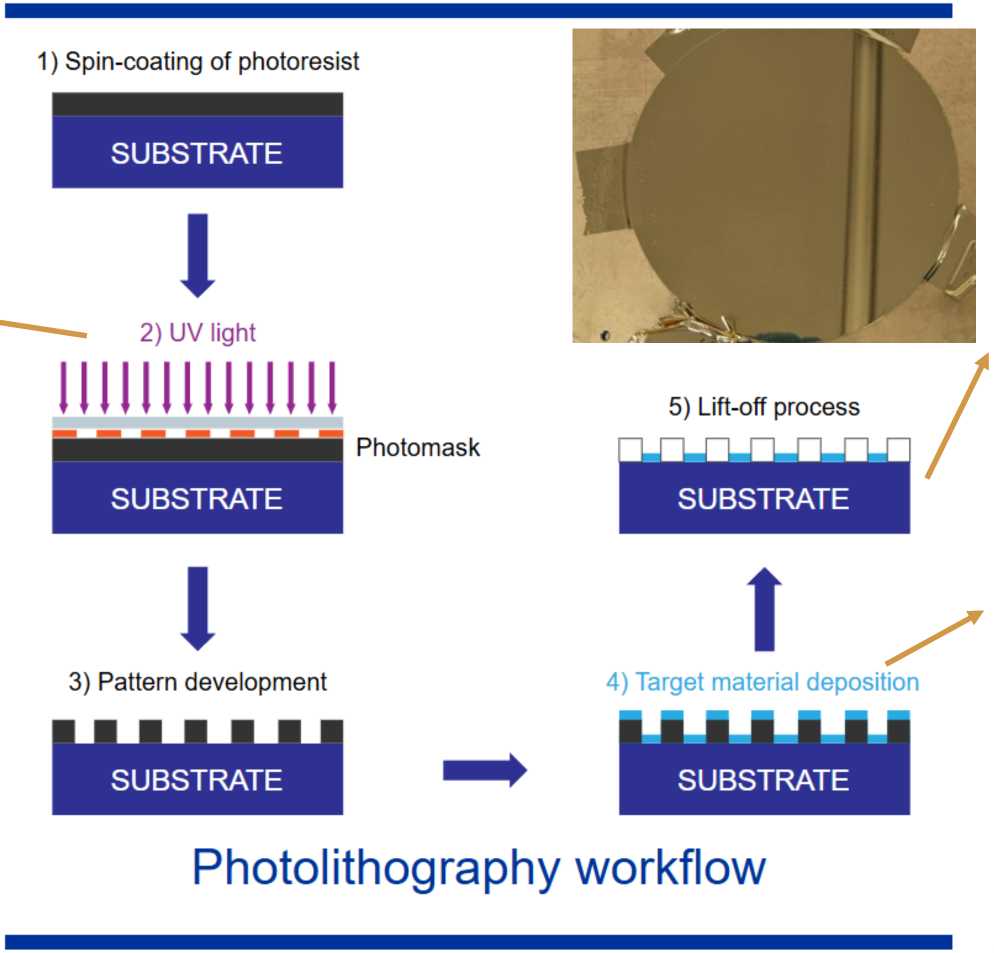
The realm of process engineering (1/2)

Photolithography example: lift-off



10 um features, 50 um SU-8 2000 coating





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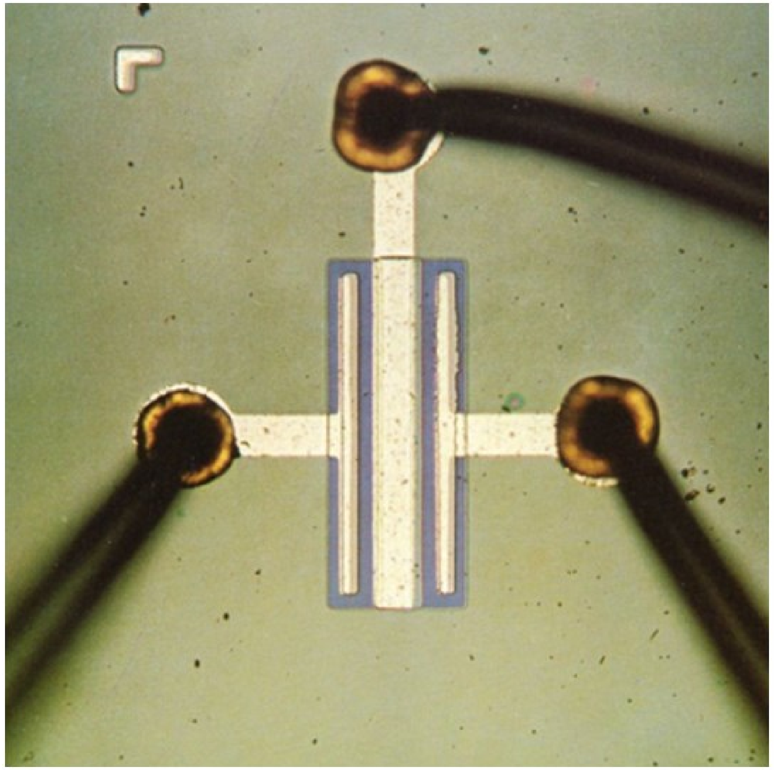
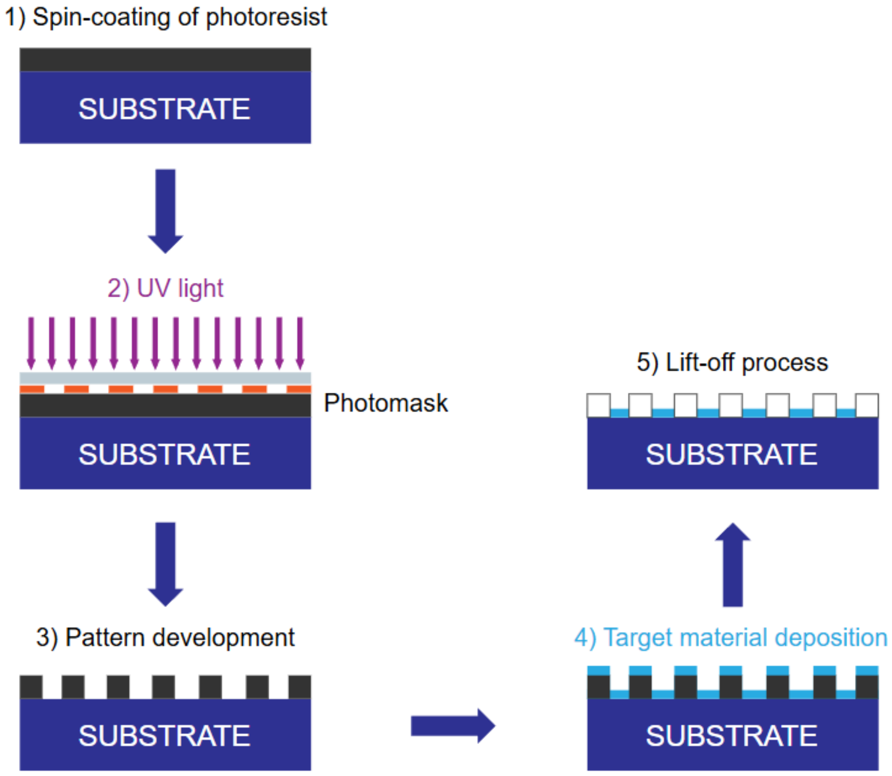
Data sheet and process flow from Kayaku and Kurt J. Lesker
Fabrication process at Indiana University cleanroom, 2021

Discuss: mask design for electrodes:



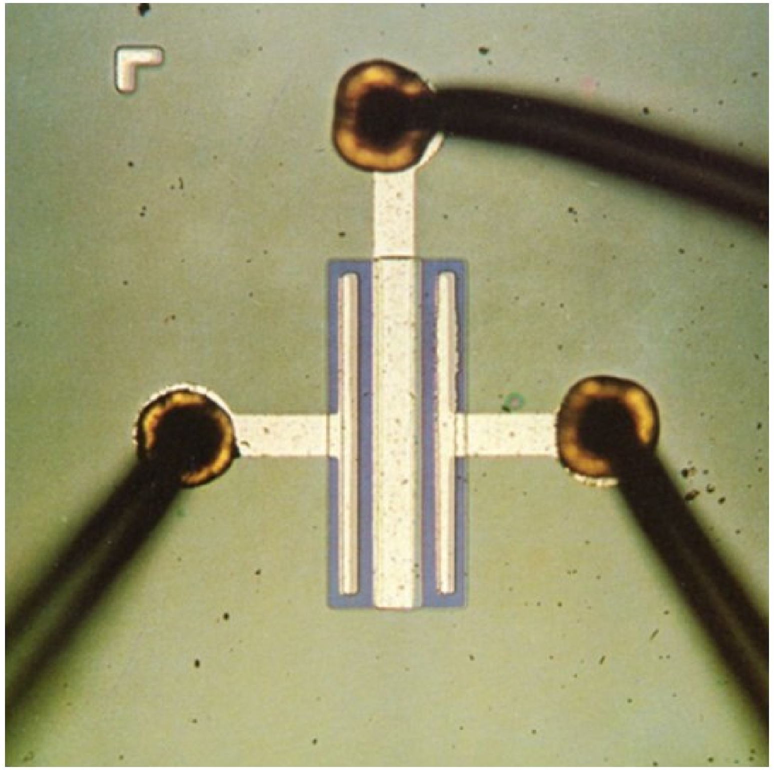
Fairchild FI 100 p-channel MOS switching transistor

Credit: Fairchild Camera & Instrument Corporation



Photolithography workflow

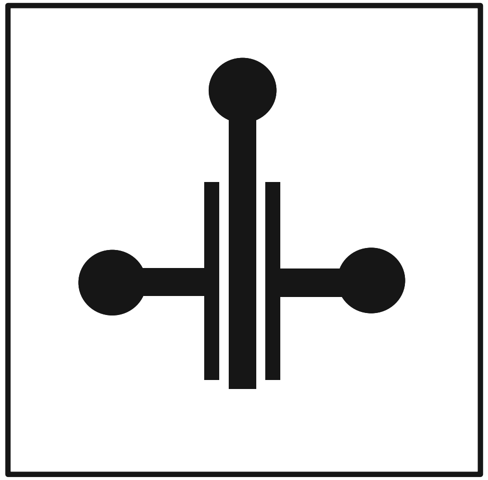
Discuss: mask design for electrodes:

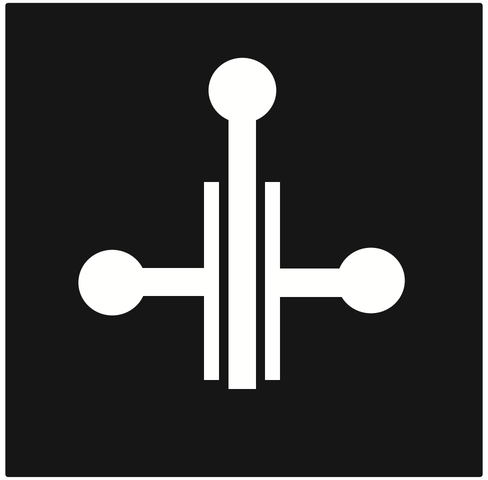


Fairchild FI 100 p-channel MOS switching transistor

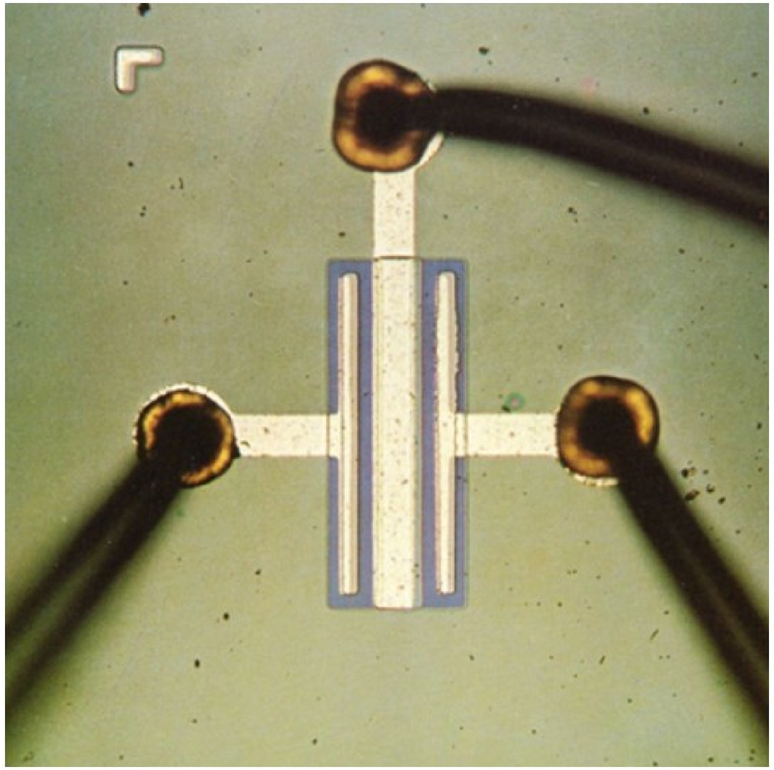
Credit: Fairchild Camera & Instrument Corporation

Which mask?





Discuss: mask design for electrodes:



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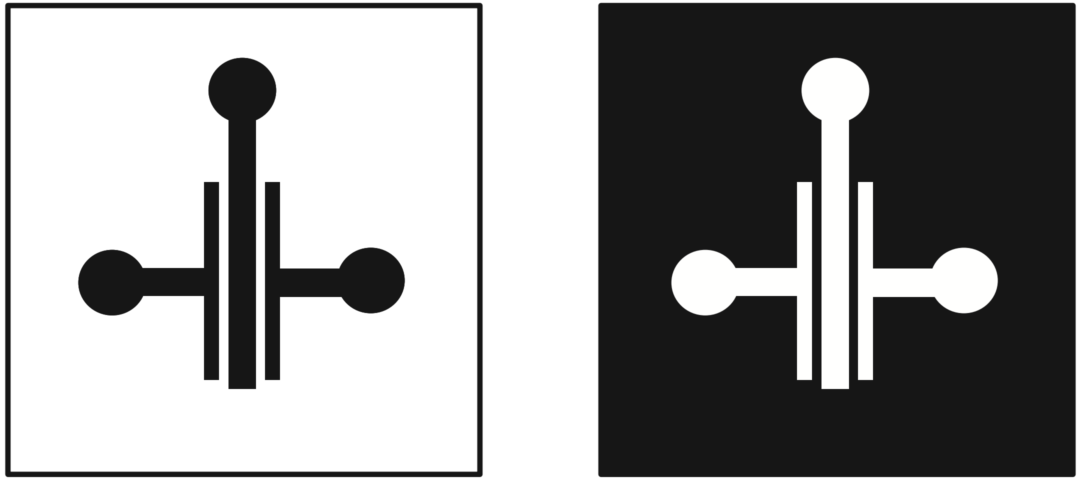
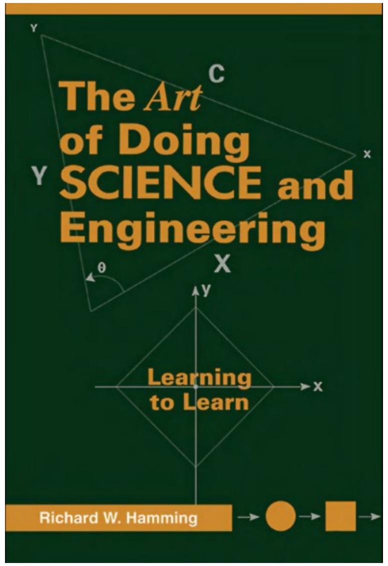


Depends on the types of PR, actually.

The realm of process engineering (2/2)

In science if you know what you are doing you should not be doing it.
In engineering if you do not know what you are doing you should not be doing it.



How could we manage the thickness control back in the 60-70s (1nm precision and 0.1 nm resolution) ?

The realm of process engineering (2/2)

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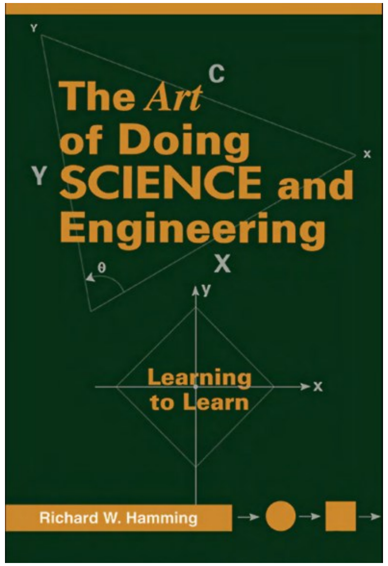
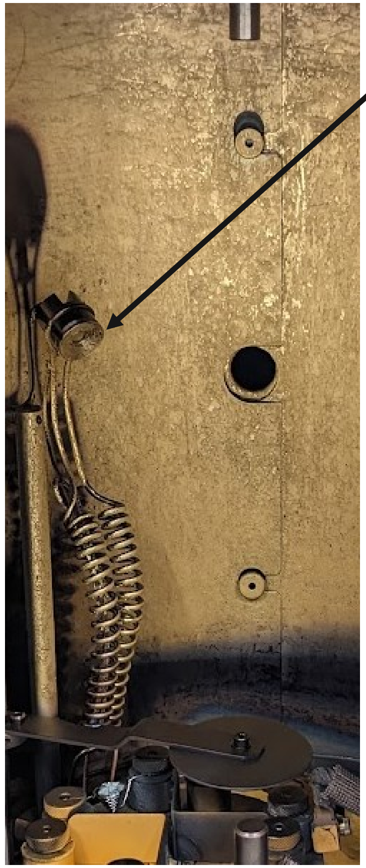


How could we manage the thickness control back in the 60-70s (1nm precision and 0.1 nm resolution) ?

1. Good vacuum pump

The realm of process engineering (2/2)



2. (Quartz Crystal Microbalance (QCM) sensor)

Typically a 6 MHz crystal, and runs until there's a 1.50 MHz shift.

The Sauerbrey equation is defined as:

$$\Delta f = -\frac{2 f_0^2}{A\sqrt{\rho_q \mu_q}} \Delta m$$

where:

- f_0 – Resonant frequency of the fundamental mode (Hz)
- Δf – normalized frequency change (Hz)
- Δm – Mass change (g)
- A – Piezoelectrically active crystal area (Area between electrodes, cm^2)
- ρ_q – Density of quartz (ρ_q = 2.648 g/cm^3)
- μ_q – Shear modulus of quartz for AT-cut crystal (μ_q = 2.947x10^{11} g·cm^{-1}·s^{-2})

A)Physical Characteristics	Fil-Tech QI8010
1)Sensor material	Single crystal Alpha Quartz
2)Angle of Cut[1]	35°15' (AT)
3)Contour	3 +/_0.5 diopter Plano-Convex
4)Surface Roughness	10 micron
5)Diameter	0.550" (13.97 mm)
6)Electrode	Gold/Chromium
B)Electrical Characteristics[2]	
1)Resonant Frequency (MHz)	5.975-5.993
2)Resistance at Resonance	<15 Ohms
3)Contact Resistance	<15 Ohms

A quartz crystal is arguably one of the most sensitive electrical devices ever invented. When used for thin film coating measurements, a crystal can detect as little as a pico-gram or 0.000000000001 gram of deposited material. This corresponds to a coating layer on the order of one atom thick!

With a device this sensitive operating in high stress coating environments you have to ask, "How can it work?" Our answer is, "Just barely!"

Tech bulletin from the QCM vendor, Fil-Tech inc.

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