ENR-325/325L Principles of Digital Electronics and Laboratory

Xiang Li

Fall 2025

COE COLLEGE

Hamming codes can be done in the EE way

- Before that, we need to acquire some basic skillsets.

Pre-step: Data forms

Step 1: Data manipulation

Step 2: Information storage

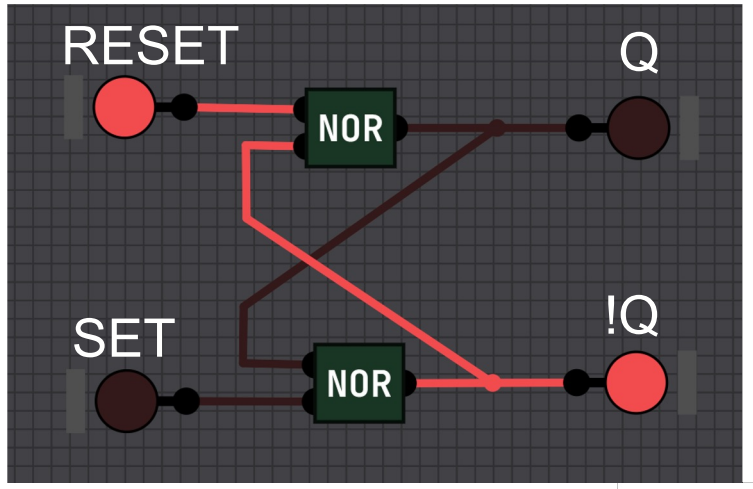
Step 3: Interface

3.1 Information flow

~~3.2 Physical contacts~~ (better stuff to talk about in PCB designs)

Understanding SR latch with truth table and timing diagram

SR latch

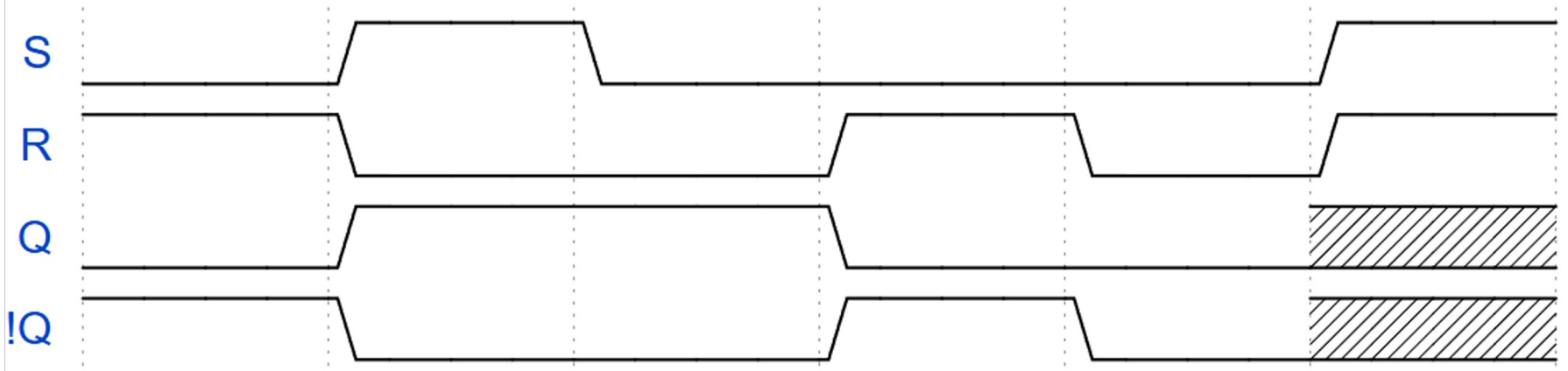


SR latch truth table

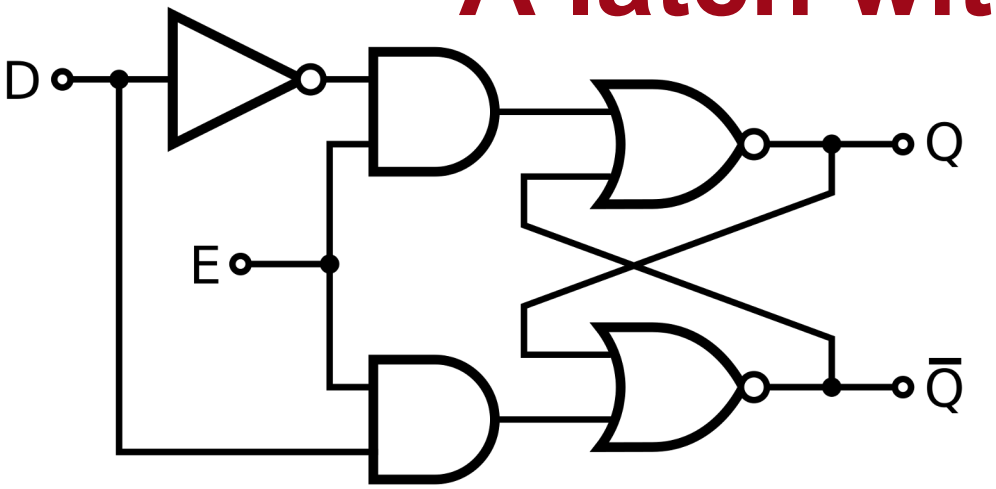
S	R	Output (Q)
0	0	**Previous State**
0	1	**0**
1	0	**1**
1	1	**0 (Invalid)**

(HOLD)

SR Latch Timing Diagram (NOR Gates)

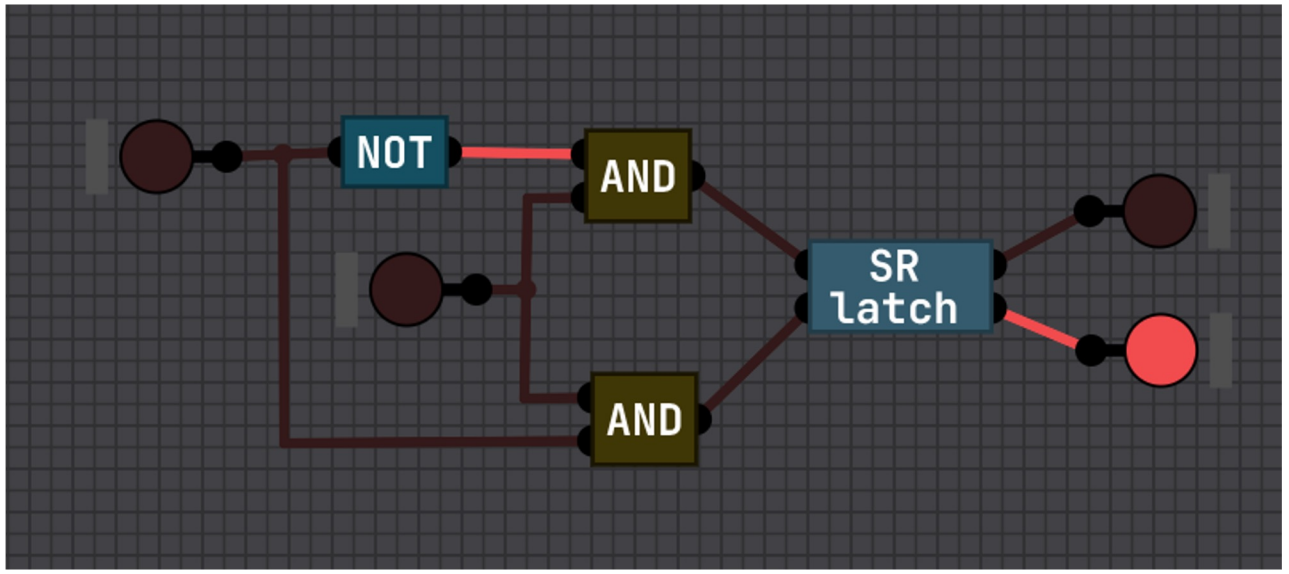


A latch with a “single” input



https://en.wikipedia.org/wiki/Flip-flop_(electronics)

A gated D latch



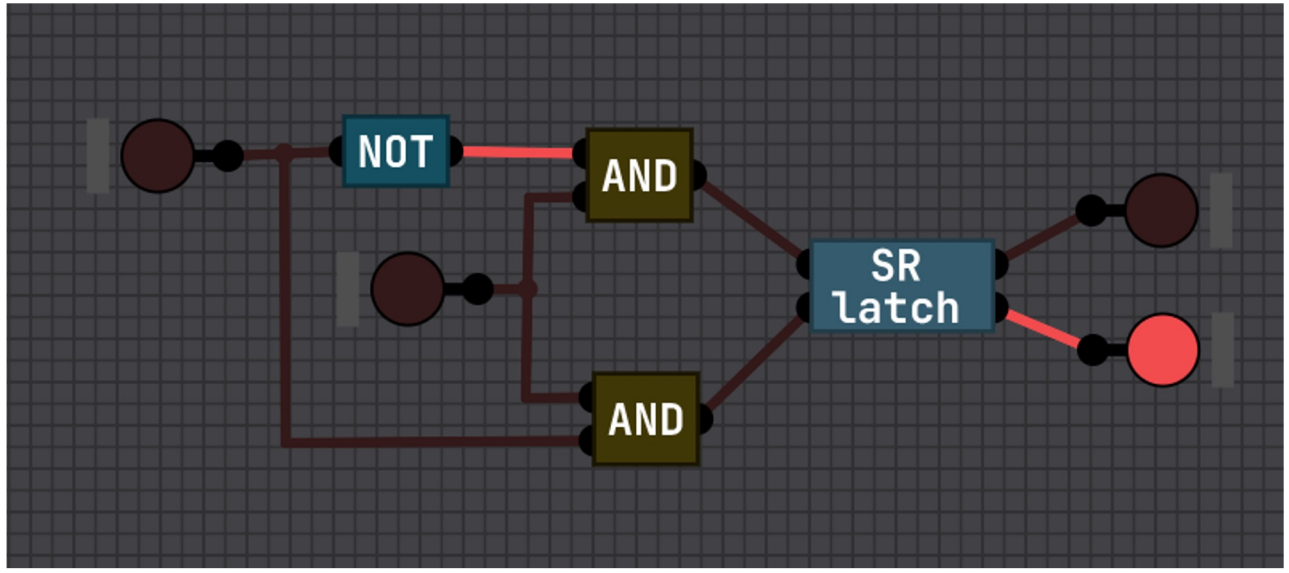
D latch truth table

D	E	Output (Q)
X	0	**Previous State**
0	1	**0**
1	1	**1**

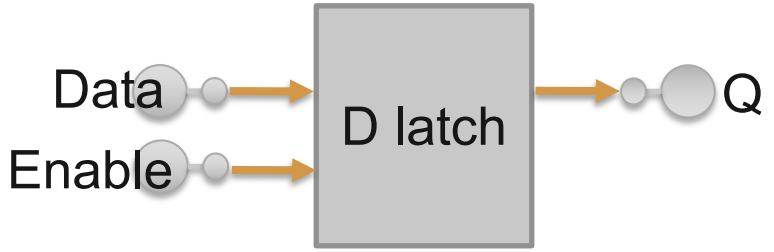
COE COLLEGE

A latch with a “single” input

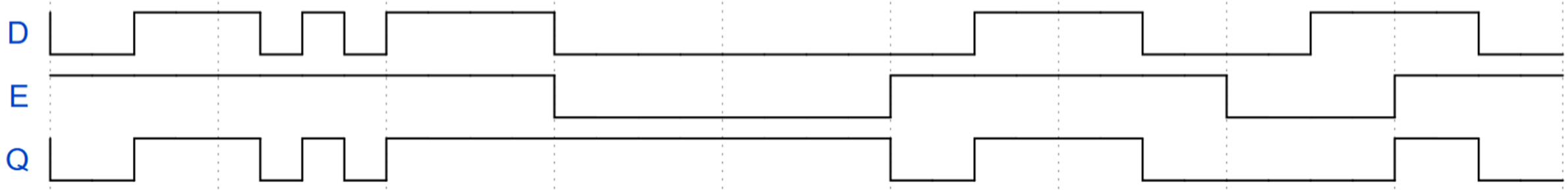
A gated D latch



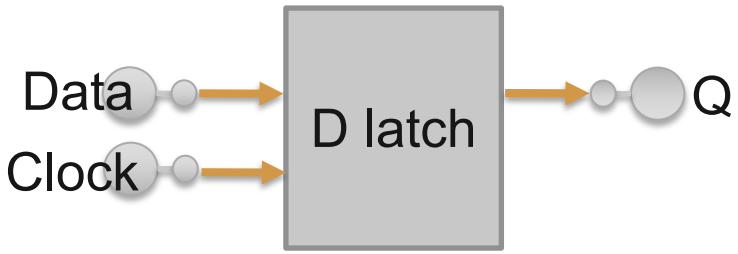
Also known as: D latch/data latch

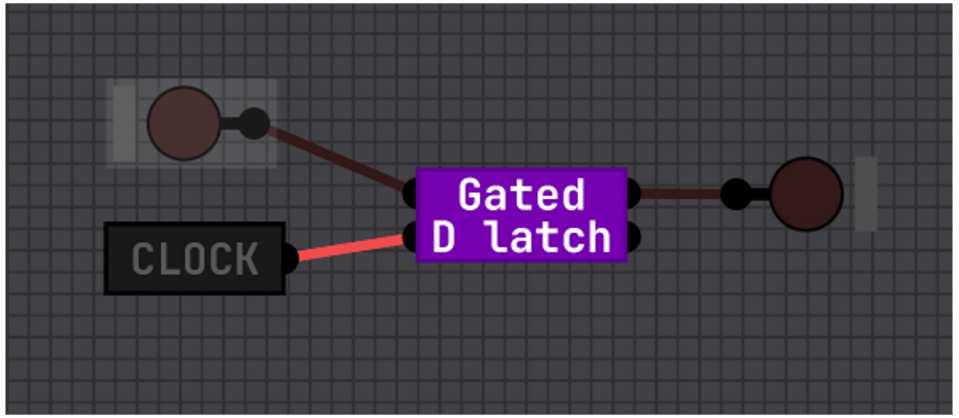


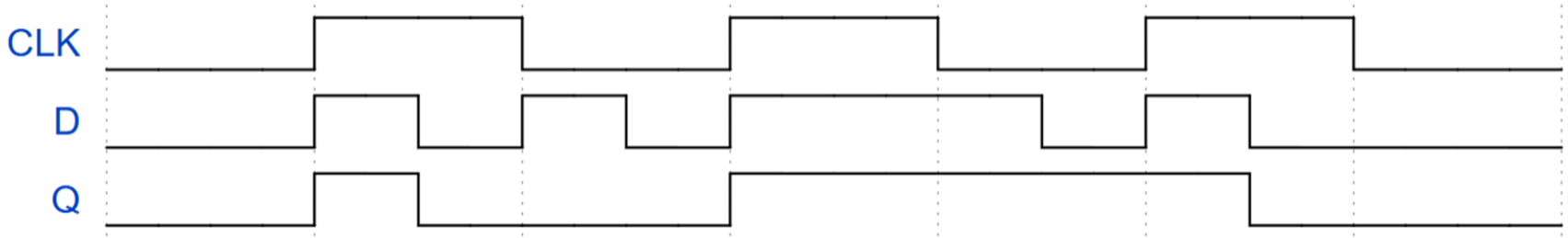
Gated D latch



A clocked D latch

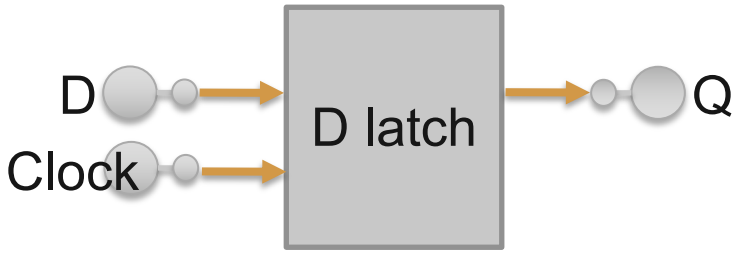




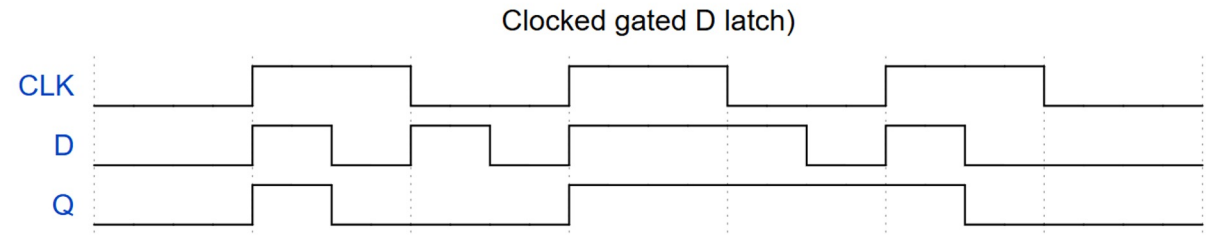


COE COLLEGE

Timing diagram code:

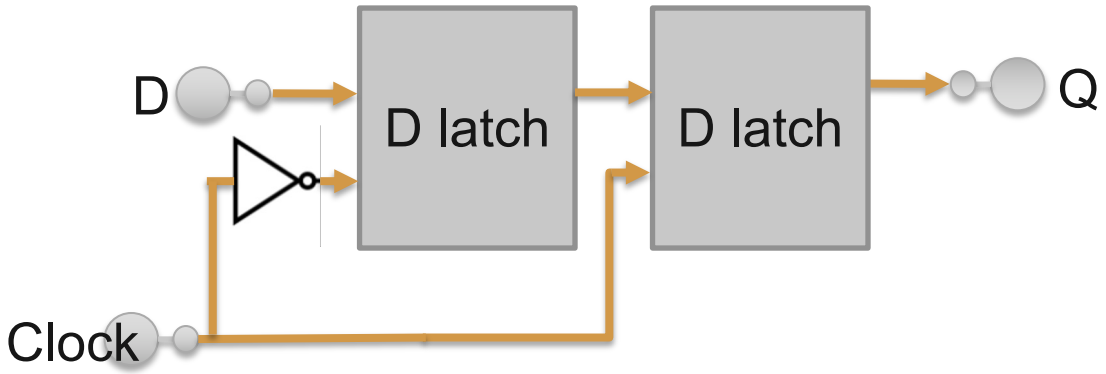



```
{
  "signal": [
    {"name": "CLK",        "wave": "lhlhlhl"},
    {"name": "D",        "wave": "lpphppl"},
    {"name": "Q",        "wave": "lplh.pl"},

  ],
  "head": {
    "text": "Clocked gated D latch)"
  },

  "config": {
    "hscale": 2
  }
}
```



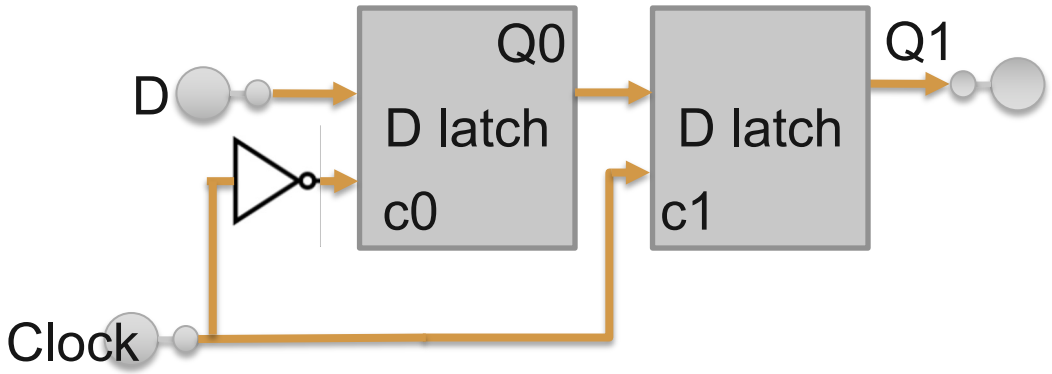
COE COLLEGE

Rising edge-triggered flip flops: synchronizing (timed trigger) achieved

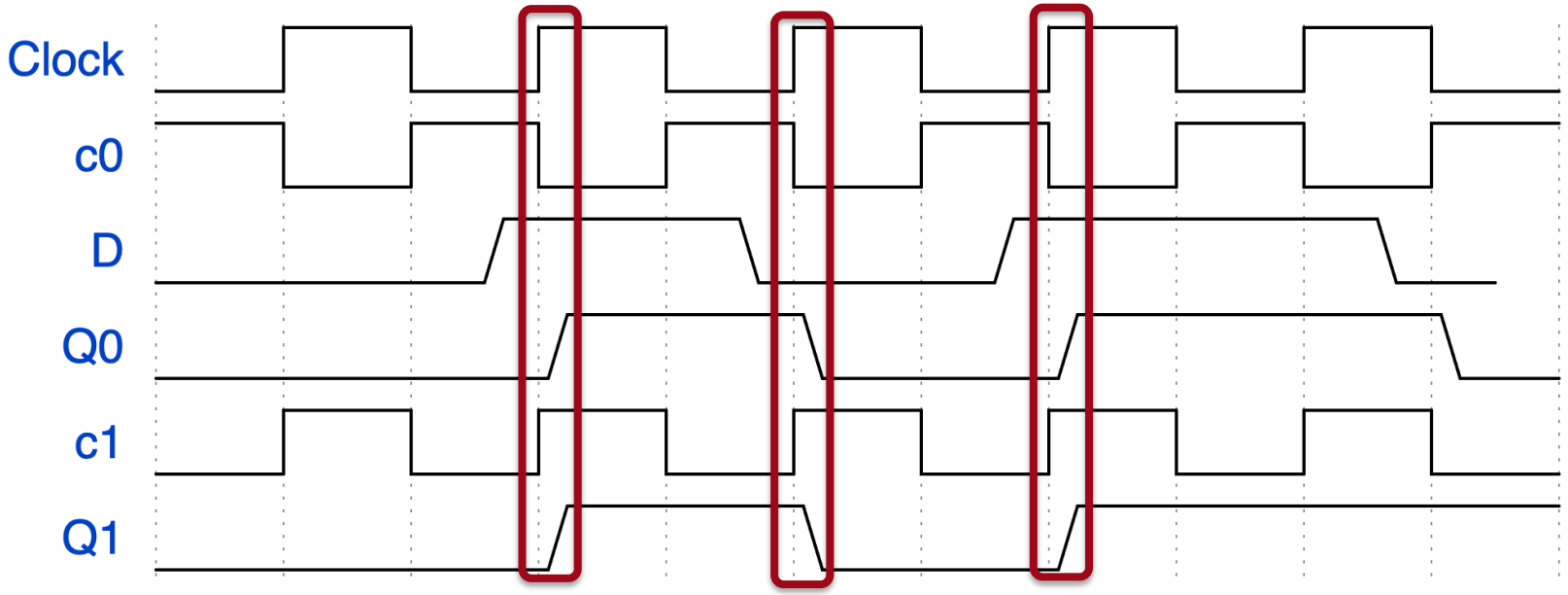


Also known as:
Master-slave D type flip flop

Rising edge-triggered flip flops: synchronizing (timed trigger) achieved

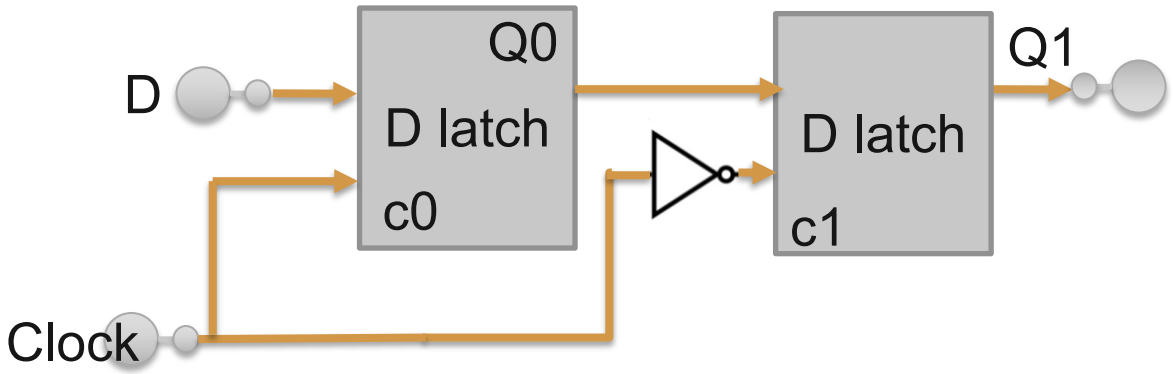


Also known as:
Master-slave D type flip flop



COLLEGE

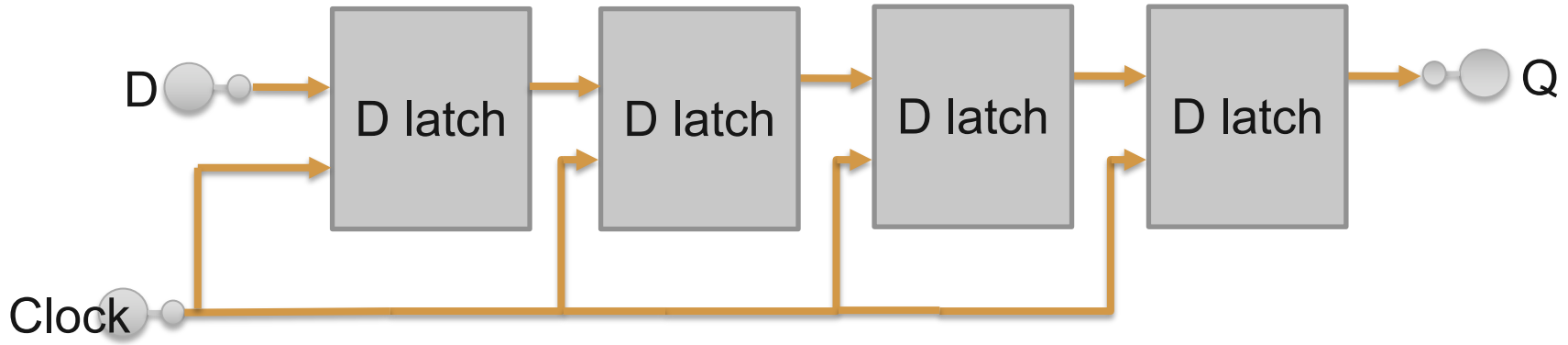
Falling edge-triggered flip flops: synchronizing (timed trigger) achieved



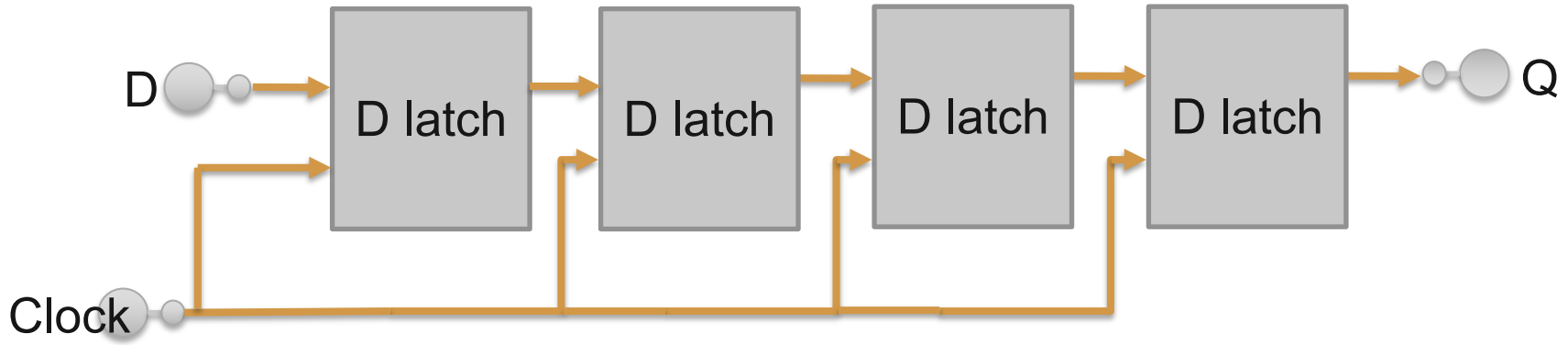
Also known as:
Master-slave D type flip flop

Timing diagram is in HW#7.

One more application with D flip-flops



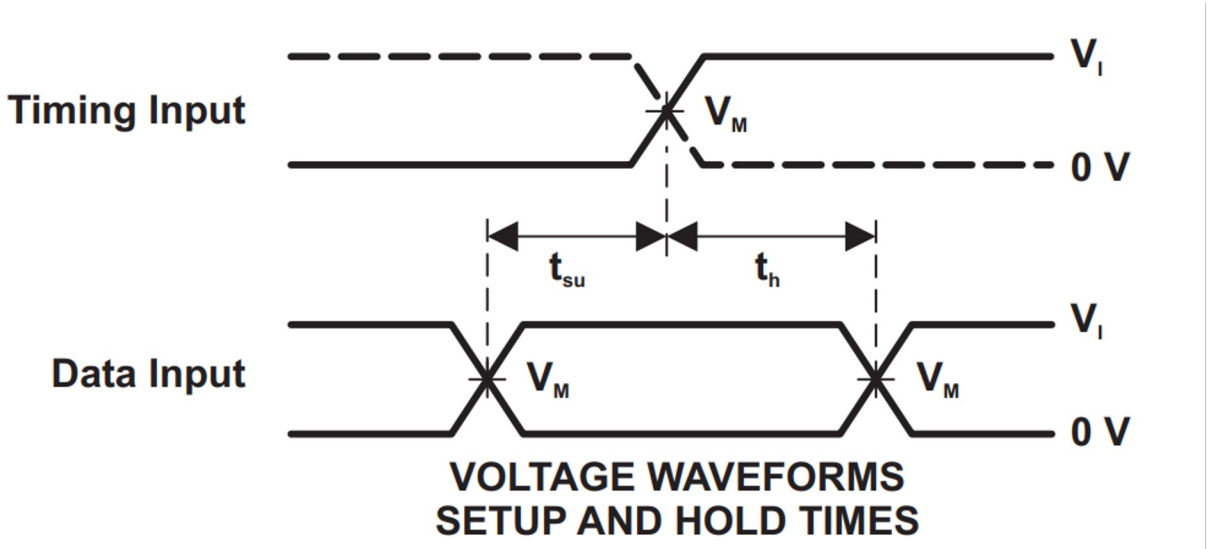
So, this is a (4 bit) shift register



- **Serial In (SI), Serial Out (SO)**
- **How about SIPO, PISO, and PIPO?**

Dynamic discipline: handling the interface between logics and time

- **A clock signal (with its edges if it's a flip-flop) to define transitions.**
- **Stable inputs during that transition window. (So, some *setup time* t_{su} and some *hold time* t_h)**
- **Thus, guaranteed viable output other than its own switching delays.**



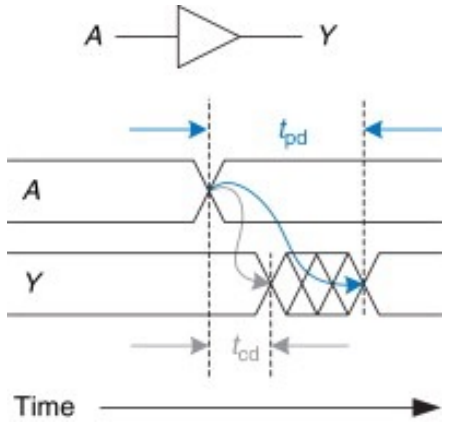
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES

COE COLLEGE

Nolan, Stephen M., Jose M. Soltero, and Shreyas Rao. "Understanding and Interpreting Standard-Logic Data Sheets." Application Report, Texas Instruments, 2002

Dynamic discipline: handling the interface between logics and time

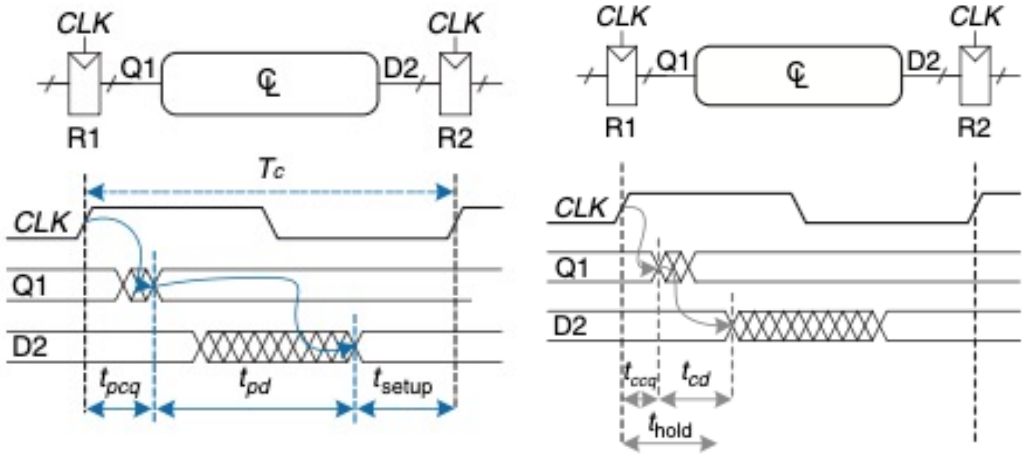
- Unlike propagation delay (t_{pd}) and contamination delay (t_{cd}) , the setup time t_{su} and some hold time t_h are intentional.



- So, the final time constraint for sequential logics is:

  Minimum clock period: $T_c \geq \Sigma\, t_{pd} + t_{su}$

  Minimum delay constraint: $\Sigma\, t_{cd} \geq t_h$



COE COLLEGE

Haris, D., and S. Haris. "Digital Design and Computer Architecture ARM Edition." (2016).

Dynamic discipline:

Timing Requirements (Over Recommended Operating Free-air Temperature Range (unless otherwise noted)) (see Figure 2)

			SN54LVTH16646				SN74LVTH16646				UNIT
			V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency			150		150		150		150	MHz
t_w	Pulse duration, CLK high or low		3.3		3.3		3.3		3.3		ns
t_{su}	Setup time, A or B before CLKAB↑ or CLKBA↑	Data high	1.2		1.5		1.2		1.5		ns
		Data low	2		2.8		2		2.8		
t_h	Hold time, A or B after CLKAB↑ or CLKBA↑	Data high	0.5		0		0.5		0		ns
		Data low	0.5		0.5		0.5		0.5		

Figure 14. Example Timing-Requirements Section

COE COLLEGE

Nolan, Stephen M., Jose M. Soltero, and Shreyas Rao. "Understanding and Interpreting Standard-Logic Data Sheets." Application Report, Texas Instruments, 2002