Bedrock-RTL Delay Line (No Reset) Specification

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# Overview

The br\_delay\_nr module implements a configurable delay line that delays an input signal in by a fixed number of clock cycles specified by the NumStages parameter. The delayed signal is output on out. If NumStages is 0, the output out is directly connected to the input in without any delay. The module supports a parameterizable bit width of the input and output signals through the BitWidth parameter. Unlike br\_delay, this variant does not include a reset signal, and the pipeline registers are not reset.

# Parameters

| Parameter | Type | Scope | Description |
| --- | --- | --- | --- |
| BitWidth | int | module | Must be at least 1. Specifies the bit width of the input and output signals. |
| NumStages | int | module | Must be at least 0. Specifies the number of pipeline stages (delay cycles). |

# Interfaces

| Interface | Port Direction | Port Type | Port Name | Description |
| --- | --- | --- | --- | --- |
| Clock | input | logic | clk | Clock signal. |
| Reset | input | logic | rst | Synchronous active-high reset signal. Only used for assertions. |
| Data Input | input | logic [BitWidth-1:0] | in | Input signal to be delayed. |
| Data Output | output | logic [BitWidth-1:0] | out | Delayed output signal. |

# Functional Behavior

* The module delays the input in by NumStages clock cycles.
* The pipeline registers do not have a reset; their initial contents are undefined upon power-up.
* For each clock cycle:
  + The input in is sampled on the rising edge of clk and progresses through the pipeline stages.
  + The output out reflects the value of in from NumStages cycles earlier:
    - out(t) = in(t - NumStages) for t ≥ NumStages.
* Before NumStages cycles have elapsed since power-up, the output out will reflect the initial contents of the uninitialized pipeline registers, which are undefined.

# Latency and Throughput

| Latency Metric | Cycles | Description |
| --- | --- | --- |
| Data Delay | NumStages | The output out reflects the input in delayed by NumStages clock cycles. |
| Throughput | 1 | The module can accept and process a new input every clock cycle. |
| Initialization Latency | NumStages | Since the pipeline registers are not reset, the output out will be undefined for the first NumStages cycles after power-up. |